Design of a 100W Radiation-Tolerant Power-Factor-Correction Buck AC/DC Converter

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Abstract

With regard to the high-luminosity upgrade of the Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN), much of the electronics is being redesigned. This includes the Distributed Input/Output Tier (DI/OT) project which aims to standardize high-reliability and high-availability custom electronics in radiation-exposed areas. This paper presents the design of a 100 W radiation-tolerant AC/DC converter, developed using commercial-off-the-shelf (COTS) components, to be used for powering the DI/OT crates, compatible with the CompactPCI-Serial standard (CPCI-S.0). The converter uses a non-isolated power-factor-correction (PFC) buck topology that takes universal AC input and gives a 36–72 V DC bus with a 10% or better peak-to-peak ripple. A subsequent DC/DC converter provides the required safety isolation and the backplane voltage rails (i.e. 12 V, 5 V) for the control cards in the crate. In order to implement a COTS-based radiation-tolerant PFC buck converter, the power MOSFET has to be severely over-rated in terms of blocking voltage (V_{DSS}). Additionally, the gate drive voltage (V_{GS}) has to be lower than normal so as to minimize threshold voltage drift with Total Ionizing Dose (TID). Both these derating measures lead to efficiency degradation owing to higher on-state resistance ($R_{DS,on}$) compared to typical cases. This paper also proposes design measures that can be taken to improve efficiency (up to 85–90%) in spite of the above constraints. This enables low-cost radiation-tolerant power supply development capable of withstanding a TID of 300 Gy, based on component-level radiation tests.

1 Choice of Topology: Boost versus Buck

Figure 1 shows the AC/DC power supply architecture for a typical 100 W unit and that for the proposed COTS-based radiation-tolerant design, called RaToPUS, a loose acronym for 'Radiation-Tolerant Power Supply' for the DI/OT project [1], [2]. PFC rectifier stages in many AC/DC power supplies are implemented using a boost topology which generates a 400 V DC bus at its output. While this is suitable for applications in radiation-free areas, it may not be a good choice for radiation-exposed applications, as explained below.

In order to minimize the probability of Single-Event Burnout (SEB) of the MOSFETs in the DC/DC stage, the breakdown voltage rating of these devices has to be chosen at double (or more) of the DC bus voltage [3], [4]. When using a PFC boost topology, this would necessitate the use of 800 V MOSFETs in the AC/DC as well as DC/DC stages of the power supply. Using such high voltage rated MOSFETs can lead to large on-state resistance ($R_{DS,on}$) and thus low efficiency. Use of a buck topology for achieving PFC enables the choice of a lower DC bus voltage. Choosing a 48 V DC link (range: 36–72 V) ensures that only the AC/DC stage requires a higher voltage MOSFET, while the DC/DC stage can use much lower voltage rated MOSFETs with substantially lower $R_{DS,on}$, thus providing an efficiency improvement.

In addition, the use of an inrush current limiting negative temperature coefficient (NTC) thermistor would be mandatory in the PFC boost topology. However, the buck topology inherently allows inrush current limiting through a soft-start procedure, which makes it possible to: (1) eliminate the NTC thermistor thus saving some board space, (2) slightly improve efficiency (A 10 Ω cold resistance NTC could be at about 1 Ω when hot, still

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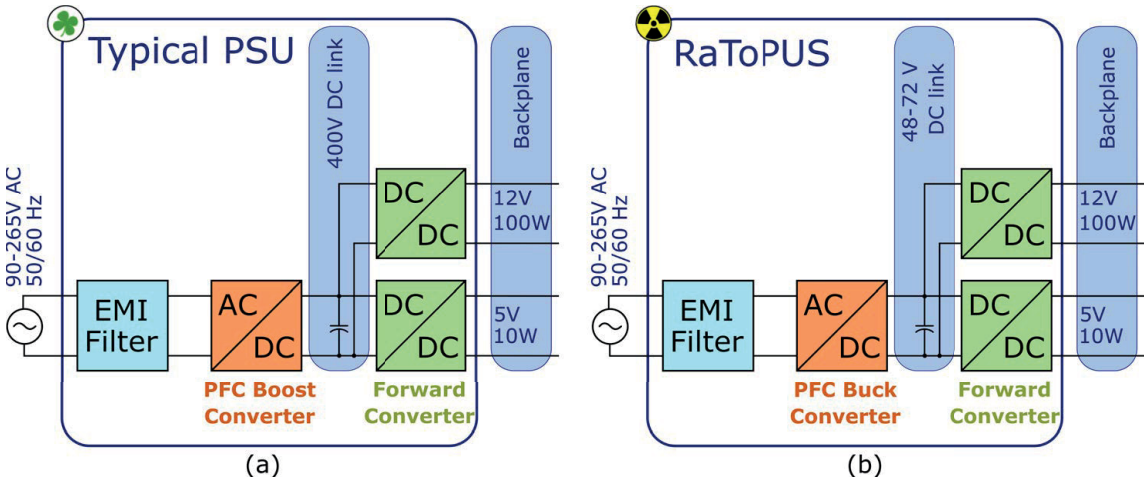

Fig. 1: (a) Typical 100 W AC/DC power supply architecture for radiation-free applications; (b) Proposed architecture (RaToPUS) for radiation-exposed applications.

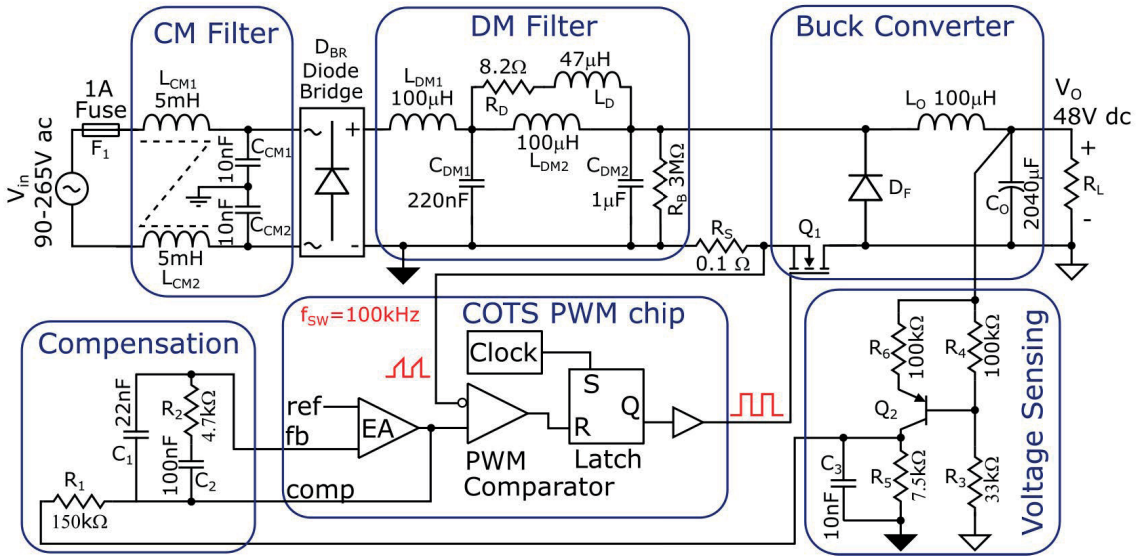

Fig. 2: Circuit schematic of the proposed PFC buck AC/DC converter including EMI filter (common-mode and differential mode) and control loop.

substantially large), and (3) use a fast blow type 1 A fuse which provides for better fire safety.

2 Design of Circuit Components

The circuit schematic for the proposed PFC buck AC/DC converter, as part of RaToPUS power supply, is shown in Fig. 2 and its design is based on the designs presented in [5]–[7]. Figure 3 shows the annotated photograph of the printed circuit board (PCB) prototype. Note that the upper half of the PCB is left vacant for the DC/DC converter that will form the next stage of the full power supply.

2.1 PFC Buck Converter Design

For the PFC buck converter, 600 V rated devices are chosen for the diode bridge (D_{BR}, Fairchild GBU6J) and freewheeling diode (D_F, Fairchild FFPF10H60S), and an 800 V rated device is chosen as the MOSFET (Q_1, Infineon IPA80R280P7). The design selection of the remaining components are described below.

2.1.1 Output Capacitor Sizing

The minimum required output capacitance in order to meet the output voltage ripple specification is

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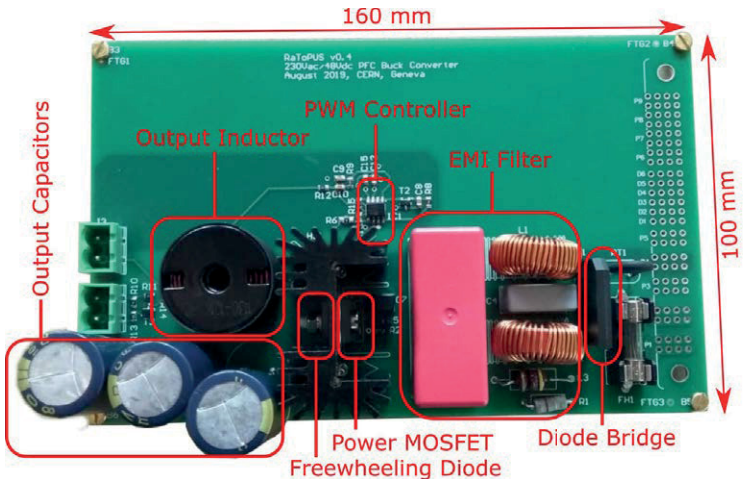

Fig. 3: Annotated photograph of the proposed 100 W PFC buck AC/DC converter PCB prototype.

calculated as follows [7]:

$$C_o = \frac{P_o \cdot (1-\theta_{cond})}{\Delta V_o \cdot V_o \cdot 2 f_{ac}} = \frac{125 \cdot (1-0.75)}{0.1 \cdot 48 \cdot 48 \cdot 100} \approx 1360\,\mu\text{F}, \quad (1)$$

where P_o is the output power, θ_{cond} is the conduction angle as a fraction of the total cycle, V_o and ΔV_o are the output voltage and the output voltage ripple, f_{ac} is the AC line frequency. The maximum required output power is 110W/η_{dcdc}=125 W, assuming a worst case DC/DC efficiency η_{dcdc} of 88%. The worst case (minimum) θ_{cond} of 0.75 is obtained at low line i.e. when V_{in}=90 V RMS.

The minimum output capacitance required to satisfy a 6 ms hold-up time (t_{hu}) is given by:

$$C_o = \frac{2 \cdot t_{hu} \cdot P_o}{V_{o,min}^2 - V_{o,min,reg}^2} \approx 1890\,\mu\text{F}, \quad (2)$$

where $V_{o,min}$=45.7 V is the minimum DC bus voltage at the trough of the ripple and $V_{o,min,reg}$=36 V is the minimum bus voltage for which the DC/DC stage can still maintain regulation at its output. Allowing for tolerances, the chosen capacitance of 2040 µF (680 µF x 3 in parallel) is well above the calculated values in Eqs. (1) and (2).

2.1.2 Output Inductor Sizing

The output inductor is sized so that the converter operates in continuous conduction mode (CCM) over the full line voltage range, at rated power. The required minimum value of inductance is calculated as follows [7]:

$$L_o = \frac{1}{2 f_{sw} I_{in,pk}} (V_{in,pk} - V_o) \frac{V_o}{V_{in,pk}} \approx 38\,\mu\text{H}, \quad (3)$$

where f_{sw}=100 kHz is the nominal switching frequency, $I_{in,pk}$=0.7 A is the peak of the filtered input current waveform, $V_{in,pk}$=375 V is the peak of the input voltage waveform at maximum line. The chosen inductance of 100 µH is well above the minimum required value.

2.2 EMI Filter Design

As shown in Fig. 2, the common-mode filter consists of a standard arrangement of a common-mode choke (coupled inductors L_{CM1} and L_{CM2}) and two Y-capacitors (C_{CM1} and C_{CM2}). The differential-mode filter consists of a two-section LC filter with $R_D L_D$ parallel damping to ensure that the converter control loop does not start oscillating because of adding the filter. This combination of cascaded LC filtering and $R_D L_D$ damping provides the most compact filter design [8]. The filter components were designed in accordance with the procedure outlined in [9].

2.3 Controller Design

The control pulses for the MOSFET are obtained from a type-II compensator based current-mode controller implemented using a standard COTS PWM controller IC, e.g. TL2843 (tested under radiation up to 500 Gy). Figure 4 shows the Bode plot of the type-II compensator as well as that for the loop gain. The compensator pole and zero locations are set as follows [10]: a zero near the $L_O C_O$ resonant frequency ($f_O \approx 350$ Hz), a low frequency pole around $0.15 f_O$, and a high frequency pole at the ESR zero of the output

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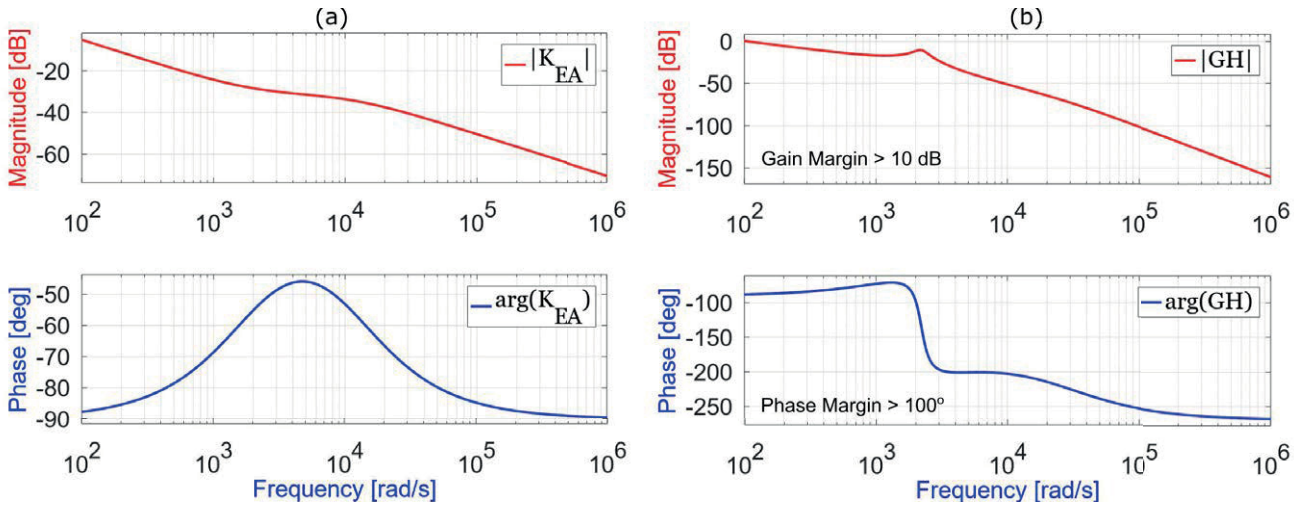

Fig. 4: Bode plots for (a) error amplifier gain (K_{EA}) with type-II compensation, and (b) loop gain (GH).

capacitor ($f_{ESR} = 1/2\pi R_{ESR} C_O \approx 1500$ Hz).

$$f_{p11} = \frac{1}{2\pi R_1 C_1} \approx 50\,\text{Hz}, \quad (4)$$

$$f_{z22} = \frac{1}{2\pi R_2 C_2} \approx 350\,\text{Hz}, \quad (5)$$

$$f_{p21} = \frac{1}{2\pi R_2 C_1} \approx 1500\,\text{Hz}. \quad (6)$$

The chosen values of resistances and capacitances satisfying the above set of equations are annotated in the compensation section of Fig. 2.

Owing to the use of a low-side MOSFET, the controller ground is different from the output side ground. This necessitates a voltage sensing circuit (see Fig. 2) that translates the measured output voltage from the output ground to the controller ground. This is achieved by converting the voltage signal into a current (using a PNP BJT, Q_2) before converting back to a voltage referenced to the new ground.

3 Design Measures for Radiation Tolerance

For radiation-tolerant system design, one approach is to choose only those components that are qualified as radiation-hard by the manufacturers. However, this approach can be prohibitively expensive, especially in large numbers, as the cost of radiation-hard components is typically one or two orders of magnitude higher than COTS components with similar electrical specifications. Hence, we take an alternate approach of using COTS components that we qualify by carrying out radiation tests to select specific part numbers (and batch numbers) which are found to degrade minimally under radiation.

In order to ensure radiation tolerance while still using COTS components, the following measures are taken. The MOSFET is identified as a vulnerable component in radiation environment owing to (1) Threshold voltage (V_{th}) drift with accumulating Total Ionizing Dose (TID) that could potentially make the MOSFET uncontrollable, and (2) Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) events that cause immediate catastrophic failure owing to shorting of the MOSFET. In order to address the V_{th} drift issue, the gate drive voltage is reduced to 10 V instead of the typical 12–15 V. This is done because the magnitude of the drift is known to increase with gate bias. Therefore a lower gate bias ensures lower drift keeping the V_{th} above zero until the end of life of the product. This ensures that there is no need to use a gate drive with negative voltage capability. Also, a negative V_{GS} is known to increase the likelihood of SEGR, and is hence good to avoid. In order to address the SEB issue, the breakdown voltage of the MOSFET (V_{DSS}) is chosen at a value double that of the maximum blocking voltage the device is expected to see in operation. In this case, at high line of 265 V RMS, the peak of the AC waveform is about 375 V. Hence an 800 V MOSFET is chosen, while a 400/500 V device would have sufficed in a

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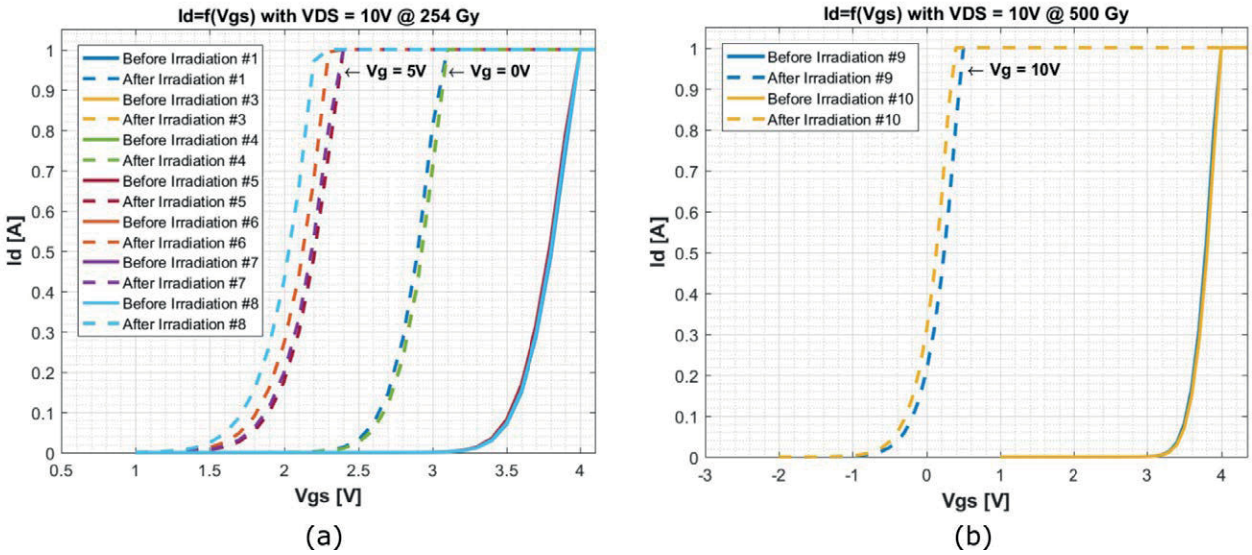

Fig. 5: Radiation test results for 800 V MOSFET IPA80R280P7: $V_{GS,th}$ drift with TID.

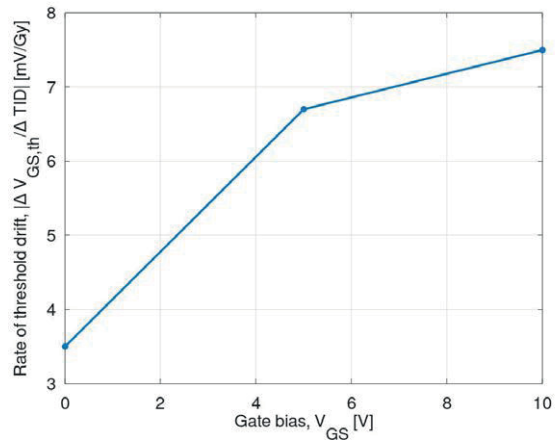

Fig. 6: Rate of threshold voltage drift with respect to gate bias for 800 V MOSFET IPA80R280P7.

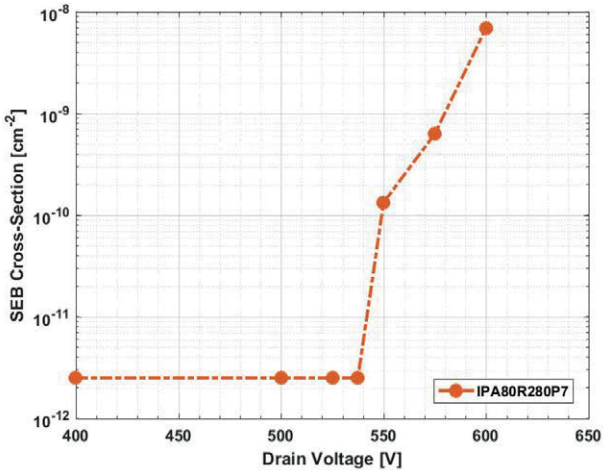

Fig. 7: Radiation test results for 800 V MOSFET IPA80R280P7: SEB cross-section versus V_{DS}.

radiation-free application.

In addition to the above derating measures, the power MOSFET was tested under radiation. Figure 5 depicts the observed drift in the gate threshold voltage ($V_{GS,th}$) with TID. The drift is larger when the gate bias is larger, as summarised in Fig. 6. The worst case scenario in terms of threshold voltage drift occurs at low line (V_{in}=90 V RMS) as it requires the highest duty ratios. At 300 Gy, $V_{GS,th}$ can potentially shift down from 2.5 V to 0.4 V. This worst case value is well above 0 V, which means that the MOSFET is still controllable up to the specified accumulated dose of 300 Gy.

Figure 7 plots the SEB cross-section versus V_{DS} for the chosen MOSFET. No SEBs are observed for V_{DS} below 550 V. This is well above the worst case blocking voltage in the power converter (375 V), and hence the design is safe.

Unfortunately, the radiation-tolerance measures mentioned earlier—V_{GS} derating and V_{DS} derating—result in a higher than typical $R_{DS,on}$ thus causing higher losses and lower efficiency. In order to improve the efficiency of the AC/DC converter, the following measures can be taken. (1) Increase the nominal DC bus voltage closer to 72 V, which increases the average duty of the buck converter thus improving its efficiency. (2) Use a silicon carbide (SiC) Schottky diode as the

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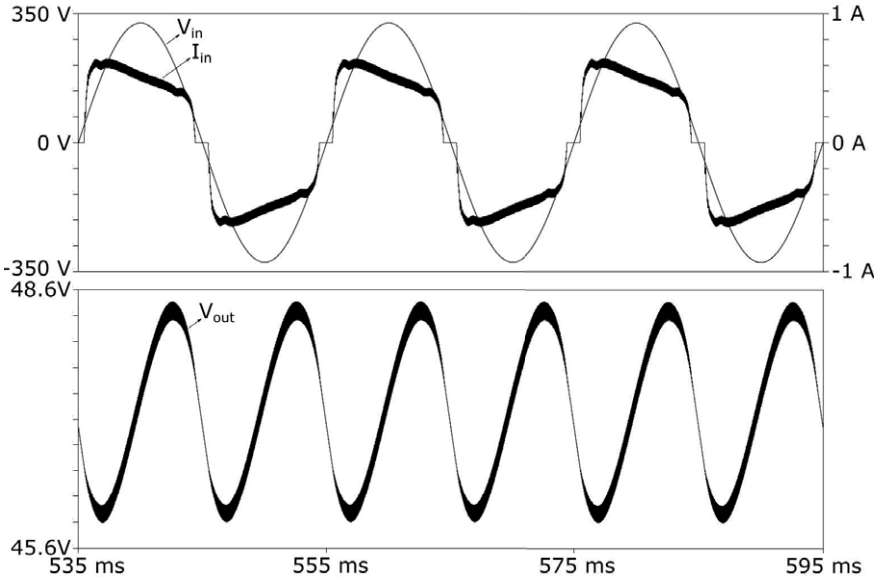

Fig. 8: LTspice simulation waveforms for PFC buck converter with 48 V output at steady state. The top panel shows AC input current (I_{in}) and input voltage (V_{in}). The bottom panel shows the output DC bus voltage (V_{dc}).

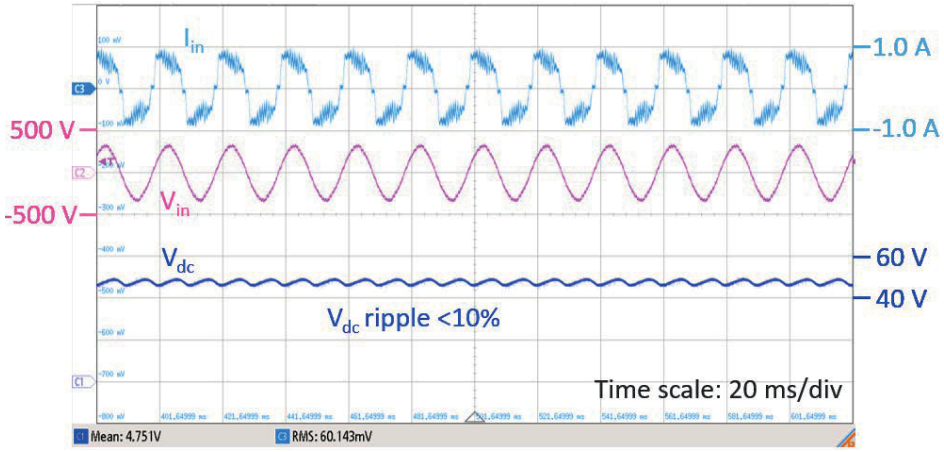

Fig. 9: Experimental waveforms for PFC buck converter with 48 V output at steady state: I_{in}, V_{in}, V_{dc}

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freewheeling diode, instead of a silicon hyperfast diode. Apart from having no reverse recovery losses, Schottky diodes tend to have a positive temperature coefficient of forward voltage, which allows for parallel operation of two devices thus reducing conduction losses.

4 Results and Discussion

Figure 8 shows the LTSpice simulation results for the PFC buck converter at steady state with a constant load of 115 W. The input current is seen to have a high power factor (>0.9) albeit with a small blanking period at the zero-crossing when input voltage magnitude is less than 48 V. The output voltage is seen to be regulated with a ripple of about 2.6 V (5.4%).

Corresponding experimental results are shown in Fig. 9. Figure 10 shows the zoomed-in waveforms of the MOSFET voltage and current at the peak of the AC voltage waveform. Figure 11 shows the experimental results for dynamic loading when the load switches between 0.5 A and 1.0 A with a slew rate of 5.0 A/ms. Note that most of the dynamic loading will be handled by the DC/DC stage that follows the PFC buck AC/DC converter, which means that the AC/DC stage can have a low bandwidth (∼10 Hz).

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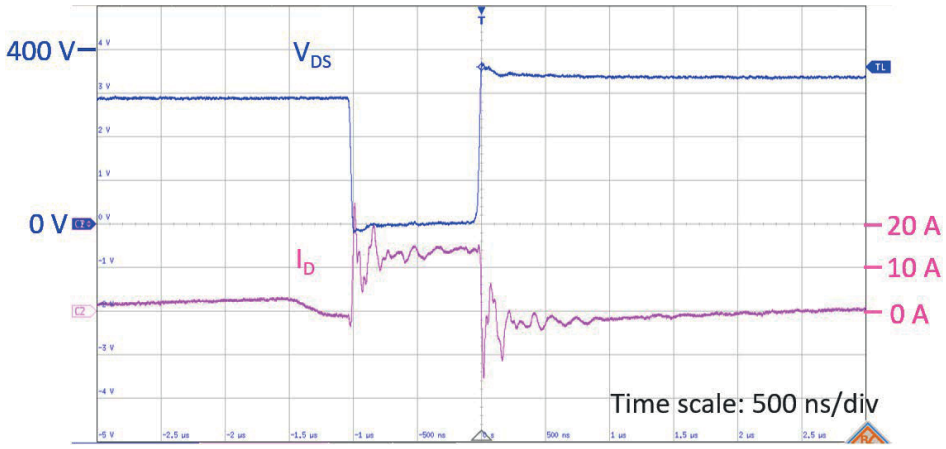

Fig. 10: Experimental waveforms for PFC buck converter with 48 V output at steady state: Zoomed-in view of MOSFET voltage (V_{DS}) and current (I_D) at the peak of the AC voltage.

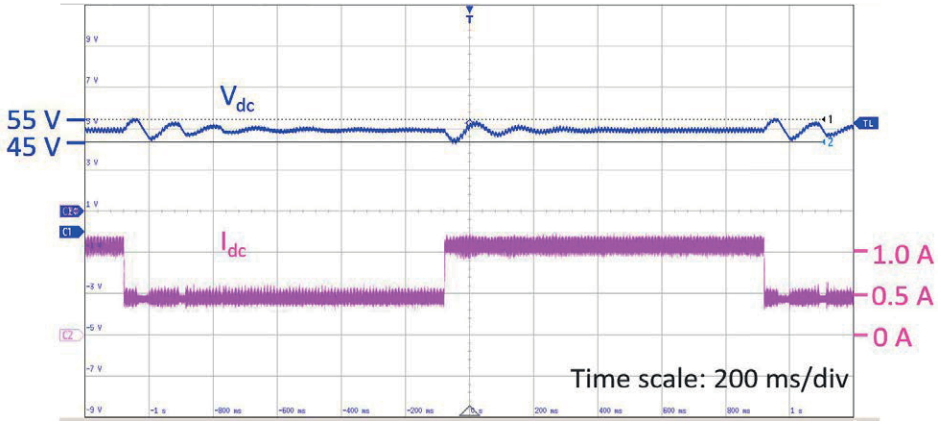

Fig. 11: Experimental waveforms for PFC buck converter with 48 V output during dynamic loading. The transient dip and rise in the bus voltage is well within specifications (36–72 V) for the DC/DC stage to continue to maintain regulation.

Figure 12 shows the measured variation of efficiency and power factor with change in load. The efficiency is found to be greater than 85% for load greater than 50% of the rated load. The power factor is found to be greater than 0.9 for load greater than 60%.

5 Conclusion

This paper proposes the design of a 100 W radiation-tolerant PFC buck AC/DC converter that uses COTS components. Key design measures for radiation tolerance are presented and required changes for performance improvements are suggested. The proposed design is validated by simulation, experiments, and component-level radiation tests. The converter achieves output voltage ripple below 10%, power factor greater than 0.9, efficiency above 85%, and can withstand a TID up to 300 Gy.

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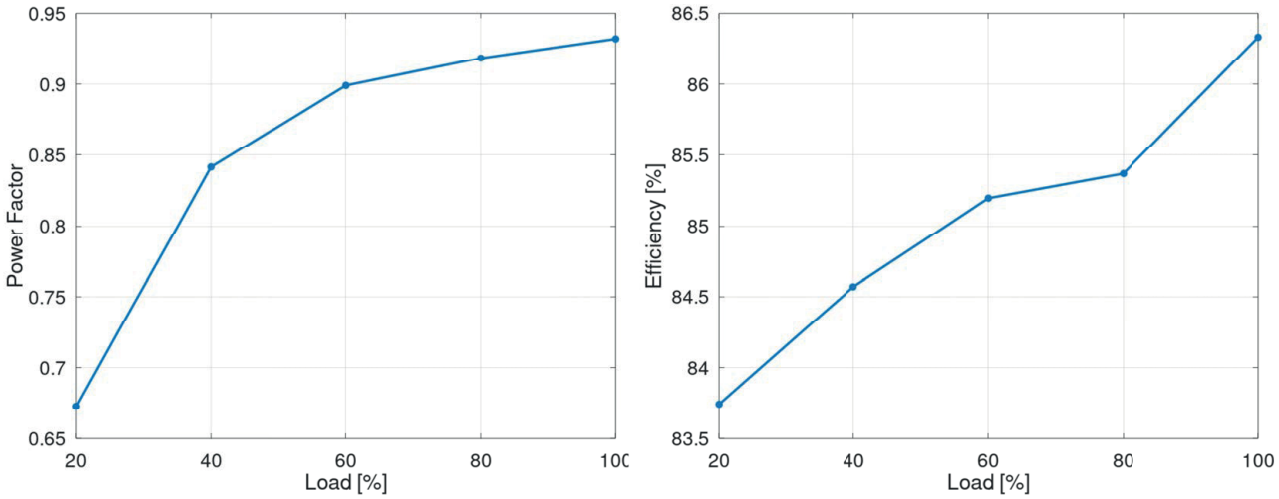

Fig. 12: Experimental measurements for efficiency and power factor of the PFC buck converter prototype.

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