R2E ACF DC/DC: List of changes from v1 to v2

1. Active Clamp Forward Converter
    a. Use correct symbol and footprint for input-side bulk capacitor (C22).
    b. Change main MOSFET T4 from SQM10250E to IPB320N20N3 (latter passed radiation test).
    c. Add SMD heatsink (HS1) for main MOSFET.
    d. Eliminate D2 and D4 (SMBJ150CA) originally added for power MOSFET protection. These do not seem to serve any purpose, and add clutter in the layout.
    e. Combine R35 and R36 (20Ω each) in the current-sense circuit into a single 10Ω resistor.
    f. Use correct symbol and footprint for secondary-side Schottky diodes (flipped and mounted on bottom side).
    g. Use more resistors for the diode snubbers (4 instead of 2 for each diode) in order to have better thermal derating.
2. Auxiliary Power Supply
    a. Combine R14 and R133 (10kΩ each) in the bootstrap bias into a single 100kΩ resistor. This will reduce standby power and increase efficiency (slightly).
    b. Divert some of the heating in the bootstrap bias from the BJTs (T1 and T2) to the series resistors by using a larger resistance (430Ωx3/2=645Ω), and more number of them (6 instead of 4) to manage the heat dissipation.
    c. Change R9 from 27Ω to 39Ω to employ T1 at a lower Icc.
    d. Increase copper areas for T1 and T2 (min. 2cm^2) to improve thermal management.
    e. Change auxiliary bias from LM317-based to Zener-BJT-based in order to tackle large voltage reference drift which resulted in Vcc2 losing to Vcc1 (poor efficiency).
3. PWM Controller and MOSFET Driver
    a. Change Delay-2 circuit from MOSFET-based to BJT-based. Remove D17 and D18. Change R48 from 100Ω to 22kΩ. Change R50 from 100kΩ to 3.9kΩ. Change R44 from 1.5kΩ to 2.2kΩ.
    b. Delay-1 circuit: Change R62 and R63 from 4.7kΩ to 15kΩ each.
    c. Slope compensation: Change R79-C49-R86 from 470Ω-100nF-3kΩ to 680Ω-1uF-3.3kΩ.
    d. Modify soft-start circuit because of change in OCP circuit. Change C29-R42 from 4.7uF-10kΩ to 10uF-1MΩ.
4. Protection Circuits
    a. Modify OCP circuit to stop spurious trips because of comparator input bias current drift under radiation. Change R52-C36-R60-R55-R49-R54 from 1kΩ-1nF-10MΩ-6.8kΩ-47kΩ-22kΩ to 100Ω-22nF-560kΩ-3.9kΩ-12kΩ-6.8kΩ. Add a hysteresis resistor, R134=220kΩ.
    b. Modify OTP circuit to better simulate over-temperature condition during testing. Change R68-R69 from 10kΩ to 3.3kΩ each.
    c. Modify UVLO circuit for disable the DC/DC for Vin<40V (instead of 36V) as there seem to be stability issues for Vin=36-40V. Change R45-R53 from 287kΩ-22kΩ to 220kΩ-15kΩ.

5. Output Voltage Sensing and Compensation
    a. Change C58 in the compensation circuit from 220pF to 560pF in order to avoid 7kHz oscillation at low line and high load conditions.

Possible further improvements (withheld for further investigation)

1. Place RT2 PTC thermistor close to T1 (pnp BJT in bootstrap bias).
2. Use 75um Cu instead of 35um for better heat dissipation and lower resistances.
3. Separate control and power grounds using 0Ω resistor (?).
4. Change 220Ω feedback resistors (R124, R125) from 0.1% to 1% tolerance.