R2E ACF DC/DC Design Report

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1. Technical specifications

Parameter	Value
Input voltage range	36-72V; Nominal: 48V
Input current	Maximum: 3 A @ 36V, full load Nominal: 2.3 A @ 48V, full load
Input inrush current	<10 A @ 48 V
Output	12 V, 8.33 A, 100 W
Output voltage ripple + noise (peak-to-peak value of PARD)	100 mV
Line regulation	±3%
Load regulation	±5%
Efficiency	≥90% @ 48 V
Switching frequency	200 kHz
Transient response	10% maximum deviation; Returns to nominal output within 1 ms maximum.
EMI filter	EN55022 Class B, FCC Part 15
Isolation	4000 V DC (input to output)
Leakage current	<20 mA
Over-voltage protection (OVP)	Set at 120% of nominal output voltage (trip point)
Short-circuit protection (SCP)	Hiccup mode
Over-current protection (OCP)	Set at 120% of nominal output current (current limit but no trip)
Total Ionizing Dose (TID)	400 Gy
Thermal environment: Ambient temperature range Active cooling	 0 to +65^{o}C No
PCB dimensions	100 mm x 160 mm x 35 mm
External control	SHUTDOWN pin for remote switching ON/OFF
Redundancy/load sharing	Two instances sharing full load: +12 V, 100 W with ±10% tolerance (40%/60% or better)

2. Power converter topology selection and design

The typical topology options for a 100W DC/DC converter are: flyback converter, 1-switch forward converter (hard switched), 2-switch forward converter (hard switched), and active clamp forward converter (zero voltage switching). The active clamp forward (ACF) topology is selected because of the following reasons:

1. Enables usage of MOSFET and diodes with lower voltage rating compared to conventional and resonant-reset forward converters. This leads to improved efficiency because of the reduced conduction losses owing to lower $R_{DS,on}$ of MOSFET and lower forward voltage drop of diode.
2. Zero-voltage switching (ZVS) at turn-on of the main MOSFET leads to lower switching losses and hence higher efficiency compared to hard switched forward converter.

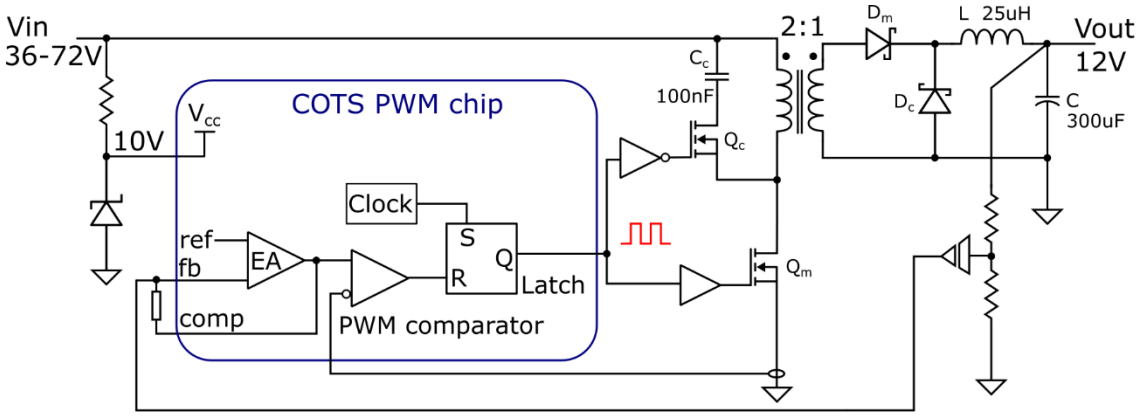

Fig. 1: Simplified schematic of the active clamp forward DC/DC converter

Fig. 1 shows a simplified schematic of the ACF DC/DC converter using a commercial off-the-shelf (COTS) current-mode PWM chip such as UC3843. The nomenclature of some of the key components is as follows: Q_m is the main MOSFET, Q_c is the clamp MOSFET, C_c is the clamp capacitor, D_m is the main rectifier diode, D_c is the catch (freewheeling) diode, L is the output filter inductor, and C is the output filter capacitor.

In the nominal case with an input voltage of 48V, it is advisable to aim for a duty ratio (D) of 0.5 so that the main and catch diodes conduct for equal time thus resulting in an even thermal stress on both. To get a 12V output voltage from a 48V line, the required transformer turns ratio (secondary/primary) is given by,

$$N = \frac{V_o}{D_{nom}V_{in}} = \frac{12}{0.5 \times 48} = 0.5$$

Owing to non-idealities such as diode forward voltage, and voltage drop in all series resistances and due to leakage flux, the chosen N has to higher than the ideal value, say 0.55.

Main and clamp MOSFETs selection:

The steady-state duty ratio for any input voltage is calculated as follows:

$$D_{ss} = \frac{V_o + V_s}{NV_{in}}$$

Where V_o is the output voltage, V_s is the sum total of all series voltage drops (diode forward voltage, series resistances, leakage flux etc.) referred to the secondary side, N is the transformer turns ratio (secondary/primary), and V_{in} is the input voltage. During dynamic loading, the duty cycle can be assumed to go to a maximum value of say 8% above the steady state value i.e.

$$D_{dyn,max} = 1.08D_{ss}$$

Fig. 2 plots the variation of the steady state and dynamic (maximum) values of the duty ratio with input voltage, as per the above two equations, assuming $V_s = 1$ V and N = 0.55. The blocking voltage for both MOSFETs is calculated as follows:

$$V_{DS} = V_{in} + V_c = V_{in} + \frac{V_{in}D}{1-D} = \frac{V_{in}}{1-D}$$

Where V_c is the clamp capacitor voltage. Fig. 3 shows the variation of MOSFET V_{DS} with respect to input voltage as per the above equation. Dynamic loading during low line (minimum V_{in}) results in the worst case blocking voltage ($V_{DS,max}$) of about 125V. Considering 50% derating for radiation, **250V devices should suffice**. Note that reducing the transformer turns ratio below 0.55 can significantly increase the required MOSFET blocking voltage as the rate of change of V_{DS} with V_{in}, i.e. dV_{DS}/dV_{in} is high in the low V_{in} region.

Table 1 lists the 250V MOSFETs under consideration for the main and clamp MOSFETs. Because of its lowest $R_{DS,on}$ and availability in a standard SMD D2PAK package, Vishay SQM10250E is selected as the main MOSFET. Unlike the main MOSFET, the clamp MOSFET only conducts the magnetizing current and not the load current, thus permitting a higher $R_{DS,on}$ and smaller package (DPAK). The Infineon IPD600N25N3 is selected as the clamp MOSFET. The $V_{GS,th}$ drift (due to TID) for selected MOSFETs must not be bad enough to warrant use of negative gate drive.

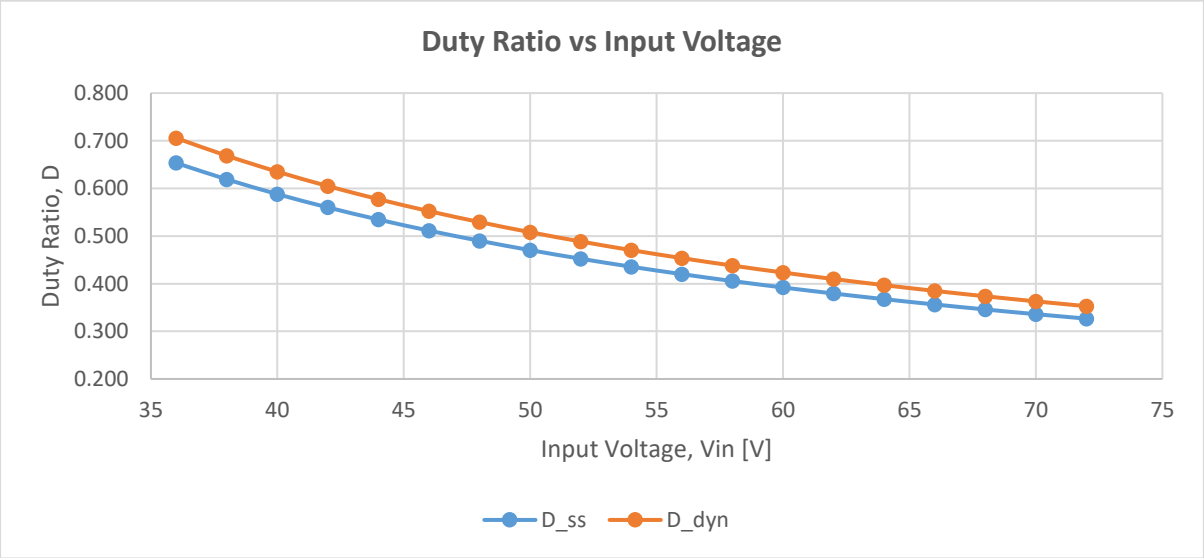

Fig. 2: Variation of duty ratio (steady state and dynamic maximum) with input voltage. D_{max}=0.7.

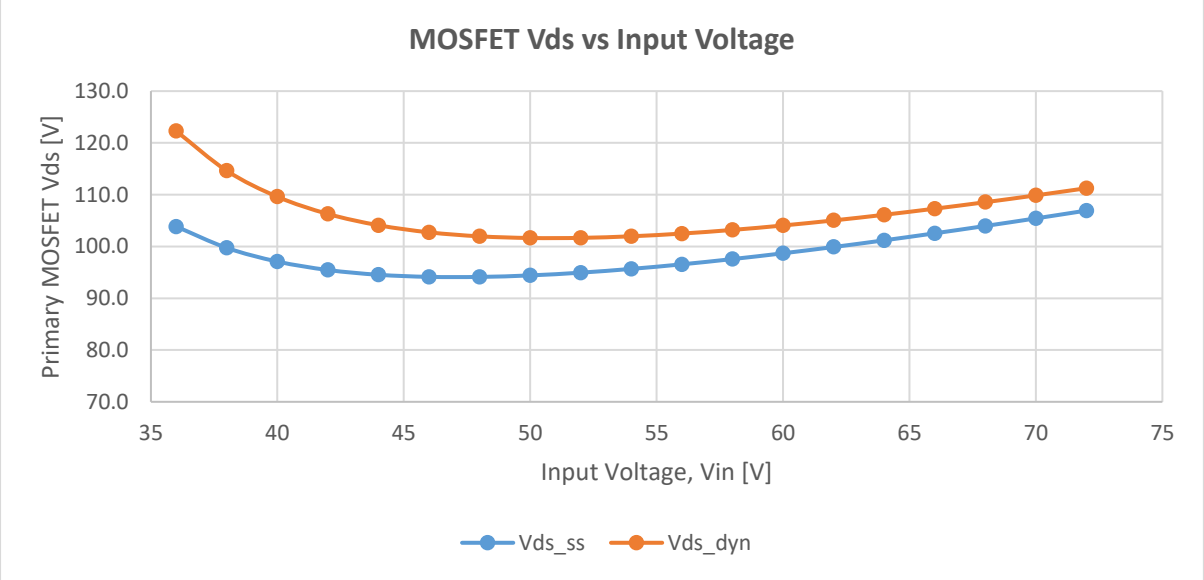

Fig. 3: Variation of MOSFET V_{DS} (steady state and dynamic maximum) with input voltage. $V_{DS,max}$ = 125V.

Table 1: Options for main MOSFET (200-500V)

Part Number	Vendor	V_{DSS}	Max. $R_{DS,on}$*	Max. Q_g	C_{oss} at V_{DS}=100V	Package	Radiation Hardness [1]
IPB107N20N3	Infineon	200 V	11 mΩ	87 nC	400 pF	D2PAK	--
SQM90142E	Vishay	200 V	15 mΩ	85 nC	400 pF	D2PAK	--
SUM90140E	Vishay	200 V	17 mΩ	96 nC	300 pF	D2PAK	--
SUM90220E	**Vishay**	**200 V**	**22 mΩ**	**48 nC**	**170 pF**	**D2PAK**	To be rad tested
IPB320N20N3	**Infineon**	**200 V**	**32 mΩ**	**29 nC**	**180 pF**	**D2PAK**	To be rad tested
IPB200N25N3	Infineon	250 V	20 mΩ	86 nC	320 pF	D2PAK	--
SQM10250E‡	**Vishay**	**250 V**	**30 mΩ**	**75 nC**	**300 pF**	**D2PAK**	To be rad tested
IPB17N25S3	Infineon	250 V	0.10 Ω	19 nC	<100pF	D2PAK	--
IRFH5025PbF	IR	250 V	0.10 Ω	37 nC		PQFN	- No SEB up to 175V - $V_{GS,th}$<0V at 325Gy (for V_{GS}=10V)
IRF634	Vishay	250 V	0.45 Ω	41 nC		TO220	No SEB up to 230V
FDP26N40	Fairchild	400 V	0.16 Ω	60 nC		TO220	--
FQP17N40	Fairchild	400 V	0.27 Ω	60 nC		TO220	--
FDP15N40	Fairchild	400 V	0.30 Ω	36 nC		TO220	--
IPA50R280CE	Infineon	500 V	0.28 Ω	33 nC	49 pF	TO220	--
IPA50R380CE	Infineon	500 V	0.38 Ω	25 nC	40 pF	TO220	--
IPA50R500CE	Infineon	500 V	0.50 Ω	19 nC	31 pF	TO220	--

*At V_{GS} = 10 V ‡Used in v0

Table 2: Options for auxiliary MOSFET

Part Number	Vendor	V_{DSS}	Max. $R_{DS,on}$*	Max. Q_g	C_{oss} at V_{DS}=100V	Package	Radiation Hardness
IPD320N20N3	**Infineon**	**200V**	**32 mΩ**	**29 nC**		**DPAK**	To be rad tested
SUD90330E-GE3	**Vishay**	**200V**	**38 mΩ**	**32 nC**		**DPAK**	To be rad tested
IPD600N25N3‡	**Infineon**	**250 V**	**60 mΩ**	**29 nC**		**DPAK**	To be rad tested
FQD18N20V2	Fairchild	200 V	0.14 Ω	26 nC		DPAK	--
IRFH5025PbF	IR	250 V	0.10 Ω	37 nC		PQFN	- No SEB up to 175V - $V_{GS,th}$<0V at 325Gy (for V_{GS}=10V)
IPD5N25S3-430	Infineon	250 V	0.43 Ω	6 nC		DPAK	No SEB up to 100V

*At V_{GS} = 10 V, T = 25°C ‡Used in v0

Secondary-side diodes selection:

Fig. 4 and 5 plot the variation of the peak inverse voltage with input voltage for the main rectifier diode and the freewheeling diode respectively. Correspondingly, the maximum values of the peak inverse voltage are 48V and 37V. The worst case for the main diode is seen during low line (V_{in}=36V) and that for the freewheeling diode is seen at high line (V_{in}=72V). Taking into account some headroom for ringing, **60V devices should suffice**. Additionally, sharing the load current on multiple diodes will reduce the forward voltage drop and hence the conduction loss. Dual Schottky diodes within the same package can be closely matched in terms of current sharing as their junction temperatures are almost the same. However, when the diodes are in separate packages it is better to have a separate filter inductor for them. Table 2 lists the Schottky power diodes in consideration for this design. In order to use four diodes for sharing the load current, the circuit configuration in Fig. 6 is used.

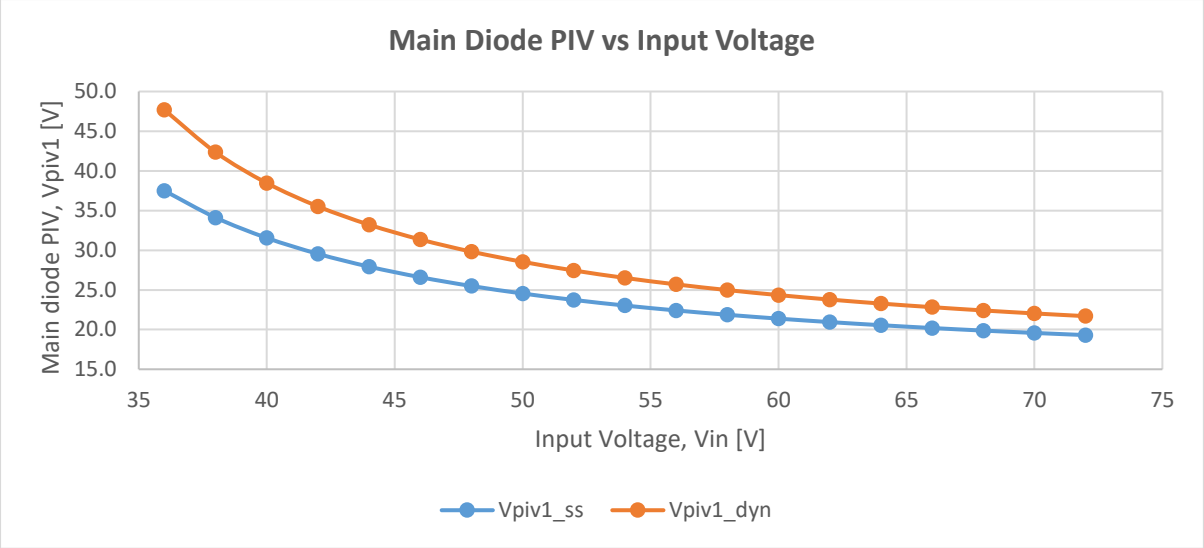

Fig. 4: Variation of main rectifier diode peak inverse voltage with input voltage. $V_{PIV1,max}$ = 38V (steady state), 48V (dynamic).

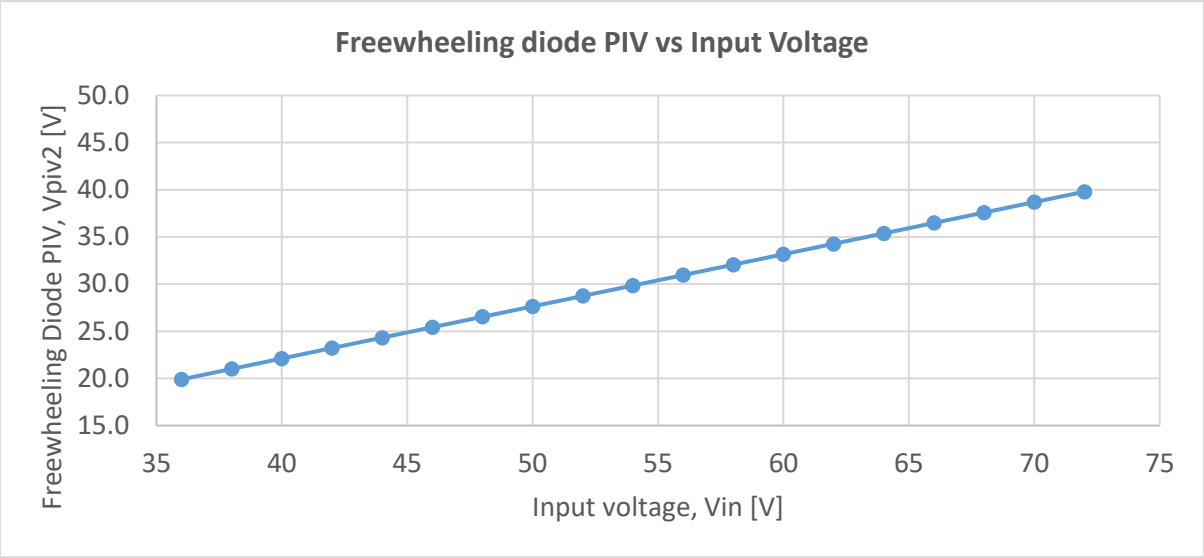

Fig. 5: Variation of freewheeling diode peak inverse voltage with input voltage (same for steady state and dynamic loading cases, i.e. independent of duty ratio). $V_{PIV2,max}$ = 40V.

Table 2: Power Schottky diode (common-cathode dual type) options

Part Number	Vendor	Blocking Voltage	V_F @2A, 75°C	V_F @5A, 125°C	C_J @30V	I_R @50V, 125°C	Package
DSTB2045C	Littelfuse	45V	0.32V*	0.33V*	0.40nF	20 mA	D2PAK
STPS40L45P	ST	45V	0.32V*	0.33V*	0.50nF	100 mA	D2PAK
HTR40U60CT	Multicomp	60V	0.24V*	0.24V*	0.45nF	50 mA	TO-220AB
HTR30L60CT	Multicomp	60V	0.30V*	0.30V*	0.35nF	10 mA	TO-220AB
HTR20L60CT	Multicomp	60V	0.32V*	0.32V*	0.25nF	9 mA	TO-220AB
MBR1060CTL	Multicomp	60V	0.39V*	0.53V*	0.08nF	10 mA	TO-220AB
RB215T-60NZC9	ROHM	60V	0.37V*	0.38V*	0.20nF	40 mA	TO-220FN
RB215T-60HZ	ROHM	60V	0.32V*	0.36V*	0.20nF	40 mA	TO-220
DST3060LC	**Littelfuse**	**60V**	**0.32V***	**0.36V***	**0.35pF**	**30 mA**	**TO-220AB**
STPS20L60CG‡	ST	60V	0.38V*	0.43V†	0.25nF	50 mA	D2PAK
STPS40SM60C	ST	60V	0.35V*	0.37V†	0.45nF	10 mA	D2PAK
MBRB2060CTG	ON Semi	60V	0.45V*	0.46V*	--	6 mA	D2PAK

RBR40NS60AFH	ROHM	60V	0.28V*	0.28V*	0.28nF	80 mA	D2PAK
RBQ30NS65AFH	**ROHM**	**65V**	**0.37V***	**0.42V***	**0.15nF**	**5 mA**	D2PAK
STPS20M80CG	ST	80V	0.43V*	0.52V†	0.15nF	2.7 mA	D2PAK
RBQ30NS100AFH	ROHM	100V	0.38V*	0.48V*	0.15nF	6 mA	D2PAK

*Typical value per diode †Maximum value per diode ‡Used in v0 demo board

In order to improve efficiency, the secondary-side diodes can be replaced by self-driven synchronous rectifiers. However, this can be challenging as the large input voltage range (36-72V) translates to large range of V_{GS} for the sync MOSFETs. This implies low efficiency at low line (because of high $R_{DS,on}$ at low V_{GS}) as well as high line (because of loss in clamping Zener diode across gate-source).

RC snubber design for secondary-side diodes:

Fig. 6-8 show the ringing voltage of the main rectifier diode (green waveform; STPS20L60C) for three different values of snubber capacitor. Based on these results, C_{sn} = 1nF is chosen as the optimal value. The measured ringing frequency f_r is about 6.8MHz. Correspondingly, the optimal damping resistor for the RC snubber is given by,

$$R_{sn} = \frac{1}{2\pi f_r C_{sn}} \approx 24\ \Omega$$

The maximum power dissipated in the snubber resistor is given by,

$$P_{sn} = C_{sn} V_{sn,max}^2 f_{sw} = 1 \times 10^{-9} \cdot 48^2 \cdot 200 \times 10^3 \approx 460\ mW$$

A single 1206 resistor can dissipate up to 250mW. Hence, two 12Ω 1206 resistors in series will suffice.

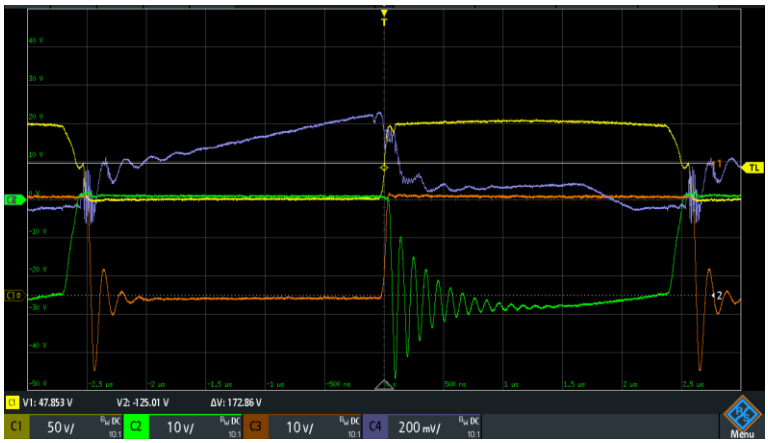

Fig. 6: C_{sn} = 220pF (for forward diode, shown in green above).

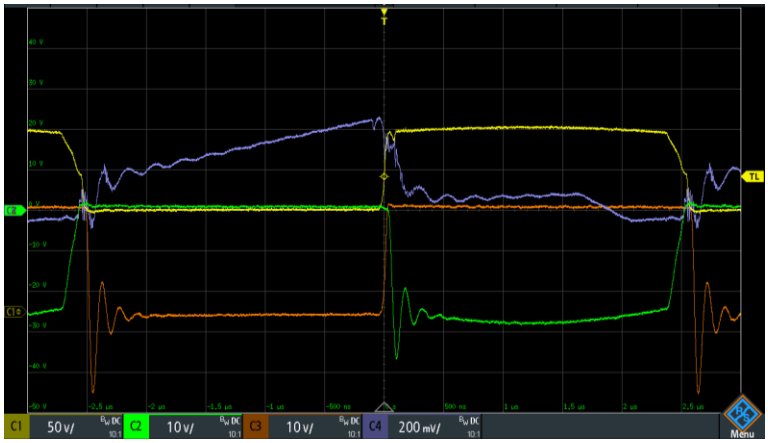

Fig. 7: C_{sn} = 1nF (for forward diode, shown in green above).

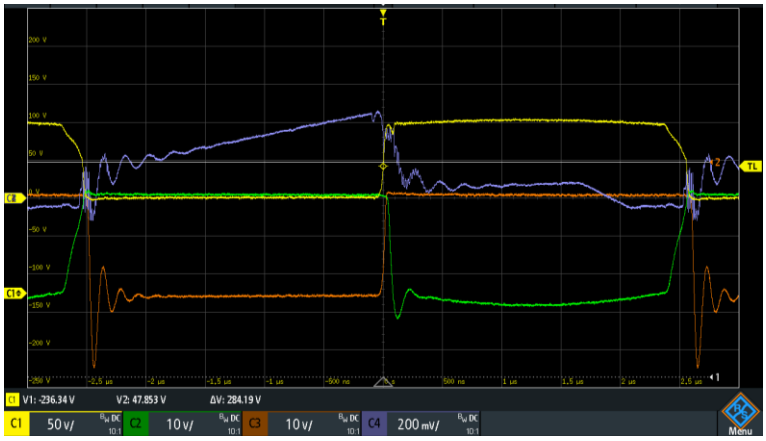

Fig. 8: C_{sn} = 2.2nF (for forward diode, shown in green above).

Loss budget at full load (100W):

Device	**Loss [W]**
Main MOSFET	1.0
Diodes:	3.2
Main rectifiers	1.6
Free-wheeling	1.6
Transformer	3.2
Inductor	1.7
Auxiliary PSU	0.8
Total	**9.9**

3. Magnetics design

Transformer design: The datasheet for this custom transformer is available here [2].

Parameter	Symbol	Value
Transformer turns ratio (secondary : primary)	N	0.55
Primary turns	N_1	11
Secondary turns	N_2	6
Permeance of gapped RM8 core	A_L	630 nH/turn^2
Transformer magnetizing inductance	L_m	76 µH
Transformer leakage inductance	L_{lk}	0.85 µH
Peak-to-peak magnetizing current	ΔI_m	1.53 A
Peak-to-peak magnetic flux	ΔB*	0.2 T
Primary winding resistance at 25°C, 200kHz	R_1	0.061 Ω
Primary winding resistance at 100°C, 200kHz	$1.3R_1$	0.080 Ω
Secondary winding resistance at 25°C, 200kHz	R_2	0.036 Ω
Secondary winding resistance at 100°C, 200kHz	$1.3R_2$	0.047 Ω

*$\Delta B = \frac{V_{in}DT_{sw}}{NA_e} = \frac{48 \cdot 2.5\times10^{-6}}{11 \cdot 55\times10^{-6}} = 0.2\ T$

In order to satisfy safety isolation requirements, the transformer requires 5 mm creepage between primary and secondary sides.

Possible measures to reduce copper loss:

1. Use a core taller than RM8 but with similar diameter of the central post so that all of the required turns of a given winding can be accommodated in a single layer (instead of two-layer primary and two-layer secondary). However, this will double the core loss (on account of the larger volume of iron) and lower the leakage inductance (potentially increasing MOSFET switching loss).
2. Attach a metal heat sink to the ferrite core. However, based on observation, there is no measureable change in efficiency. If copper loss is dominant, cooling the ferrite core of a transformer does not reduce the losses in, or improve the efficiency of, a transformer. This is because there is insulation and air between the copper and the ferrite which means cooling the iron does not result in a cooling the copper.

Inductor design: Output inductor with extra winding for deriving auxiliary power. The datasheet for this custom inductor is available here [3].

Parameter	Symbol	Value
Turns ratio (secondary : primary)	N	0.83
Primary turns (for auxiliary power supply)	N_1	18
Secondary turns	N_2	15
Permeance of gapped RM8 core	A_L	115 nH/turn^2
Secondary inductance	L	26 µH
Peak-to-peak inductor current at V_{in}=72V	ΔI_L	1.55 A
Peak-to-peak magnetic flux at V_{in}=72V	ΔB*	0.05 T
Primary winding resistance at 25°C, DC	R_1	0.409 Ω
Secondary winding resistance at 25°C, DC	R_2	0.025 Ω

*$\Delta B = \frac{V_o(1-D_{min})T_{sw}}{NA_e} = \frac{12 \cdot (1-0.327) \cdot 5\times10^{-6}}{15 \cdot 55\times10^{-6}} \approx 0.05\ T$

4. Auxiliary power supply design

Auxiliary power supply: Current budget

Part No.	Max. current [mA]	Comments
Main MOSFET gate	15	75 nC x 200 kHz
Clamp MOSFET gate	6	30 nC x 200 kHz
ACPL-C87B	15	VDD2 side
UC2843	7	
Miscellaneous	5	
Total	**48**	

Fig. 9 shows the circuit schematic for the auxiliary power supply, which comprises two main parts: (1) Bootstrap bias, and (2) Auxiliary bias. The auxiliary bias is powered by the auxiliary winding on the output inductor, which in turn is driven by the output voltage when the freewheeling diodes conduct. However, under some conditions the output voltage is not near its nominal value. For instance, (1) during power supply start-up, (2) during output short-circuit, (3) power supply external shutdown. In order to power the control circuits during these three scenarios, a bootstrap bias circuit, directly powered by the input DC bus (48V), is required.

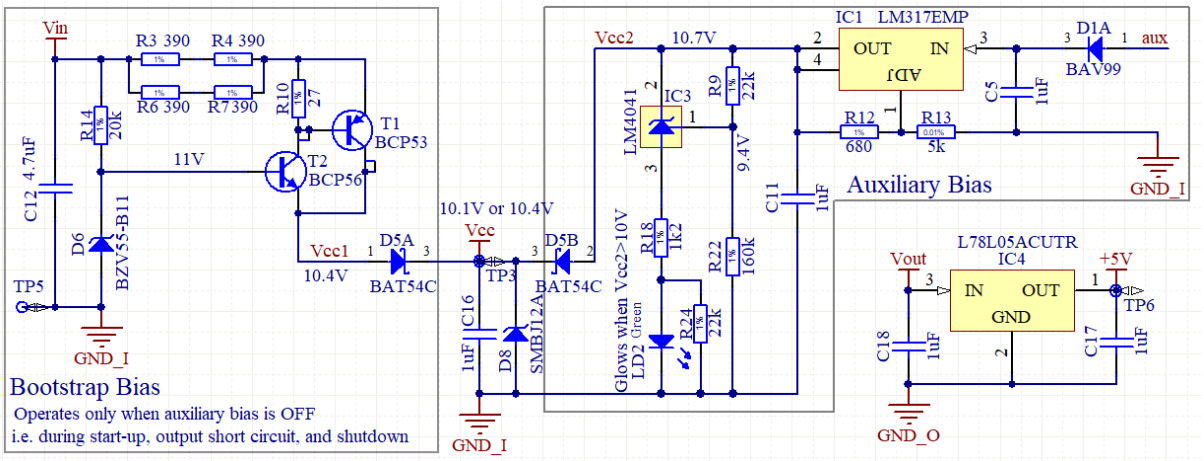

Fig. 9: Circuit schematic for auxiliary power supply, comprising a bootstrap bias circuit (on the left hand side, produces Vcc1) and an auxiliary bias circuit (on the right hand side, produces Vcc2). The higher of Vcc1 and Vcc2 'wins' by diode-ORing (via D5A and D5B) to produce the Vcc rail used for powering the control circuits.

Owing to the high value of V_{in} (36-72V) compared to V_{aux} (nominal 13-15V), the dissipation in the bootstrap bias is much higher than that in the auxiliary bias. In fact, this is why the auxiliary bias should 'win' over the bootstrap under normal operation. However, when V_{aux} is lower than its nominal value, it must be ensured that the power dissipation in the bootstrap bias is within safe bounds. Fig. 10 plots the power dissipated in the bootstrap bias for two extreme values of V_{in} (relevant octave script: bootstrap_bias_loss_calc.m). Expected value of the current drawn (I_{cc}) is about 50mA, which would result in just over 1W dissipation in each of the two transistors (npn and pnp). This loss can be managed with SOT-223 package and about 1 cm^2 copper area on top layer. Caveat: Using a 10V Zener diode, instead of a 11V one (D6), will result in a low value of Vcc (about 9.1V) which will keep the PWM and gate driver chips externally in UVLO, and the power supply will never start.

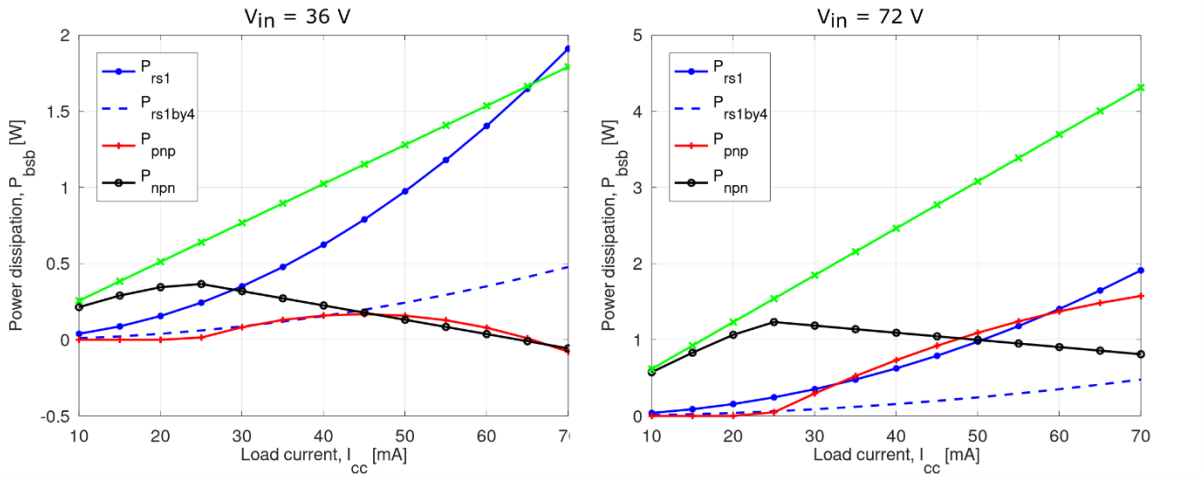

Fig. 10: Power dissipated in the bootstrap bias circuit (P_{bsb}) for different values of load current (I_{cc}). R_{s1} is the series resistor (390Ω) comprising of four 1206 resistors (R3, R4, R6, R7) each capable of dissipating 250 mW.

5. PWM controller and MOSFET driver design

Current sense circuit:

Using 70:1 current sense transformer (CST). X_{Lm} = 1.2 kΩ at 200 kHz. Hence, measurement error due to magnetizing inductance = 10Ω/1200Ω = 0.8% <1%.

Signal transistor selection:

$V_{GS,th}$ for BST82 reaches 0V at about 340 Gy, and is no longer controllable. BC817 seems to perform well until 1000 Gy, but draws too much current compared to MOSFETs. With V_{GS}=3.3V, the $V_{GS,th}$ for BSS316N is almost 0V at 500Gy, while that of **MGSF1N02** is about 0.3V. So definitely, the latter is better. Note that MOSFETs used in protection circuits (OCP/OVP/OTP/UVLO) are normally biased at 0V and hence do not experience large threshold voltage drift.

Unlike the MOSFETs used in protection circuits, that used in the PWM pulse delay circuit is not nominally biased at 0V. In order to minimize the average gate bias on this signal MOSFET, a series Zener diode is used between the PWM controller output and the delay MOSFET, as shown in Fig. 9 below. For a 50% duty ratio, and Vcc of 10V, this technique reduces average V_{GS} from 5V to 1.9V. However, addition of the Zener diode also raises the off-state V_{GS} from 0V to about 0.7V, which could be higher than the MOSFET threshold voltage at large TID. This will result in the signal MOSFET being always on irrespective of the pulses coming in. In order to avoid this problem, Schottky diodes are added in parallel with the Zener diode (Fig. 11) to lower the off-state V_{GS} to about 0.2V (Fig. 12).

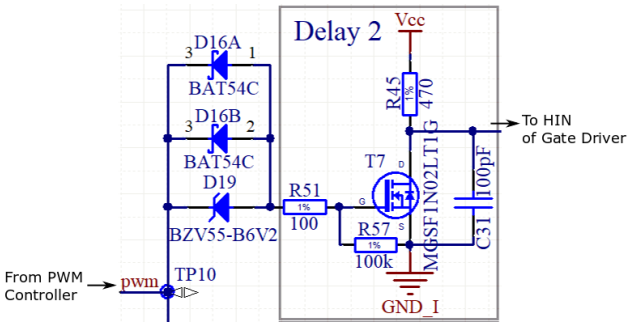

Fig. 11: Circuit schematic for increasing radiation tolerance of signal MOSFET (MGSF1N02L) by reducing the average gate bias using a series Zener diode (BZV55-B6V2).

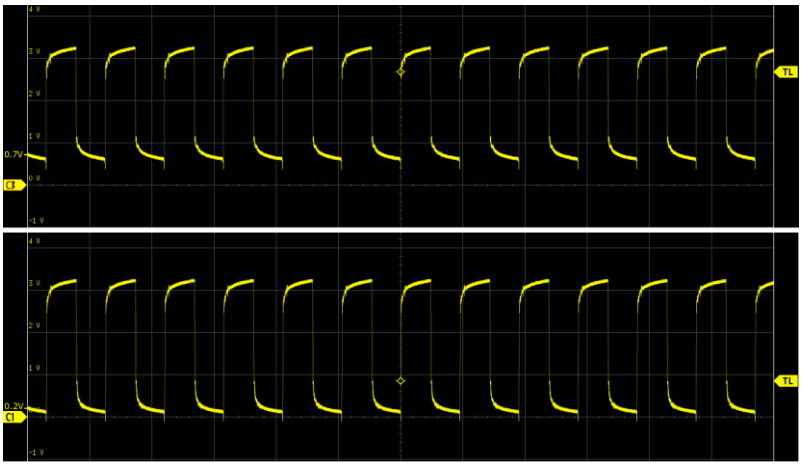

Fig. 12: Reduction in off-state V_{GS} from 0.7V to 0.2V due to addition of Schottky diodes in parallel with the Zener diode.

Protection circuits:

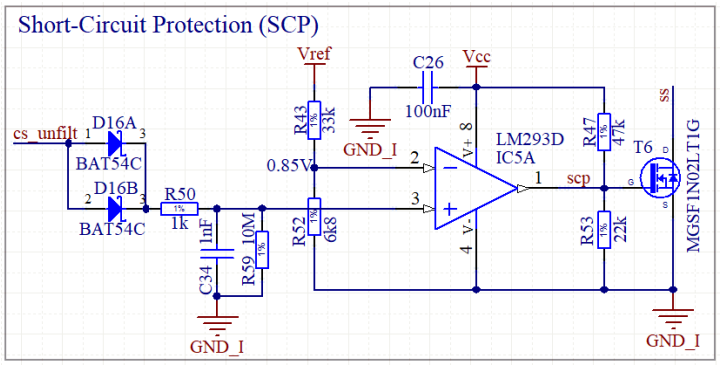

Fig. 11: Circuit schematic for short-circuit protection: peak detector followed by comparator

Short-circuit protection (SCP): The current mode control PWM chip inherently limits current to 1V/0.14Ω = 7.14A, which suffices to provide over-current protection during normal operation. However, a short circuit presents an extreme over-current condition. The current going into the short can far exceed the 7.14A limit within the very short current-blanking duration when the PWM chip is essentially blind to the current value. Hence, a dedicated SCP circuit is required. Fig. 11 shows the circuit schematic for SCP, which includes a peak detector followed by a comparator that turns on a trip MOSFET. No positive feedback hysteresis resistor should be used because it pulls up the non-inverting input of the comparator during startup, which means that the DC/DC will never power up. Instead, hysteresis is provided by the fact that the 47kΩ pull-up resistor takes finite time (time constant≈6ms) to charge the input capacitance of the signal MOSFET (C_{iss}≈125pF). The trip voltage of 0.85V corresponds to a trip current of (0.85V+0.27V)/(0.14V/A) = 8A. Using the above circuit, the

power draw of ACF DC/DC v0 (demo board) under short circuit condition was found to be about 11W, 7W, and 6W for V_{in} of 36V, 48V, and 72V respectively. Fig. 12 shows the waveforms when the DC/DC goes into hiccup mode in the short circuit condition for the three above-mentioned input voltage values. Caveat: The moment the short is introduced, MOSFET V_{DS} briefly rises up to 150-180V which can lead to SEB under radiation.

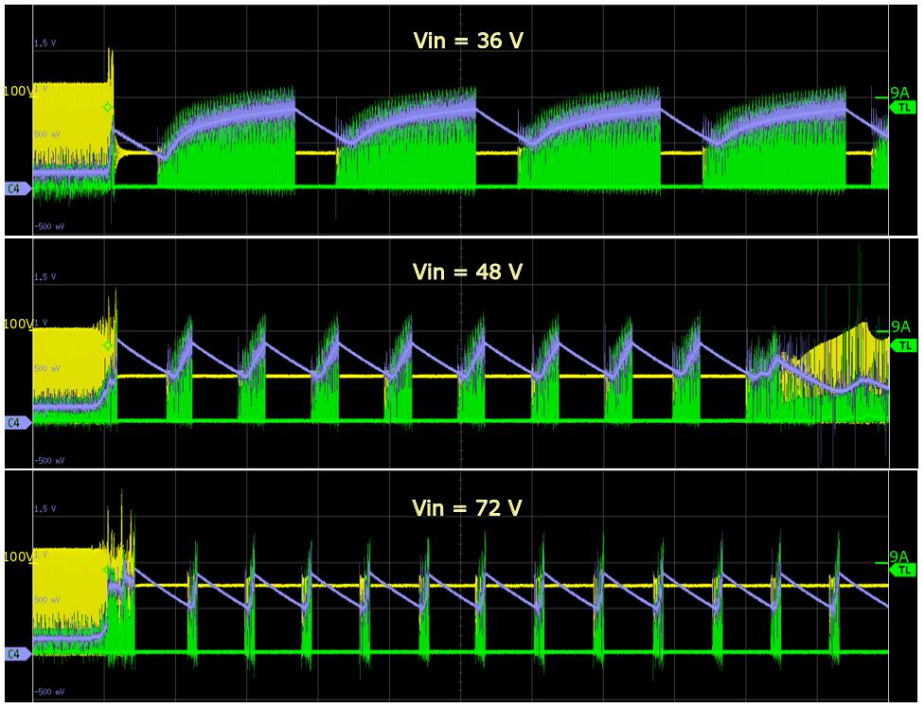

Fig. 12: Waveforms when the DC/DC goes into hiccup mode under short-circuit condition. Green: MOSFET current (unfiltered); Blue: MOSFET current after peak detection; Yellow: MOSFET V_{DS}; Time scale: 2ms/div.

Over-voltage protection (OVP): Considering the importance of OVP, the circuit path used for conveying OVP information (optocoupler) should be separate from that used for output voltage regulation. Fig. 13 shows the circuit used for OVP. Over-voltage is detected on the secondary side when the output voltage goes above 120% of its nominal value. When this happens the trip signal is sent to the controller on the primary side using the optocoupler HCNR200-300E. Photodiode current of this optocoupler is too weak, in the order of microamperes. This could be potentially doubled by using a parallel combination of both photodiodes available in the chip. However, that would seriously compromise the safety isolation in the product. Instead, a BJT is used as a current amplifier for a single photodiode.

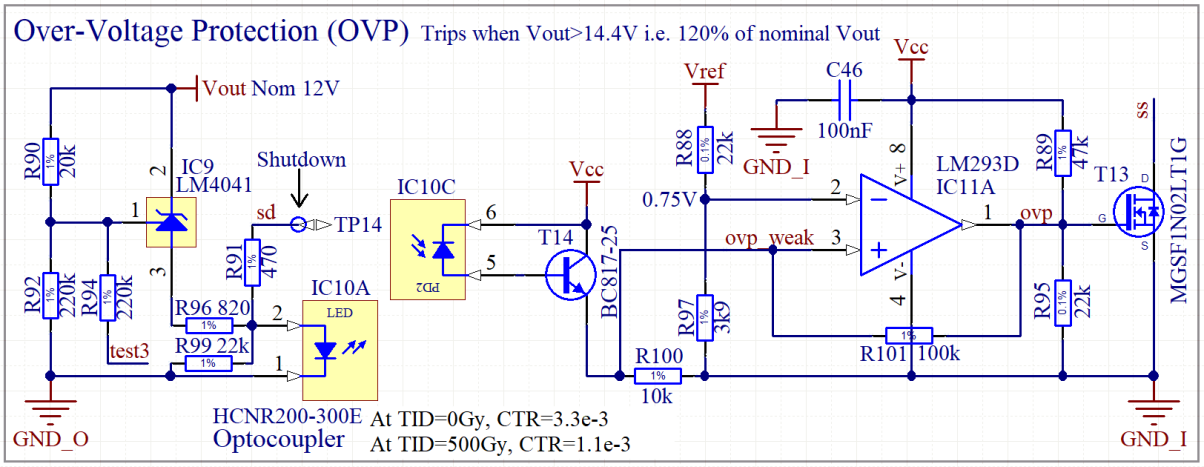

Fig. 13: Circuit schematic for over-voltage protection (OVP): Secondary-side comparator, opto-coupler, current amplifier, primary-side comparator, trip MOSFET. External shutdown is also implemented in the same circuit.

External shutdown:

This signal will come from a board referenced to the secondary-side ground, whereas the DC/DC controller is referenced to the primary side ground. This requires a means to transfer the shutdown signal through an isolation barrier. This is achieved by piggybacking on the existing isolator (optocoupler) used for transferring the OVP signal to the primary side as shown in Fig. 13.

6. Feedback and compensation

Fig. 14 shows the circuit schematic for the full feedback path including type-2 compensation on the secondary side, an isolation amplifier to take the feedback signal over the isolation barrier, followed by a difference amplifier and error amplifier on the primary side. The corresponding LTSpice simulation file is *acf_feedback_path_cl.asc* that incorporates a simplified (averaged) closed-loop simulation of the ACF DC/DC converter using the feedback and compensation circuit detailed here. The relevant equations for the voltage levels at various stages of the signal chain are given below.

$$V_a \in (0.3, 1.3)\ V$$
$$V_{csb} = V_a + V_{bias} + V_f \in (1.8, 2.8)\ V$$
$$V_{comp} = -\frac{R_2}{R_1} V_{csb} + 2.5\left(1 + \frac{R_2}{R_1}\right) \in (1.9, 3.9)\ V$$

Where, V_a is the voltage at the isolation amplifier input, V_{csb} is the voltage at the current share bus, V_{bias} is a fixed 1.24 bias voltage, V_f is the Schottky diode forward voltage (about 0.3V), and V_{comp} is the 'comp' signal which is representative of the peak current value used inside the PWM chip (TL2843). The isolation amplifier (ACPL-C87B) accepts an input voltage (V_a) in the range 0-2V and generates a differential voltage at its two output lines. In order to convert this differential voltage to a single-ended voltage, a difference amplifier (using LM358) is required. However, this difference amplifier also needs to add a bias voltage V_{bias} that helps keep V_a well below the 2V limit even at no load. Without V_{bias}, V_a would hit the upper limit of the control band at light load. In the present design, V_a varies from 0.3V to 1.3V (full load to no load). V_{csb} varies from 1.8V to 2.8V (full load to no load). V_{comp} required at any load is defined based on current sense circuit (1/70, 10 ohm) as well as PWM chip internals, and varies from 1.9V to 3.9V (no load to full load).

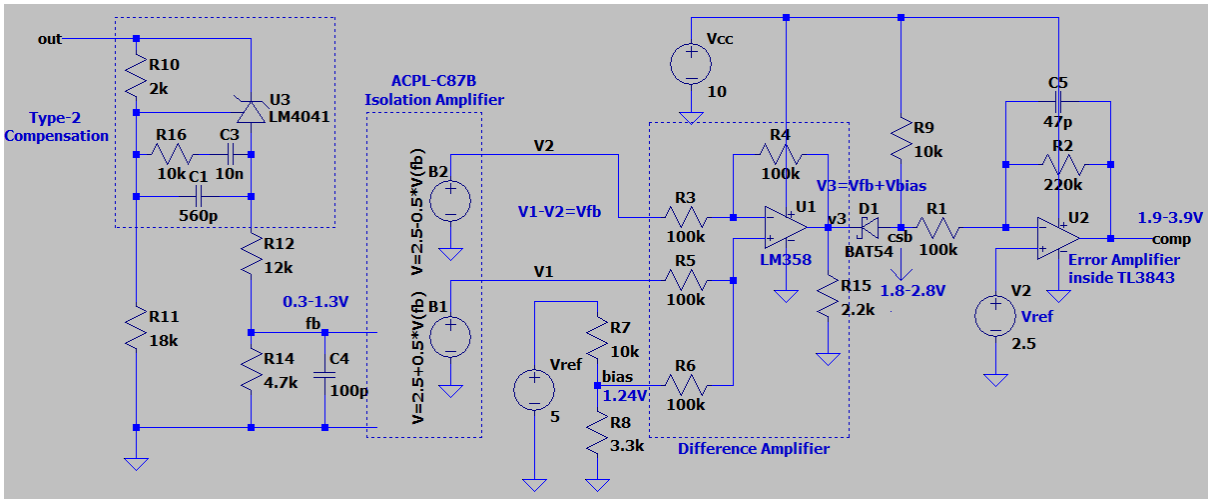

Fig. 14: Circuit schematic for the full feedback path for the ACF DC/DC converter.

In terms of radiation tolerance, the internal reference of the LM4041 has been found to be well within specification (less than 0.1% drift) up to 200 Gy TID, but has not been tested up to 500 Gy [4]. The voltage gain of the isolation amplifier (ACPL-C87B) has also been found to be well within specification up to 500 Gy TID [5]. This is in fact the reason for using an isolation amplifier instead of a standard optocoupler that is generally used in non-rad-tol DC/DC converters, but are known to suffer from severe CTR degradation under radiation. The PWM controller (TL2843) has also been tested up to 500 Gy and has been found to work as expected [6].

Open questions

1. Does a 150V TVS diode (SMBJ150CA) suffice for MOSFET protection (main and clamp)? Should we use SMBJ130CA instead? Are these diodes required considering that they can destroy the gate driver while trying to protect the MOSFET? **Answer:** These diodes can protect the MOSFET from high Vds that can potentially cause an SEB.
2. How does SMBJ150CA perform under radiation? Does leakage current increase?
3. Can we use 45V Schottky diodes for secondary side diodes? **Answer:** 45V Schottky diodes will have lower forward voltage drop, but will leave too little voltage headroom, and also have high junction capacitance.
4. Should we use current foldback (or frequency foldback) for SCP? How to implement it? **Answer:** Implementing frequency foldback for SCP is difficult because the short-circuit information is in the output voltage value (not available to the controller on the primary side).
5. For snubber resistors (0.5W or 1W), is it better to use 1206 resistors in parallel or series? (from layout point of view) **Answer:** Series is probably fine.
6. How to change layout as to not place ceramic capacitors C1 and C53 (common-mode capacitors) at edge of PCB (danger of cracking)?
7. Is there a possibility that because of production spread and/or with increasing TID the Zener voltage for D6 (BZV55-B11) goes up enough as to make the bootstrap bias win over the auxiliary bias? Does the internal reference voltage of the LM317 rise enough to compensate for this effect?
8. What is the effect of radiation on the UVLO threshold of the gate driver chip? Does this shift enough to cause it to shutdown?
9. Can we add a heat spreader for the transformer core in the four copper layers of the PCB (underneath the RM8 core)? Will it improve efficiency by cooling the copper windings? Will

it compromise the safety isolation? **Answer:** Because of thermal insulation between copper and ferrite, cooling the ferrite does not result in any improvement (tested experimentally with small metal piece attached to the ferrite). However, adding extra copper to the top node of the primary winding (cold point in terms of EMC), could help in reducing winding temperature, thus reducing resistance and hence copper losses.

10. What was the reason for double pulses in PWM output after subjecting the converter to short circuit test? **Answer:** From simulation, this seems to be a problem of insufficient slope compensation. Upon appropriately increasing the extent of slope compensation, this problem is eliminated.

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