NFTC v1.00

NanoFIP test board

HLP Technologies

35 rue Tournefort
75005 Paris

www.hlp.fr

Title: Cover		
Size: A4	Document Number: 1016-10-1.00-SCH-A-003	Rev: 003
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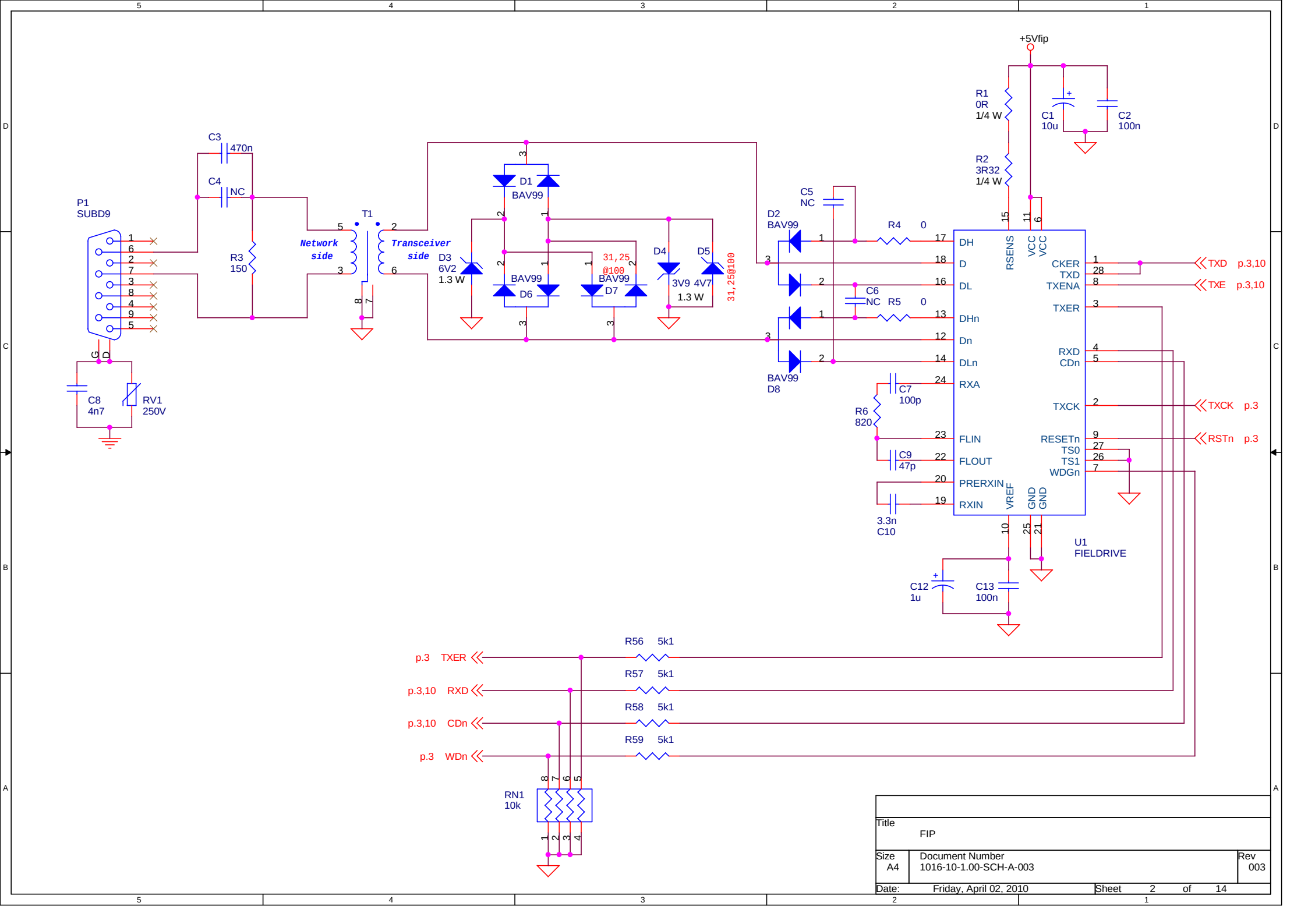

Title	FIP	
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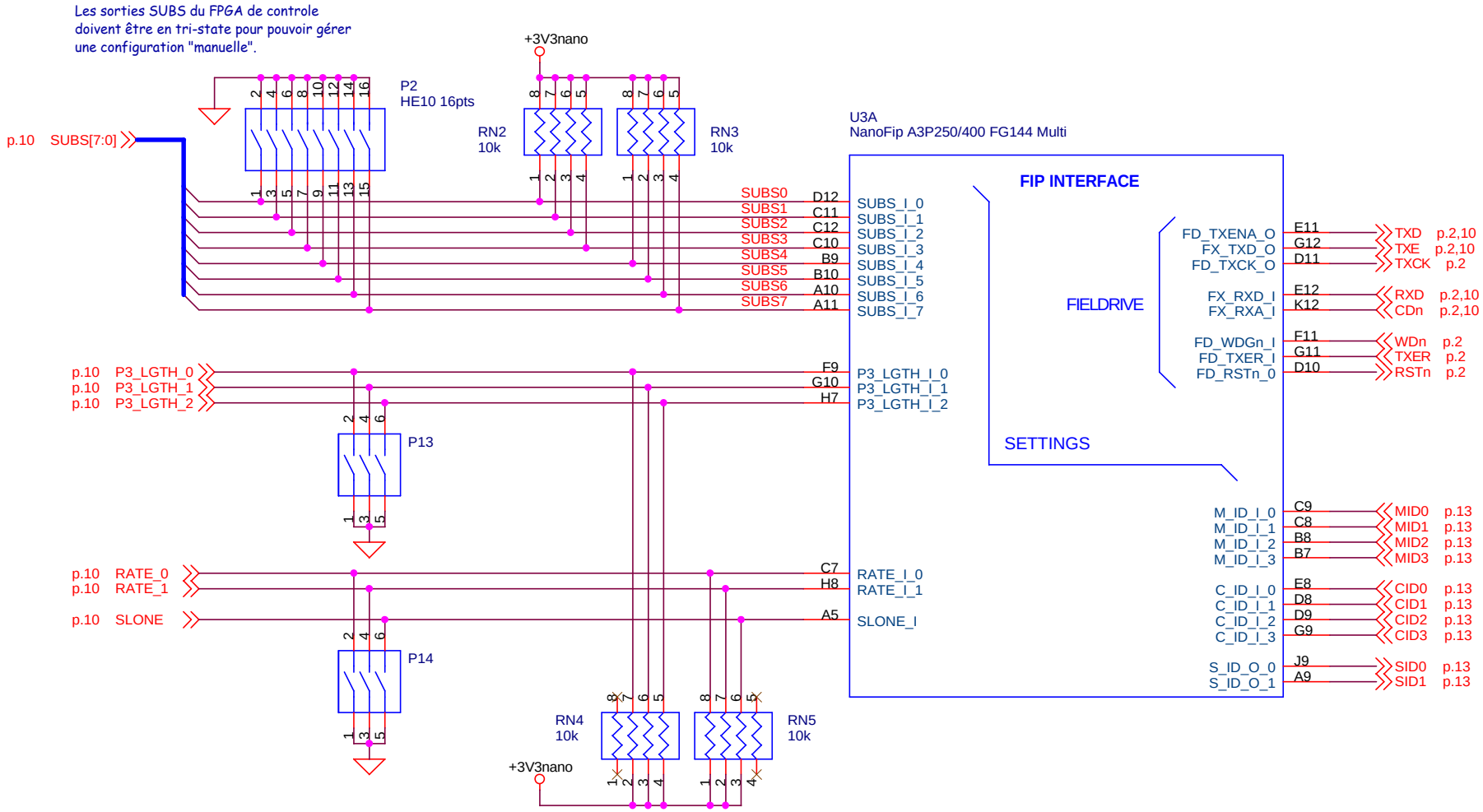

Si l'alimentation du NanoFip est coupée, les entrées
doivent être à 0.
Le FPGA de controle doit gérer des sorties tri-state

RATE_0	RATE_1	
0	0	31.25 kbps
0	1	1 Mbps
1	0	2.5 Mbps
1	1	reserved

Title	NanoFip 1	
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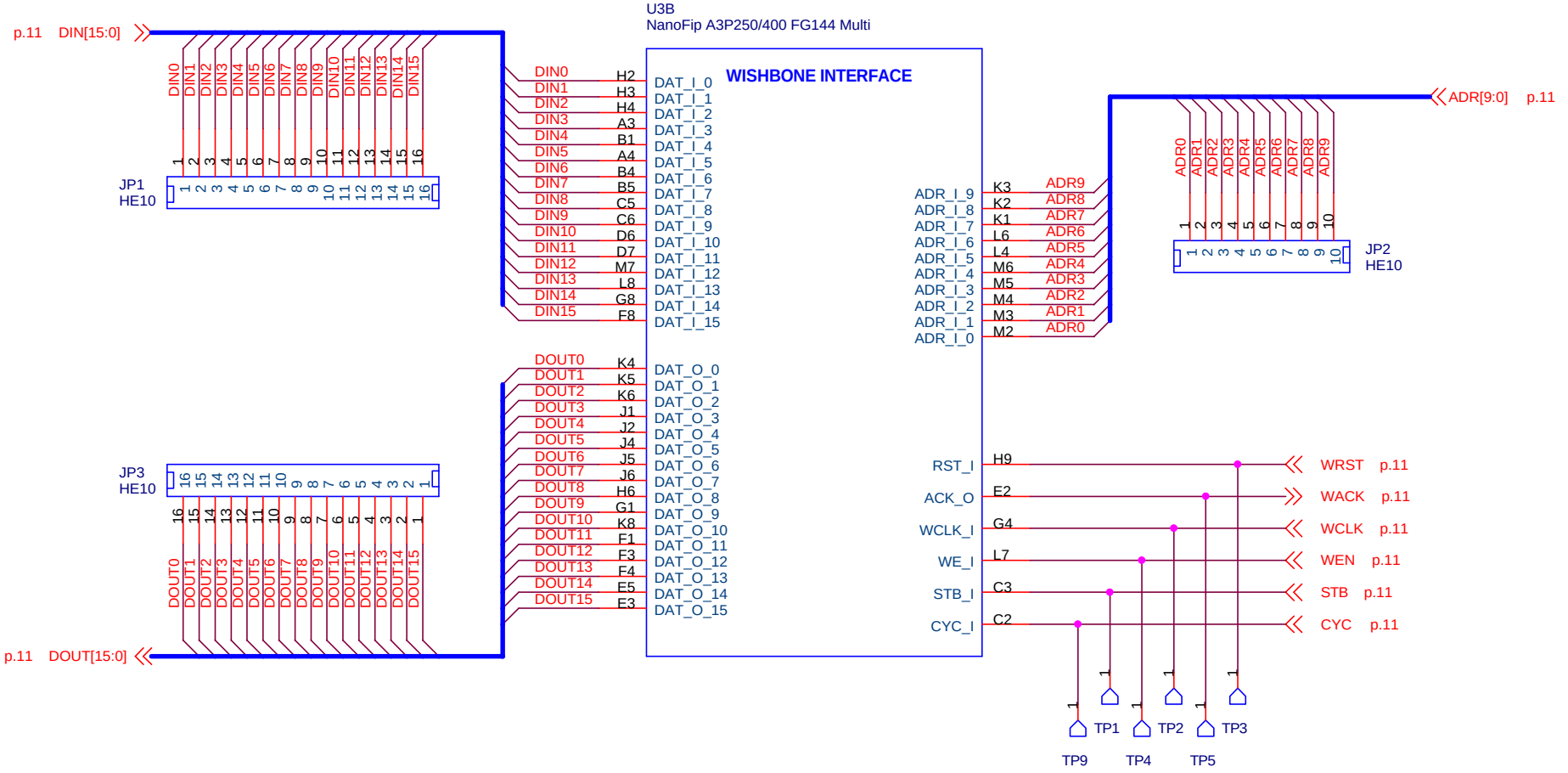
Si l'alimentation du NanoFip est coupée, les entrées
doivent être à 0.
Le FPGA de controle doit forcer ses sorties à 0



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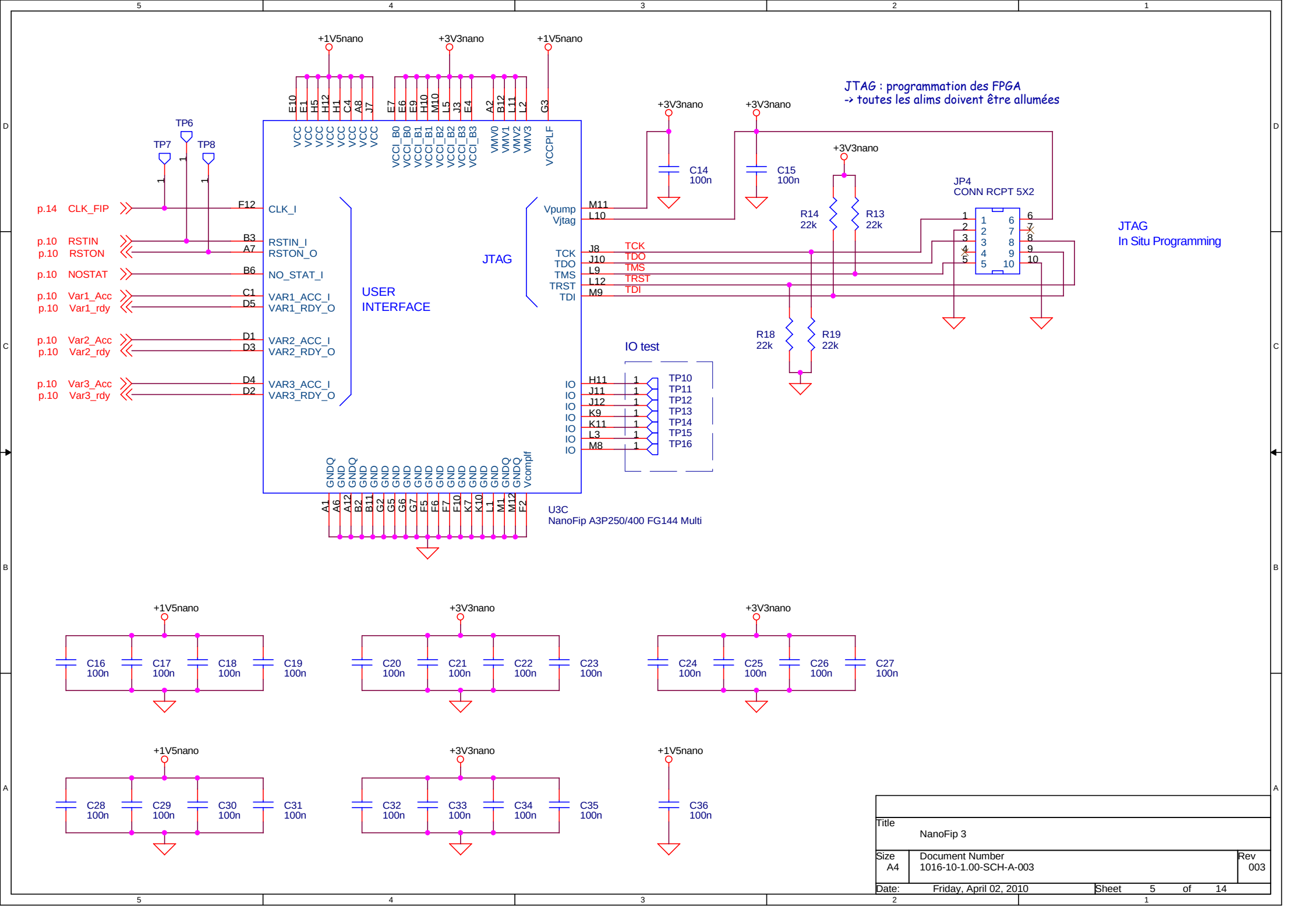

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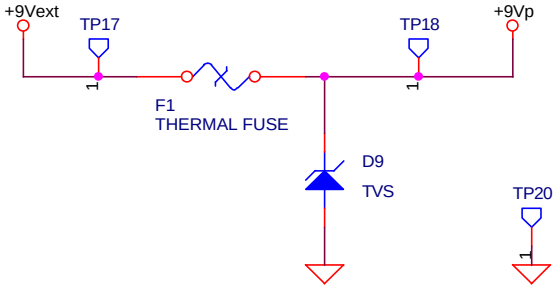
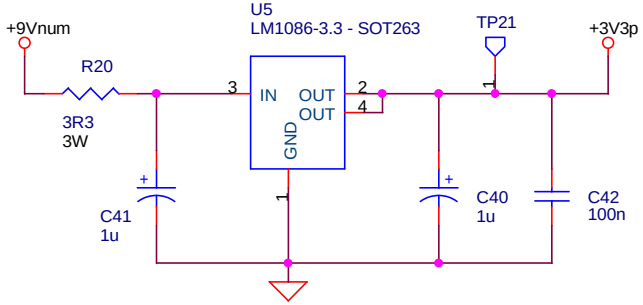
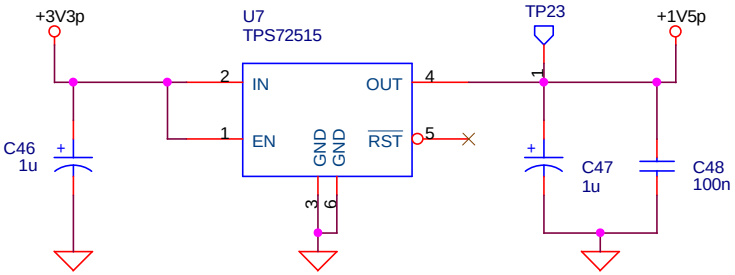


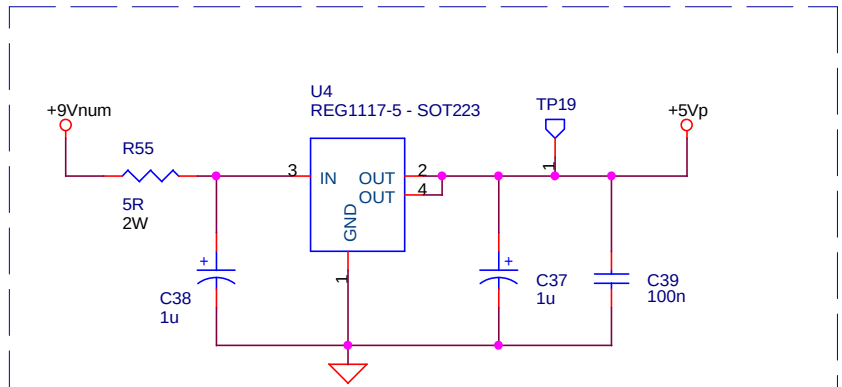
ALIMENTATION 3V3



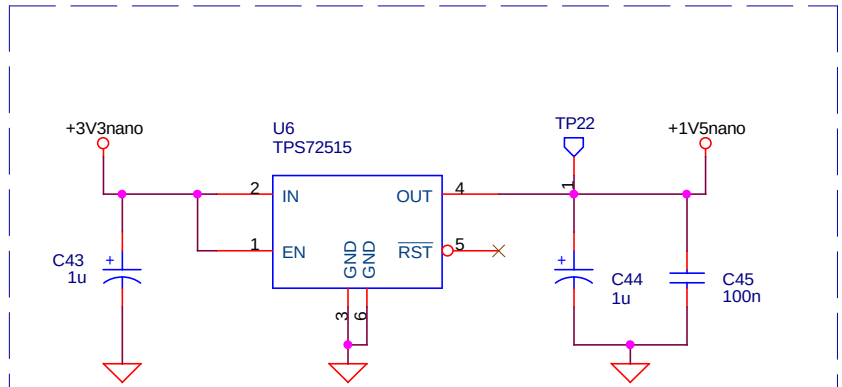
ALIMENTATION 1V5



ALIMENTATION 5V



ALIMENTATION 1V5 (NanoFip)



Title: Alimentation		
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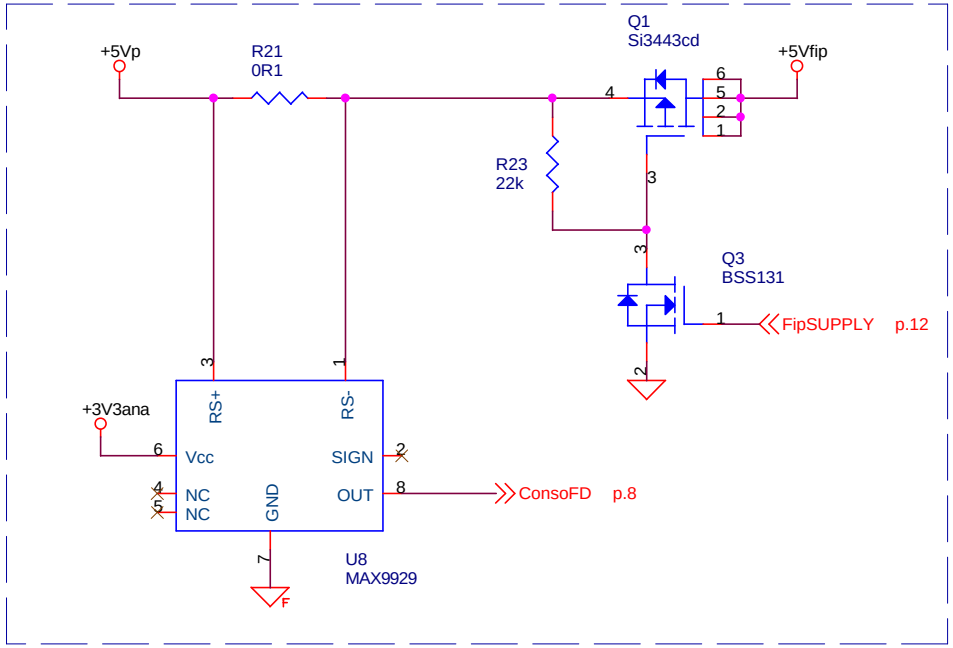
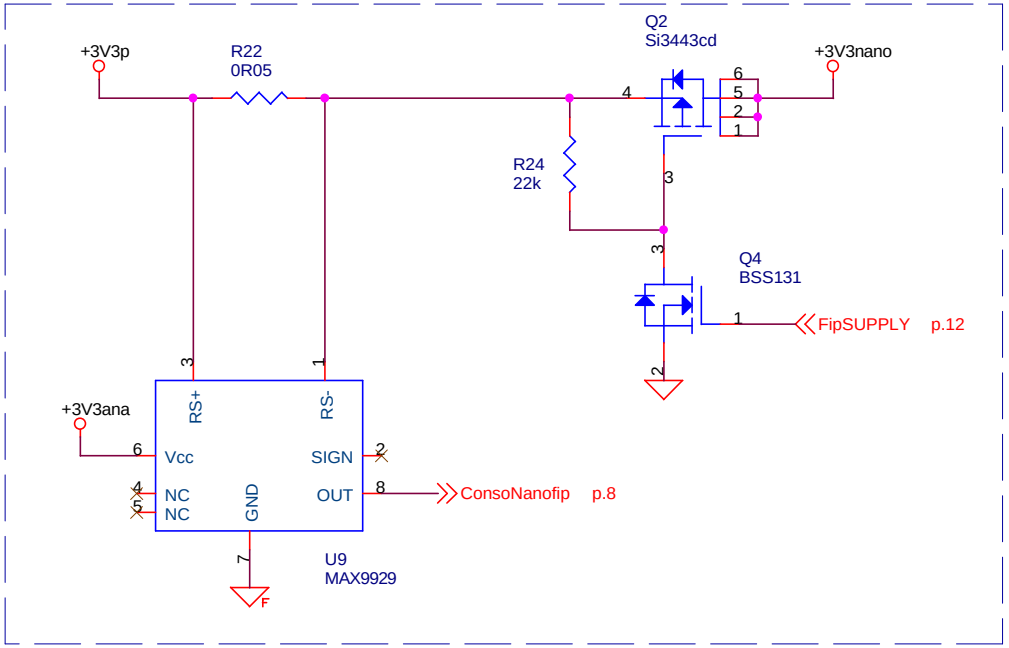
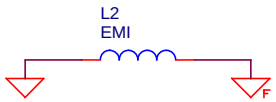
Mesure consommation du Fieldrive



Mesure consommation du NanoFip





Title: Current sense		
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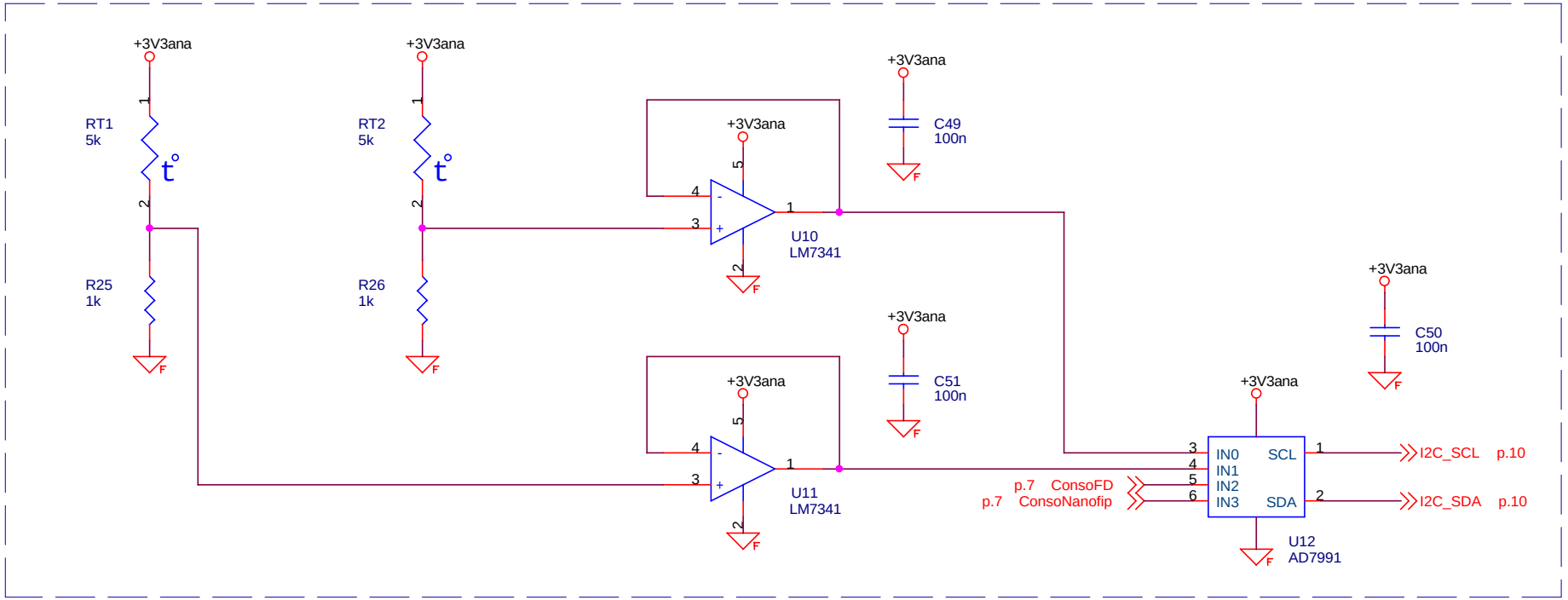
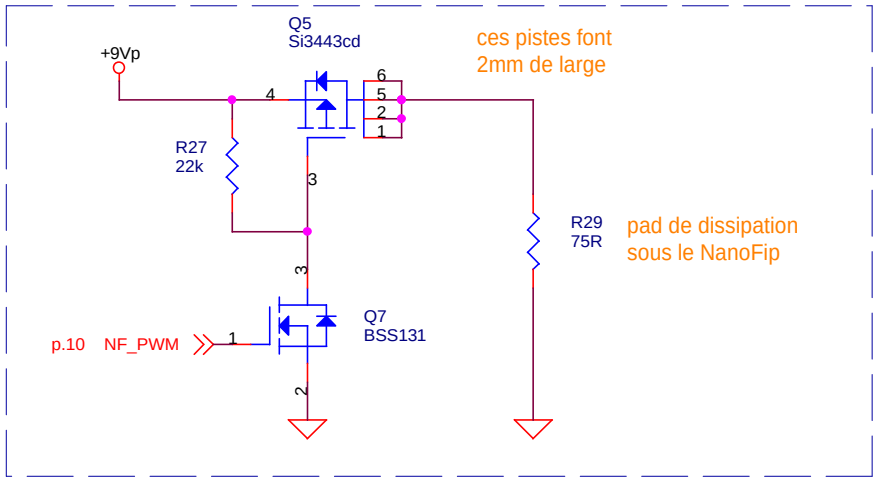
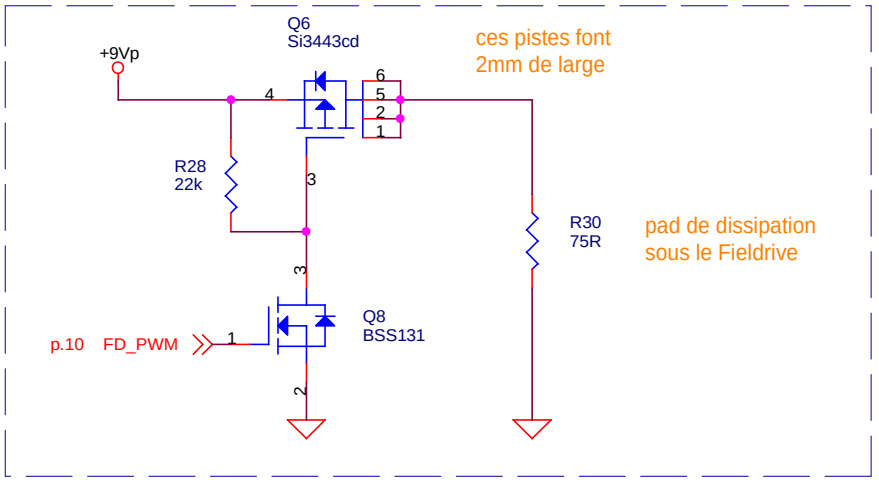
Mesure température Fieldrive & NanoFip



Commande chauffage NanoFip



Commande chauffage Fieldrive



Title: Temperature management		
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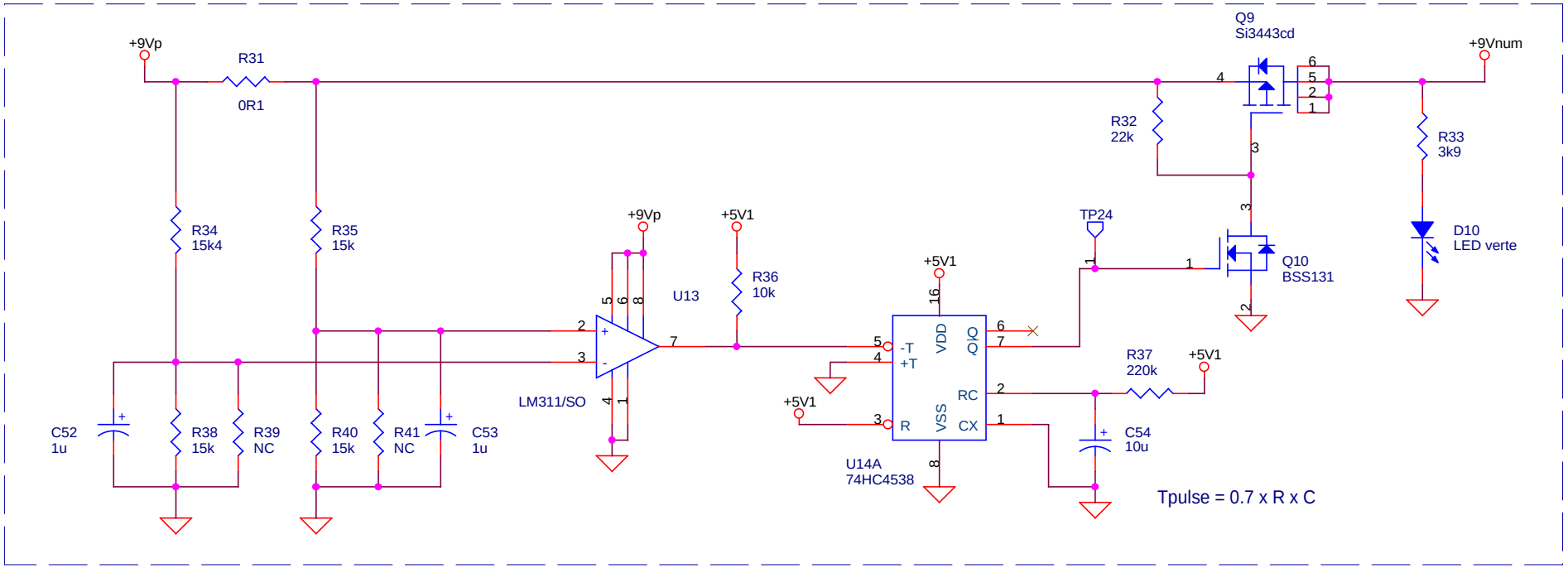
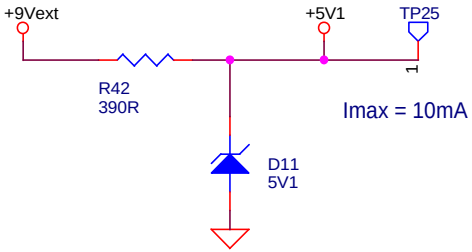
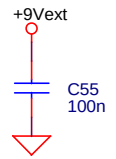
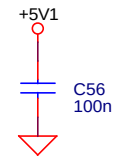
Protection Latch-up



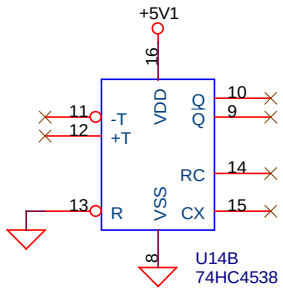




Découplage LM311



Découplage 74HC4538



Title: Latch-up		
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Les sorties doivent être forcée à 0 si
l'alimentation 3V3nano est coupée.

P3
SUBD9

R43
220R

+3V3p

U16
ADM3078

C57
100n

+5Vp

R44
390R

D12
LED bleue

Q13
BSS131

FIP_activity

p.5 RSTIN
p.5 RSTON
p.5 NOSTAT
p.8 NF_PWM
p.8 FD_PWM
p.2,3 TXD
p.2,3 TXE
p.2,3 RXD
p.2,3 CDn
p.8 I2C_SCL
p.8 I2C_SDA

FIP_RST
FIP_RST_EXT
NOSTAT
PWM_NF
PWM_FD
FIP_RXE
FIP_RXD
FIP_TXD
FIP_TXE
IO
IO
IO
IO
IO
IO117RSB1
IO116RSB1
IO115RSB1
IO79RSB1
SCL
SDA

TP26
TP27
TP28
TP29

SUBS_0
SUBS_1
SUBS_2
SUBS_3
SUBS_4
SUBS_5
SUBS_6
SUBS_7
SUBS0
SUBS1
SUBS2
SUBS3
SUBS4
SUBS5
SUBS6
SUBS7
SUBS[7:0] p.3

P3_LEN_0
P3_LEN_1
P3_LEN_2
P3_LGTH_0 p.3
P3_LGTH_1 p.3
P3_LGTH_2 p.3

RATE_0
RATE_1
SLONE
RATE_0 p.3
RATE_1 p.3
SLONE p.3

Var1_RDY
Var1_ACC
Var1_rdy p.5
Var1_Acc p.5

Var2_RDY
Var2_ACC
Var2_rdy p.5
Var2_Acc p.5

Var3_RDY
Var3_ACC
Var3_rdy p.5
Var3_Acc p.5

IO82RSB1
IO81RSB1
IO80RSB1
TP30
TP31
TP32

U15A
Actel A3P125 - TQ144 Multi

Les sorties doivent être forcée à 0 si
l'alimentation 3V3nano est coupée.

EEPROM serie I2C

+3V3p
+3V3p
+3V3p

C58
100n

R46
22k
R47
22k
R45
22k
R48
NC

SDA
SCL
VCC
GND
WC
E0
E1
E2

U17
24C01-WMN

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Controle WISHBONE

Le bus DIN doit être forcé à 0 si l'alimentation 3V3nano est coupée.

p.4 DIN[15:0]

RN6 10k — DIN0 DIN1 DIN2 DIN3
RN7 10k — DIN4 DIN5 DIN6 DIN7
RN8 10k — DIN8 DIN9 DIN10 DIN11
RN9 10k — DIN12 DIN13 DIN14 DIN15

DIN0	65	WDout_0
DIN1	66	WDout_1
DIN2	67	WDout_2
DIN3	86	WDout_3
DIN4	79	WDout_4
DIN5	80	WDout_5
DIN6	83	WDout_6
DIN7	84	WDout_7
DIN8	101	WDout_8
DIN9	102	WDout_9
DIN10	103	WDout_10
DIN11	104	WDout_11
DIN12	105	WDout_12
DIN13	106	WDout_13
DIN14	109	WDout_14
DIN15	110	WDout_15

DOUT0	111	WDin_0
DOUT1	112	WDin_1
DOUT2	113	WDin_2
DOUT3	114	WDin_3
DOUT4	115	WDin_4
DOUT5	116	WDin_5
DOUT6	120	WDin_6
DOUT7	121	WDin_7
DOUT8	122	WDin_8
DOUT9	123	WDin_9
DOUT10	124	WDin_10
DOUT11	125	WDin_11
DOUT12	126	WDin_12
DOUT13	127	WDin_13
DOUT14	128	WDin_14
DOUT15	129	WDin_15

p.4 DOUT[15:0]

RN13 10k — DOUT0 DOUT1 DOUT2 DOUT3
RN14 10k — DOUT4 DOUT5 DOUT6 DOUT7
RN15 10k — DOUT8 DOUT9 DOUT10 DOUT11
RN16 10k — DOUT12 DOUT13 DOUT14 DOUT15

Le bus ADR doit être forcé à 0 si l'alimentation 3V3nano est coupée.

ADR[9:0] p.4

RN10 10k — ADR0 ADR1 ADR2 ADR3
RN11 10k — ADR4 ADR5 ADR6 ADR7
RN12 10k — ADR8 ADR9

WAdr_0	130	ADR0
WAdr_1	131	ADR1
WAdr_2	132	ADR2
WAdr_3	133	ADR3
WAdr_4	137	ADR4
WAdr_5	138	ADR5
WAdr_6	139	ADR6
WAdr_7	140	ADR7
WAdr_8	141	ADR8
WAdr_9	142	ADR9

WRST	1	WRST p.4
WACK	2	WACK p.4
WCLK	3	WCLK p.4
WEN	4	WEN p.4
STB	49	STB p.4
CYC	90	CYC p.4

Les sorties sont forcées à 0 si l'alimentation 3V3nano est coupée.

U15B
Actel A3P125 - TQ144 Multi

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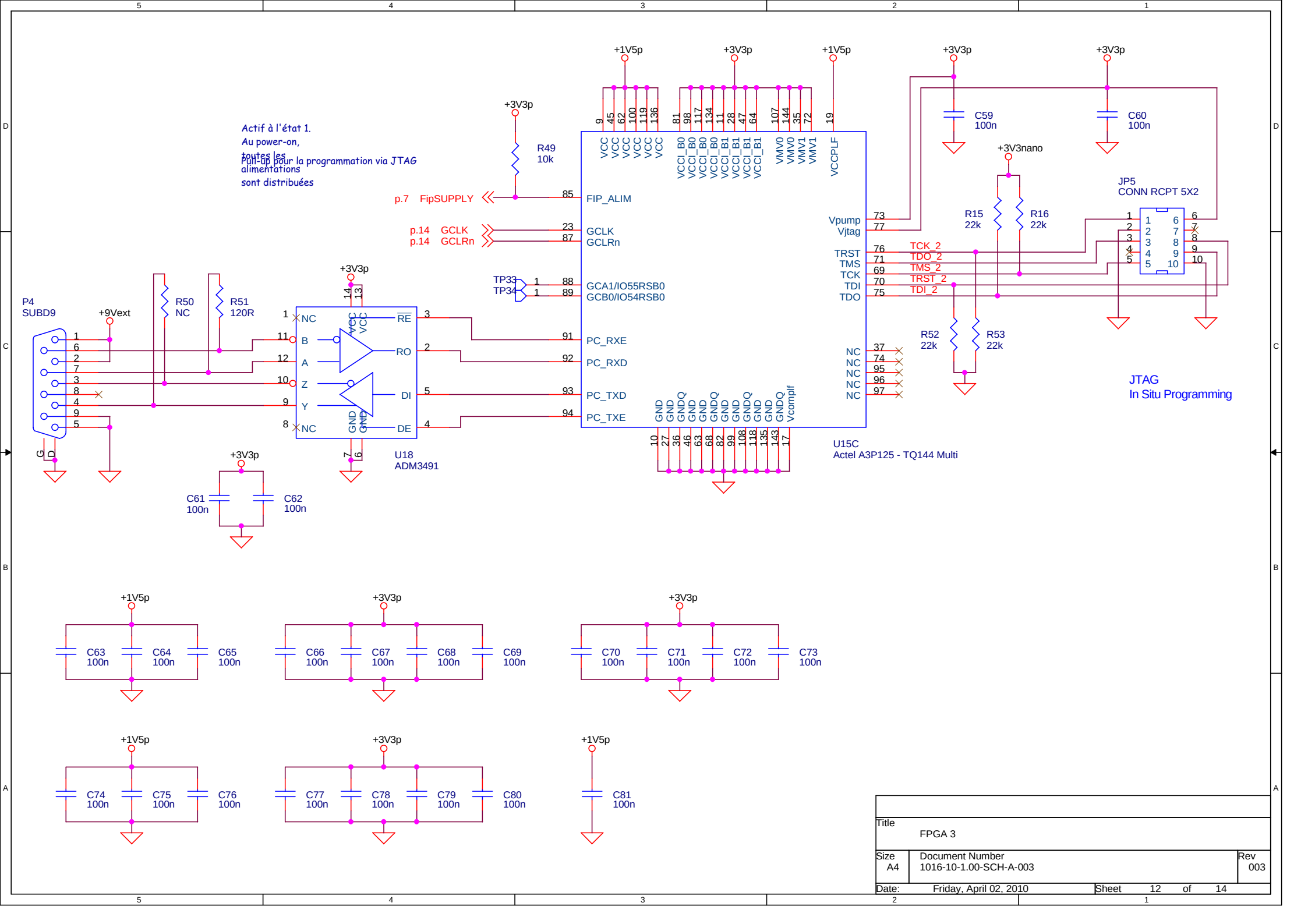
Actif à l'état 1.
Au power-on,
toutes les
alimentations
sont distribuées
Pull-up pour la programmation via JTAG
+1V5p
+3V3p
+3V3nano
+9Vext
R49
10k
R50
NC
R51
120R
R15
22k
R16
22k
R52
22k
R53
22k
C59
100n
C60
100n
C61
100n
C62
100n
C63
100n
C64
100n
C65
100n
C66
100n
C67
100n
C68
100n
C69
100n
C70
100n
C71
100n
C72
100n
C73
100n
C74
100n
C75
100n
C76
100n
C77
100n
C78
100n
C79
100n
C80
100n
C81
100n
P4
SUBD9
U18
ADM3491
U15C
Actel A3P125 - TQ144 Multi
JP5
CONN RCPT 5X2
JTAG
In Situ Programming
p.7 FipSUPPLY
p.14 GCLK
p.14 GCLRn
FIP_ALIM
GCLK
GCLRn
GCA1/IO55RSB0
GCB0/IO54RSB0
PC_RXE
PC_RXD
PC_TXD
PC_TXE
TP33
TP34
Vpump
Vjtag
TRST
TMS
TCK
TDI
TDO
TCK_2
TDO_2
TMS_2
TRST_2
TDI_2
VCCPLF
Vcompllf
Title
FPGA 3
Size
A4
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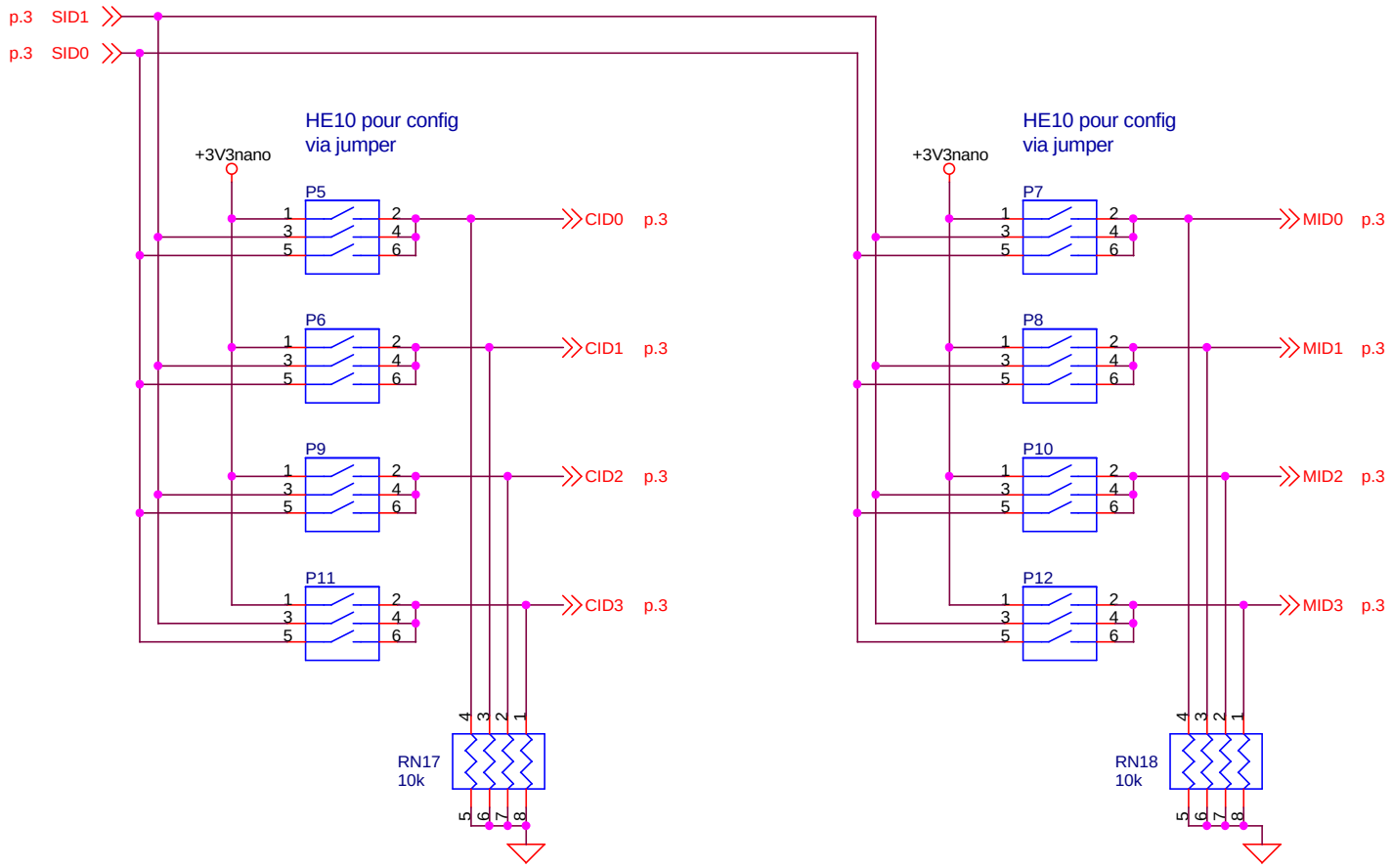

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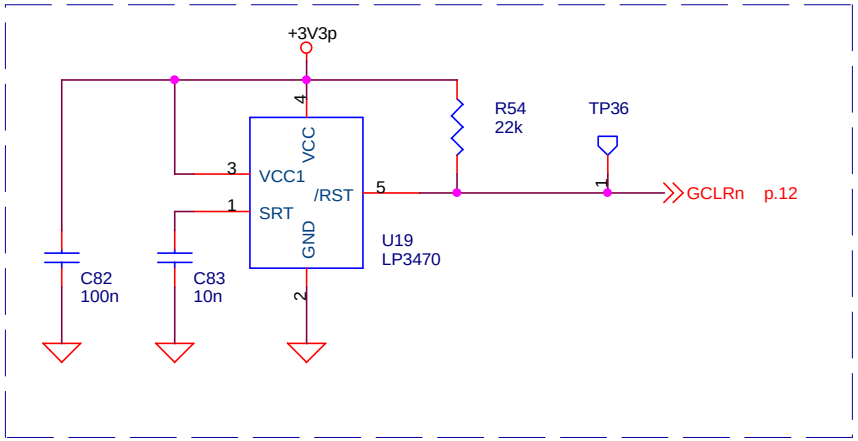
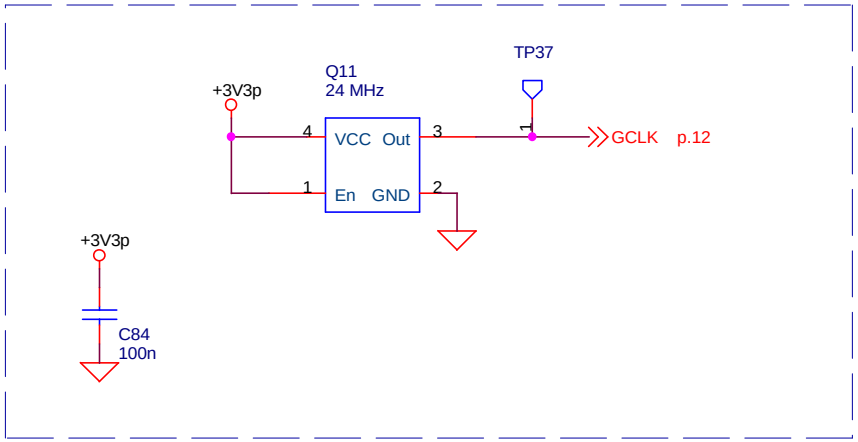
RESET



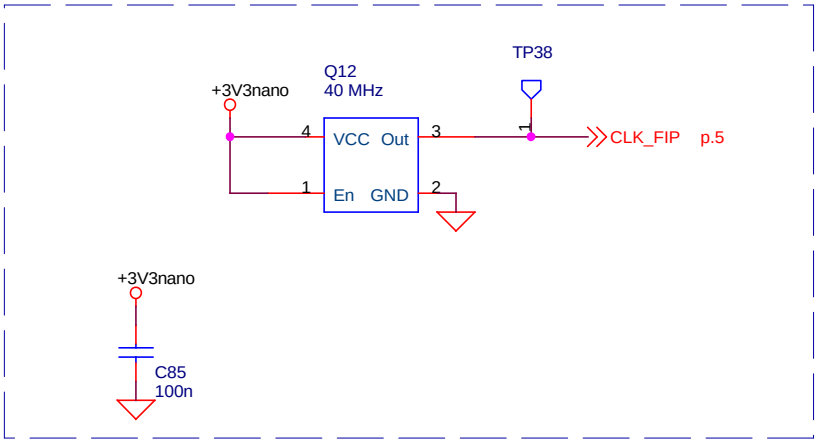
FIX1 FIX2 FIX3 FIX4

Percages de fixation

Horloge FPGA



Horloge NanoFip (40 MHz)



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