2. Formatting Rules

2.2 Line Width: maximum 100 characters per line.

2.3 Tabulators: no use of “hard tabulators”, only sequences of spaces.

2.4 File Header: Standardized header for each file.

2.5 Comments: Extensive commenting of important operations/ definitions.

2.6 Keywords: all VHDL keywords are written in lower case and there is no use of keywords in the signal names, entities names etc.

3. Name Style Rules

3.1 Signals, Variables, Constants, Types, Generics, Files:

variables	prefix	v_	
clock	prefix	clk_	nanoFIP clk names: uclk, wb_clk
constants	prefix	c_	
type definition	prefix	t_	
generic	prefix	g_	
low active signal	suffix	_n	
unit input signal	suffix	_i	
unit output signal	suffix	_o	
internal signal	prefix	s_	
asynchronous signal	suffix	_a	
delayed signal	suffix	_dn	
counter signal	suffix	_c	
pulse signal	suffix	_p	All _p in the design refer to 1 uclk wide pulses, unless stated otherwise

3.2 Blocks, Processes and other Labels: Use of labels for all the blocks in the code.

3.3 Entity Architecture, Configuration: Entity names describe the functionality of the blocks. The full name of the entity is in the comment above the entity declaration. The 3 parts of an architecture (declaration, begin, end) are marked with appropriate comments.

3.4 Files: File names have the same name as the entity name of the corresponding unit and only lower case letters are used.

3.5 Directories: There are separate folders for the
source code (http://svn.ohwr.org/cern-fip/trunk/hdl/design)
test bench code (http://svn.ohwr.org/cern-fip/trunk/hdl/test_bench)
synthesis (http://svn.ohwr.org/cern-fip/trunk/hdl/cad/libero/NanoFip/synthesis)
implementation (http://svn.ohwr.org/cern-fip/trunk/hdl/cad/libero/NanoFip/designer)

4. Coding Rules

4.1Notation for Bused Signals: Only MSB to LSB notation; only "downto" used.

4.2 Bussed Ports Width Rules: No use of busses of width one. Always comparison of buses of the same width.

4.3 Top Level Module Structure: The top level module (wf_nanofip) is used only for connectivity, without any logic.

4.4 Component Instantiation: In a component instantiation the ports are associated by name.
In the majority of the cases components instantiation is kept together in the same part of the code; there are few cases though where separation was found to be giving better code overview.

4.5 Reset for Sequential Blocks: 2 main synchronous resets: one for the WISHBONE logic only and one for the all the rest.

4.6 One statement per line

4.7 Finite State Machines: Each FSM is written in Moore style (outputs depend only on the current state) and has 4 segments (declaration, one synchronous process for the storage of the current state, one combinatorial process for the state transitions and one combinatorial process for the outputs).

4.8 Input Buffers: Triple buffers used to synchronize all input ports.

4.9 Operator Precedence: Brackets are always used to specify the intended precedence.

4.10 The Value "don t care": No use of the value "don't care".

4.11 Internal Tri-State: No use of internal tri-state signals.

4.12 Prefer IEEE 1076.3 over Synopsis Arithmetic Packages: No use of the ieee.std_logic_arith.all.

4.13 Signals and variables: No use of variables in the design.

4.15 Latches in the design: No latches created in the design.

4.16 VHDL Coding Standards: Only VHDL 93 used.