MAROC

FPGA CONNECTIONS

PAGE 2

CLOCK GENERATOR

AND CONTROL DACS

PAGE 5

CTEST DAC
LEDS
SWITCHES

PAGE 8

DC-DC CONVERTERS

3.5V (MAROC)
3.3V

PAGE 10

LVDS I/O CONNECTIONS

(DIN 41612)

FPGA CONNECTIONS

PAGE 3

SFP CAGES

ESATA CONNECTORS

FPGA CONNECTIONS

PAGE 6

DC-DC CONVERTERS

1.2V (VCCINT)
2.5V

PAGE 9

POWER CONNECTIONS
VCCINT=1.2V
VCCAUX=2.5V
VCCO(LVDS)=2.5V
VCCO(MAROC)=3.3V

DECOUPLING

PAGE 11

BUSSED LINES -

CLOCKS, TRIGGERS

PAGE 4

SPI FLASH

JTAG CONNECTIONS

M0,M1 CONNECTIONS

PAGE 7

	Tue Jun	3 10:41:38	2014			
			DAVID CUSSANS			
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TITLE uob_hep_pc049a_lib

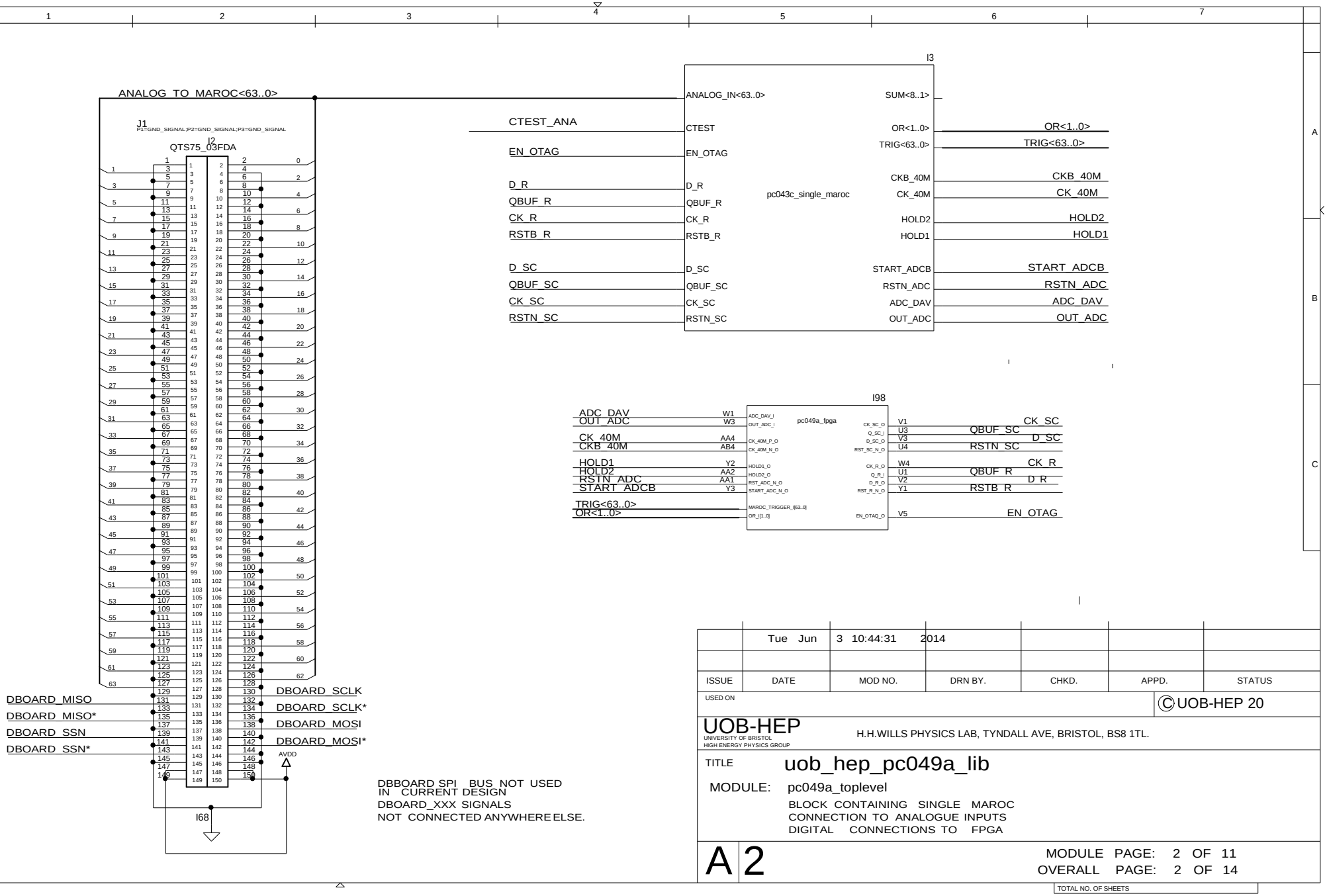
MODULE: pc049a_toplevel

OVERALL LAYOUT

A2

MODULE PAGE: 1 OF 11
OVERALL PAGE: 1 OF 14

TOTAL NO. OF SHEETS



	Tue Jun	3 10:44:31 2014				
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TITLE **uob_hep_pc049a_lib**

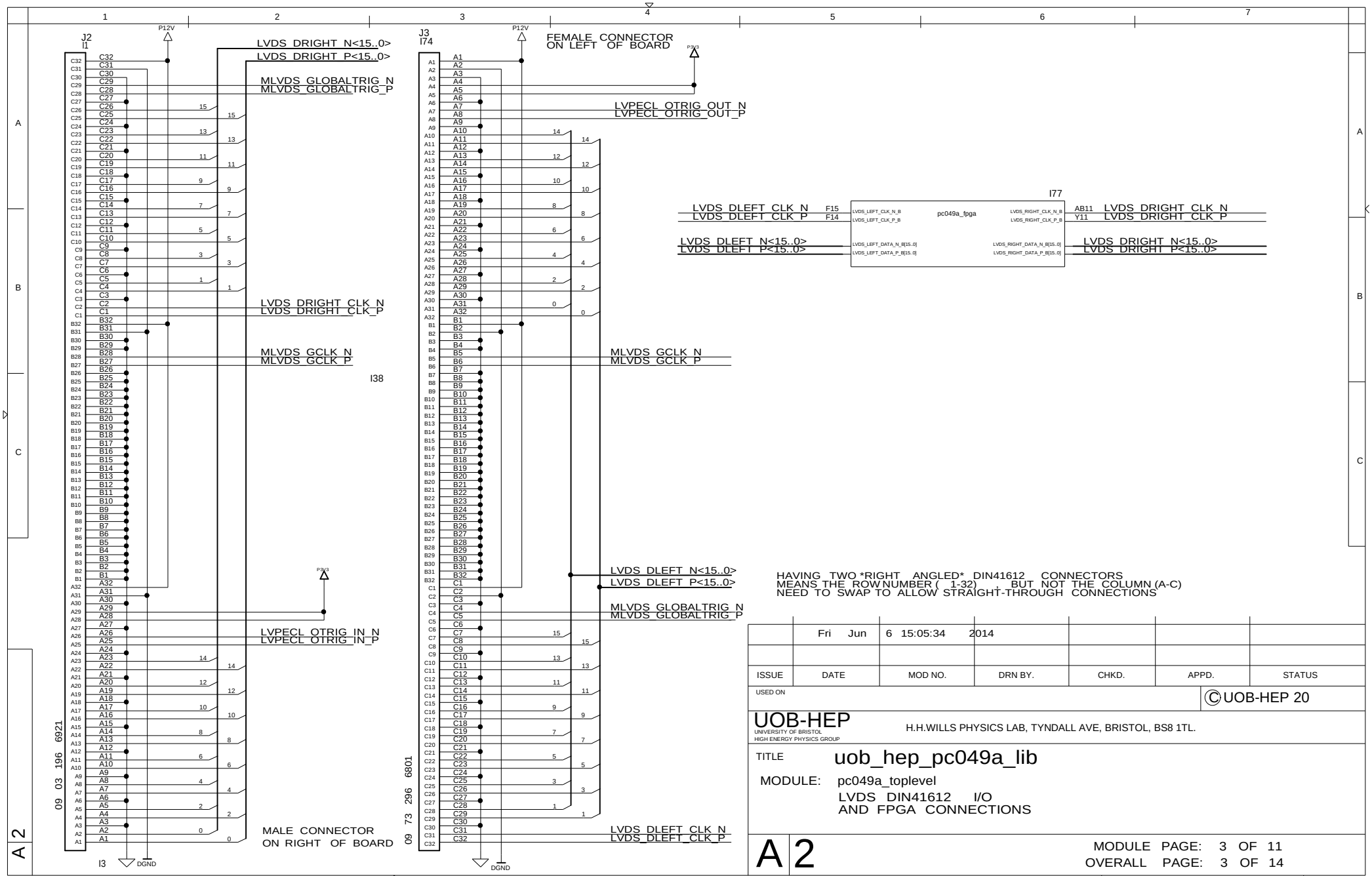
MODULE: pc049a_toplevel

BLOCK CONTAINING SINGLE MAROC
CONNECTION TO ANALOGUE INPUTS
DIGITAL CONNECTIONS TO FPGA

A2

MODULE PAGE: 2 OF 11
OVERALL PAGE: 2 OF 14

TOTAL NO. OF SHEETS


J2
I1
P12V
LVDS_DRIGHT_N<15..0>
LVDS_DRIGHT_P<15..0>
MLVDS_GLOBALTRIG_N
MLVDS_GLOBALTRIG_P
LVDS_DRIGHT_CLK_N
LVDS_DRIGHT_CLK_P
MLVDS_GCLK_N
MLVDS_GCLK_P
I38
P3V3
LVPECL_OTRIG_IN_N
LVPECL_OTRIG_IN_P
MALE CONNECTOR
ON RIGHT OF BOARD
I3
DGND
J3
I74
FEMALE CONNECTOR
ON LEFT OF BOARD
LVPECL_OTRIG_OUT_N
LVPECL_OTRIG_OUT_P
LVDS_DLEFT_N<15..0>
LVDS_DLEFT_P<15..0>
MLVDS_GLOBALTRIG_N
MLVDS_GLOBALTRIG_P
LVDS_DLEFT_CLK_N
LVDS_DLEFT_CLK_P
I77
pc049a_fpga
LVDS_DLEFT_CLK_N
LVDS_DLEFT_CLK_P
LVDS_DLEFT_N<15..0>
LVDS_DLEFT_P<15..0>
LVDS_DRIGHT_CLK_N
LVDS_DRIGHT_CLK_P
LVDS_DRIGHT_N<15..0>
LVDS_DRIGHT_P<15..0>
HAVING TWO *RIGHT ANGLED* DIN41612 CONNECTORS
MEANS THE ROW NUMBER (1-32) , BUT NOT THE COLUMN (A-C)
NEED TO SWAP TO ALLOW STRAIGHT-THROUGH CONNECTIONS
Fri Jun 6 15:05:34 2014
ISSUE
DATE
MOD NO.
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APPD.
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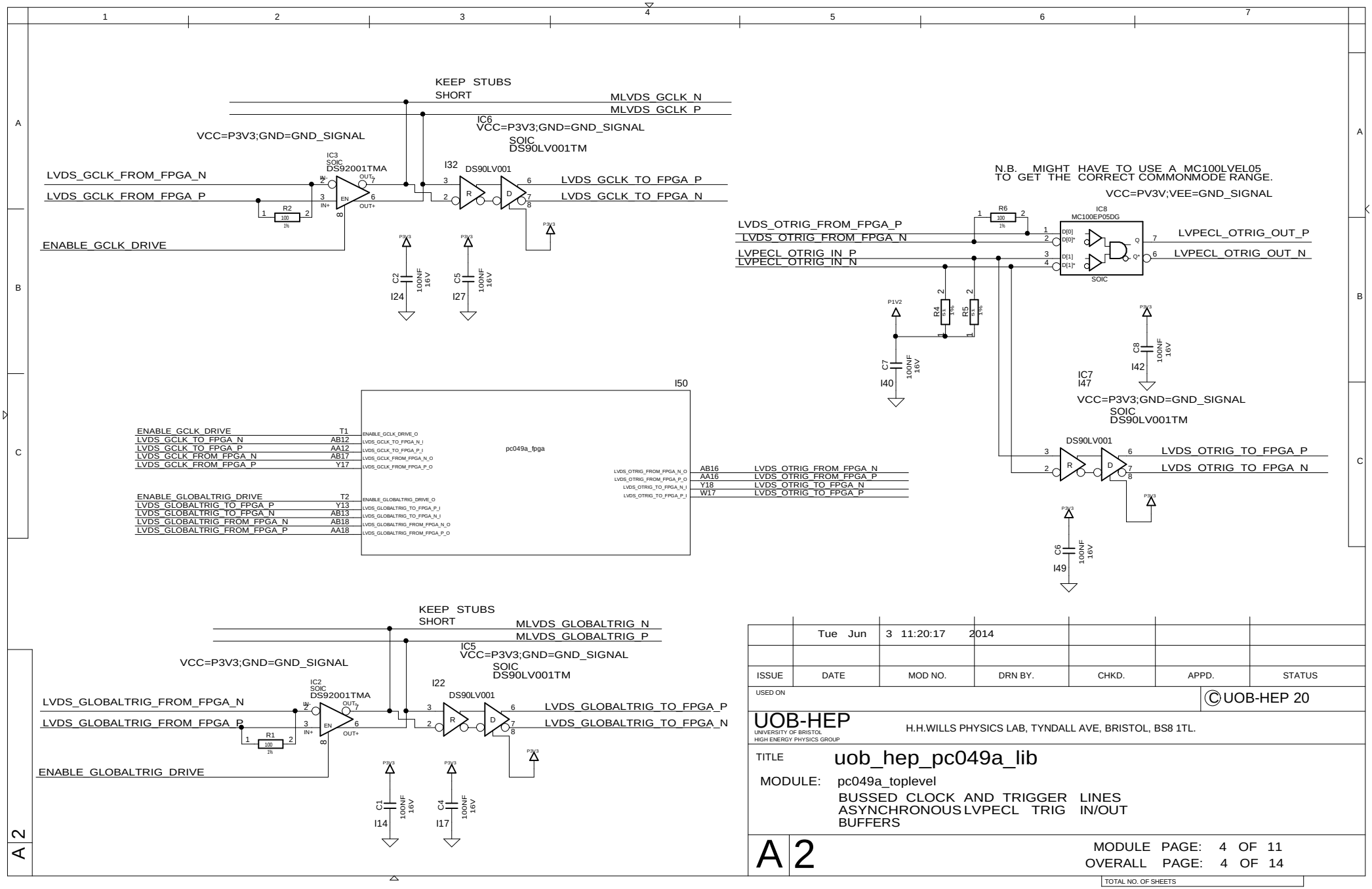
TITLE
uob_hep_pc049a_lib
MODULE: pc049a_toplevel
LVDS DIN41612 I/O
AND FPGA CONNECTIONS
A2
MODULE PAGE: 3 OF 11
OVERALL PAGE: 3 OF 14
TOTAL NO. OF SHEETS



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TITLE uob_hep_pc049a_lib

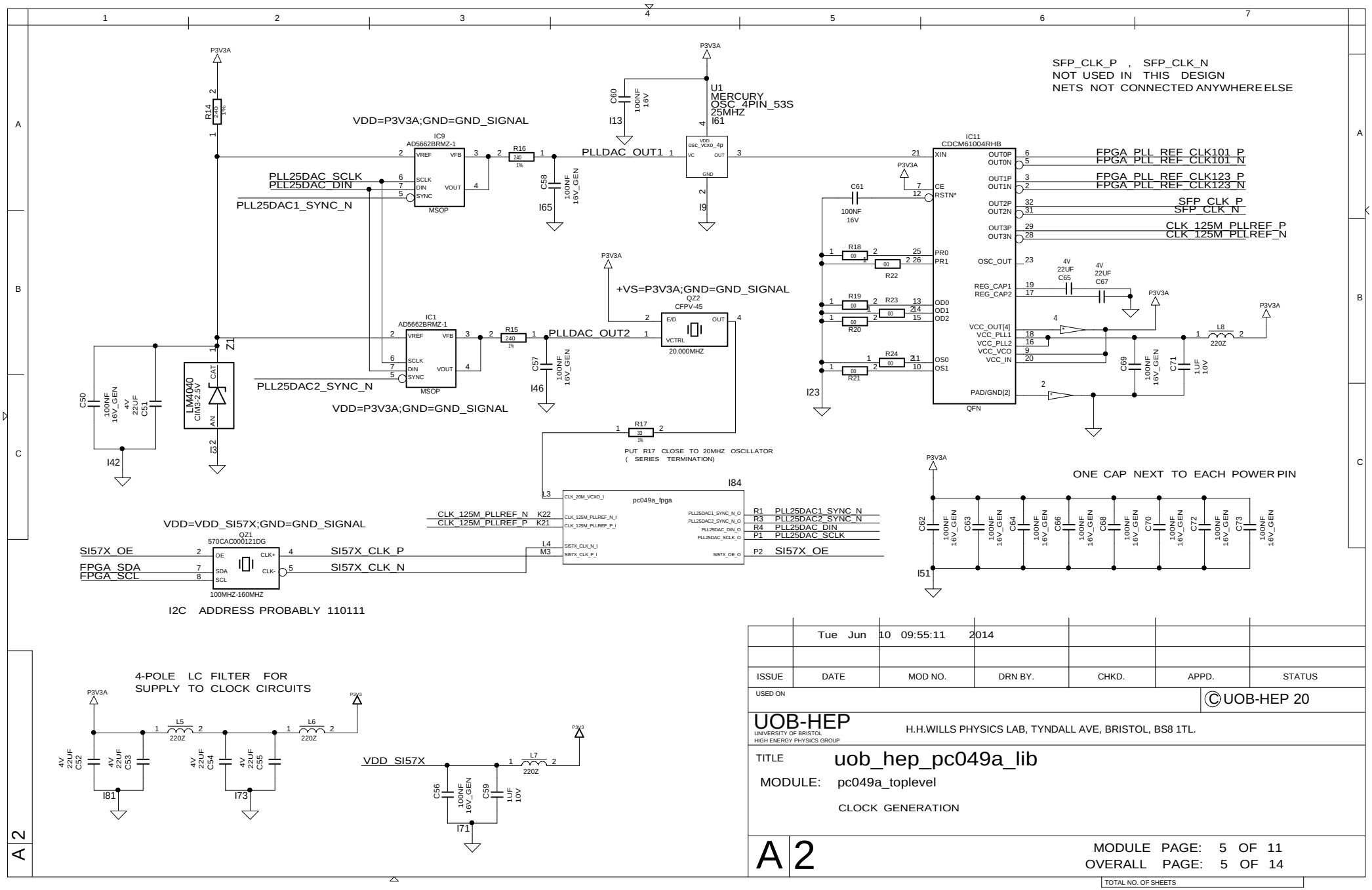
MODULE: pc049a_toplevel

BUSSED CLOCK AND TRIGGER LINES
ASYNCHRONOUS LVPECL TRIG IN/OUT
BUFFERS

A2

MODULE PAGE: 4 OF 11
OVERALL PAGE: 4 OF 14

TOTAL NO. OF SHEETS



ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel

CLOCK GENERATION

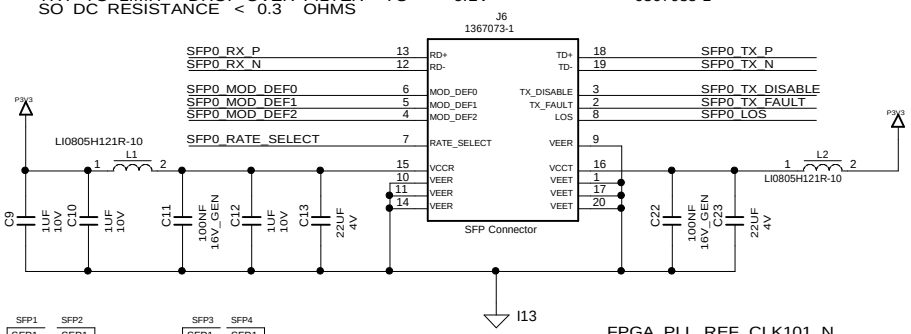
A2

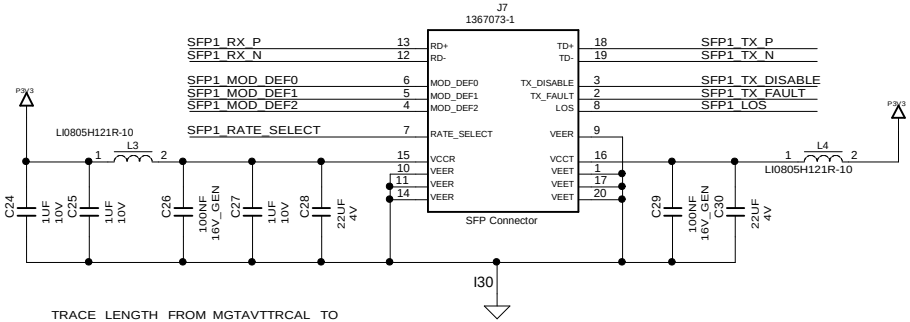
MODULE PAGE: 5 OF 11
OVERALL PAGE: 5 OF 14

TOTAL NO. OF SHEETS

SFP POWER CONSUMPTION UP TO 1W
TRY TO LIMIT DROP OVER FILTER TO < 0.1V
SO DC RESISTANCE < 0.3 OHMS

ORIENT CONNECTOR WITH
PINS 1-10 TOWARDS BEZEL
USE WITH A TYCO SFP CAGE
6367035-1

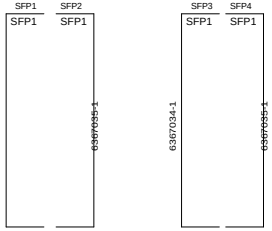




I13

I30

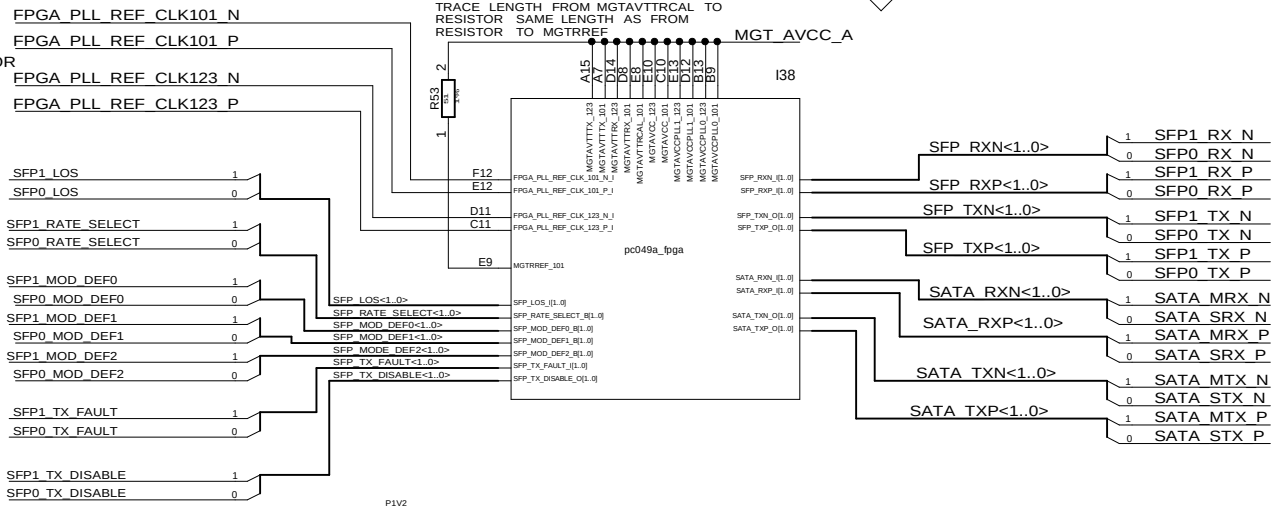
SFP CAGES IN TWO PARTS
SEPARATE FROM SFP CONNECTOR



TRACE LENGTH FROM MGTAVTTRCAL TO
RESISTOR SAME LENGTH AS FROM
RESISTOR TO MGTRREF

MGT_AVCC_A

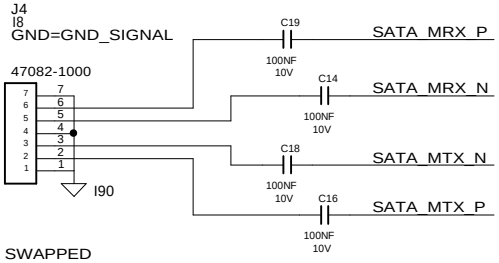
I38



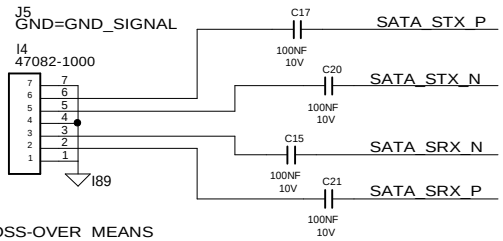
E-SATA CONNECTORS

ONE NORMAL CONNECTIONS (MASTER)
OTHER WITH RX/TX SWAPPED (SLAVE)

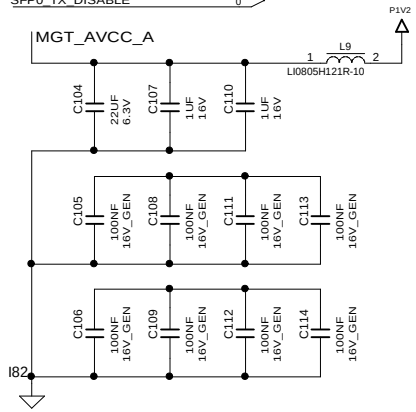
NORMAL CONNECTIONS
(MASTER) J4



TX/RX SWAPPED
(SLAVE) J5



CROSS-OVER MEANS
CAN PLUG MASTER INTO SLAVE
WITH NORMAL ESATA CABLE



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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel
GIGABIT SERIAL LINKS

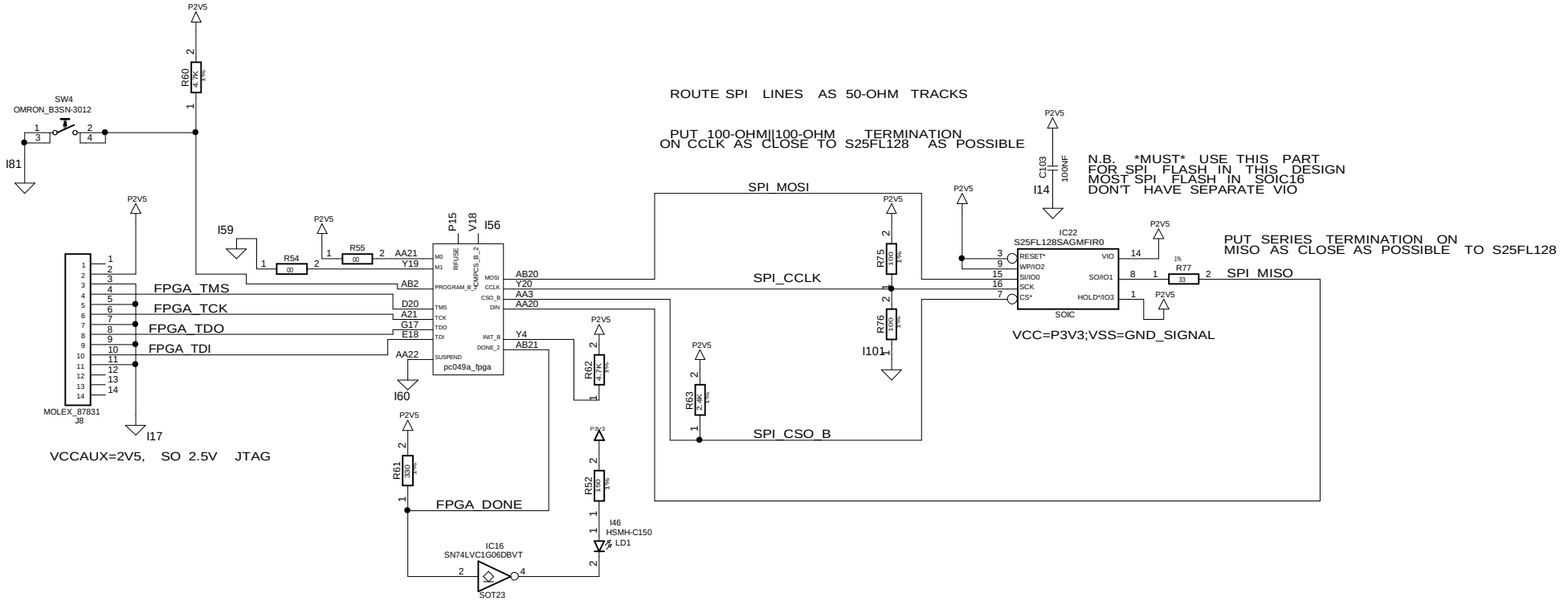
TWO SFP , TWO ESATA

A2

MODULE PAGE: 6 OF 11
OVERALL PAGE: 6 OF 14

TOTAL NO. OF SHEETS

FPGA CONFIGURES AT POWER-ON
PRESS BUTTON TO RE-CONFIGURE



ROUTE SPI LINES AS 50-OHM TRACKS

PUT 100-OHM||100-OHM TERMINATION
ON CCLK AS CLOSE TO S25FL128 AS POSSIBLE

N.B. *MUST* USE THIS PART
FOR SPI FLASH IN THIS DESIGN
MOST SPI FLASH IN SOIC16
DON'T HAVE SEPARATE VIO

PUT SERIES TERMINATION ON
MISO AS CLOSE AS POSSIBLE TO S25FL128

SEE FIGURE 2-12 IN XILINX UG380
FOR DIAGRAM OF CONFIGURATION CIRCUIT

AVOID ATTACHING LARGE, CAPACITIVE LOAD OF LED
FROM DONE PIN BY USING BUFFER
DONE GOES HIGH AND LED LIGHTS
AT END OF CONFIGURATION

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TITLE uob_hep_pc049a_lib

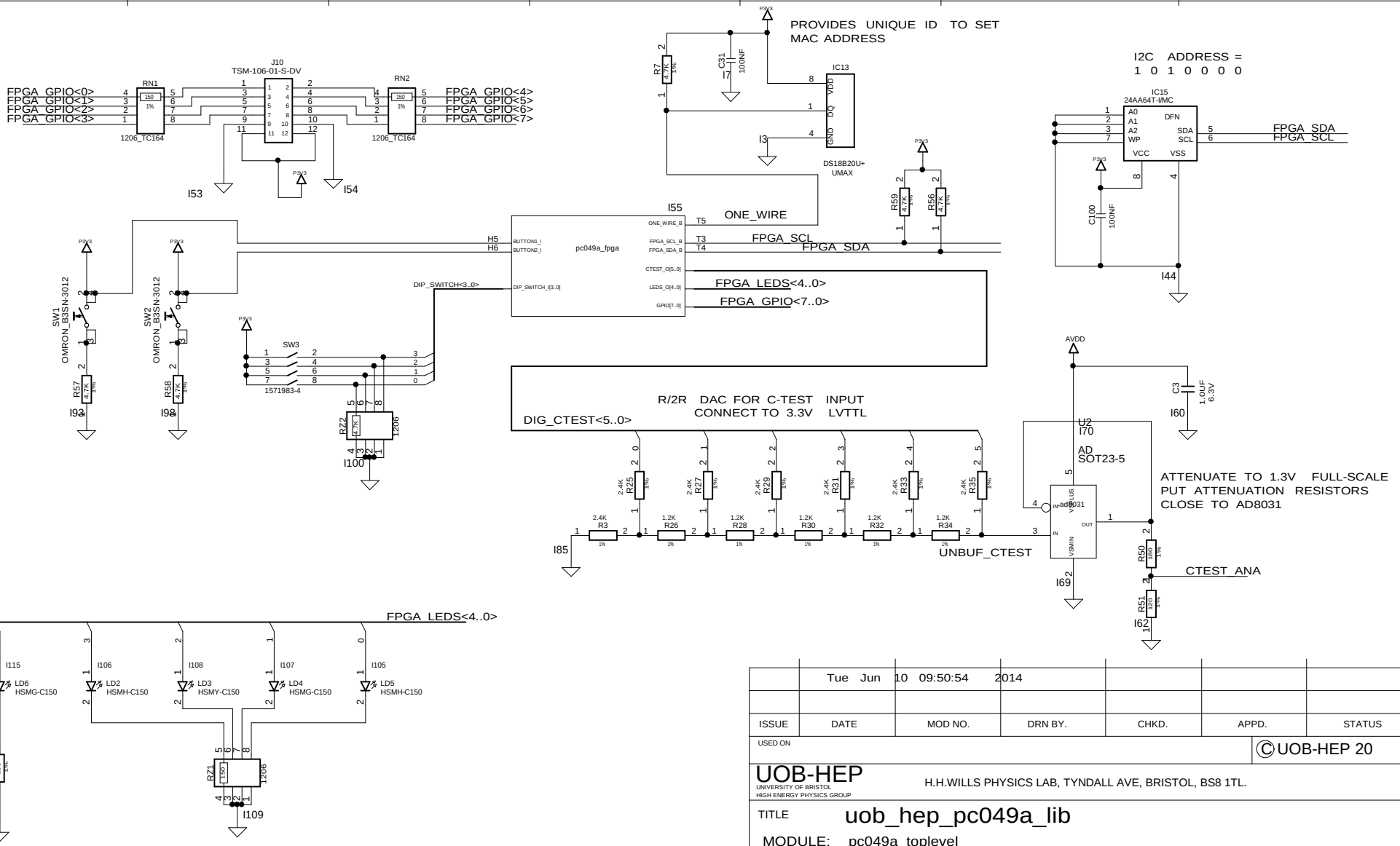
MODULE: pc049a_toplevel

SPI FLASH AND JTAG CONFIGURATION

A2

MODULE PAGE: 7 OF 11
OVERALL PAGE: 7 OF 14

TOTAL NO. OF SHEETS



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TITLE: uob_hep_pc049a_lib

MODULE: pc049a_toplevel

I2C-EEPROM , R/2R DAC FOR CTEST

1-WIRE THERMOMETER/UNIQUE ID CHIP , GPIO , LEDS , DIP-SWITCHES

A2

MODULE PAGE: 8 OF 11

OVERALL PAGE: 8 OF 14

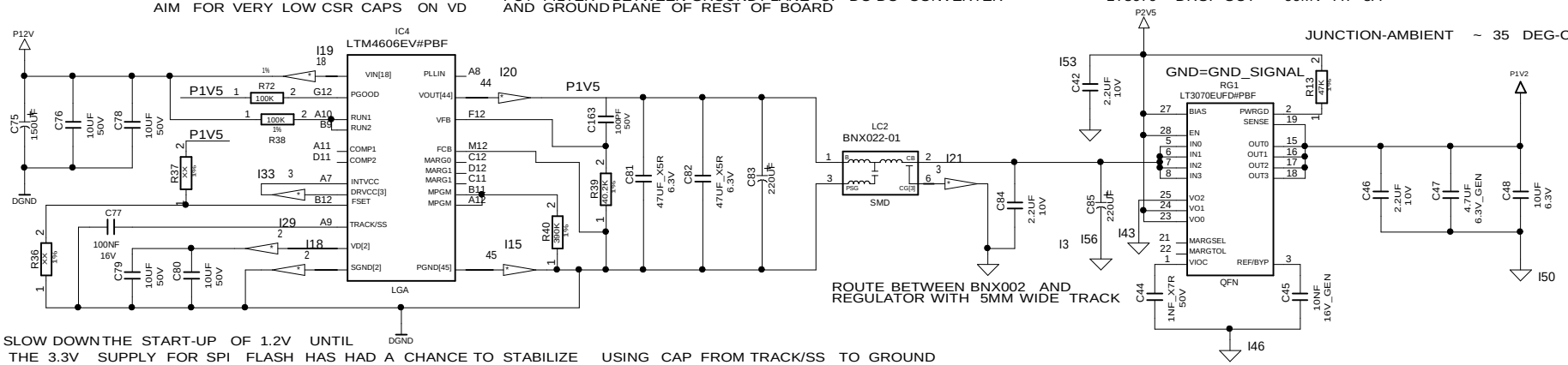
TOTAL NO. OF SHEETS

WANT TO KEEP GROUND AND POWER-PLANE NOISE AWAY FROM MAROC
PUT FILTER BETWEEN GROUND PLANE OF DC-DC CONVERTER
AND GROUND PLANE OF REST OF BOARD

AIM FOR VERY LOW CSR CAPS ON VD

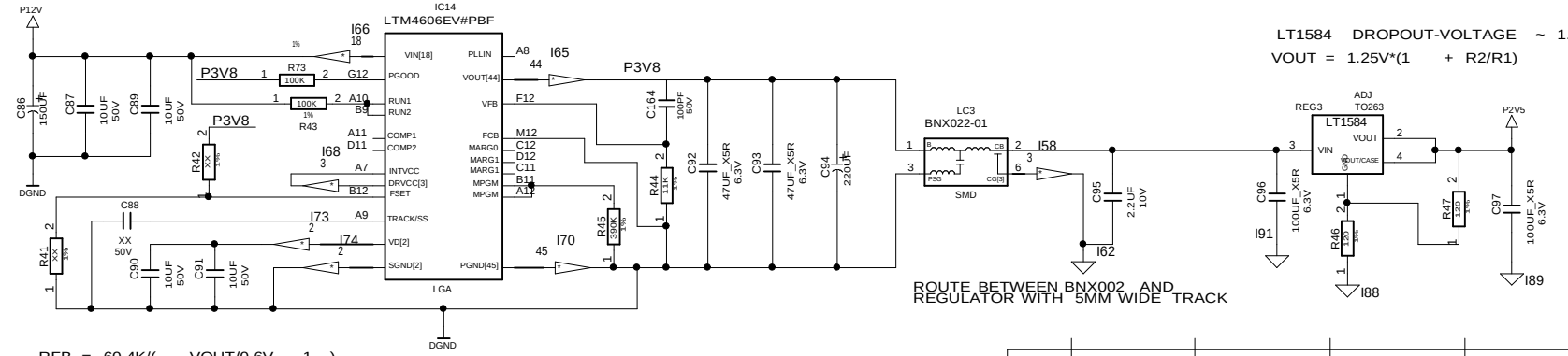
PUT LINEAR REGULATOR NEAR FPGA
LT3070 DROP-OUT = 90MV AT 5A

JUNCTION-AMBIENT ~ 35 DEG-C/W



ROUTE BETWEEN BNX002 AND REGULATOR WITH 5MM WIDE TRACK

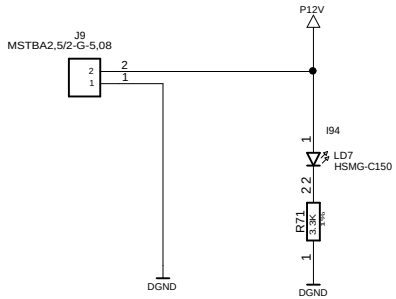
SLOW DOWN THE START-UP OF 1.2V UNTIL THE 3.3V SUPPLY FOR SPI FLASH HAS HAD A CHANCE TO STABILIZE USING CAP FROM TRACK/SS TO GROUND



LT1584 DROPOUT-VOLTAGE ~ 1.2V @ 4.5A , 25-DEGC
VOUT = 1.25V*(1 + R2/R1)

ROUTE BETWEEN BNX002 AND REGULATOR WITH 5MM WIDE TRACK

RFB = 60.4K/(VOUT/0.6V -1)



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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel
DC-DC CONVERTERS
(1.2V , 2.5V FOR FPGA)

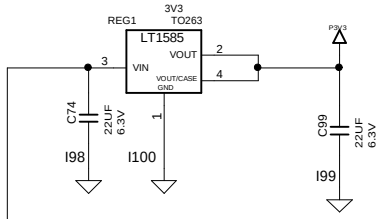
A2

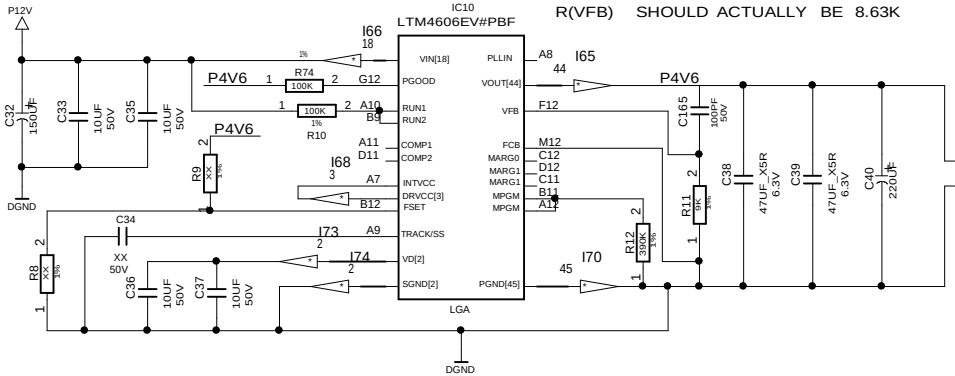
MODULE PAGE: 9 OF 11
OVERALL PAGE: 9 OF 14

TOTAL NO. OF SHEETS

3.3V @ 4.6A
3.5V @ 0.4A (THERMALLY LIMITED)

LT1585 DROPOUT-VOLTAGE ~ 1.2V @ 4.5A , 25-DEGC
VOUT = 1.25V*(1 + R2/R1)

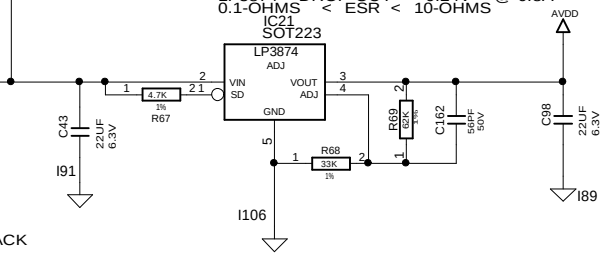




RFB = 60.4K/(VOUT/0.6V -1)

ROUTE BETWEEN BNX002 AND REGULATOR WITH 5MM WIDE TRACK

MAROC USES A MAXIMUM OF 300MA AT 3.5V
VOUT=1.216(1+R1/R2)
~ 150 DEG-C/W
LP3874 DROP-OUT = 0.24V @ 0.8A
0.1-OHMS < ESR < 10-OHMS



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TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel
DC-DC CONVERTERS
(3.3V FOR FPGA , 3.5V FOR MAROC)

A2

MODULE PAGE: 10 OF 11
OVERALL PAGE: 10 OF 14

TOTAL NO. OF SHEETS

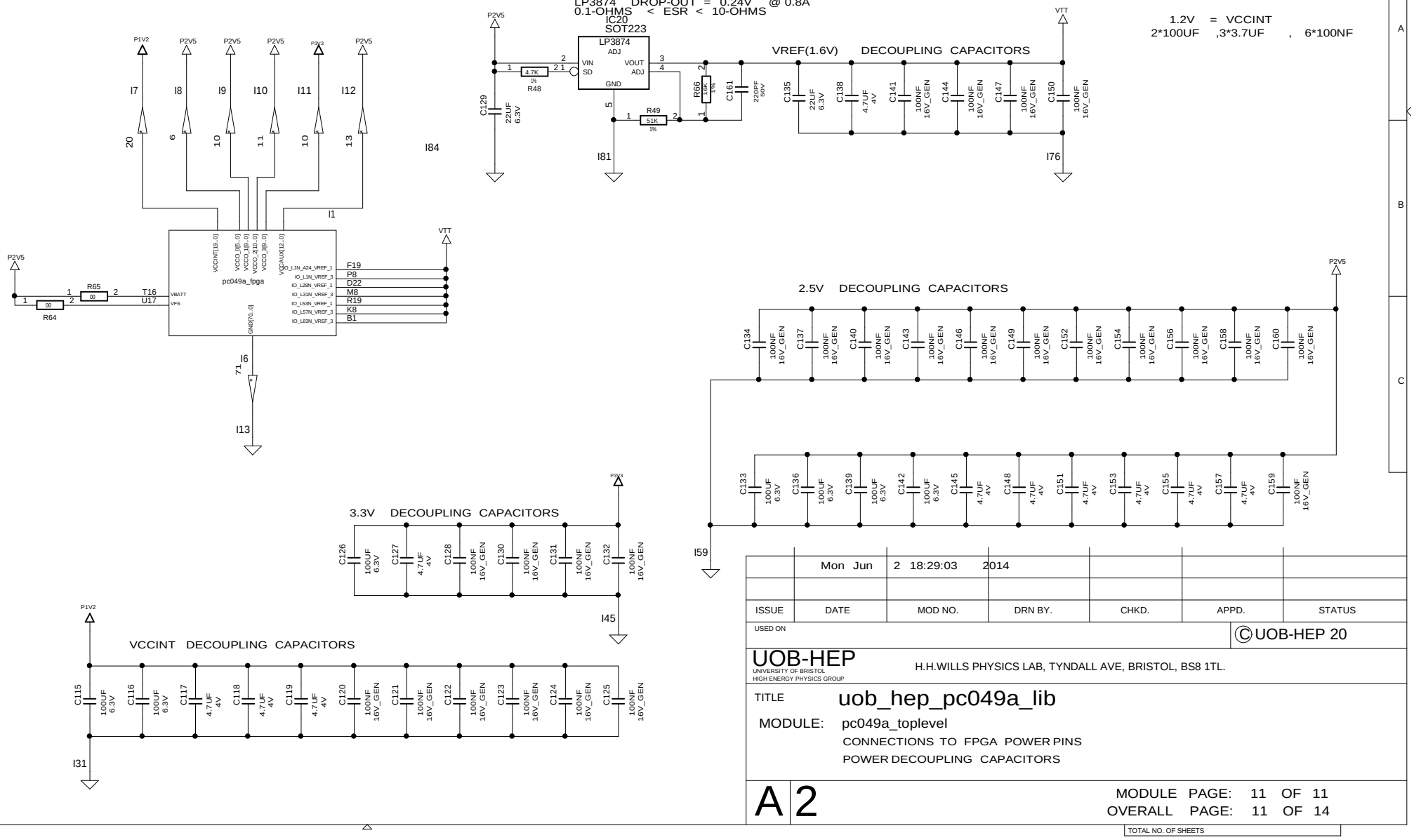
REMEMBER:
RESISTORS FOR SSTL VT (TRIGGER , DATA SIGNALS)
LOOKS LIKE RESITORS ARE *NOT* NEEDED IN SPARTAN6 TO SELECT DIFF TERM VALUE (FOR LVDS INPUTS)
REFER TO XILINX UG393 FOR DECOUPLING CAPACITOR RECOMMENDATIONS

2.5V = VCCAUX , VCCO(0,1,2) =
(1+1+1+1)*100UF , (2+1+1+1)*4.7UF , (4+2+3+3)*100NF

3.3V = VCCO(3) =
1*100UF , 1*4.7UF , 3*100NF

1.2V = VCCINT
2*100UF ,3*3.7UF , 6*100NF

VOUT=1.216(1+R1/R2)
~ 150 DEG-C/W
LP3874 DROP-OUT = 0.24V @ 0.8A
0.1-OHMS < ESR < 10-OHMS



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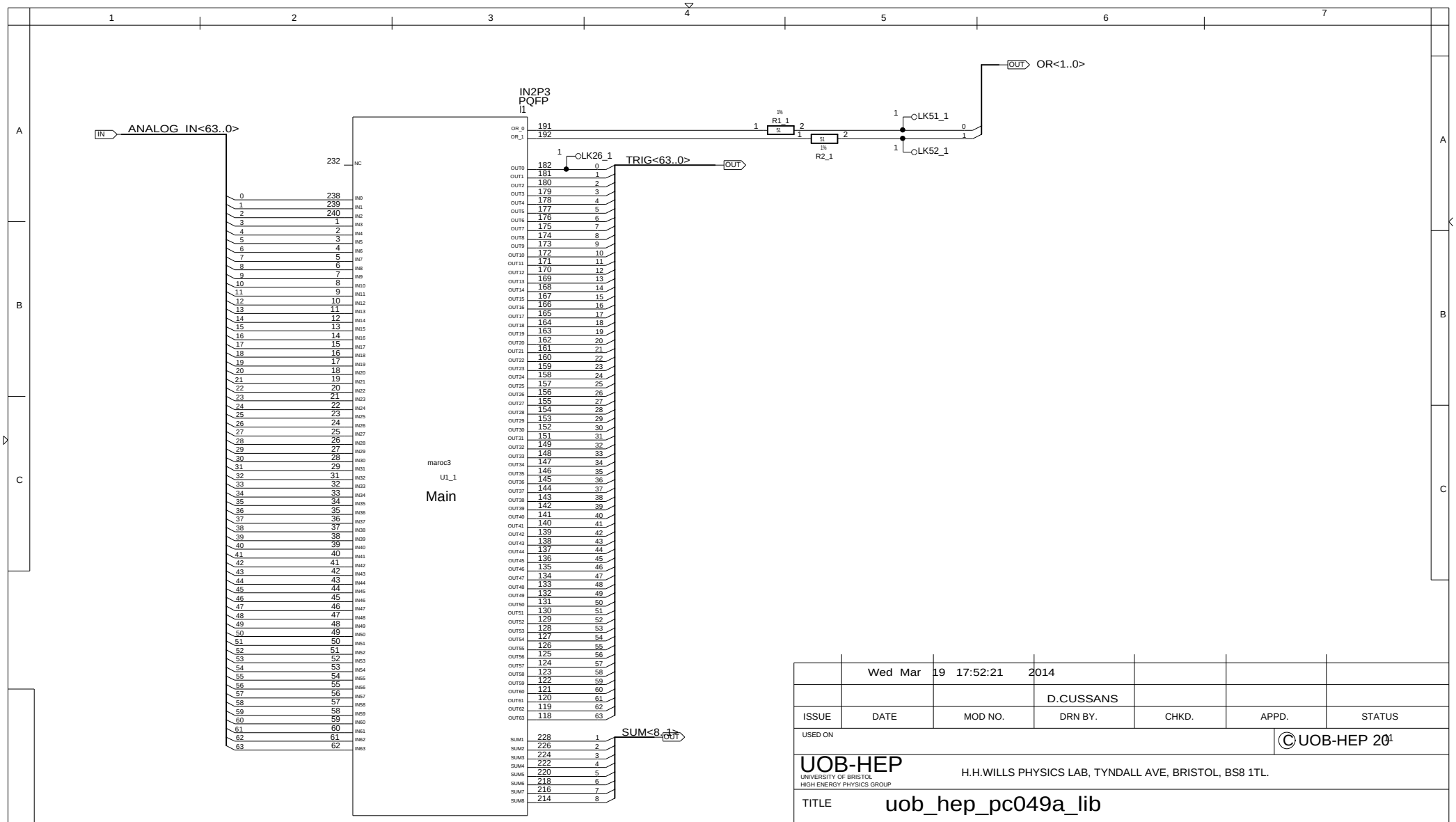
TITLE uob_hep_pc049a_lib

MODULE: pc049a_toplevel
CONNECTIONS TO FPGA POWER PINS
POWER DECOUPLING CAPACITORS

A2

MODULE PAGE: 11 OF 11
OVERALL PAGE: 11 OF 14

TOTAL NO. OF SHEETS



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TITLE uob_hep_pc049a_lib

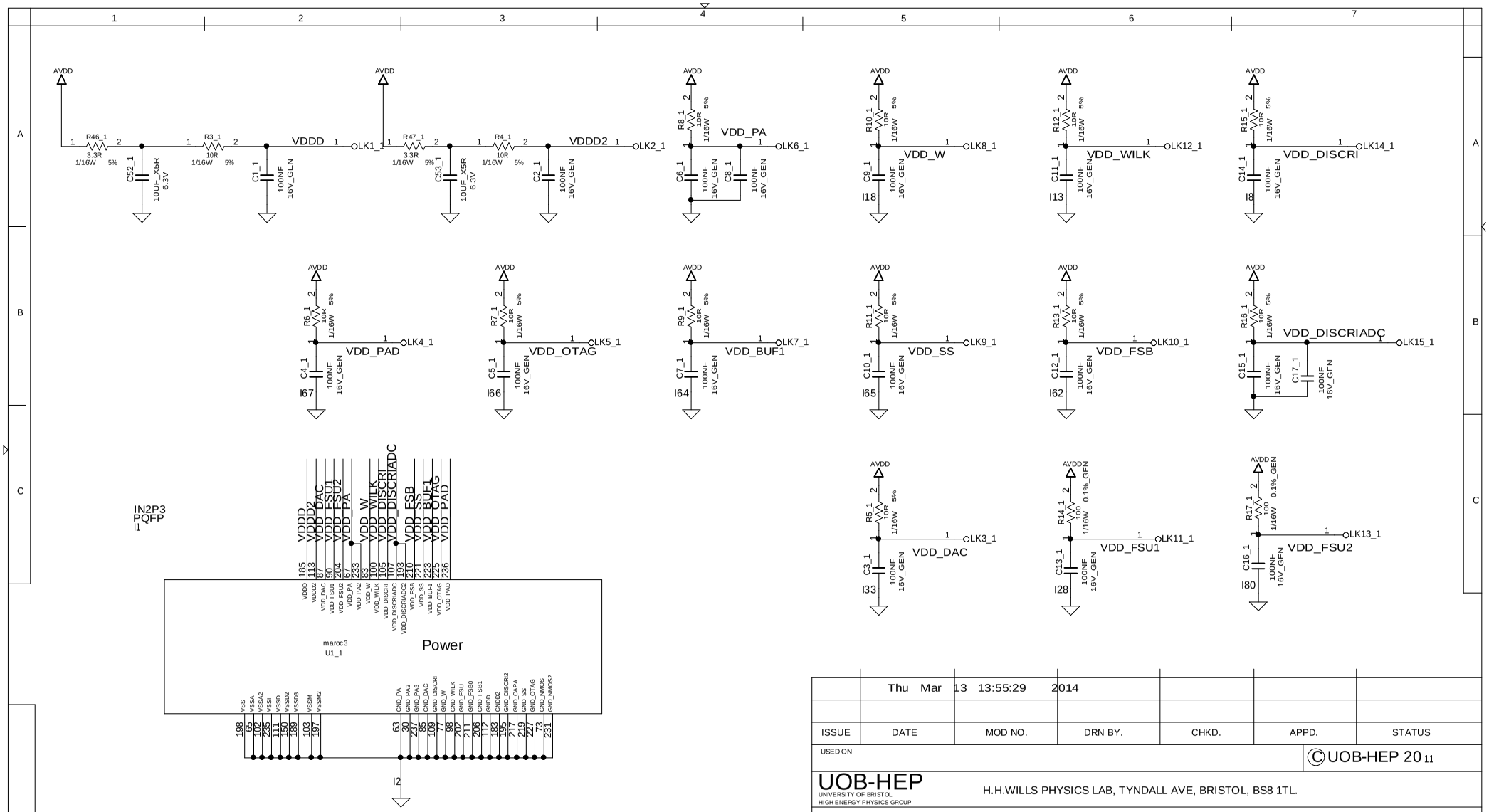
MODULE: pc043c_single_maroc

ANALOGUE INPUTS, TRIGGER OUTPUTS AND SUM OUTPUTS

A2

MODULE PAGE: 1 OF 3
OVERALL PAGE: 12 OF 14

TOTAL NO. OF SHEETS



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TITLE uob_hep_pc049a_lib

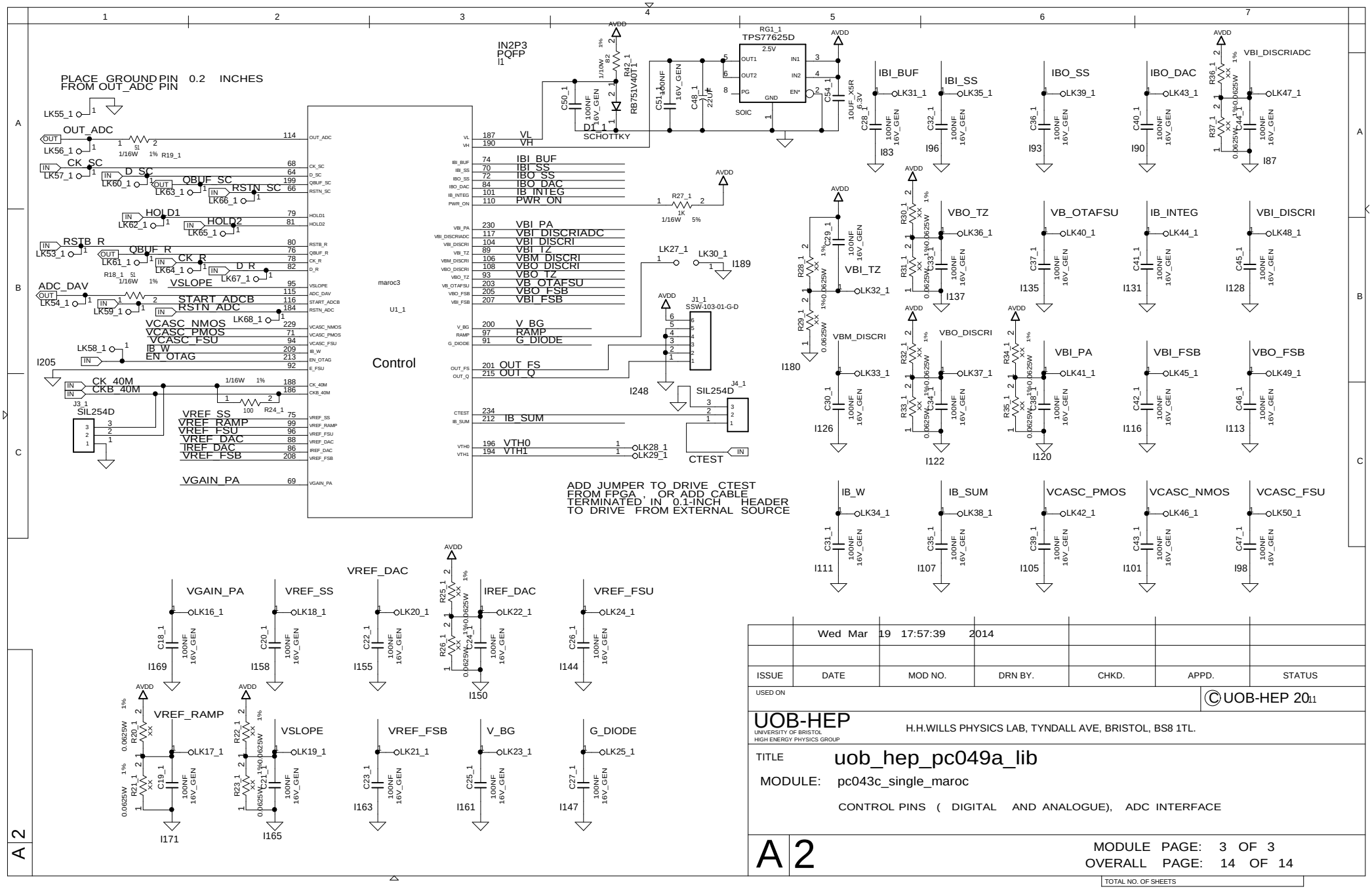
MODULE: pc043c_single_maroc

POWER SUPPLY PINS

A2

MODULE PAGE: 2 OF 3
OVERALL PAGE: 13 OF 14

TOTAL NO. OF SHEETS



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TITLE **uob_hep_pc049a_lib**

MODULE: pc043c_single_maroc

CONTROL PINS (DIGITAL AND ANALOGUE), ADC INTERFACE

A2

MODULE PAGE: 3 OF 3
OVERALL PAGE: 14 OF 14

TOTAL NO. OF SHEETS