CERN Beam Instrumentation Group

Document Type: Functional Specifications

VME FMC Carrier Functional Specifications.

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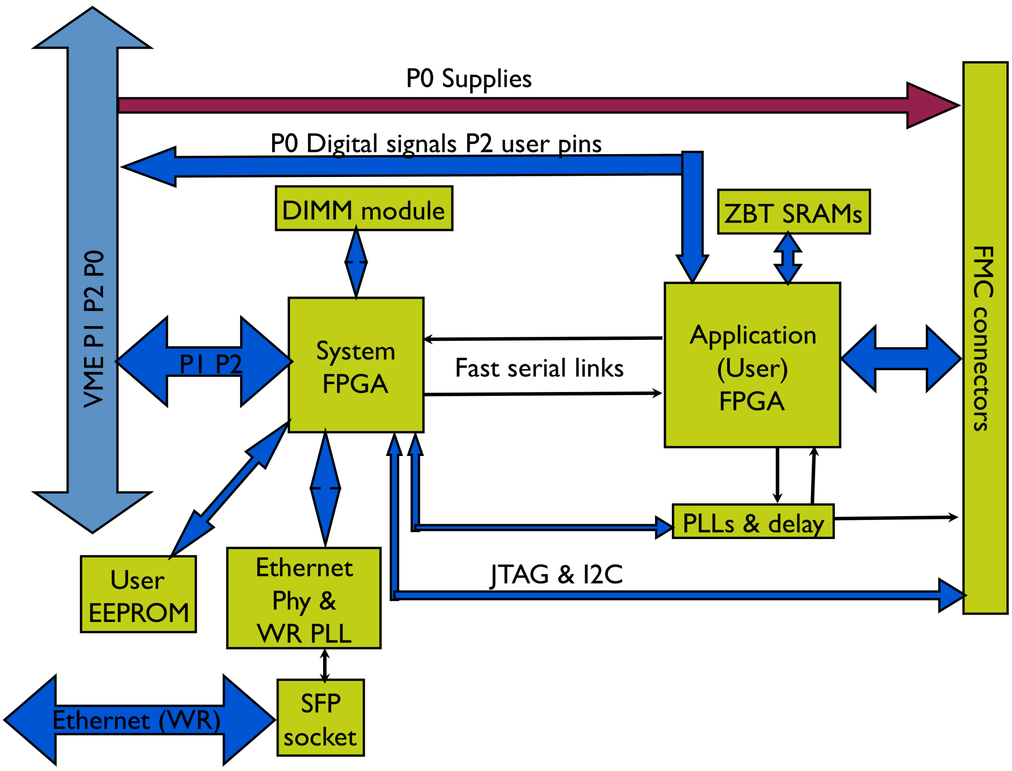
Summary:

The VME FMC Carrier (VFC) is a general-purpose carrier for 2 low pin count FMC (VITA 57) with VME 64x and Ethernet interfaces. The Ethernet interface is designed to be White Rabbit (www.ohwr.org) enabled.
The board uses connectors of type CC-HPC-10 instead of CC-LPC-10 to accommodate some signal and power supply lines required by CERN BE-BI and BE-CO on the unused pins. This breaks rule 3.9 of the standard, but still ensures full compatibility with commercial low pin count mezzanines.



History of Changes

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Date	Pages	Changes
03/08/2009	All	Initial Submission
25/09/2009	All	Corrected the English and added the paragraphs suggested on EDMS

Table of Contents

1. System monitoring and power up accessibility

A System FPGA (S-FPGA) shall be dedicated to monitoring the board status and configuration as well as providing VME and ethernet access after power up. For this purpose it shall be loaded at power up from a non volatile memory with a non application dependent firmware.
The S-FPGA shall give the possibility to configure the Application FPGA via the VME bus, the ethernet bus or using a configuration previously stored in an on board non volatile memory.
The following quantities shall be monitored and/or accessible via the S-FPGA:

- Board temperature
- PCB version
- System firmware version
- Board unique ID
- Status of the FMC connectors (used or not)
- Status of the FMC power supply
- Status of the Application FPGA (configured or not)

The S-FPGA is also meant to abstract the actual interface to the board (VME or Ethernet) for the application logic designer.

2. Application FPGA

The one or more FPGAs implementing the application logic (A-FPGA) shall have direct connection to the mezzanine user pins as specified by the VITA 57 standard.
The link between the A-FPGA and the S-FPGA shall have an effective, sustainable bandwidth higher than 40MB/s to exclude that this link can become the bottleneck for data transfer over the VME bus.
A medium to high density, state of the art device shall be chosen as A-FPGA to ensure that designers will have sufficient space for the implementation of their algorithm.
To allow easy and fast implementation of algorithms requiring a high amount of memory the A-FPGA shall have full access to 2 independent ZBT SRAMs.

3. Interfaces

3.1. VME 64x Interface

The board shall have all the electrical connections required to implemet a fully capable VME64x slave interface.
The VME interface implemented in the S-FPGA shall be available since power up and be capable of using the Geographical Addressing scheme to determine its base address or have it set manually by the user via switches or an equivalent mechanism.

3.2. White Rabbit enabled Ethernet interface

The board shall be accessible via ethernet on power up. The implemented ethernet interface shall be White Rabbit (WR) enabled.
The board will be equipped with a SFP socket to allow the user to choose the media for the communication.
The base protocol for data transfer will be a custom one chosen by BE-CO and shall give the same access possibility as VME.

3.3. P0 connectivity as defined for the CERN-BE/BI crates

The digital connectivity on the P0 as defined for the CERN-BE/BI crates shall be preserved.

	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	GND	BusLine[0]	-5V2RET	-5V2RET	HwLowByte[0]	HwHighByte[0]	GND
2	GND	BusLine[1]	-5V2RET	-5V2RET	HwLowByte[1]	HwHighByte[1]	GND
3	GND	BusLine[2]	-5V2RET	-5V2RET	HwLowByte[2]	HwHighByte[2]	GND
4	GND	BusLine[3]	-5V2	-5V2	HwLowByte[3]	HwHighByte[3]	GND
5	GND	BusLine[4]	-5V2	-5V2	HwLowByte[4]	HwHighByte[4]	GND
6	GND	BusLine[5]	-5V2	-5V2	HwLowByte[5]	HwHighByte[5]	GND
7	GND	BusLine[6]	-2VRET	-2VRET	HwLowByte[6]	HwHighByte[6]	GND
8	GND	BusLine[7]	-2VRET	-2VRET	HwLowByte[7]	HwHighByte[7]	GND
9	GND		-2V	-2V	DaisyChain1_i	DaisyChain1_o	GND
10	GND		-2V	-2V	DaisyChain2_i	DaisyChain2_o	GND
11	GND						GND
12	GND		+5V	+5V	BunchSelect[0]	LvdsTurnClockP_i	GND
13	GND		+5V	+5V	BunchSelect[1]	LvdsTurnClockN_i	GND
14	GND		+5VRET	+5VRET	BunchSelect[2]	TtlTurnClock_i	GND
15	GND		+5VRET	+5VRET	BunchSelect[3]	GND	GND
16	GND		+15V	+15V	BunchSelect[4]	LvdsBunchClockP_i	GND
17	GND		+15VRET	+15VRET	BunchSelect[5]	LvdsBunchClockN_i	GND
18	GND		-15VRET	-15VRET	BunchSelect[6]	TtlBunchClock_i	GND
19	GND		-15V	-15V	BunchSelect[7]	GND	GND

P0 connector pin definition for the CERN-BE/BI VME crates (slots 3-11 and 13-21)

- **BusLine[7:0]** : bidirectional bus shared by all the cards in slots 3..11 AND 13..21
- **HwLowByte [7:0]**
HwHighByte [7:0]
BunchSelect [7:0] : input bus driven by the board in slot 12 and common to all the cards in the same slots group (3..11 OR 13..21)
- **LvdsTurnClockP_i**
LvdsTurnClockN_i : LVDS input driven by slot 12
- **LvdsBunchClockP_i**
LvdsBunchClockN_i : LVDS input driven by the card in slot 12
- **TtlTurnClock_i**
TtlBunchClock_i : LVTTL inputs driven by the card in slot 12
- **DaisyChain1_i**
DaisyChain2_i : LVTTL input from the previous slot
- **DaisyChain1_o**
DaisyChain2_o : LVTTL output to the next slot

The digital signals shall be sent to or come from the Application FPGA after the required buffering. The power supply and ground connections shall be routed to the FMC mezzanine and to the P2 connector.

Note on the power supplies: The possibility to have the power supplies generated on board should be tested. If the quality of the generated signals is satisfactory then this solution shall be preferred as it would allow them to be switched off when not needed and to use BI mezzanines in non BI crates.

3.4. P2 user pins

The highest possible number of P2 user pins shall be connected straight to the Application FPGA, with the aim being for 40 single ended lines which could also be configureable as 20 LVDS pairs.
An LVDS output from each of the PLL clock sources for the FMC mezzanines shall also be routed to the P2 connector.
In addition all the power supplies and grounds connections foreseen on the P0, or their on board generated equivalents, shall be routed to the P2 user pins.

3.5. Front panel 50Ω input and outputs

2 LVTTL 50Ω inputs and 2 LVTTL 50Ω outputs shall be available on the front panel.

3.6. FMC connectors

The carriers shall be equipped with 2 High Pin Count FMC connectors and be capable of accepting 2 single or 1 double standard, Low Pin Count mezzanine. All the logical signals defined for the LPC connectors in the FMC standard shall be routed to the A-FPGA, except for the JTAG and I2C buses that will be connected to the S-FPGA in order to be able to identify the plugged mezzanines and obtain their power supply requirement prior to the configuration of the Application FPGA.

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Low pin count connector definition

The supply and ground returns coming from the P0, or their equivalents generated on board, will be provided to the mezzanines using pins of the CC-HPC-10 connector not assigned in the LPC pin definition (rows K, J, F, E, B, A). These can be used with FMC mezzanines fitted with a High Pin Count connector but which respect the Low Pin Count definition.

If possible some of the multi gigabit transceiver pairs as defined in the High Pin Count connectors shall be populated.

The clock lines CLK0_C2M_P and CLK0_C2M_N will probably change in the new revision (1.1) of the VITA 57 standard in mezzanine to carrier clocks and will therefore be connected directly to the FPGA. A clean clock source, coming from a PLL with phase and delay compensation, will be provided from the carrier on pins J2 and J3, unused on the LPC connector and defined as C2M clock for the HPC connector in the current revision of the standard.

4. On Board memory

The static memory connected to the S-FPGA and used to store the configuration for the A-FPGA shall be capable of storing more than 1 version of the firmware.
Each of the 2 ZBT SRAMS connected to the A-FPGA shall have at capacity of at least 16Mb and allow access to 32 bit words per read (write) cycle.
A DRAM module shall be available to the S-FPGA for buffering data coming from the A-FPGA before transmission and for generalpurpose non real time storage.

5. Testability

The testability of the board must be kept in mind during the whole design process. Special test firmware shall be produced for the S-FPGA and A-FPGA.
The automated test of the board shall include:

- connection verification and trace integrity
- complete memory test
- external interface test

6. Functional Specifications Evaluated but not Retained

6.1. Embedded HTTP server

It was requested to have an HTTP server based either on an external or embedded uController. The server was foreseen as a general interface for the system and would have given access to the status registers in the S-FPGA as well as to the internal registers of the application for test or monitoring without the need of a dedicated expert tool. The idea was also to reduce the general effort in the design of interfaces, reducing their proliferation.
For the following reasons this functionality was not retained in the final functional specification:

- the system debug should be done by experts and they will not use an HTTP application/browser for such a task.
- an HTTP application is not suited for operation.
- to be able to access the Application FPGA register in a non expert mode (direct addressing) the HTTP server would have to be modified at each change of the application itself and require server and client side applications. As this cannot be the expert/test application or the operational application such a server would not lead to a reduction in the number of interfaces required.
- Giving access to the internal register via a standard browser would decrease the security level of the card.

6.2. P2 - FMCs connections

It was requested to have 16 digital connections configurable as LVDS lines and 8 analog connections between the P2 connector and the FMC connectors.
The signal integrity of the analog lines could not be guaranteed as they need to cross the whole carrier. Those lines could therefore only be used for slow signals and would consequently be better preserved if digitized directly on the P2 extension card or on the FMC mezzanine with their value passed via a serial link.
It would not be possible to connect bidirectional LVDS lines between 3 end points in a generic way. A more flexible solution is to pass in the Application FPGA that would act as a programmable switch. This would also have the advantage of preserving the FMC standard. The final specification therefore only foreseen digital links between the P2 connector and the A-FPGA (see section 3.4).

6.3. On board DSP

It was requested to have a DSP on board in addition to the A-FPGA.
This would have been used mainly for testing the card in the absence of a processor in the VME crate. Such a functionality can be provided directly by the A-FPGA without any major silicon waste. Similarly if there is a need for an embedded processor for some specific application, given the size of the A-FPGA there will be no problem instantiating a soft processor inside it while leaving enough silicon for most of other applications to run.

It was suggested that some applications (e.g. wire scanners) might require complex controls that would be better suited to a DSP than an FPGA. If such cases arise as a specific requirement of a single application then the solution of implementing a real DSP on the FMC mezzanine still exists.
The final specification therefore does not foresee any on board DSP.

6.4. FMC mezzanines in the JTAG chain

Was requested to have the possibility to add the mezzanines to the JTAG chain with the System and the Application FPGA. After some study, there were no identified cases where this would represent a clear advantage over having the JTAG pins of the FMC connector controlled by the system FPGA.