

A

B

C

D

E

A

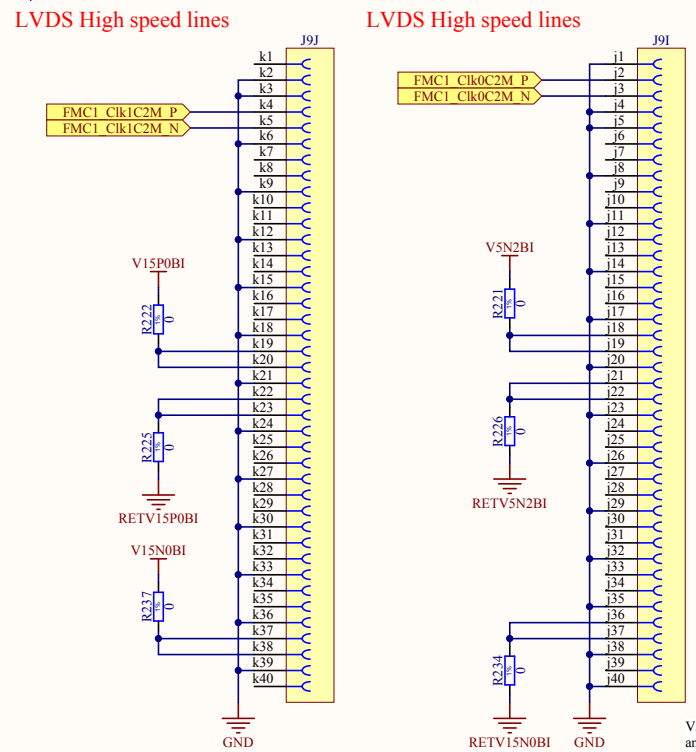
B

C

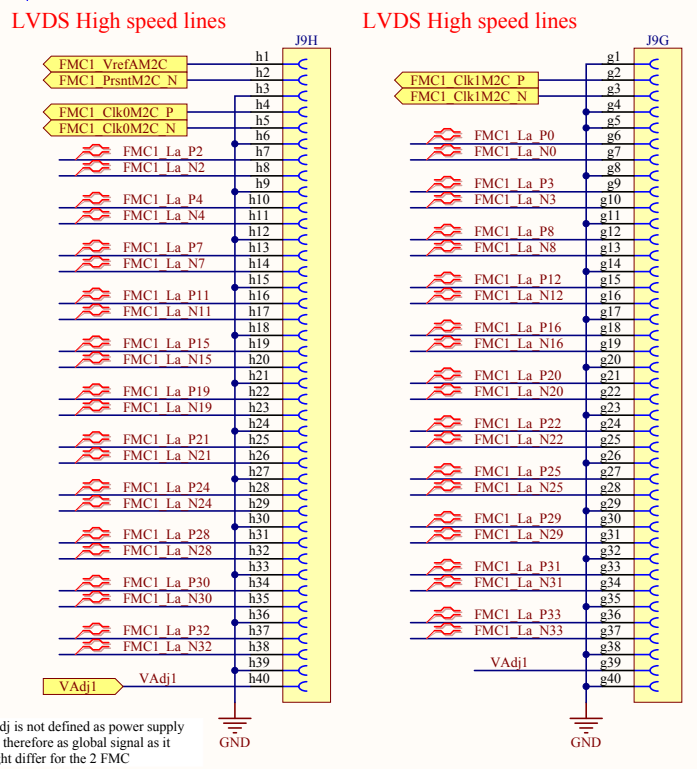
D

E

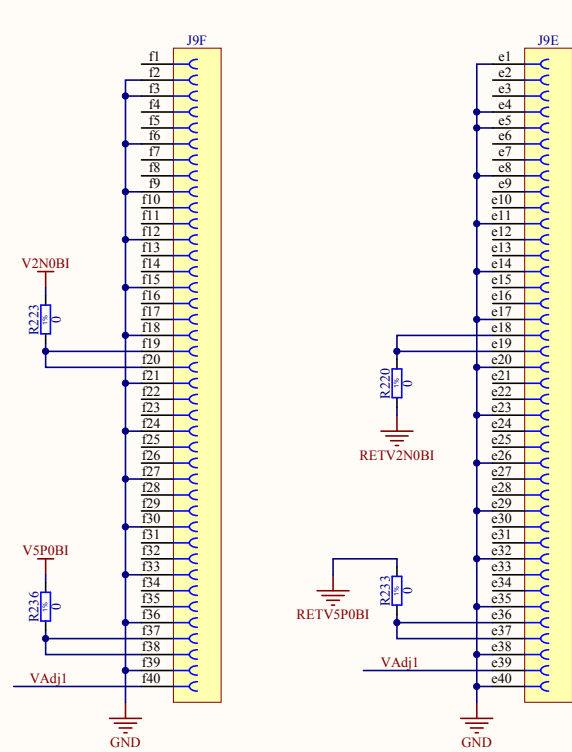
High Pin Count Rows



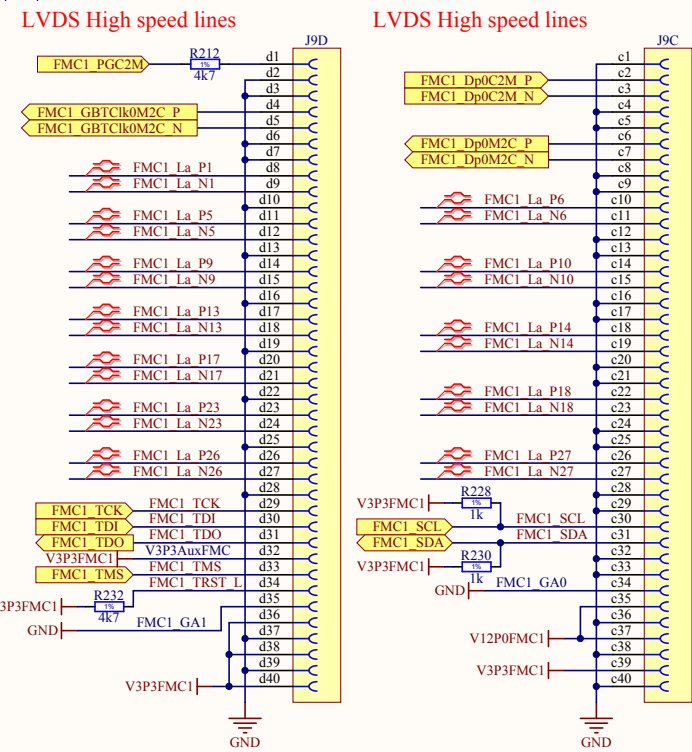
Low Pin Count Rows



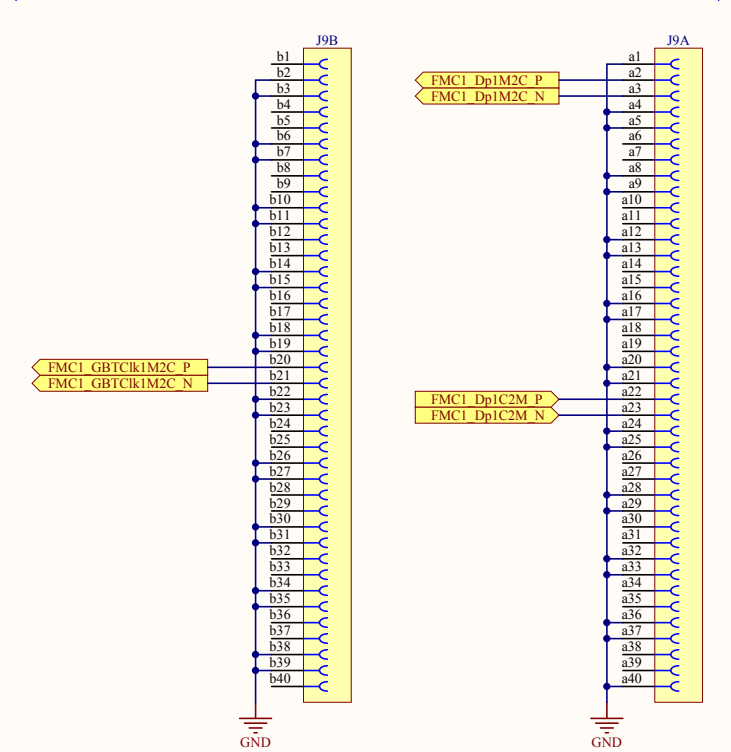
High Pin Count Rows



Low Pin Count Rows



High Pin Count Rows



LaP and LaN are LVDS lines

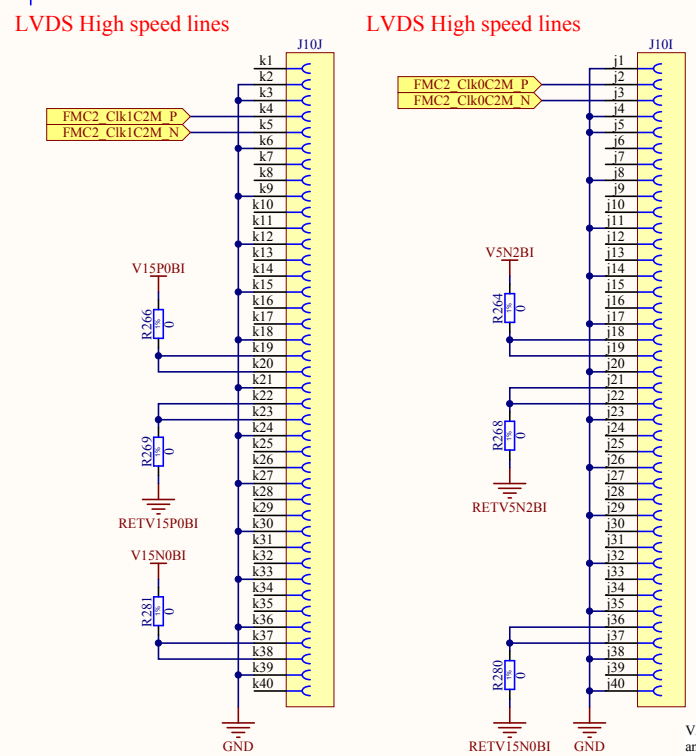


NB: the LVDS pairs must have a differential impedance of 100 ohm and be routed with no skew between the P and the N lines. The skew between the various La pairs should be kept as low as possible.

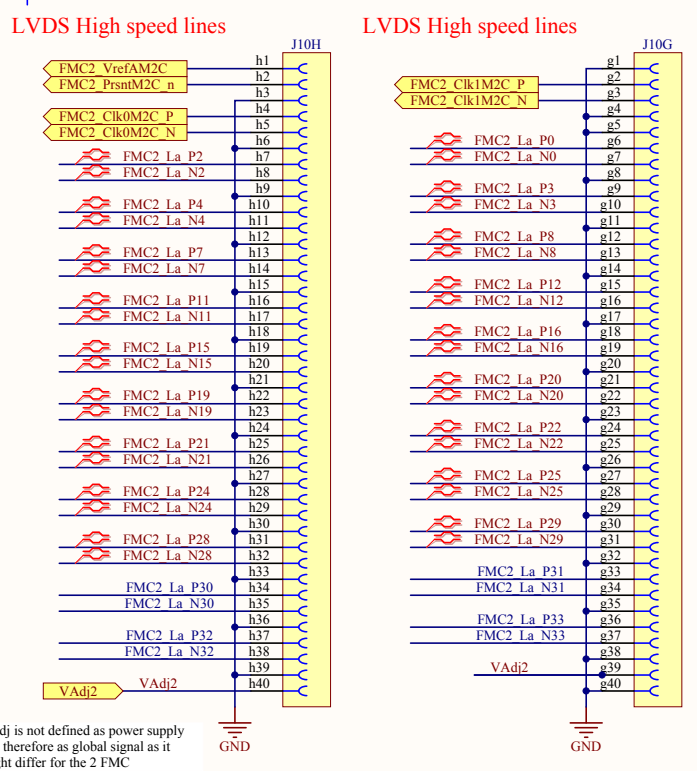
LaP and LaN are LVDS lines



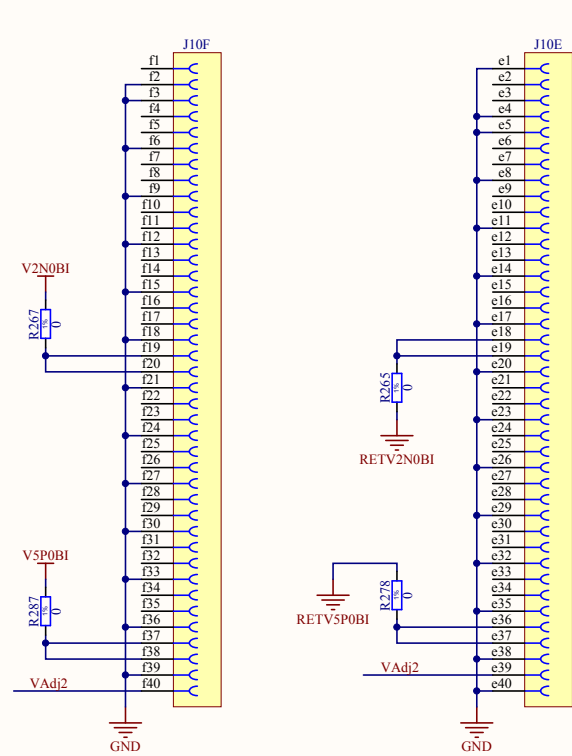
High Pin Count Rows



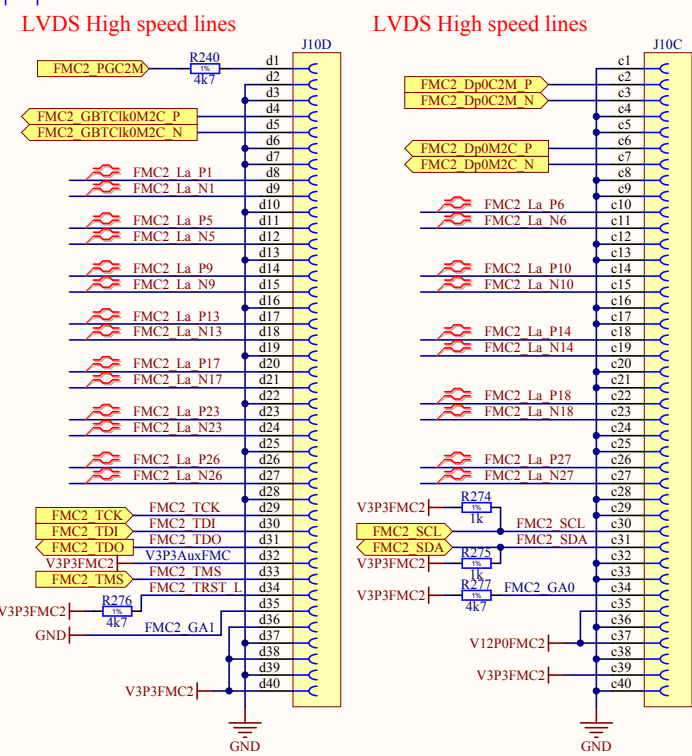
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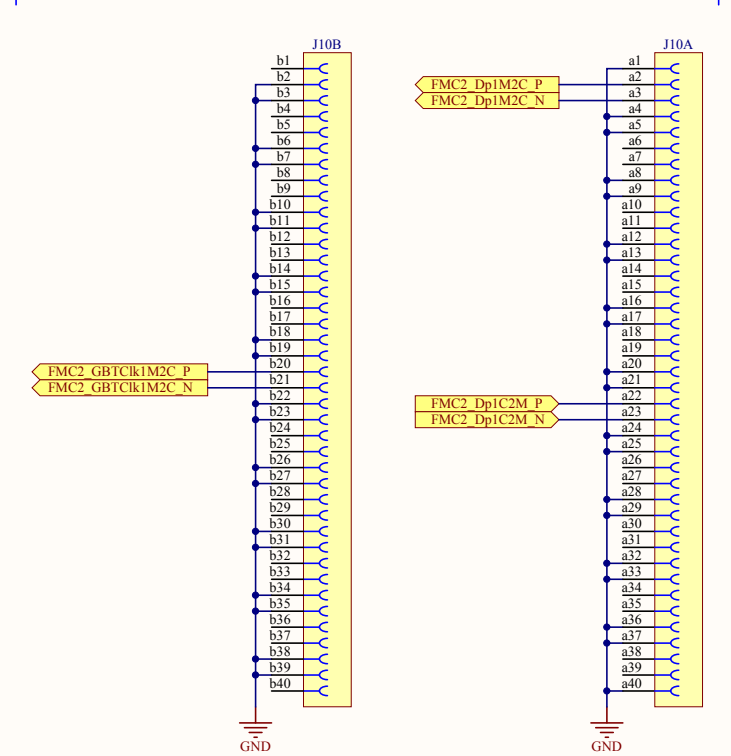
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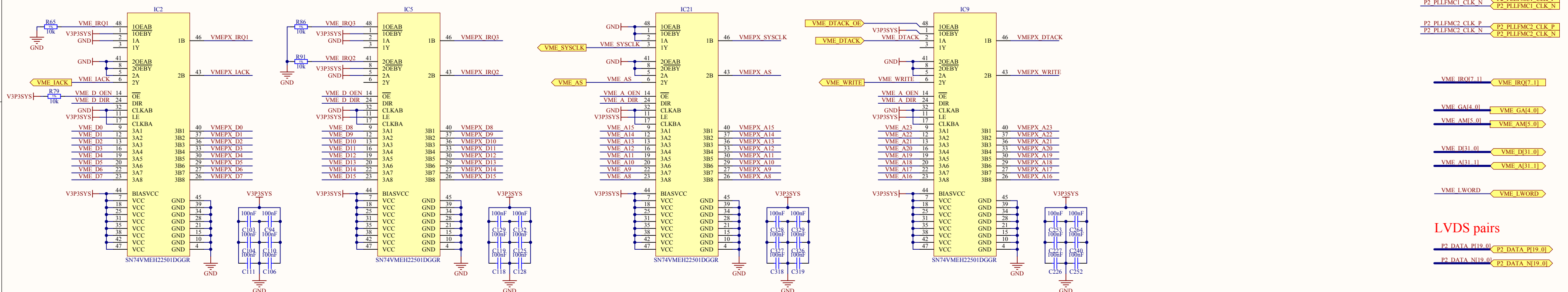
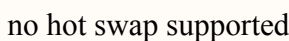


Low Pin Count Rows

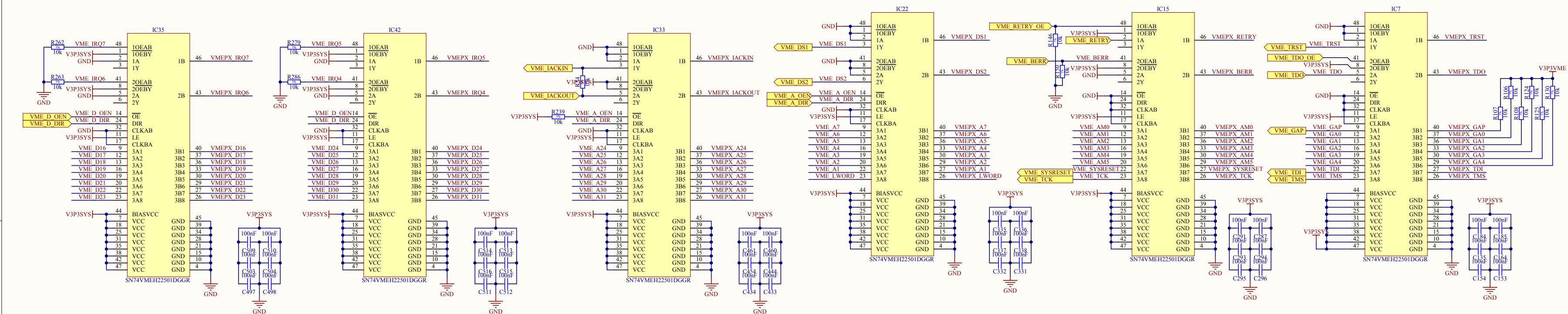


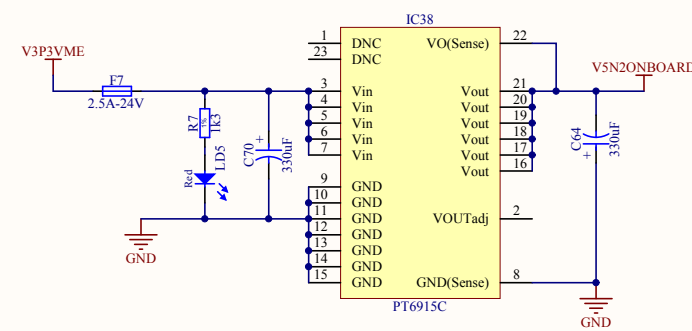
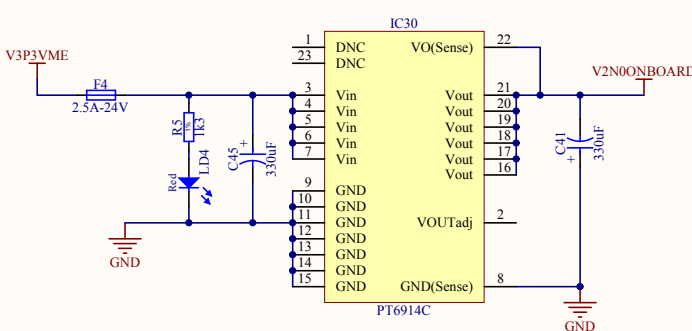
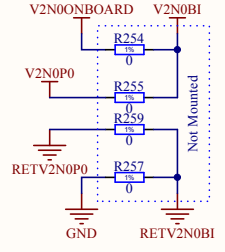
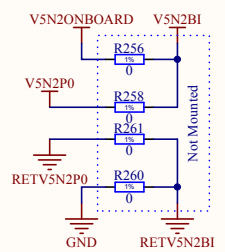
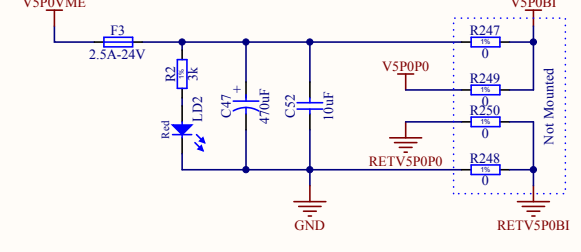
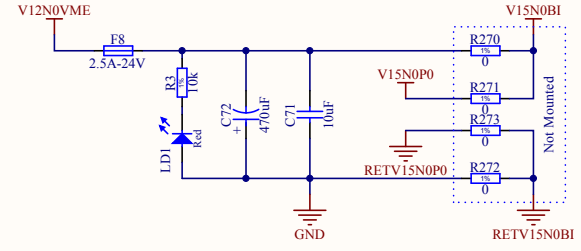
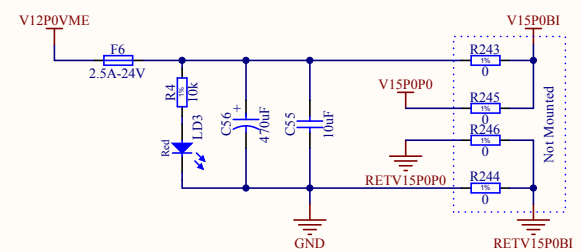
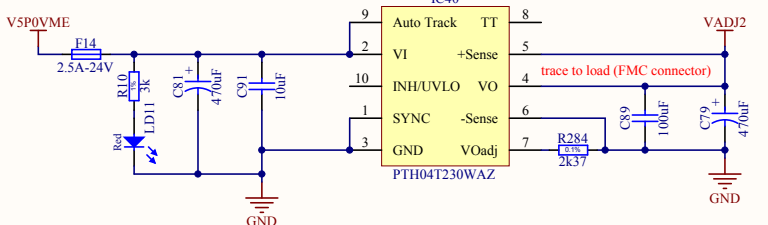
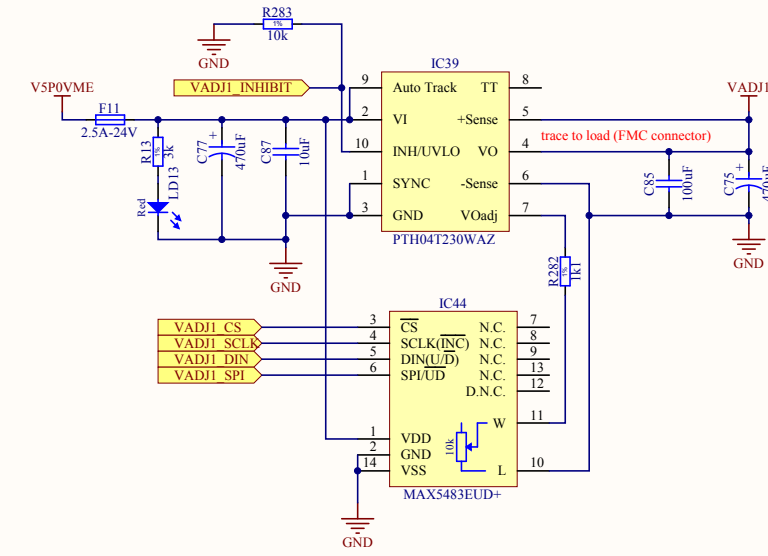
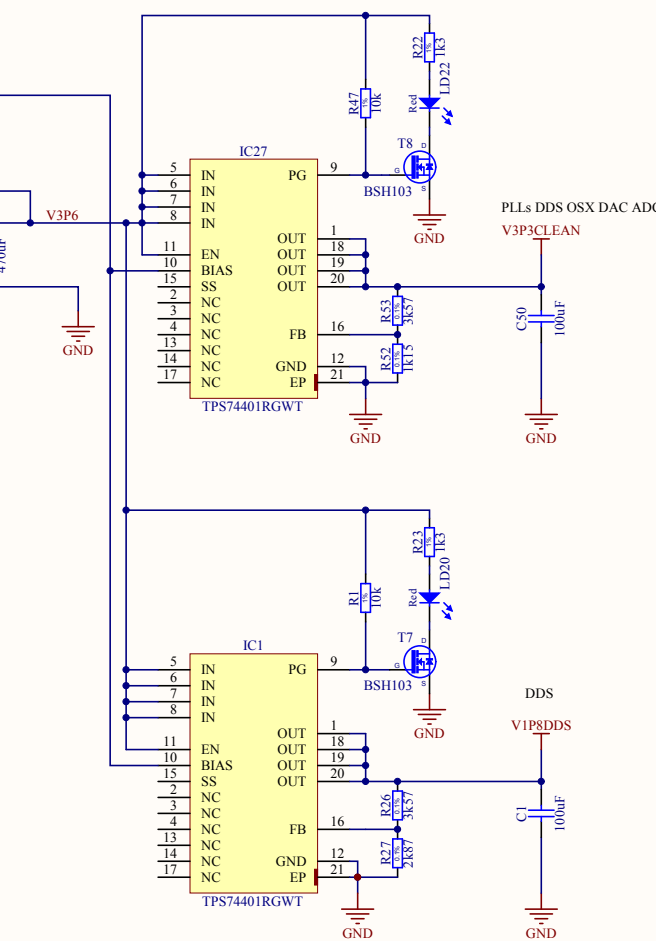
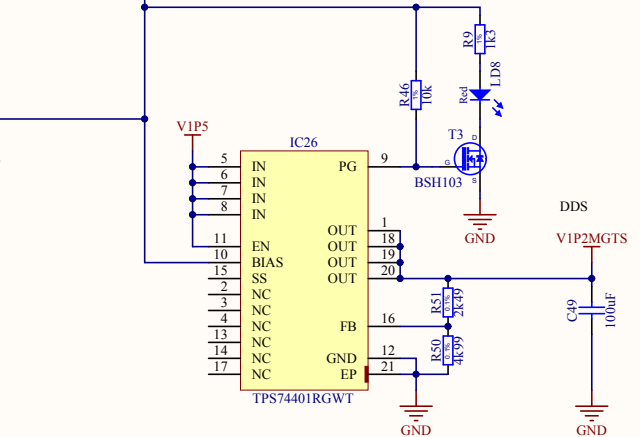
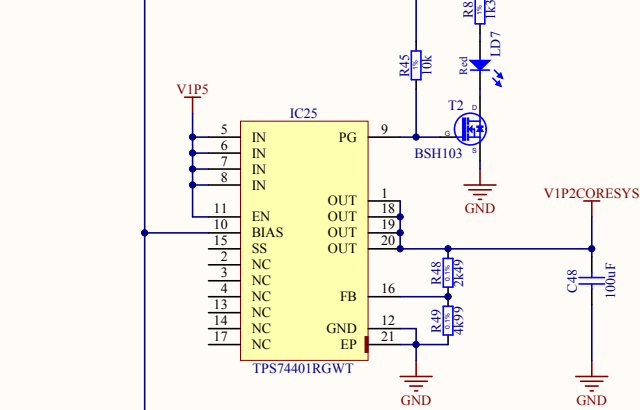
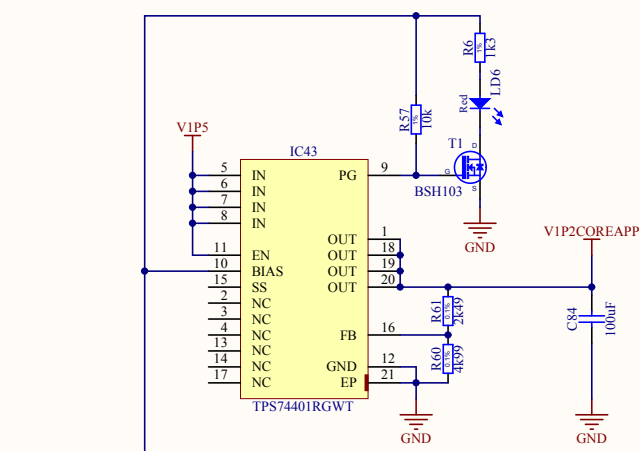
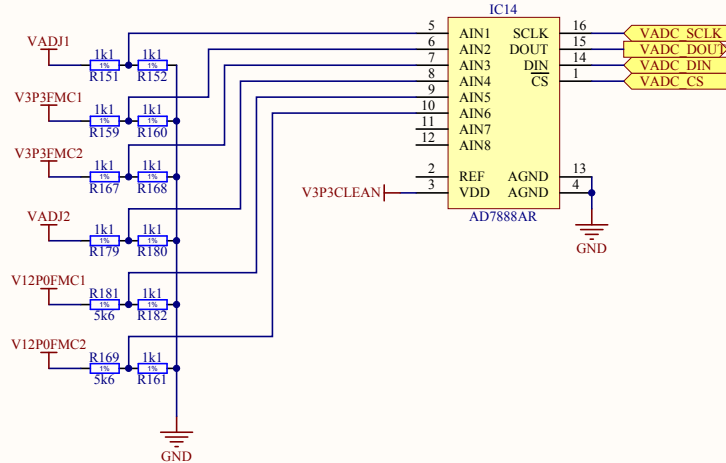
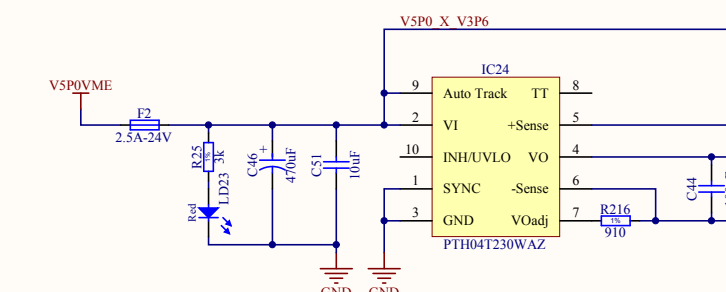
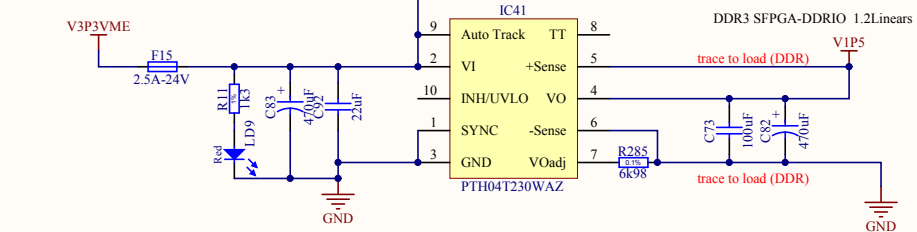
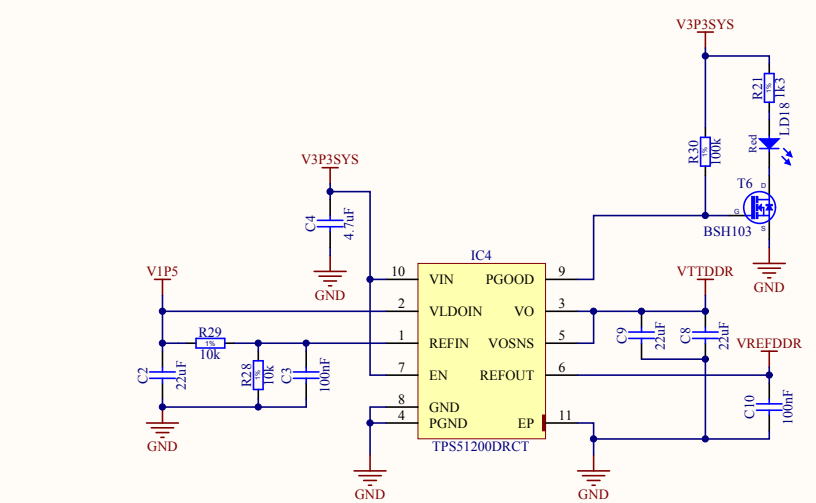
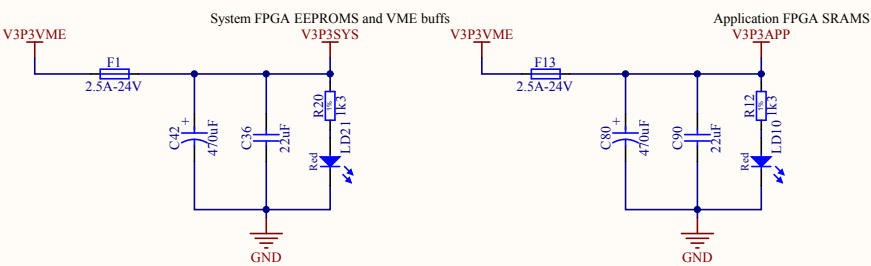
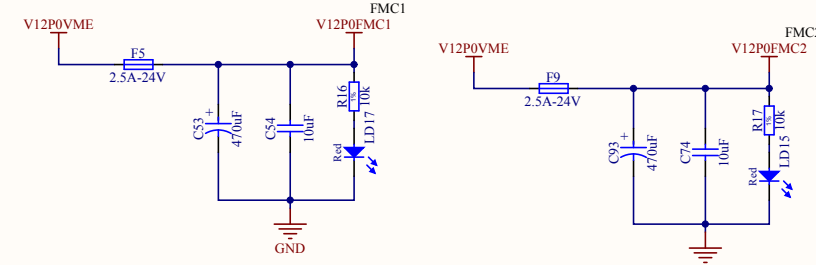
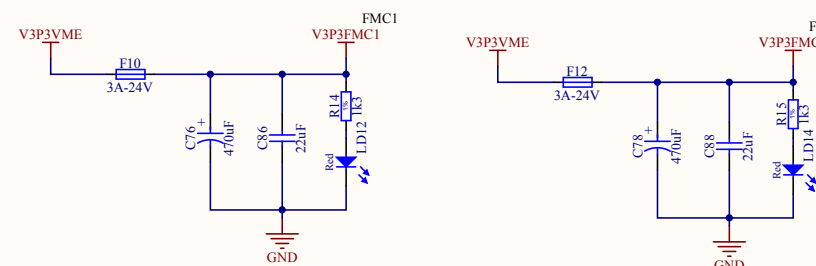
High Pin Count Rows

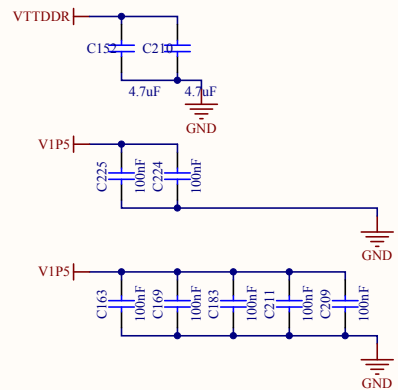
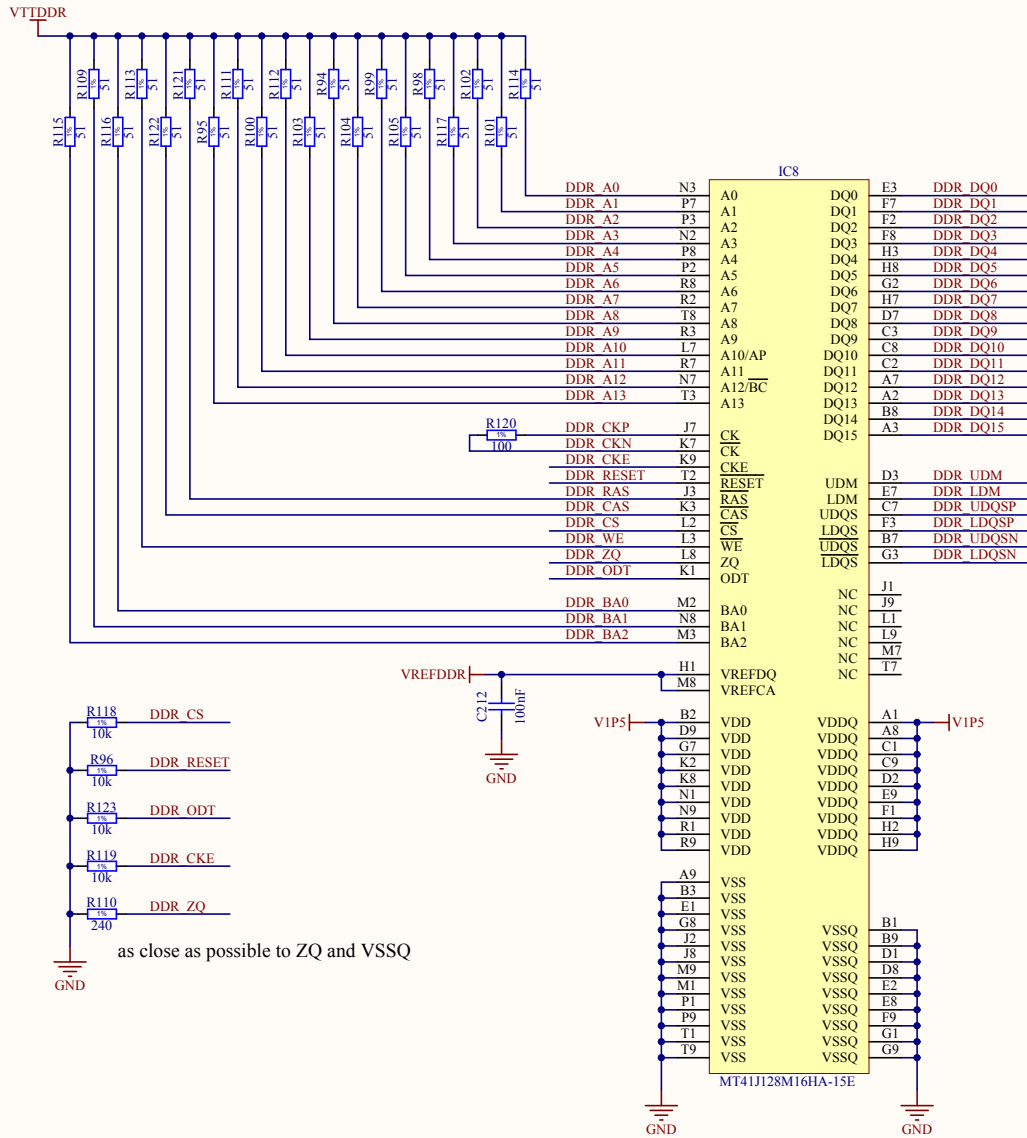
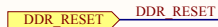
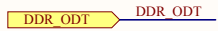
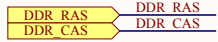
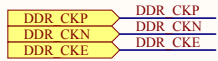




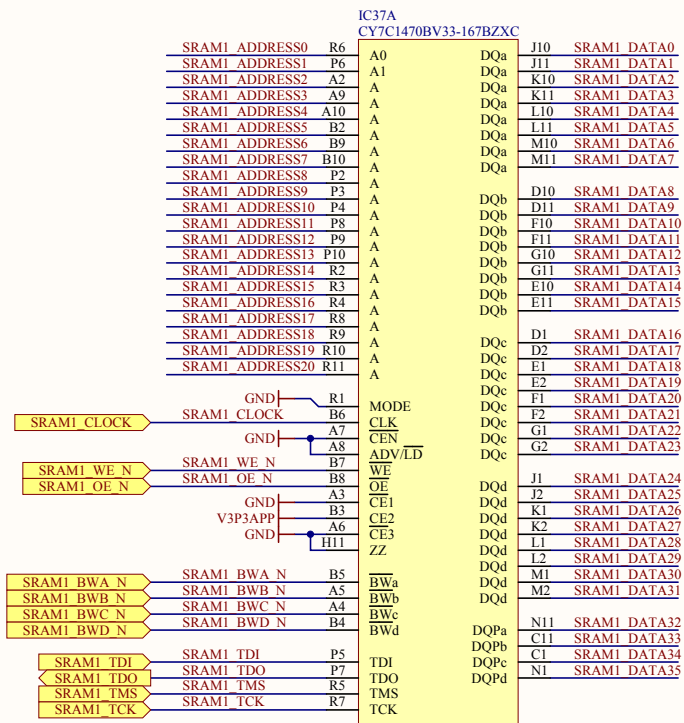
LVDS pairs



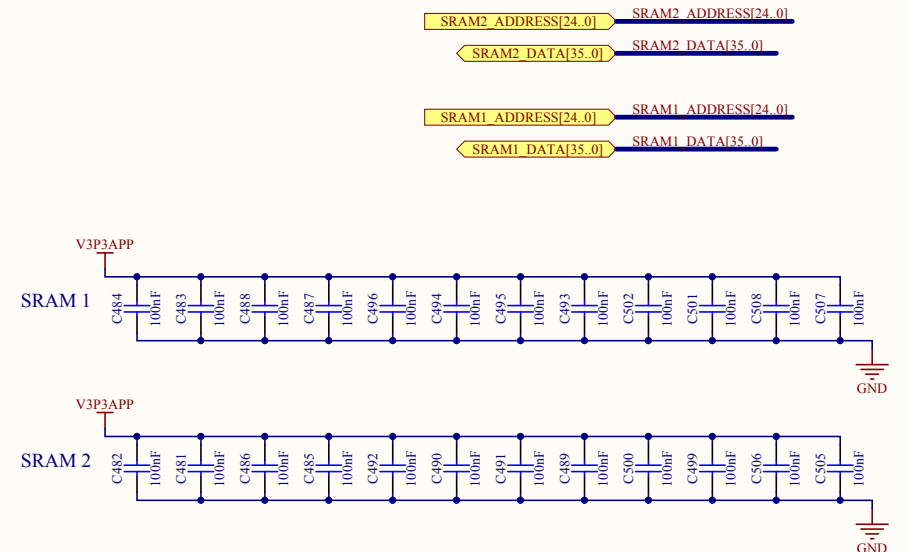
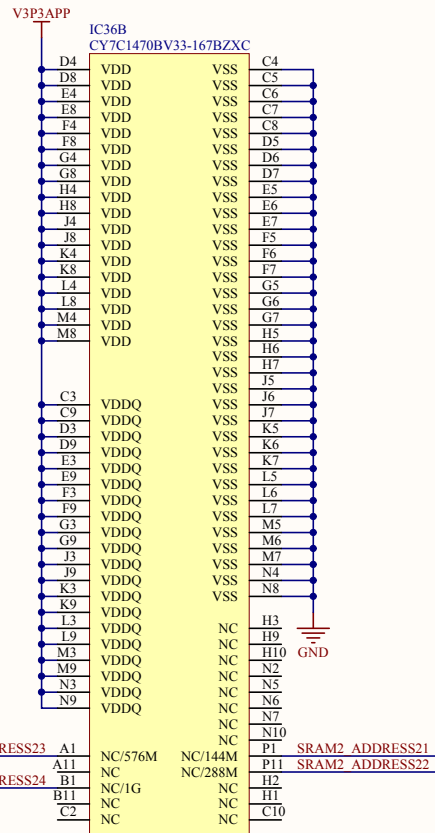
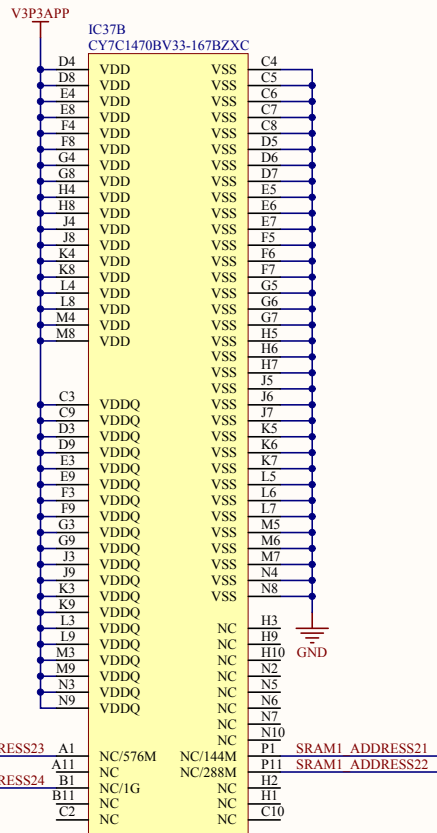
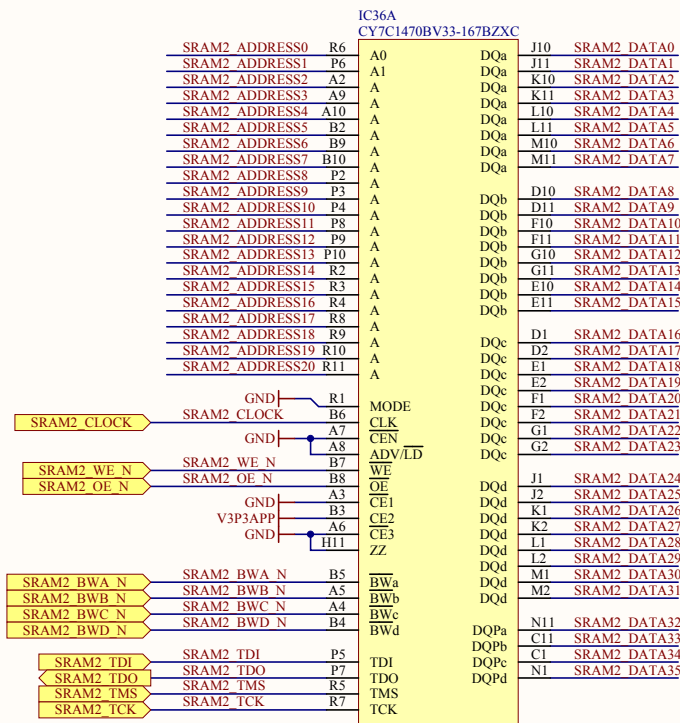


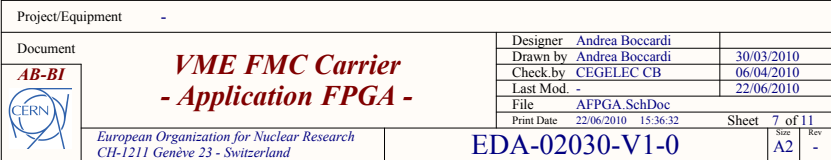


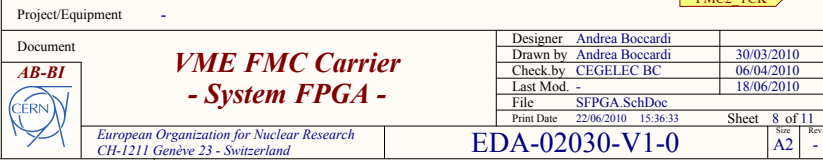
SRAM 1



SRAM 2







A

B

C

D

E

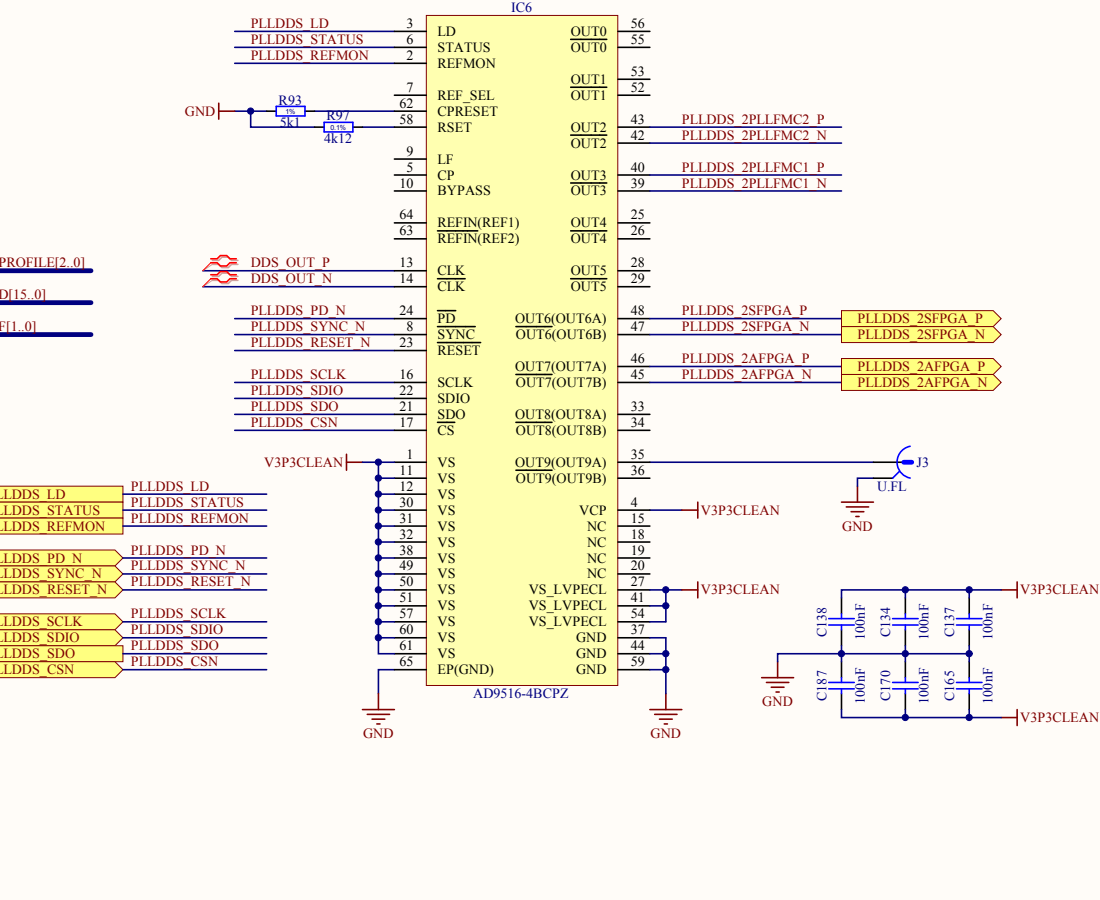
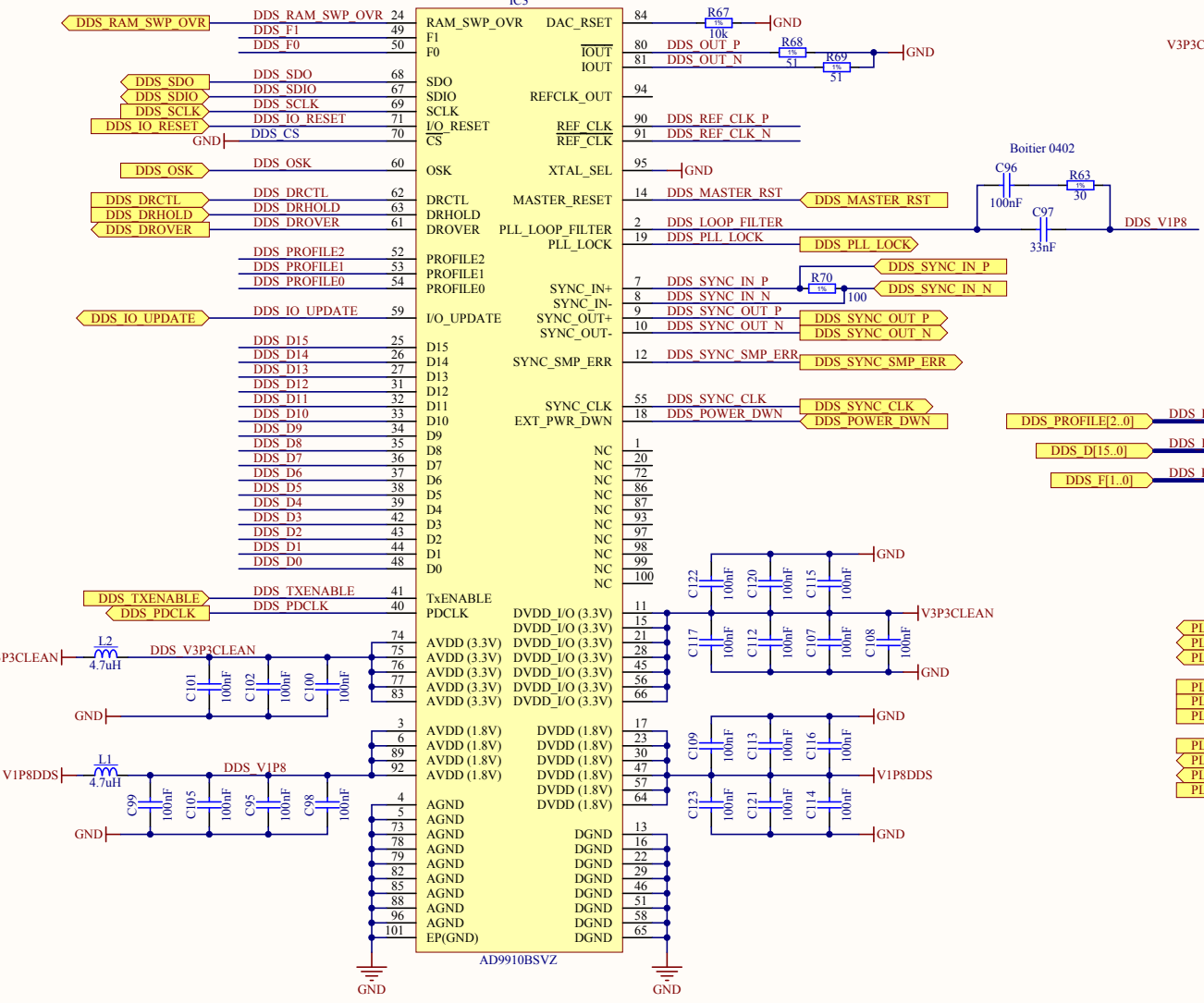
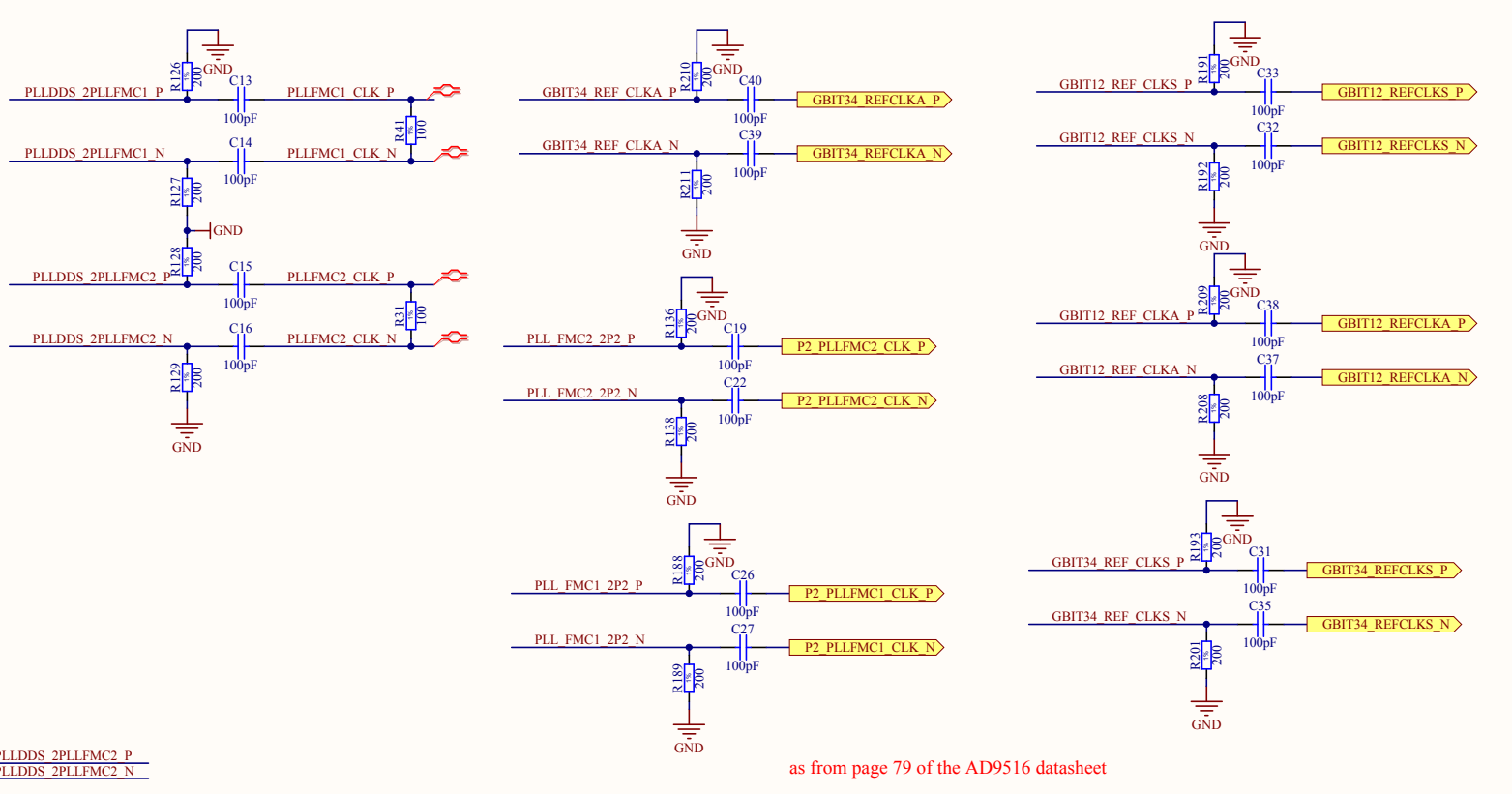
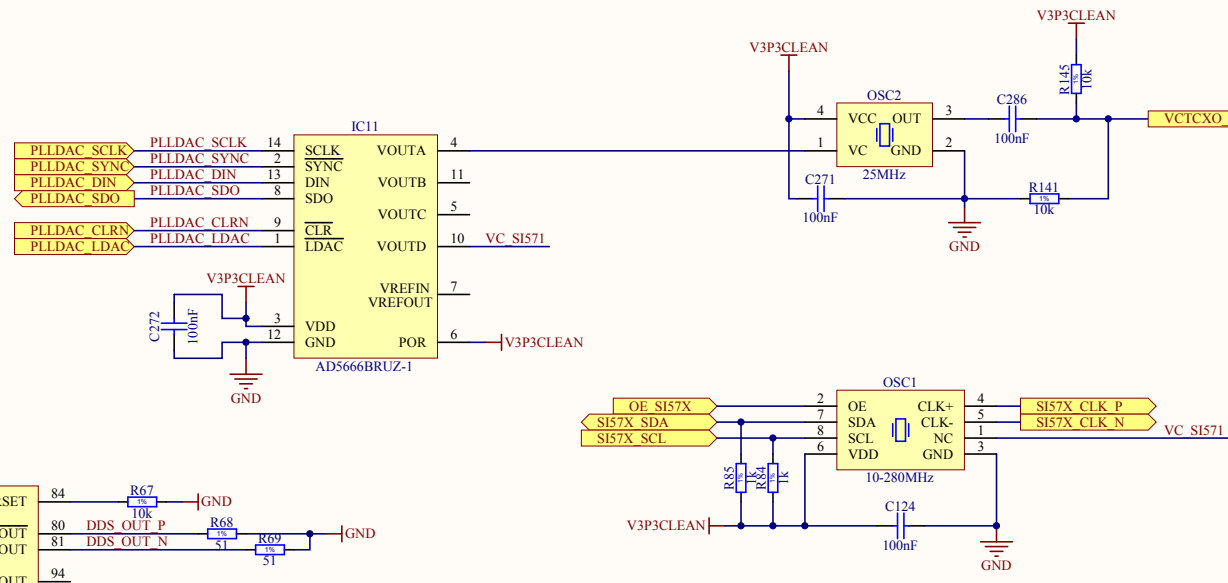
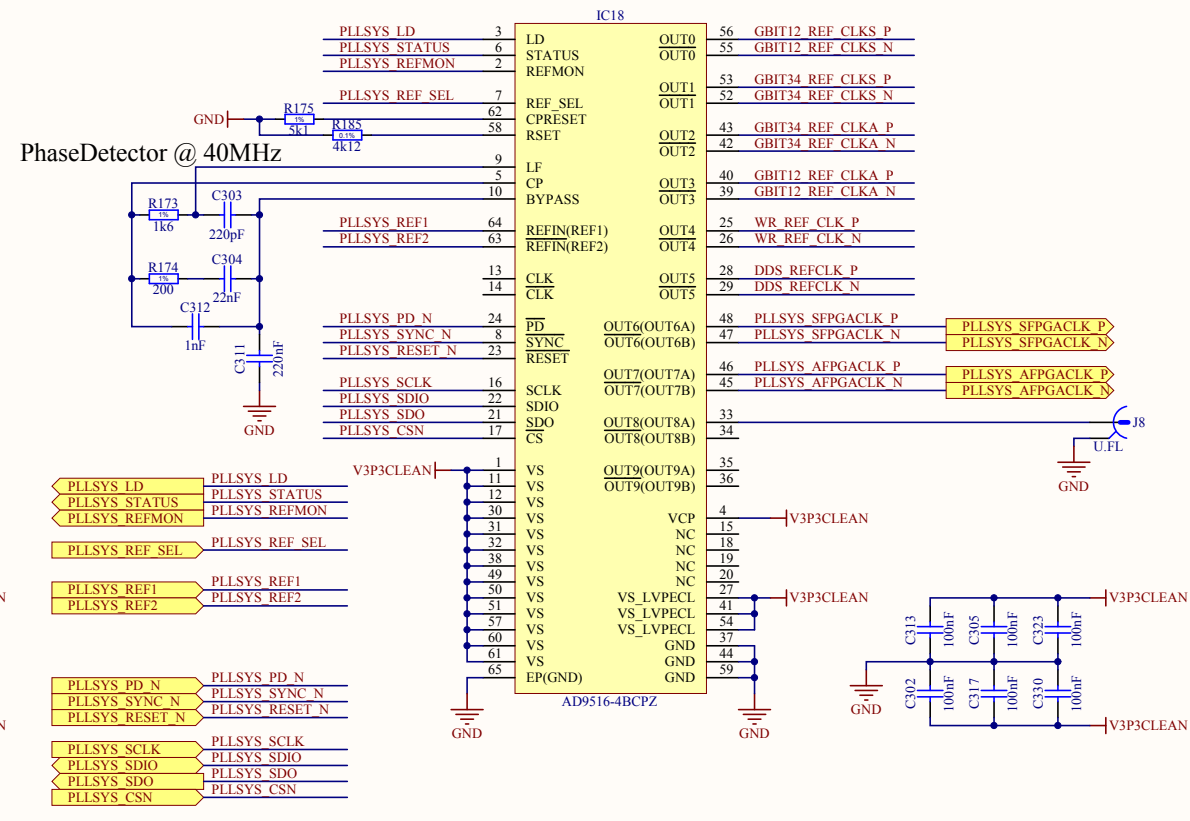
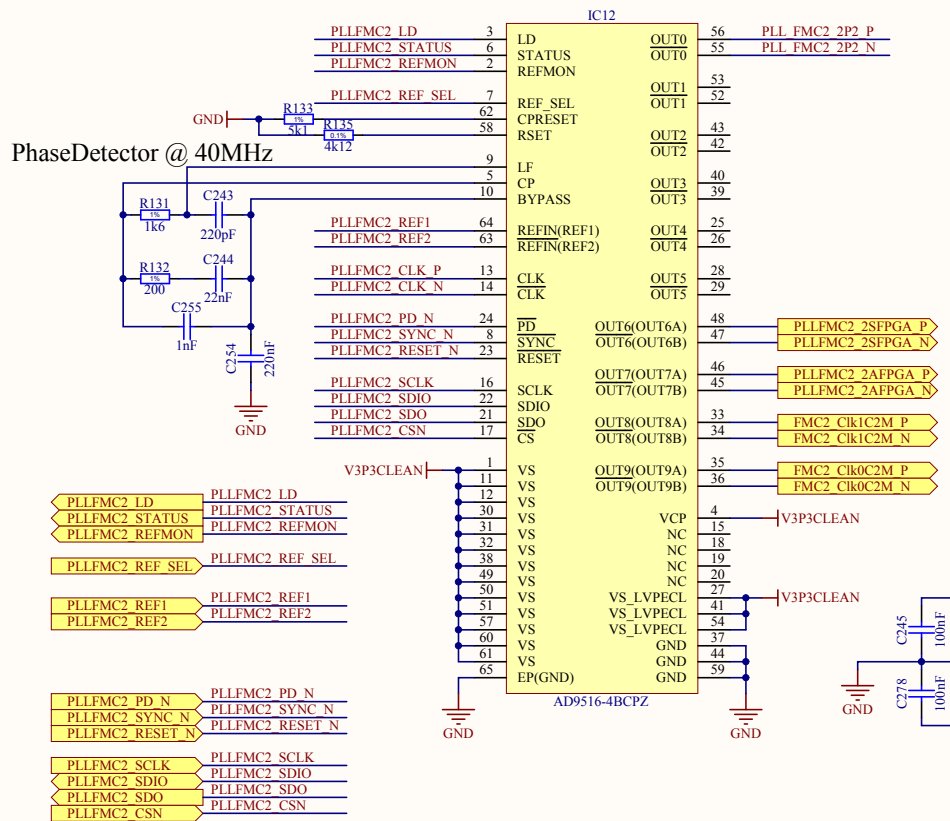
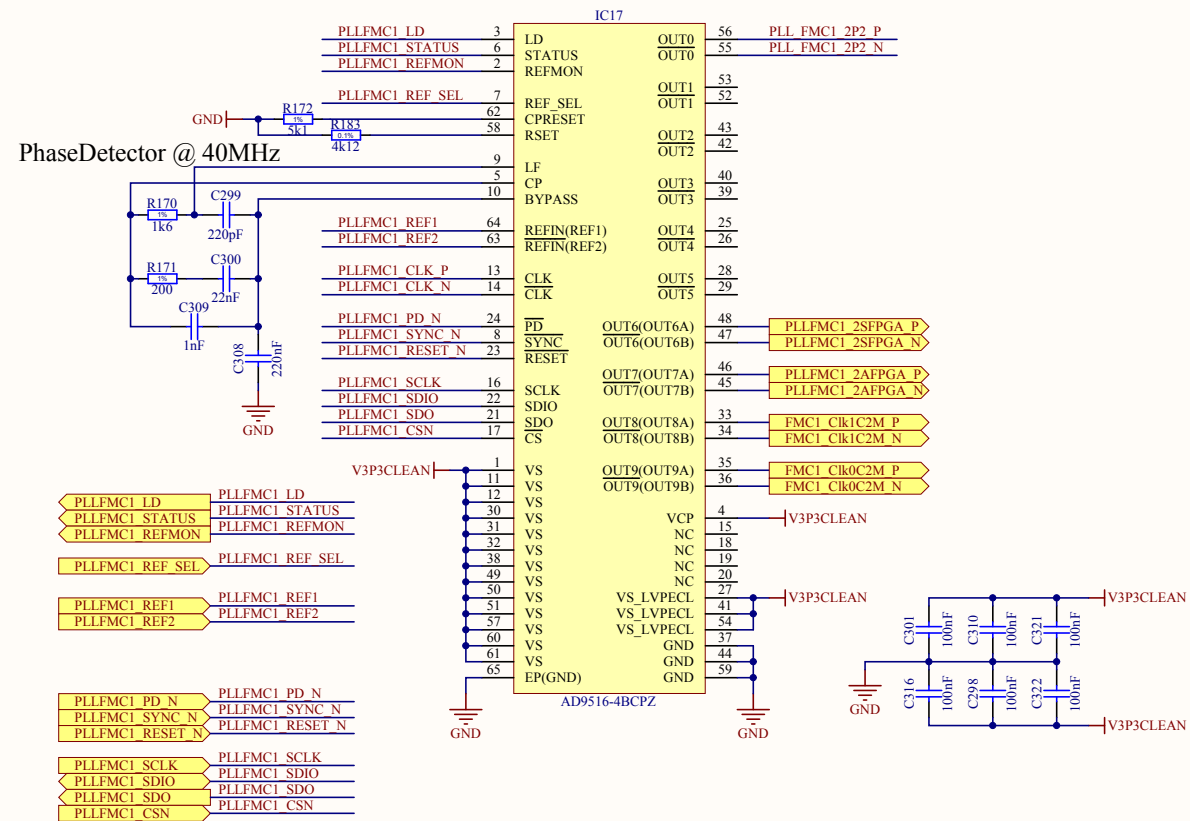
A

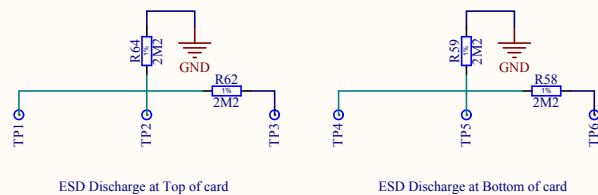
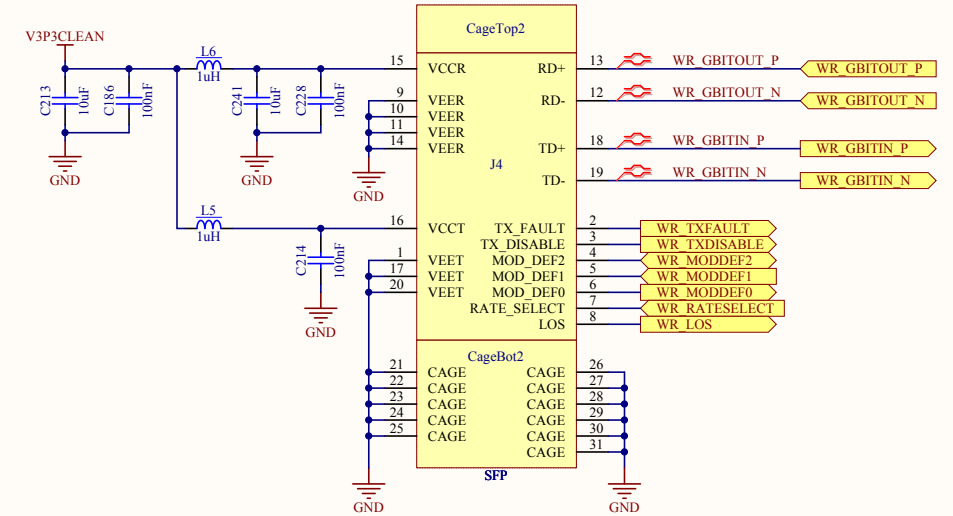
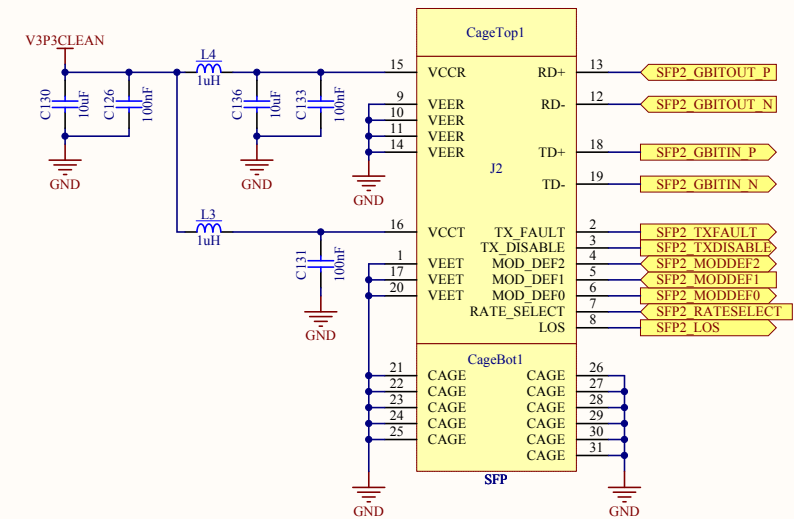
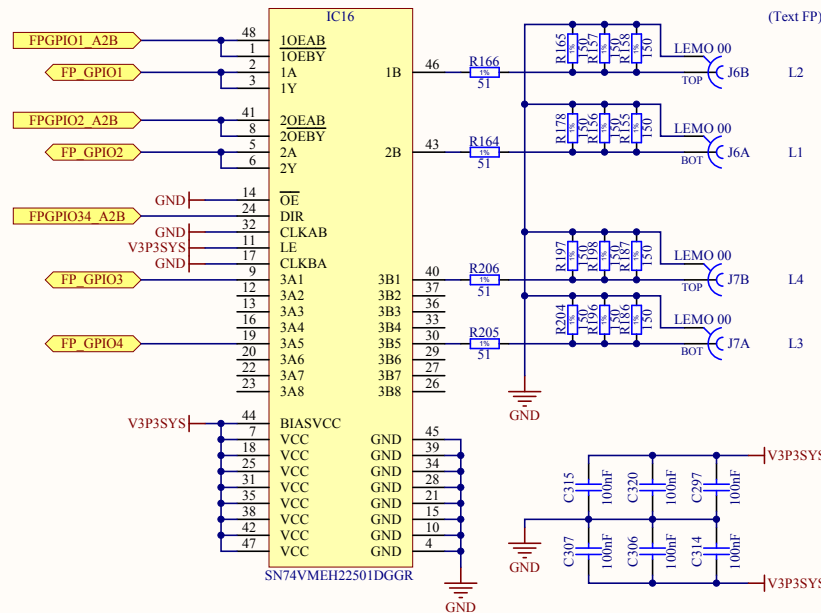
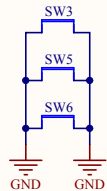
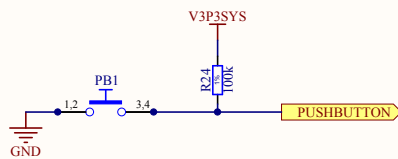
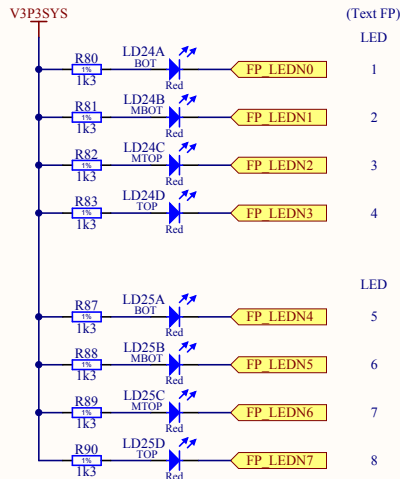
B

C

D

E





Project/Equipment	-	Designer	Andrea Boccardi	30/03/2010
Document	EN-ICE	Drawn by	Andrea Boccardi	06/04/2010
		Check by	CEGELEC BC	22/06/2010
		Last Mod.	-	22/06/2010
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VME FMC Carrier

- Front Panel -

European Organization for Nuclear Research

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