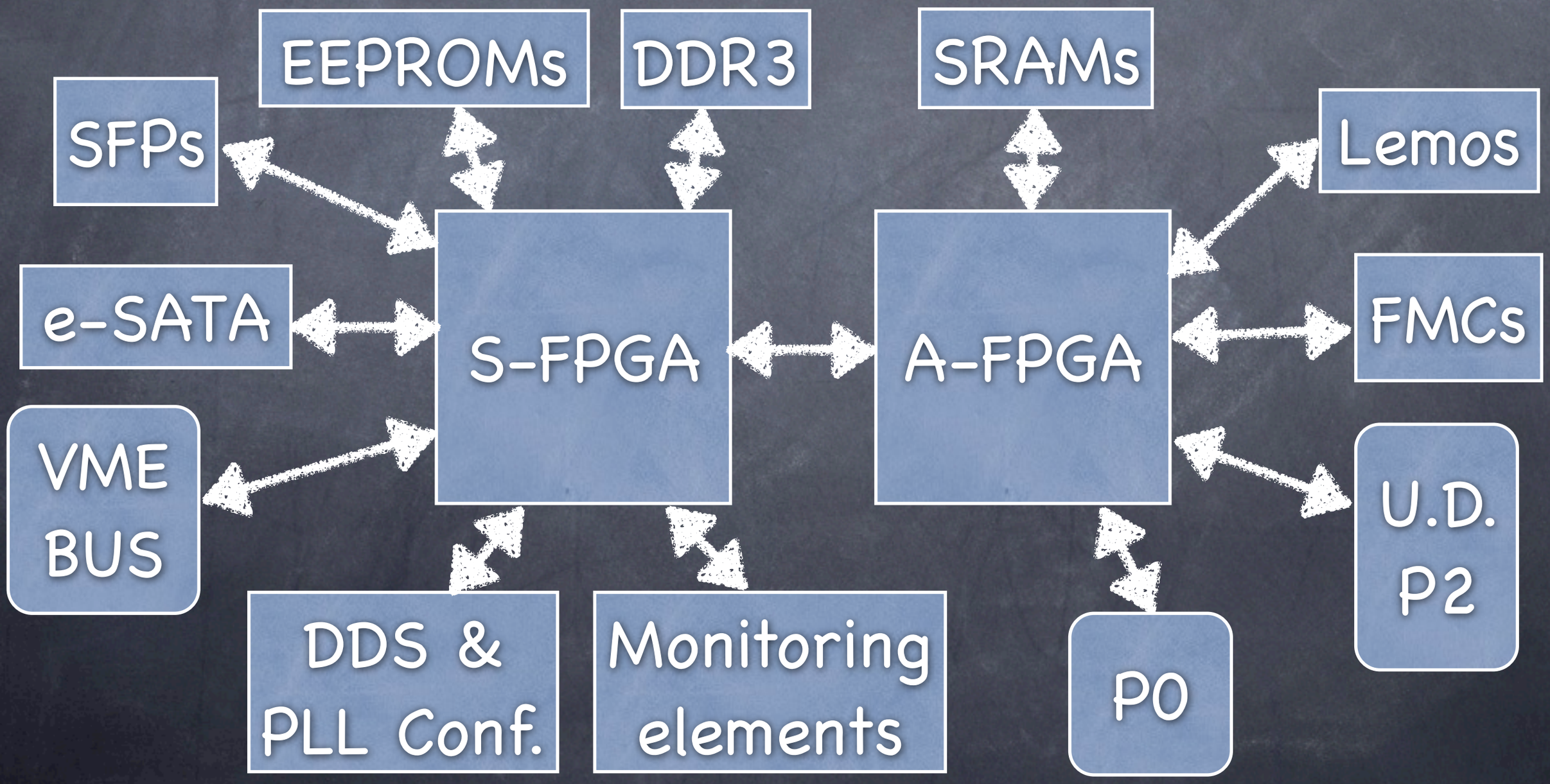
VME FMC Carrier

Technical specifications' review (Schematic review)

Overview

Simplified logic connections' scheme



Overview

- Interfaces
  - VME64x with BI specific P0 and P2
  - 2 SFP (small formfactor pluggable) transceivers
  - 4 fully configurable lemos
  - 1 e-Sata connector

Overview

- Programmable logic
  - 1 System FPGA (S-FPGA)
  - 1 Application FPGA (A-FPGA)
- the 2 FPGAs are XC6LX150T-FGG676
  - 184k FFs (internal logic)
  - 1.3Mb of distributed memory
  - 180 18x18 multipliers with their dedicated adder and accumulator
  - 6 internal PLL (excluding the MGT ones)
  - 8 MGT lanes

EP1S40:
56 18x18 multipliers
12 PLLs
3.4Mb of SRAM
41.2k internal FFs

Overview

- Clocking resources
  - 1 VCTCXO @ 25MHz controlled by a DAC
  - 1 any-rate I2C programmable VCXO
  - 1 DDS (14 bit DAC@1Gs/s)
  - 3 multi output PLLs (1 per FMC plus a system one)

Overview

- Memories
  - 1 DDR3 module (2Gb as 128M X 16b)
  - 2 fully independent ZBT SRAMs (each one from 2M to 32M x 36b)
  - 2 fully independent SPI flash EEPROMs (128Mb each)

Overview

- Mezzanines
  - 2 LPC FMCs with extras on the HPC connector part: 1 multi Gb/s lane, 2 dedicated C2M clocks, connection to the BI defined power supplies
  - P2 transition module with up to 40 single ended data lines (20 LVDS), 2 dedicated clock lines and BI defined power supplies

Overview

- Miscellaneous
  - Board temperature and 64bit identification 1-wire chip
  - FMC mezzanine power supply's voltage monitoring
  - Board PCB revision
  - Non GA VME address setting via switches

FMC connections

- PrsntM2C_n, as well as the JTAG and I2C buses are connected to the S-FPGA
  - The S-FPGA can verify which mezzanines are connected and set the appropriate Vadj value before loading the A-FPGA FW
- PGC2M driven by the S-FPGA on 3.3V
  - 3.3V, 12V and Vadj are monitored by the S-FPGA using a dedicated ADC
- GA[1:0] connected as 00 for the 1st mezzanine, 01 for the 2nd mezzanine using a PU to 3.3V

FMC connections

- La[33:0] are connected to differential pairs on the A-FPGA
- La0 and La1 can be routed as global clock lines in the FPGA
- La33 and La32 could not be connected for the 2nd mezzanine because of constraints on the FPGA side

FMC connections

- Clk0M2C, Clk1M2C (was Clk0C2M) are connected to global clock inputs on the A-FPGA
- GBTClk0M2C, Dp0M2C, Dp0C2M are connected to a MGT lane of the A-FPGA
- GBTClk1M2C, Dp1M2C, Dp1C2M (located on the HPC part of the connector) are connected to a MGT lane of the A-FPGA

FMC connections

- On the HPC section of the connector 2 dedicated C2M clock lines have been connected: Clk0C2M (was Clk1M2C in the FMC specs) and Clk1C2M
  - Those lines are connected to the output of a dedicated PLL (one per mezzanine)
    - The PLL is configured via the S-FPGA that also select the mode of operation and the reference source
    - The reference for the PLL can come from the S-FPGA assuring a constant delay from Application to application synthesis
    - The reference for the PLL can come from the A-FPGA allowing more flexibility and the possibility to use special reference sources without the need to reconfigure the S-FPGA
    - The PLL can also be used as clock distribution element for the on board DDS and in this case the DDS output doesn't pass through any FPGA

FMC connections

- V3.3 and V3.3Aux are connected as a single power supply and come from the VME 3.3V
- The V12 comes from the VME 12V
- each mezzanine has its own distribution for 3.3V and 12V with a dedicated fuse and decoupling capacitors
- Vadj is generated by a switching DC-DC (<16mV ripple) adjusted from the S-FPGA with a digital potentiometer (1024 steps)
  - considering the tolerances Vadj min ranges from 1.15V to 1.35, while the max is always slightly higher than 3.3V
- VrefAM2C is not connected for the 2nd mezzanine because of constrains on the FPGA IOs
- The BI specific power supply are common to the 2 mezzanines
  - if not connected to the PS those lines remain as straight connection to the P2

SRAMs

- 2 NoBL (= ZBT) SRAMs are connected to the A-FPGA in a completely independent way
- The selected component is CY7C1470BV33 is a 2M x 36bit SRAM, but the connection have been made to accomodate the requirements for bigger memories of the same family (up to 32M deep)
- The write cycles can be also performed at byte level
- The maximum working frequency for those memories is 250MHz (interface up to 9Gb/s)
- The JTAG bus of the SRAMs is controlled by the S-FPGA

DDR3

- A 2Gb DDR3 is connected to a dedicated DDR memory control interface of the S-FPGA (up to 800Mb/s with a peak bandwidth of 12.8Gb/s)
- The selected component is the MT41J128M16 (16bit wide interface)
- Possible use of this memory includes:
  - Memory for an embedded processor in the S-FPGA
  - PM data storage
  - Data buffer (FIFO like?) for the processed data before transmission in order to keep the SRAMs available for processing

EEPROMs

- 2 Serial (SPI) flash memories are connected to the S-FPGA
- The selected component is the M25P128: 128Mbit with SPI bus interface up to 50MHz
- One of those is connected to the programming interface of the S-FPGA and can be used for multi-boot programming even using part of the memory for the storage of an embedded processor program and the related OS
- The 2nd flash is available to store a few A-FPGA configurations and permanent critical settings

Front panel connections

- 2 SFPs (small formfactor puggable) are connected to the MGTs of the S-FPGA
  - the reference clock for those can be selected from any global clock of the S-FPGA or come from the System PLL (reference provided from the S-FPGA)
- 4 GPIO lemo are connected to the A-FPGA via direction programmable buffers
- 8 leds on the front panel are connected to the S-FPGA
  - only 4 will be connected in case of lack of space
- 1 e-SATA connector is connected to the S-FPGA
  - the reference for this channel must come from one of the S-FPGA global clocks
  - the e-SATA will be connected to the front panel only if there will be sufficient space left

Misc

- A temperature sensor with 1-Wire interface is connected to the S-FPGA
- A unique ID (64bit) is also stored in the temperature sensor and available trough the same interface
- The 7bit PCB version is available to the S-FPGA
  - this could also be used to code special components' configurations
- 8 switches (single package) are connected to the S-FPGA
  - 6 are supposed to be used to bypass the VME geographical addressing
  - 2 have no use yet
- A push button is connected to both the FPGAs (A and S)
  - The push button can be used as manual reset during the development phase
  - The push button can be connected to the program_b input line of the S-FPGA via a resistor allowing a forced refresh of the FW triggered by the S-FPGA or by the A-FPGA

VCTCXO

- A voltage controlled temperature compensated crystal oscillator centered at 25MHz is connected to the S-FPGA
- The Voltage control input is connected to a 16 bit DAC
- The output of this XO is the default clock source for the S-FPGA
- A phase detector will be implemented in the S-FPGA to lock the crystal to the SFP communication clock (WR)

I2C X0

- A voltage controlled oscillator with center frequency programmable via I2C is connected to the S-FPGA
- The Voltage control input is connected to a 16 bit DAC
- This flexible device could be used to generate a BST locked clock source

PLLs

- 4 PLL chips have been used in the design:
  - 1 for the FMC1
  - 1 for the FMC2
  - 1 system PLL
  - 1 used as low phase noise clock distribution for the DDS output
- The selected component is the AD9516-4 that is capable of delivering clocks with a jitter below 0.5ps using the internal VCO
- All the AD9516 are configured via the S-FPGA

System PLL

- The reference clocks for this PLL are both connected to the S-FPGA that also controls its configuration bus
- The output of this PLL goes to:
  - the S-FPGA
  - the A-FPGA
  - the DDS
  - the dedicated clock references of the MGTs for the SFPs
  - the MGT dedicated clock references for the inter FPGAs communication

FMC PLLs

- The 2 references come from the S-FPGA and the A-FPGA respectively
- The clock input for the clock distribution mode is connected to the DDS PLL
- The outputs are connected to
  - the 2 dedicated C2M clocks of the FMC
  - the A-FPGA
  - the P2

DDS

- The selected DDS is the AD9910: the one used by the RF group for their modules
- The dds has a 14bit DAC @1Gs/s and is capable to deliver clocks up to 400MHz
- The reference clock for the DDS comes from the system PLL
- A dedicated AD9516 (PLL) is used as clock buffer to distribute the DDS output to:
  - The S-FPGA
  - The A-FPGA
  - The FMC1 PLL (if configured in clock distribution mode)
  - The FMC2 PLL (if configured in clock distribution mode)
- The DDS is connected to the clk input and not to the reference input to allow fast phase resynchronization bypassing the PLL

VME bus (P1 and non-U.D. P2)

- The electrical connections allow the implementation of a fully compliant VME64x interface
- Live insertion is not supported
- The VME lines and the buffers are controlled by the S-FPGA
- It is possible to bypass the geographical addressing and set manually the base address via switches

P2 u.d. pins

- 40 of the P2 u.d. pins are straight connected to the A-FPGA and can be configured as single ended lines (3.3V LVCMOS) or as LVDS pairs
- 1 LVPECL output from each of the FMC PLLs is connected to P2 u.d pins
- All the BI specific power supplies and returns are connected to P2 u.d.
  - those lines result straight connected to the FMCs and as such can be used if the BI p.s. are not connected (note that they go in parallel to both the mezzanines)

P0

- The P0 definition is kept as in the BI crates:
  - 3 8bit busses connected to the A-FPGA
  - 2 daisy chains connected to the A-FPGA
  - 2 dedicated single ended clock lines connected to the A-FPGA
  - 2 dedicated LVDS clock lines connected to the S-FPGA
  - floating power supplies: +15V, +5V, +3.3V, -2V, -5.2V, -15V and their independent return
    - they need a 0Ω resistors to be connected

'Standard' Power Supplies

- When possible the power supplies have been used directly the VME power supplies after a fuse and decoupling capacitors
- Most of the components works on the 3.3V that has been split in different lines each with its fuse and decoupling
  - a led is used to indicate the status of each of the PS branches
  - V3P3sys is used to power the S-FPGA IOs and VCCaux, the 2 flash and the VME buffs
  - V3P3app is used by the A-FPGA IOs and VCCaux and the SRAMs
- A clean 3.3V is generated to power the DDS, the PLLs, the ADC and the DAC: a DC-DC generates a 3.6V with 20mV ripple cleaned up with a low drop linear regulator
- The 1.8V for the DDS is obtained from the VME 3.3V using a linear regulator (it takes a small amount of current)
- The 1.5V for the DDR is obtained with a DC-DC converter
- Each of the FPGA cores is powered from a dedicated linear regulator starting from the 1.5V
- The MGTs of the A-FPGA are all powered from a linear regulator starting from the 1.5V

BI power supplies

- The BI power lines to the FMC and P2 can be connected via 0Ω resistors either to the P0 floating power supplies or to
  - ±15V to the VME ±12V
  - +5V to the VME 5V
  - +3.3V to the VME 3.3V
  - -2V to an onboard generated -2V
  - -5.2V to an onboard generated -5.2V
- Each of the return can be connected via a 0Ω to the board ground
- It is possible to leave all the lines floating

A-FPGA

- The A-FPGA receives the data lines from
  - both the FMC mezzanines
  - the P2
  - the P0
- It has the full control of the 2 SRAMs (except for the JTAG port)
- It is connected to the 4 FP lemos
- It is connected to the S-FPGA via
  - 18 GPIO lines (2 are on global clock lines)
  - 4 MGT lanes
- The Push button
  - this can be connected also to the PROGRAM of the S-FPGA
- The VME sys reset

A-FPGA

- Its global clock inputs are connected to
  - the 2 dedicated M2C clock lines of each mezzanine
  - La0 and La1 of each mezzanine
  - 1 output of each FMC PLL
  - 1 output of the system PLL
  - 1 output of the DDS PLL
  - 1 differential pair of the S-FPGA (also a global clock capable IO for the S-FPGA so that can be used in the other direction)
  - the P0 TTL turn clock
  - the P0 TTL buch clock

A-FPGA

- The 8 MGT lanes are connected to
  - 2 MGT lanes of the FMC1
    - ref clk from FMC1
  - 2 MGT lanes of the FMC2
    - ref clk from FMC2
  - 4 MCT lanes of the S-FPGA
    - ref clk from the system PLL
    - 2 should be enough to guarantee sufficient bandwidth to fully cover the VME and/or the ethernet bandwidth even considering possible protocol overheads
    - 2 could be used to give 'direct' access to:
      - the DDR3
      - the 2nd SFP
      - the eSATa
      - DDS

A-FPGA

- Of the 18 GPIOs connected to the S-FPGA
  - 2 are connected to a global clock on both sides
  - 2 are regular GPIOs
  - 14 are programming lines that can become GPIOs once the FW loaded (M[1:0], D[7:0], CCLK, INIT, RDWR and CSI)

A-FPGA

- The A-FPGA can be loaded
  - via JTAG using the platform cable from XILINX (it is in the chain with the S-FPGA)
  - by the S-FPGA
    - the FW to be loaded can be obtained in this case from
      - the VME
      - one of the serial inetrface (SFP or e-SATA)
      - one of the SPI flashs
- the protocol used can be
  - slave serial (the preferred one)
  - SelectMAP
    - if the SelectMAP interface is retained after loading the FW, it can also be used by the S-FPGA to read back the configuration at any moment

S-FPGA

- The S-FPGA has the full control of the VME bus
- It has the control of the DDR3 that is connected to one of its dedicated DDR memory controllers
- It controls all the PLLs and the DDS
- It controls the VCTCXO and I2C XO DAC
- It has the control of the programming port of the I2C XO
- It monitors the FMCs voltages via the ADC and therefore is the master of the PGC2M FMC signal
- It has access to the board temperature and the unique ID chip
- It controls the JTAG and the I2C of the 2 FMCs and is connected to the PRSNT_N mezzanine lines
- It controls the FP leds
- It is directly connected to the SFPs and the e-SATA
- It is connected to the A-FPGA via several GPIOs and MGTs (see A-FPGA)
- It is connected to the push button and the switches for the manual setting of the VME base address