Clocking guidelines for FMC Carriers

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FMC Clock signals

In the FMC standard there are defined four different sorts of clock signals.

1) Gigabit transceiver reference clocks, named as GBTCLKx_M2C. These signals should be connected directly to the transceivers reference clock.
2) *Differential Reference Clocks, named as* CLK[0..1]_M2C_P, CLK[0..1]_M2C_N. These signals are generated by the mezzanine on the low pin count connector and should be attached to a global clock IO. They are LVDS compatible irrespective of VADJ (Rule 5.)
3) *Bidirectional Differential Reference Clocks* CLK[2..3]_BIDIR_P, CLK[2..3]_BIDIR_N on the high pin count connector. These signals can be driven either by the carrier or the mezzanine. The pin CLK_DIR defines the direction. CERN's FMC carriers will always drive these signals.
4) User defined pins (LA_, HA_, HB) marked with a CC. These are recommended to be used as a clock in source synchronous applications.

Spartan6 clocking resources

There is some confusion on how to use CLK[0..1]_M2C and the LAX_CC clock lines. CLK[0..1]_M2C can be placed on any bank as any IO can be used as LVDS input regardless of its VCCO. On the other hand LAX_CC are preferred as synchronous clock source. In the Spartan6 there are two primitives to deserialize data, the IDDR2 and the ISerDes2. For the discussion I will centre on the ISerDes2 primitive.

The ISerDes2 can accept data at up to 950Mb/s and deserialize at a lower rate towards the FPGA user logic. This is performed by means of a simple shift register clocked at the data rate speed. Phase alignment is achieved by an adjustable delay unit and a phase detector.

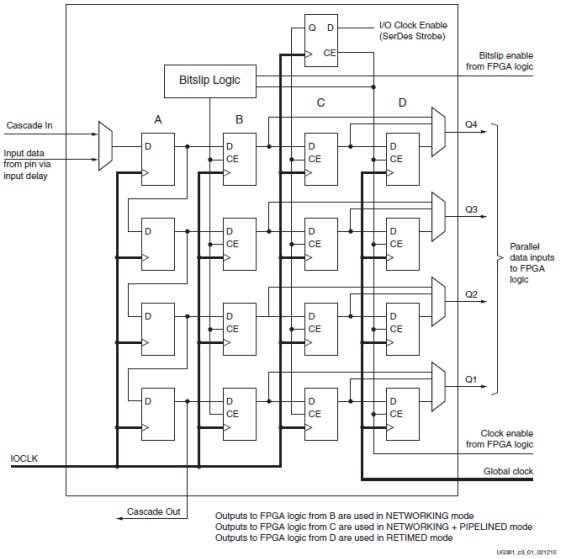

Figure 3-1: **Overview of the ISERDES2 Block**

Figure 1

DDR registers are mimicked by using a clock doubler. When the user provides a clock whose frequency is half of the bit rate the clock doubler is used and the SerDes works in DDR mode. This mode works up to 800Mb/s. When the user provides a clock whose frequency is that of the data rate, the clock is directly attached to the SerDes and the clock rate can be of up to 950Mb/s.

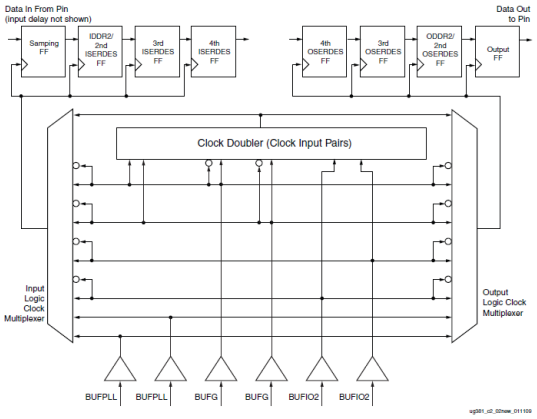

Figure 2-2: **IOI Logic Clocking Resources**

Figure 2

The SerDes2 can receive its reference clock from 3 different types of clock buffers.

1) BUFG. Comes from the FPGA logic. It can work up to 350MHz
2) BUFIO2. Local to half of a bank. It works up to 500MHz
3) BUFPLL. Local to a whole bank and comes from an internal PLL. It works up to 950MHz.

As it is illustrated in Figure 3, for a BUFIO2 to work properly its source must come from the same bank where the data lines are connected. Ideally it should be connected to the same half bank to minimize the skew. On the other hand the BUFPLL is designed to drive a whole edge.

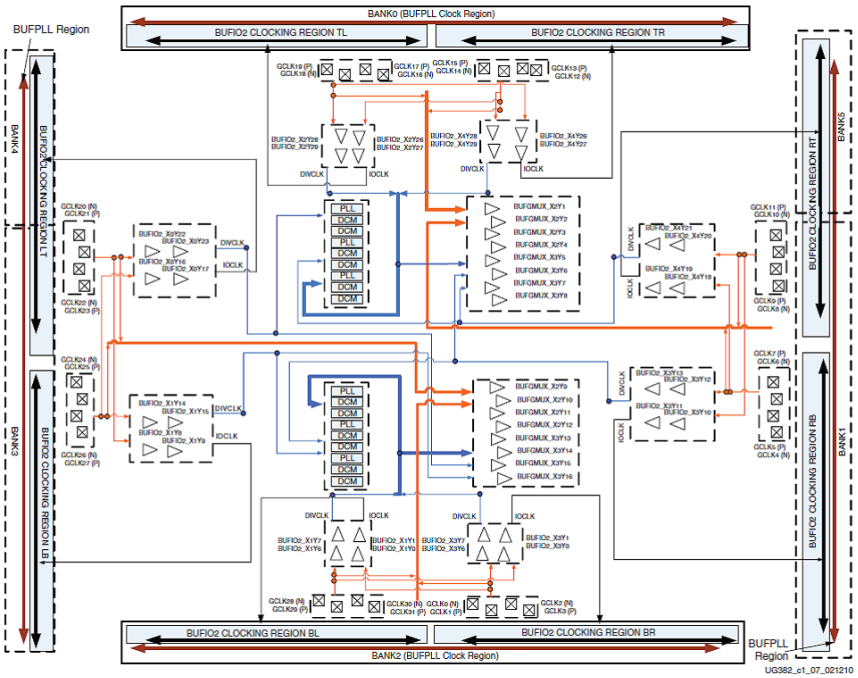

Figure 1-8: **Spartan-6 FPGA Clock Pin Layout—Devices with Additional Bank 4 and Bank 5**

Figure 3

In applications where the input clock is run at the frequency of the parallel data and not the serial data, such as the pixel clock for video applications, the input clock must be multiplied up to create a high-speed I/O clock. Figure 1-13 shows a PLL providing the high-speed I/O clock required for the ISERDES.

GCLK clock inputs are automatically routed to the PLL and DCM clock inputs using a BUFIO2. This BUFIO2 routing path allows the input path to be deskewed using the BUFIO2FB (if needed).

The PLL drives the I/O clock network with the CLKOUT0 output. BUFIO2FB is balanced to deskew the input routing delays associated with the primary BUFIO2. The FPGA clock domain is driven by a separate PLL clock output using a BUFG.

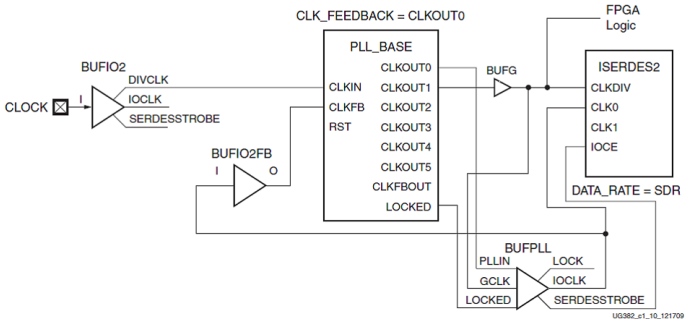

Figure 1-13: **Example 3: Basic PLL ISERDES2 (SDR)**

Figure 4

In DDR applications where serialized data is clocked in on both the rising and falling edges of the input clock, a second inverted clock is required to drive CLK1 as shown Figure 1-12. Because data is clocked in on both edges of the IOCLK, DIVCLK is divided by a DIVIDE/2 by setting USE_DOUBLER = TRUE.

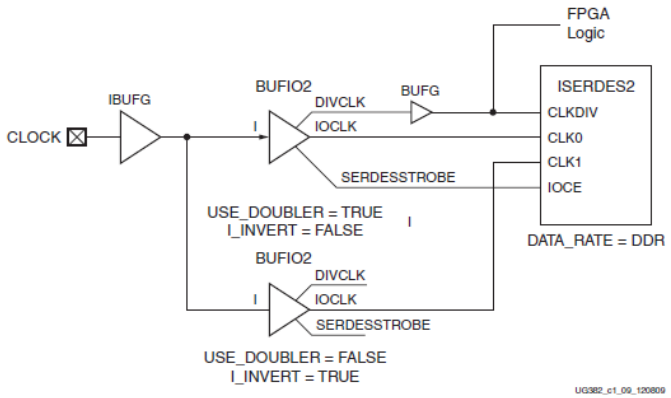

Figure 1-12: **Example 2: BUFIO2 Driving ISERDES2, DATA_RATE = DDR**

Figure 5

Board Layouts

Optimal FMC connexions for Spartan6 XC6SLX150T-2FGG676C:

1) LA00_CC connected to GCLK15,GCLK14 on Bank 0
2) LA01_CC connected to GCLK13,GCLK12 on Bank 0
3) LA17_CC connected to GCLK19,GCLK18 on Bank 0
4) LA18_CC connected to GCLK17,GCLK16 on Bank 0
5) LA00_CC to LA_16 connected to TR bank on Bank 0
6) LA17_CC to LA_33 connected to TL bank on Bank 0
7) CLK0_M2C and CLK1_M2C connected to a global clock on a different bank
8) CLK[2..3]_BIDIR depends on the application

Complex PCIe FMC Carrier (PFC)

There is only Bank 0 connected to the FMC.

1) CLK0_M2C connected to GCLK19,GCLK18
2) CLK0_M2C connected to GCLK13,GCLK12
3) LA00_CC connected to GCLK15,GCLK14
4) LA01_CC connected to GCLK17,GCLK16
5) LA17_CC and LA18_CC are not connected to a global clock
6) LA00_CC to LA_16 connected to TR bank (except LA_01)
7) LA18_CC to LA_33 connected to TL bank
8) LA17_CC connected to TR bank
9) CLK[2..3]_BIDIR driven by AD9516.

VME FMC Carrier (VFC)

1) FMC1 is connected to Bank 0 and FMC2 is connected to Bank 2. In both CLK[0..1]_M2C are connected to global clocks of Bank 0 and 2. LAX_CC are not connected to global clocks. CLK[2..3]_BIDIR driven by AD9516.

Simple PCIe FMC carrier (SPEC)

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Conclusions

1) CLK[0..1]_M2C can be routed to IO banks not powered by VADJ.
2) LA00_CC, LA01_CC, LA16_CC and LA17_CC should be connected to dedicated clocking IOs.
3) A synchronous source decoding clock up to 950MHz could also be generated from internal logic by using a PLL. Therefore the use of the use of CLK[0..1]_M2C as synchronous source clocks should not be problematic.
4) The PFC and SPEC boards could reach the optimal FMC pin layout without major modifications
5) The VFC should at least connect LA00_CC and LA17_CC to a global clock IO

Extracts from the Vita 57 standard:

Recommendation 5.1: Signals with a „_CC" postfix should be used as the preferred signals for clocks in source synchronous applications and should be connected to pins on the FPGA, which are identified for this purpose.

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5.2. Differential Reference Clocks
There are four reference clocks, which have a bus between the carrier card and the IO mezzanine module. The clocks can have two configuration;
1. When „CLK_DIR" is connected to „GND" or unconnected on the mezzanine module, then **CLK[0..1]_M2C_P, CLK[0..1]_M2C_N, CLK[2..3]_BIDIR_P, CLK[2..3]_BIDIR_N** are four differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card.
2. When „CLK_DIR" is connected to „3P3V" via a 10KΩ pull up resistor on the mezzanine module, then **CLK[0..1]_M2C_P, CLK[0..1]_M2C_N** are two differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card, and, **CLK[2..3]_BIDIR_P, CLK[2..3]_BIDIR_N** two differential pairs that are assigned for clock signals, which are driven from the carrier card to the IO Mezzanine Module
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Rule 5.4 all CLK[0..3] shall use the LVDS standard

References

Spartan6 Clocking resources

http://www.xilinx.com/support/documentation/user_guides/ug382.pdf

Spartan6 SelectIO resources

http://www.xilinx.com/support/documentation/user_guides/ug381.pdf

Spartan6 DC and Switching characteristics

http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf