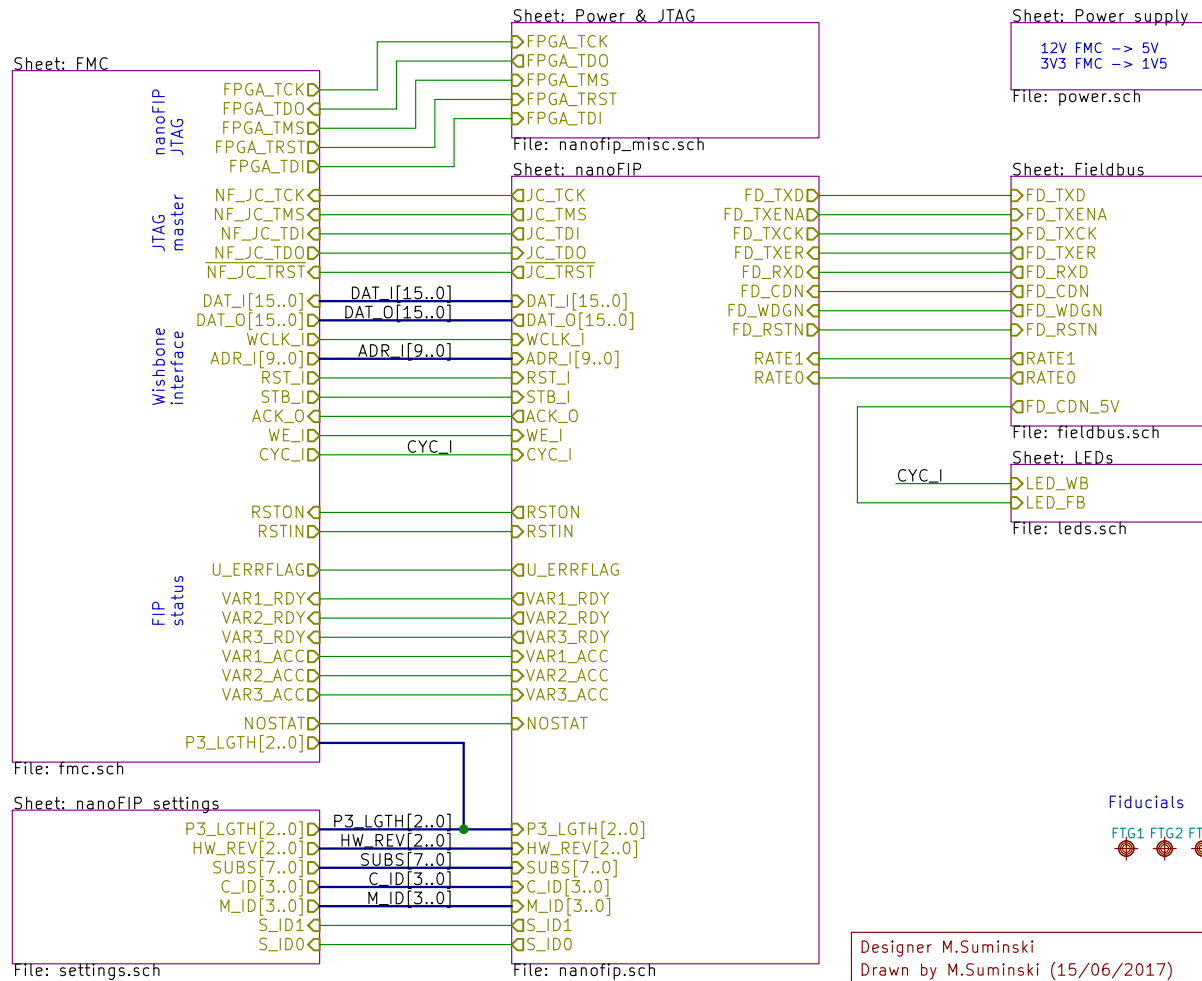


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<http://www.ohwr.org/projects/fmc-nanofip>



Fiducials

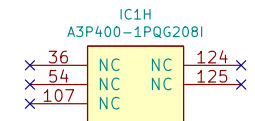
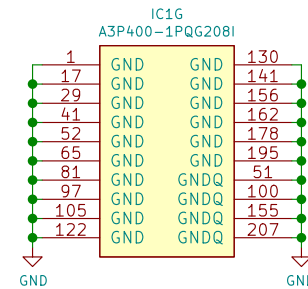
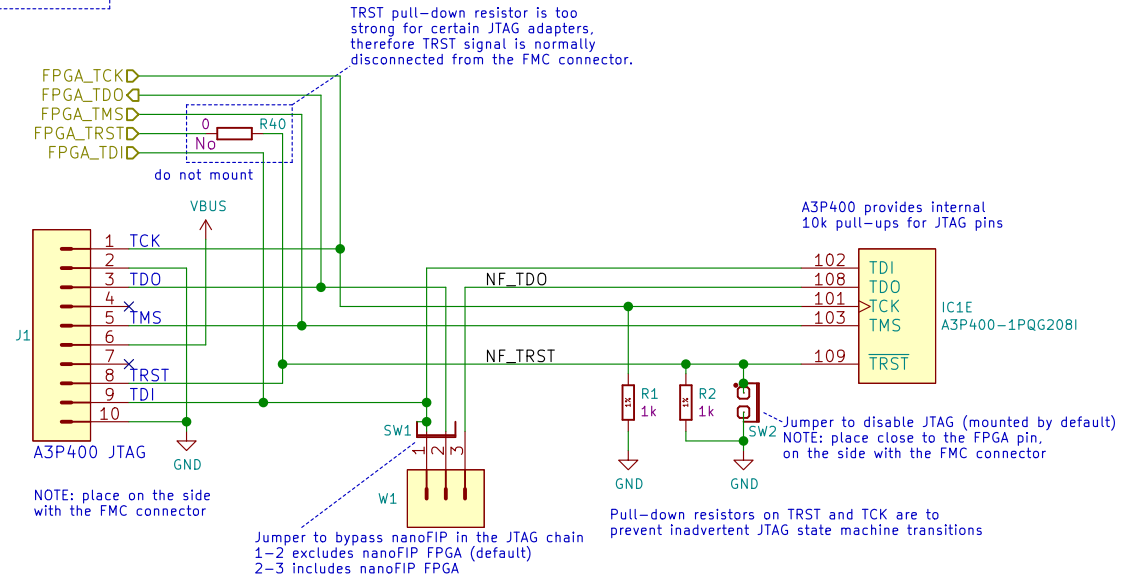
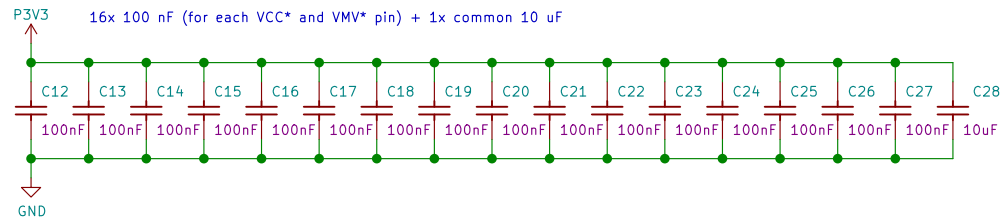
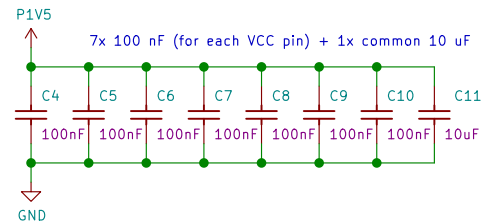
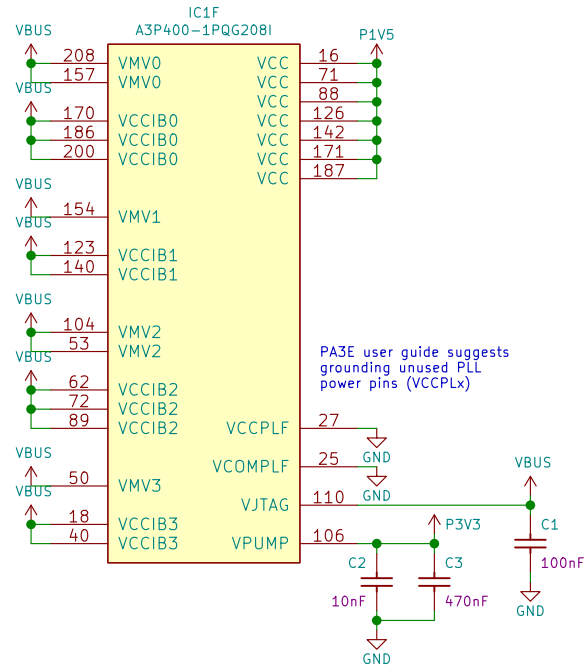
FTG1 FTG2 FTG3 FTG4 FTG5 FTG6

Screw holes for mounting
the mezzanine to the carrier

B1 B2 B3 B4
GND GND GND GND

Designer M.Suminski
Drawn by M.Suminski (15/06/2017)
Check by M. Ricci (27/09/2017)
Last Mod. C. Gentsos (02/07/2021)
CERN, European Organization for Nuclear Research, CH–1211 Genève 23 – Switzerland
Sheet: /
File: EDA–03613–V3–1.sch
Title: EDA–03613–V3–1 FMC–nanoFIP (Bus Speed 31.25k)
Size: A4 Date: 2018–04–27 Rev: 1
KiCad E.D.A. kicad 5.1.9 Id: 1/8

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Drawn by M.Suminski (15/06/2017)
Check by M. Ricci (27/09/2017)
Last Mod. M.Suminski (27/04/2018)

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Sheet: /Power & JTAG/
File: nanofip_misc.sch

Title: EDA-03613-V3-1 FMC-nanoFIP Power & JTAG

Size: A4 Date: 2018-04-27

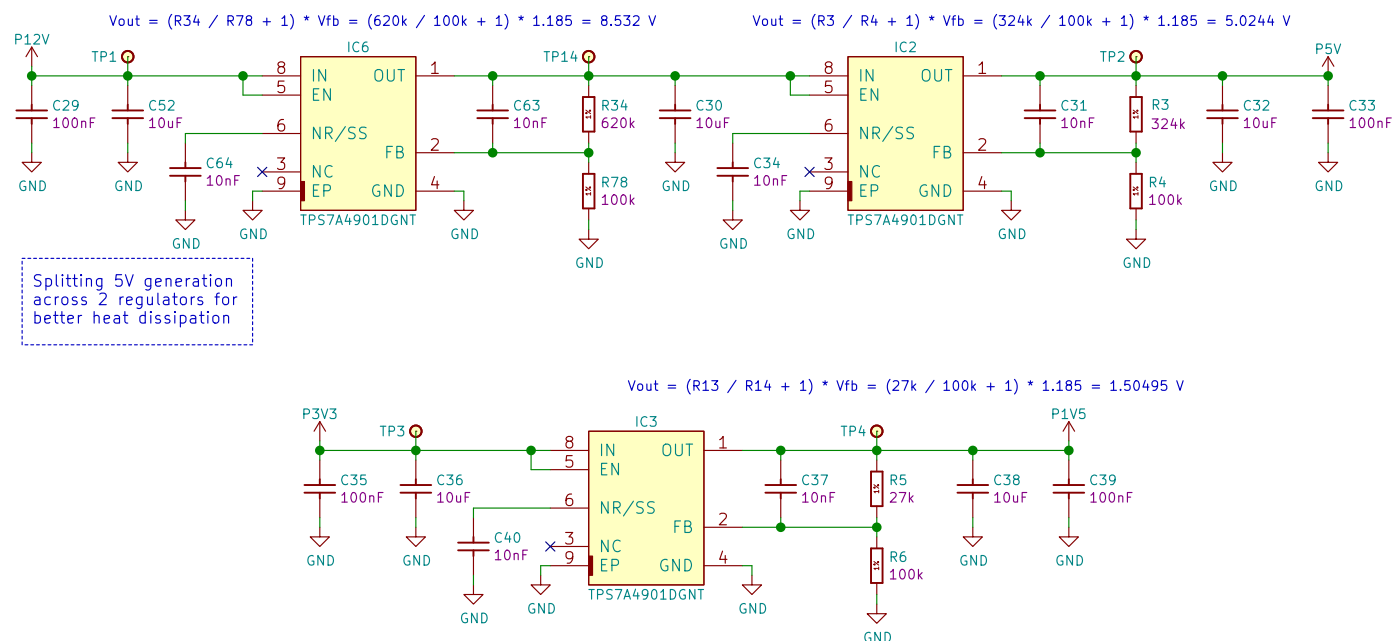
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Rev: 8

Id: 2/8

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NOTE: place testpoints on the side without the FMC connector







Splitting 5V generation
 across 2 regulators for
 better heat dissipation

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Drawn by M.Suminski (15/06/2017)	
Check.by M. Ricci (27/09/2017)	
Last Mod. C. Gentsos (02/07/2021)	
CERN	
Sheet: /Power supply/	
File: power.sch	
Title: EDA-03613-V3-1 FMC-nanoFIP Power Supply	
Size: A4	Date: 2018-04-27
KiCad E.D.A. kicad 5.1.9	Rev: 8
	Id: 3/8

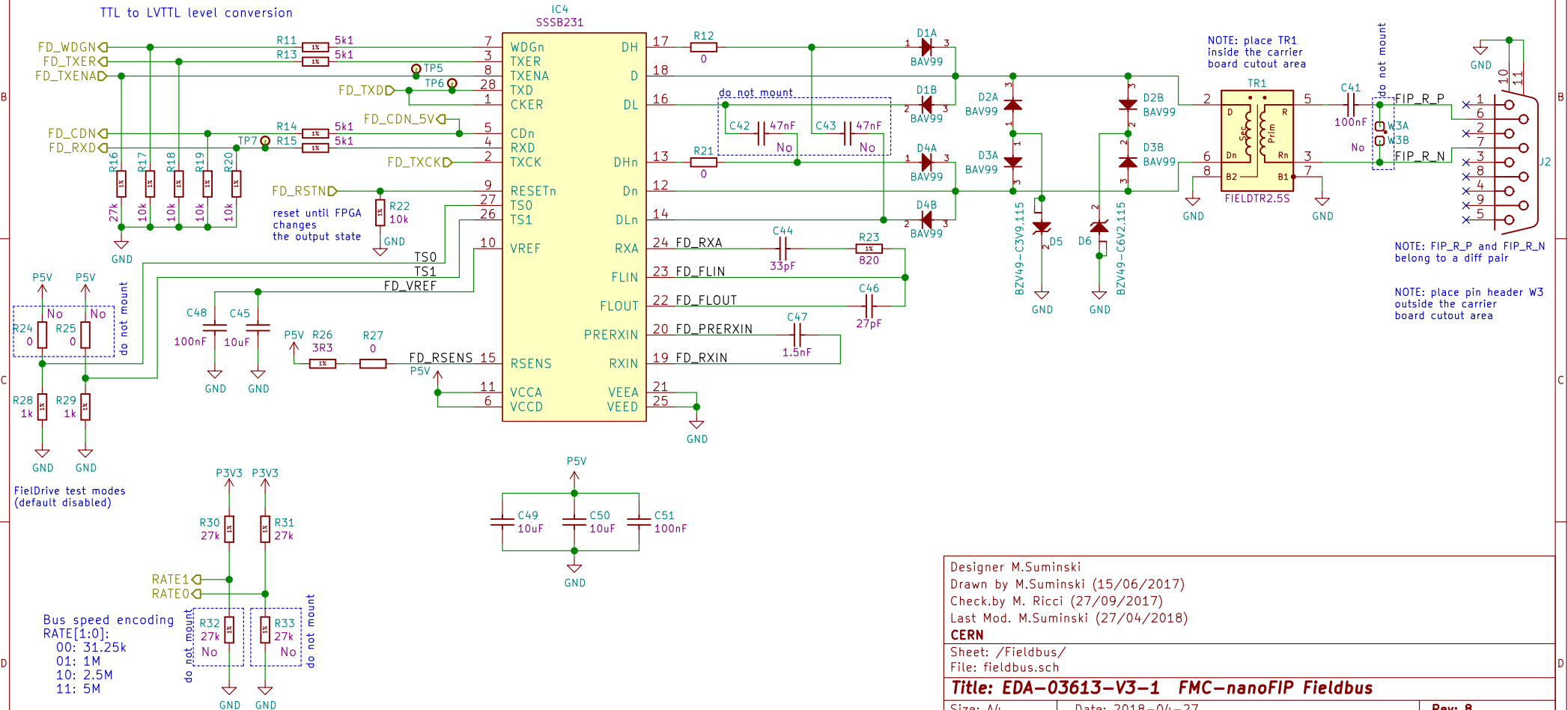
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nanoFIP bus speed

marking resistor	31.25k 	1M 	2.5M 	5M 
	do not mount	do not mount	do not mount	do not mount
C41	3.3uF	470nF	100nF	100nF
C47	100nF	3.3nF	1.5nF	1.5nF
C46	4nF	47pF	27pF	27pF
C44	15nF	100pF	33pF	33pF
C42, C43	47nF	not mounted	not mounted	not mounted
D6	BZV49–C8V2	BZV49–C6V2	BZV49–C6V2	BZV49–C6V2
D1, D4	BAT54S	BAV99	BAV99	BAV99
D5	BZV49–C4V7	BZV49–C3V9	BZV49–C3V9	BZV49–C3V9
R27	3R3	0R	0R	0R
R23	330R	820R	820R	820R
R30	not mounted	not mounted	27k	27k
R31	not mounted	27k	not mounted	27k
R32	27k	not mounted	not mounted	not mounted
R33	27k	not mounted	27k	not mounted
TR1	FIELDTR 31.25S	FIELDTR 1S	FIELDTR 2.5S	FIELDTR 2.5S

selected variant

NOTE: place a label indicating bus speed next to the marking resistors



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Check by M. Ricci (27/09/2017)
Last Mod. M.Suminski (27/04/2018)

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Sheet: /Fieldbus/
File: fieldbus.sch

Title: EDA-03613-V3-1 FMC-nanoFIP Fieldbus

Size: A4 Date: 2018-04-27

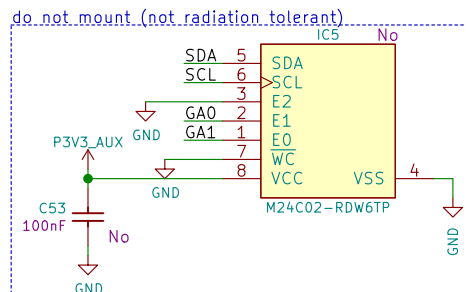
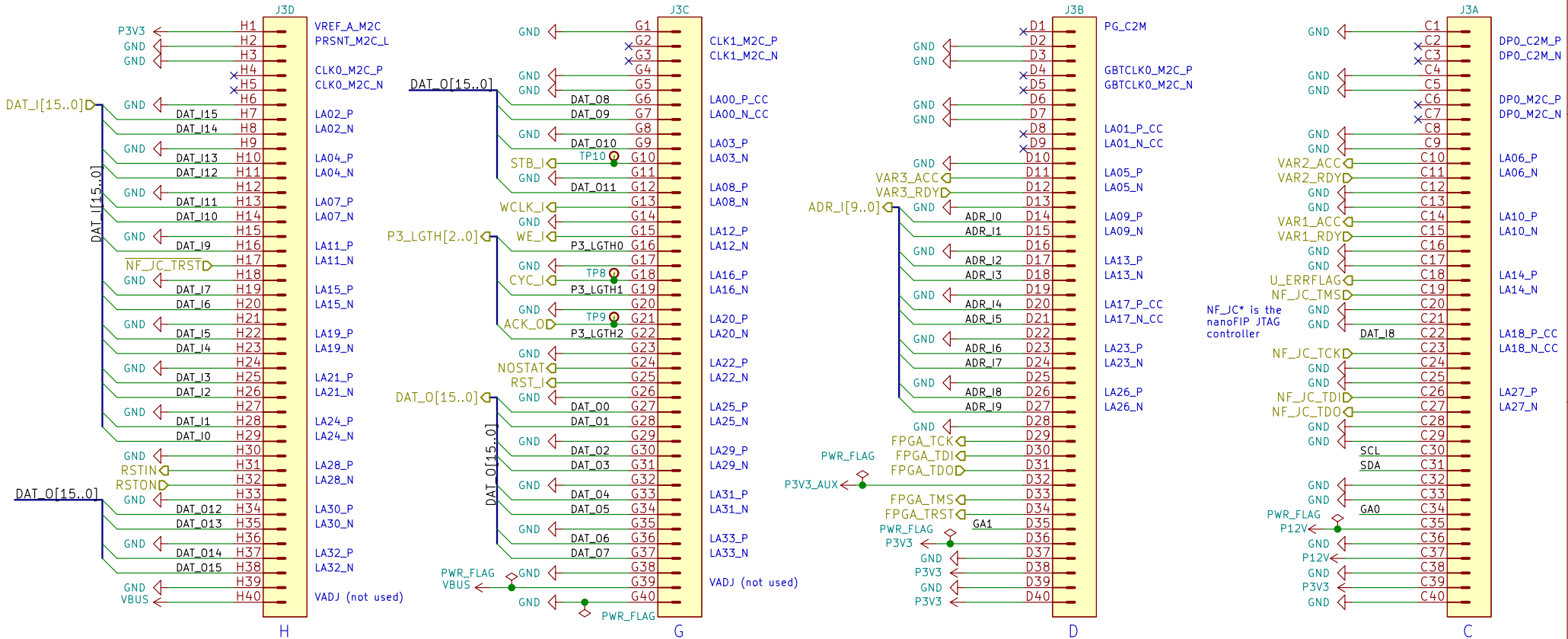
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Rev: 8

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NOTE: pin swapping between LA* pins possible
place test points on the side without the FMC connector



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Check by M. Ricci (27/09/2017)
Last Mod. C. Gentsos (02/07/2021)

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Sheet: /FMC/
File: fmc.sch

Title: EDA-03613-V3-1 FMC-nanoFIP FMC

Size: A4 Date: 2018-04-27

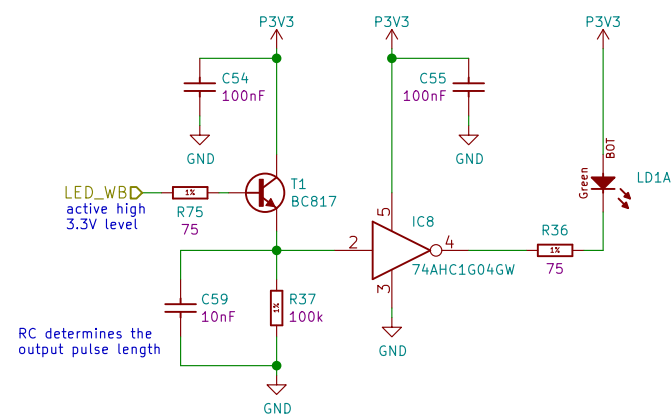
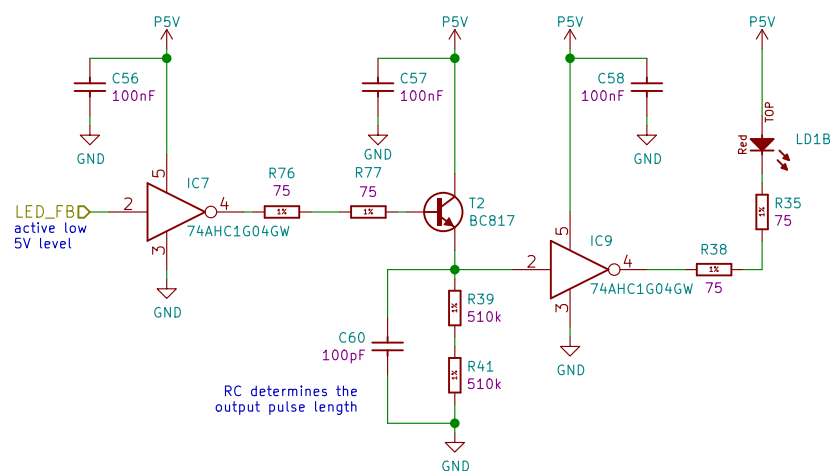
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One-shot triggers to extend the LED pulse duration



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 Check.by M. Ricci (27/09/2017)
 Last Mod. C. Gentsos (02/07/2021)

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Sheet: /LEDs/
 File: leds.sch

Title: EDA-03613-V3-1 FMC-nanoFIP LEDs

Size: A4 Date: 2018-04-27

KiCad E.D.A. kicad 5.1.9

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SUBS[7..0]

P3V3

GND

SW6

place dip-switches on the side without the FMC connector

Hardware revision

HW_REV2
HW_REV1
HW_REV0

R66 R67 R68

do not mount

P3V3

GND

P3_LGTH2
P3_LGTH1
P3_LGTH0

P3_LGTH[2..0]

do not mount

R69 R70 R71

Produced variable data length

P3_LGTH[2:0]:
000: 2 bytes
001: 8 bytes
010: 16 bytes
011: 32 bytes
100: 64 bytes (default)
101: 124 bytes
other: reserved

(FMC signals can override the value set with resistors)

C_ID0
C_ID1
C_ID2
C_ID3
M_ID0
M_ID1
M_ID2
M_ID3

C_ID[3..0]
M_ID[3..0]

place dip-switches on the side without the FMC connector

SW3 SW4 SW5

P3V3

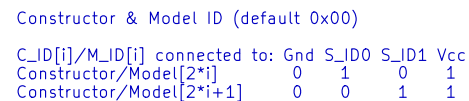
GND

R52 R53 R54 R55 R56 R57 R58 R59

Constructor & Model ID (default 0x00)

C_ID[i]/M_ID[i] connected to: Gnd S_ID0 S_ID1 Vcc
Constructor/Model[2*i] 0 1 0 1
Constructor/Model[2*i+1] 0 0 1 1

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Drawn by M.Suminski (15/06/2017)
Check.by M. Ricci (27/09/2017)
Last Mod. M.Suminski (27/04/2018)
CERN
Sheet: /nanoFIP settings/
File: settings.sch
Title: EDA-03613-V3-1 FMC-nanoFIP settings
Size: A4 Date: 2018-04-27 Rev: 8
KiCad E.D.A. kicad 5.1.9 Id: 7/8



CERN
Sheet: /nanoFIP settings/ File: settings.sch
Title: EDA-03613-V3-1 FMC-nanoFIP settings

Size: A4	Date: 2018-04-27
KiCad E.D.A. kicad 5.1.9	

Rev: 8
Id: 7/8

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NOTE: pin swapping not possible
(only GPIO pins can be moved)
nanoFIP FPGA (IC1) is preprogrammed

