

		Mon May 08 11:23:42 2017				
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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HIGH ENERGY PHYSICS GROUP

H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_toplevel_e

FMC CONNECTOR
AND I2C EEPROM

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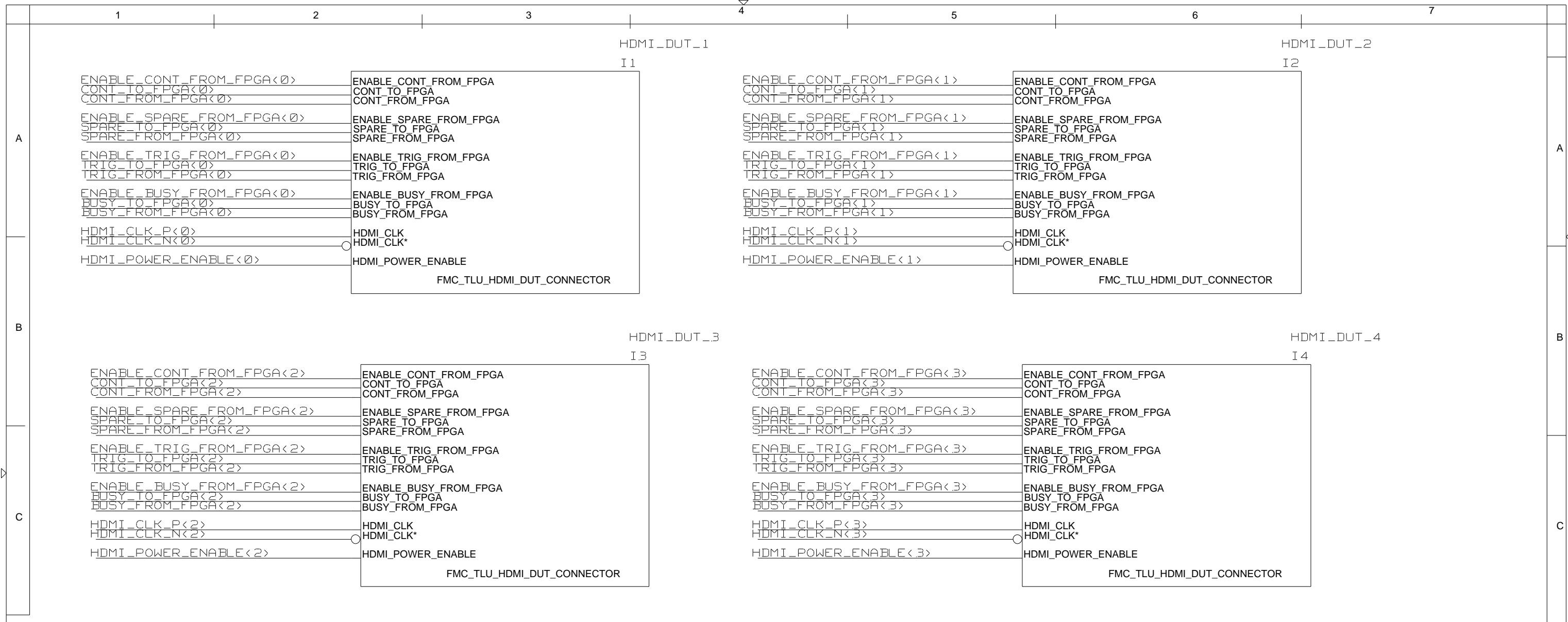
A 2

I2C EEPROM (ADDR= 0X50)
CONTAINS PRE-PROGRAMMED
UNIQUE ID CODE

A 2

MODULE PAGE: 1 OF 7
OVERALL PAGE: 1 OF 29

TOTAL NO. OF SHEETS



	Thu May 24 13:37:48 2017					
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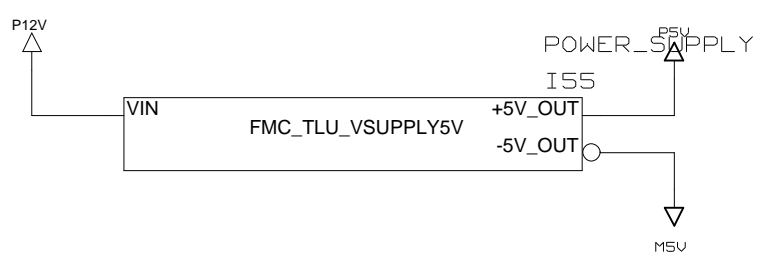
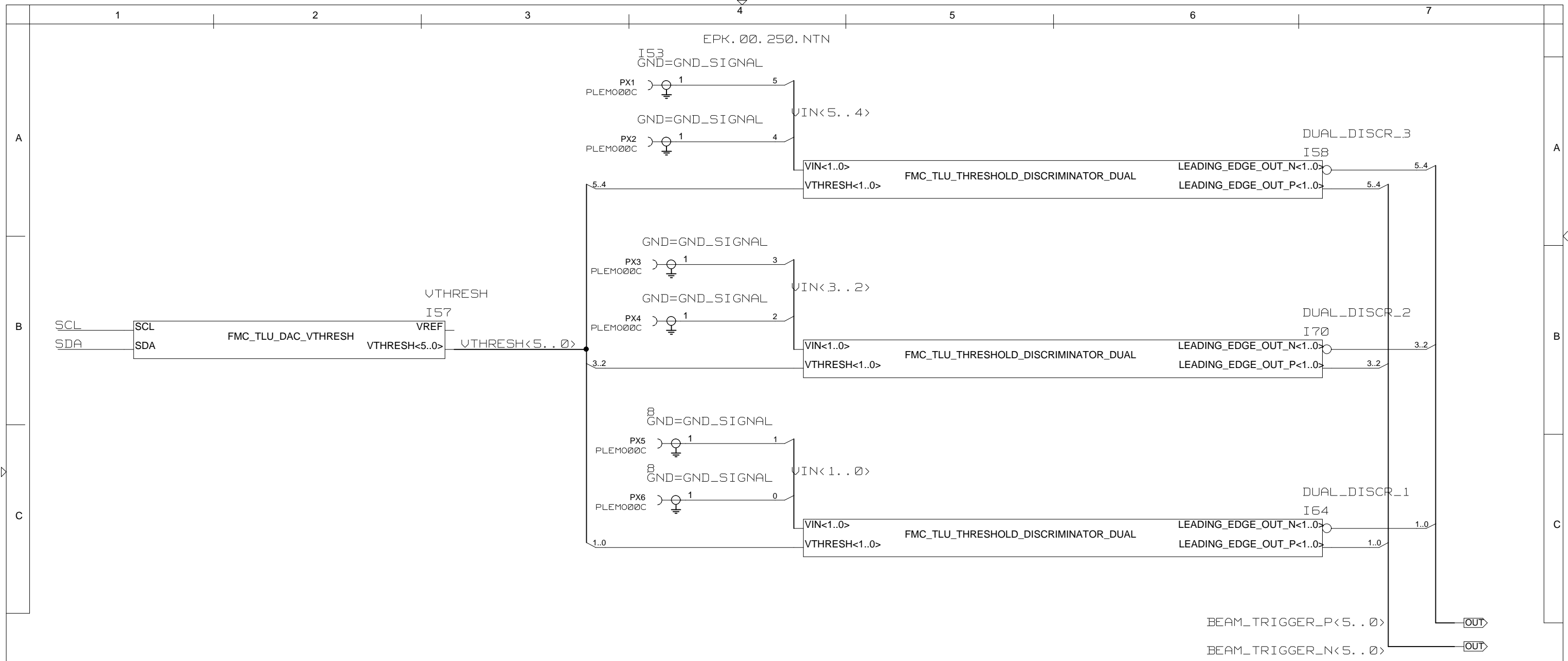
UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib FRONT PANEL DUT CONNECTORS
MODULE: fmc_tlu_toplevel_e 3 X HDMI (DUT ONLY)
1 X HDMI (DUT OR UPLINK)

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A 2

A 2 MODULE PAGE: 2 OF 7
OVERALL PAGE: 2 OF 29

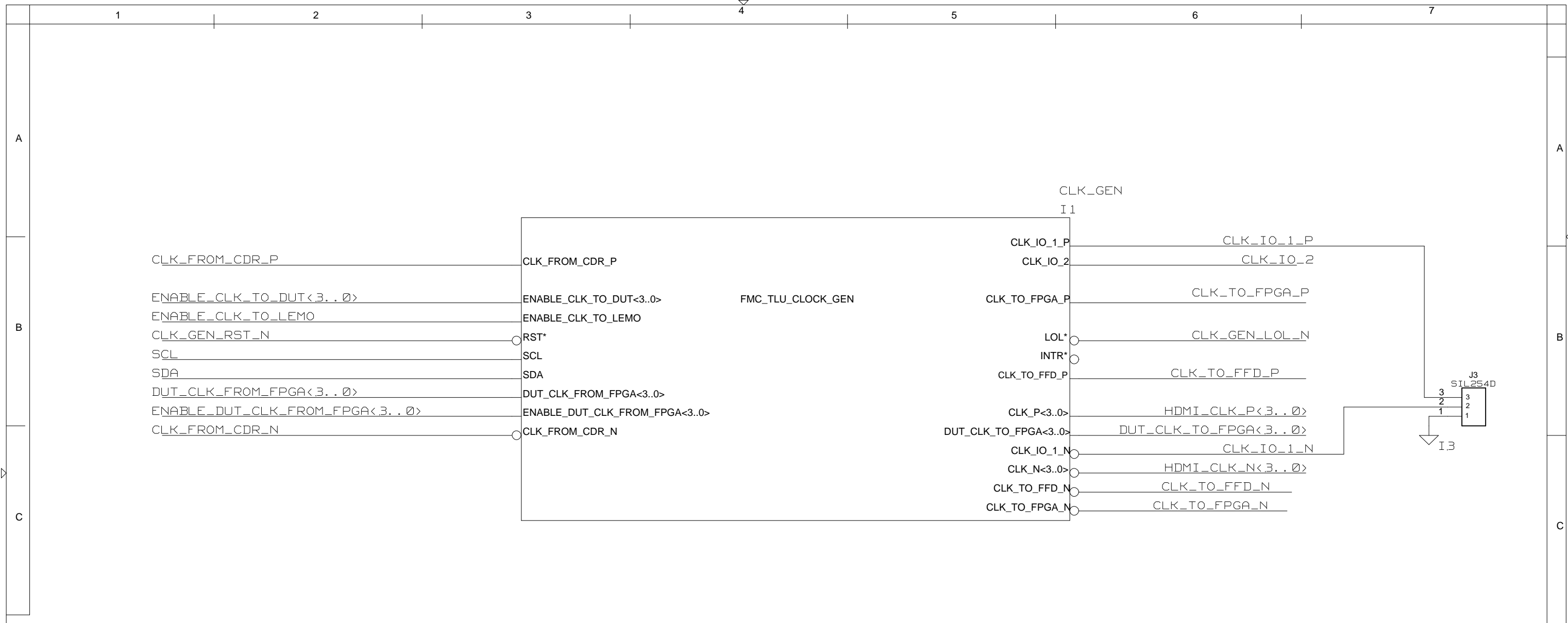


	Mon Mar 27 17:58:51 2017					
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HIGH ENERGY PHYSICS GROUP

TITLE fmc_tlu_v1_lib
MODULE: fmc_tlu_toplevel_e
DISCRIMINATORS



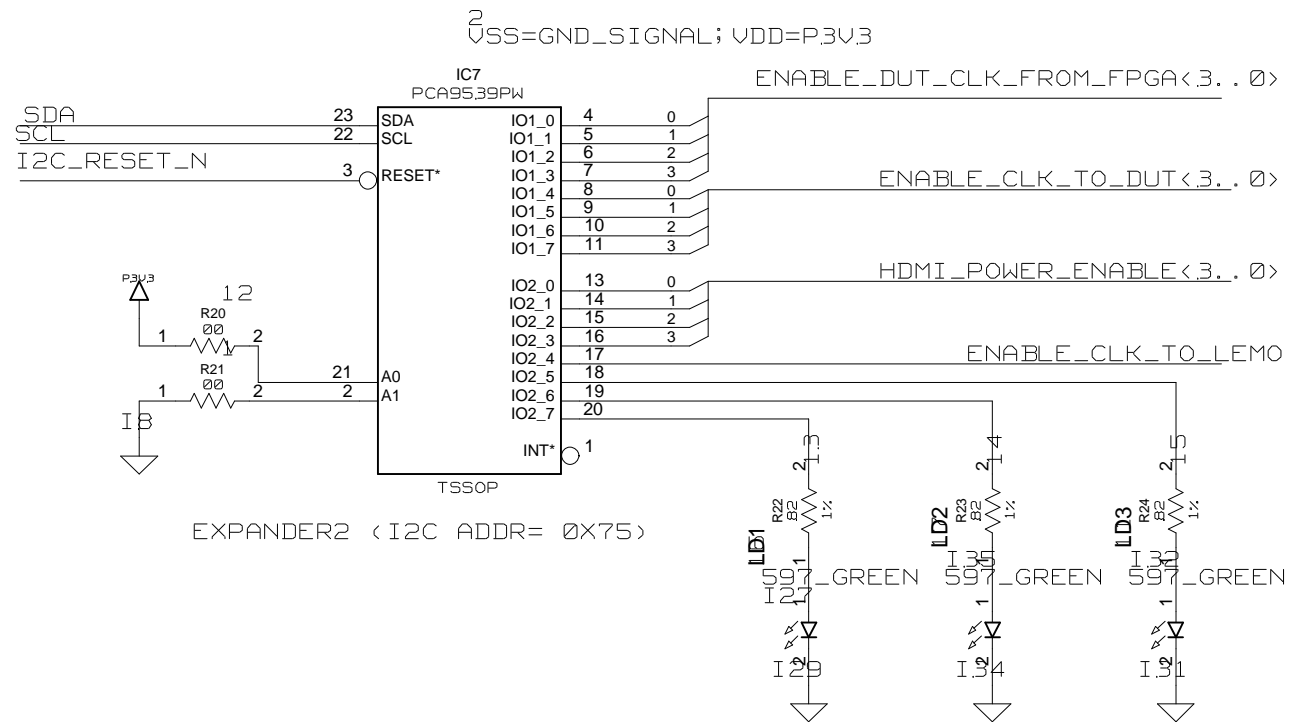
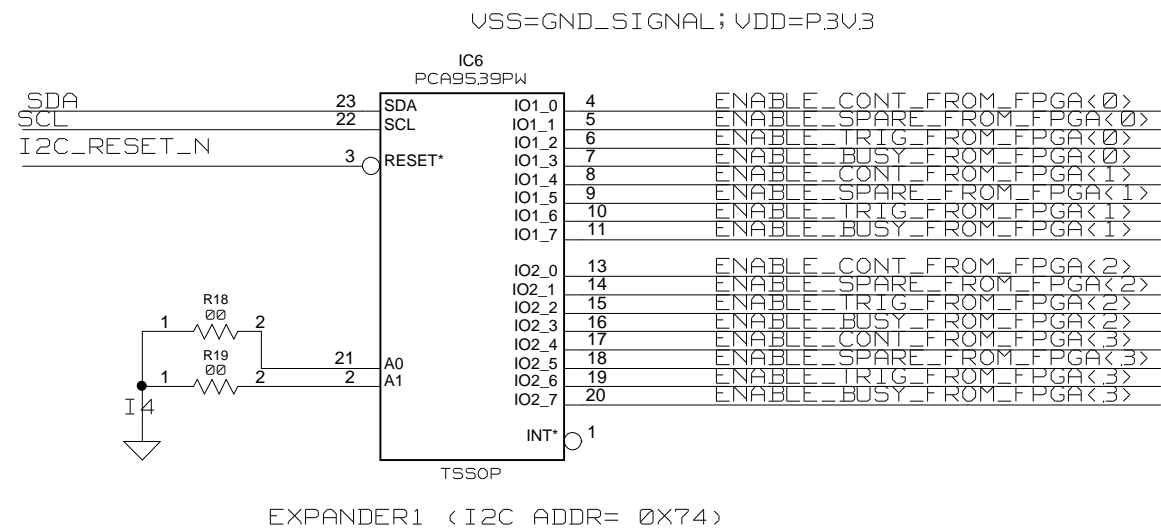
	Thu Mar 30 17:10:57 2017					
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TITLE `fmc_tlu_v1_lib` CLOCK GENERATION
MODULE: `fmc_tlu_toplevel_e`

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	Mon Mar 27 17:58:54 2017					
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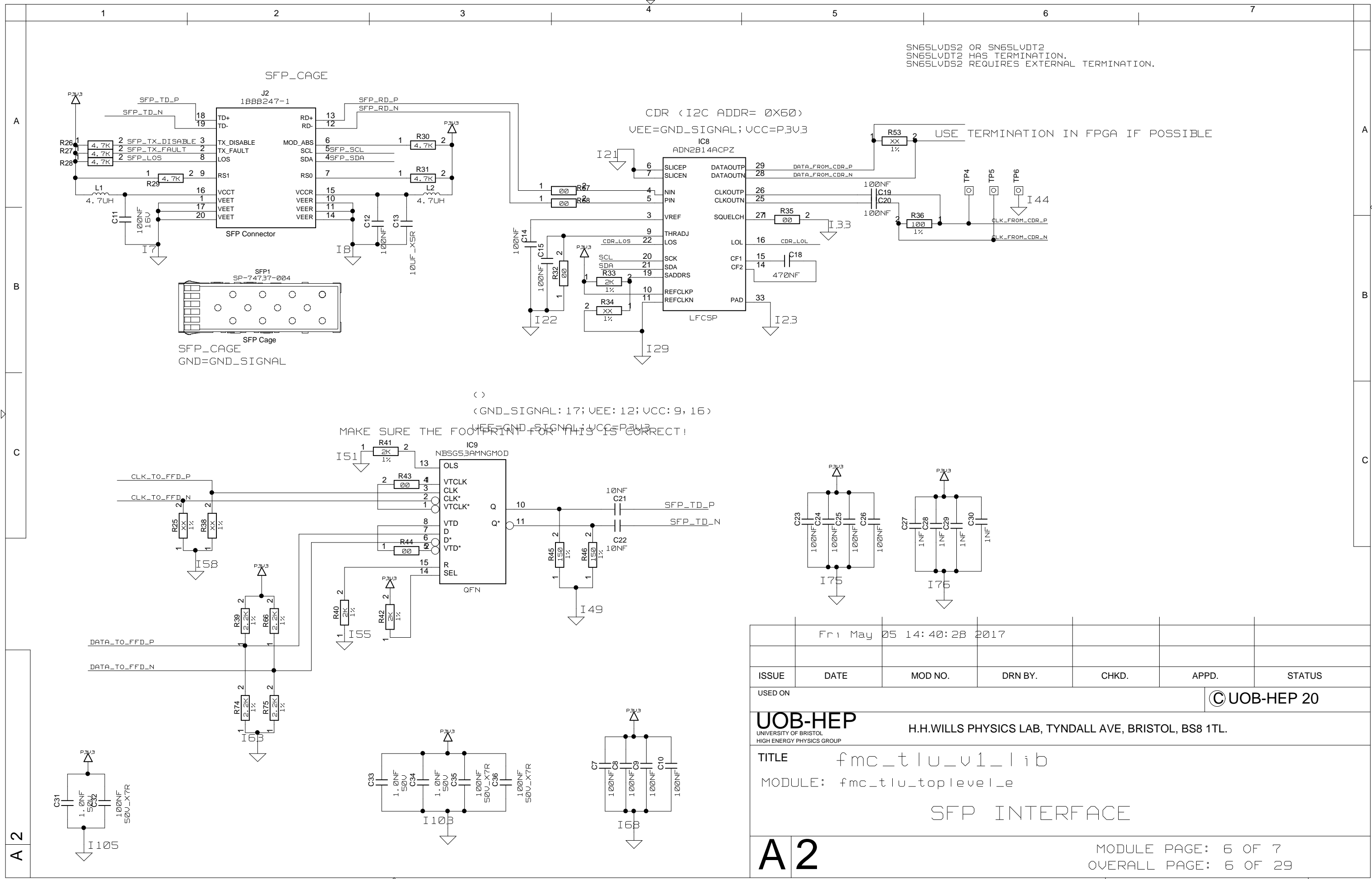
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE fmc_tlu_v1_lib I2C I/O EXTENDERS
MODULE: fmc_tlu_toplevel_e

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A 2 MODULE PAGE: 5 OF 7
OVERALL PAGE: 5 OF 29

TOTAL NO. OF SHEETS



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	Fri May 05 14:40:28 2017					

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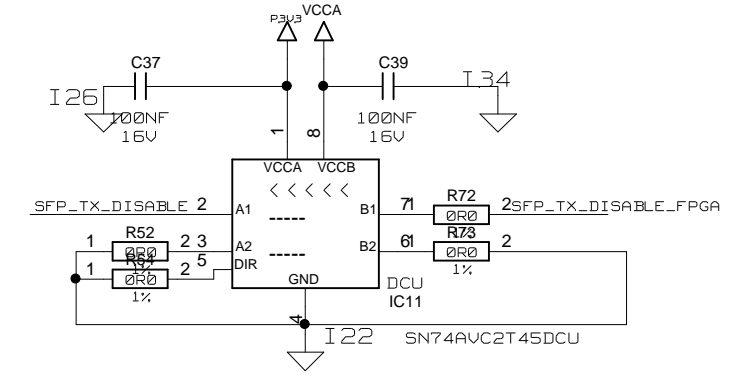
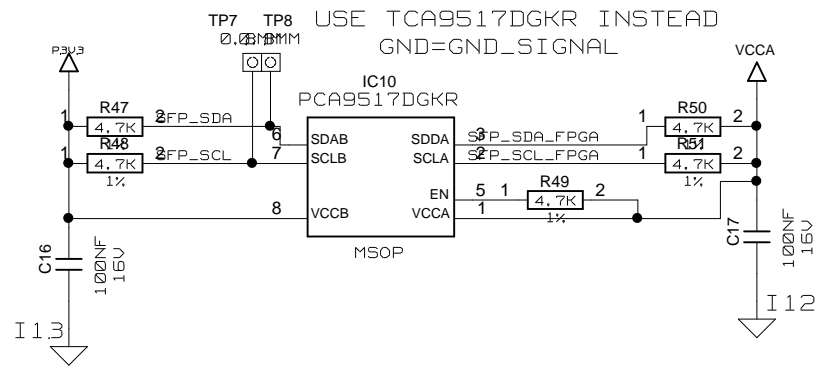
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UNIVERSITY OF BRISTOL
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H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

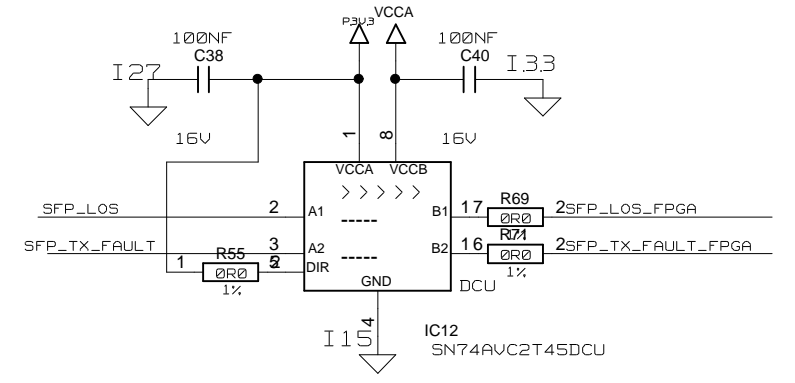
TITLE fmc_tlu_v1_lib

MODULE: fmc_tlu_toplevel_e

SFP INTERFACE



DIR LOW : B -> A
 DIR HIGH: A -> B



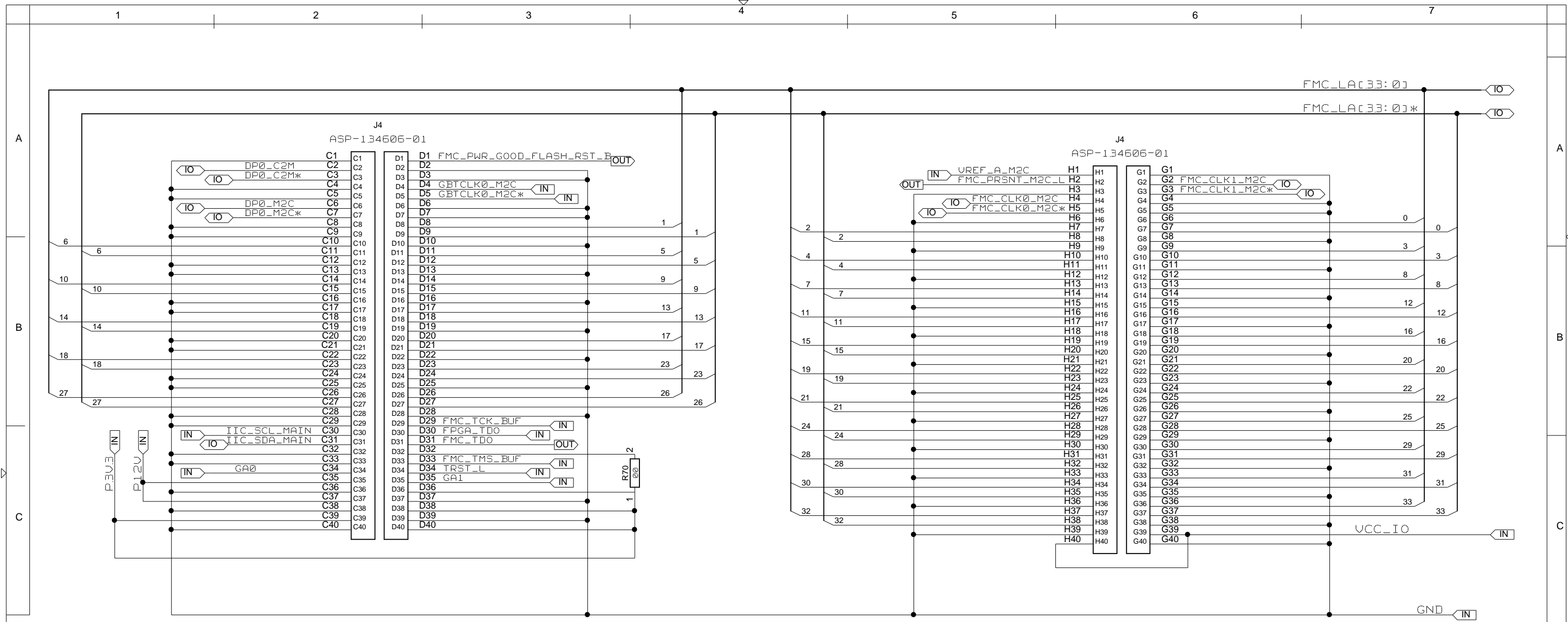
	Thu Mar 30 17:11:07 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE `fmc_tlu_v1_lib`
 MODULE: `fmc_tlu_toplevel_e`

LEVEL TRANSLATORS

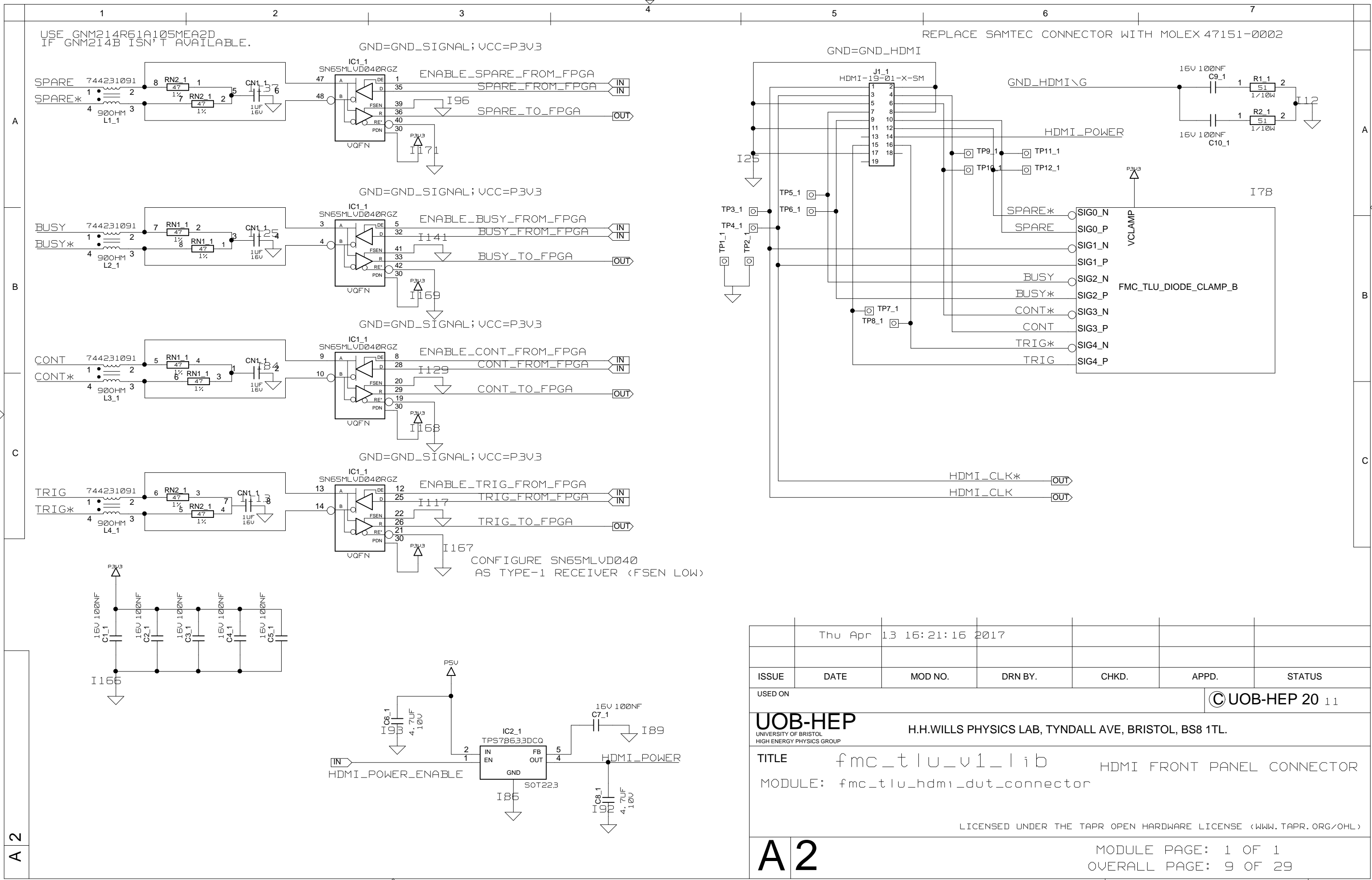


ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
	Thu Mar 30 11:19:40 2017		D. CUSSANS	C. JESKE	D. CUSSANS	

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TITLE `fmc_tlu_v1_lib`
 MODULE: `pc036a_fmc_lpc_connector`
 FMC LPC



ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
	Thu Apr 13 16:21:16 2017					

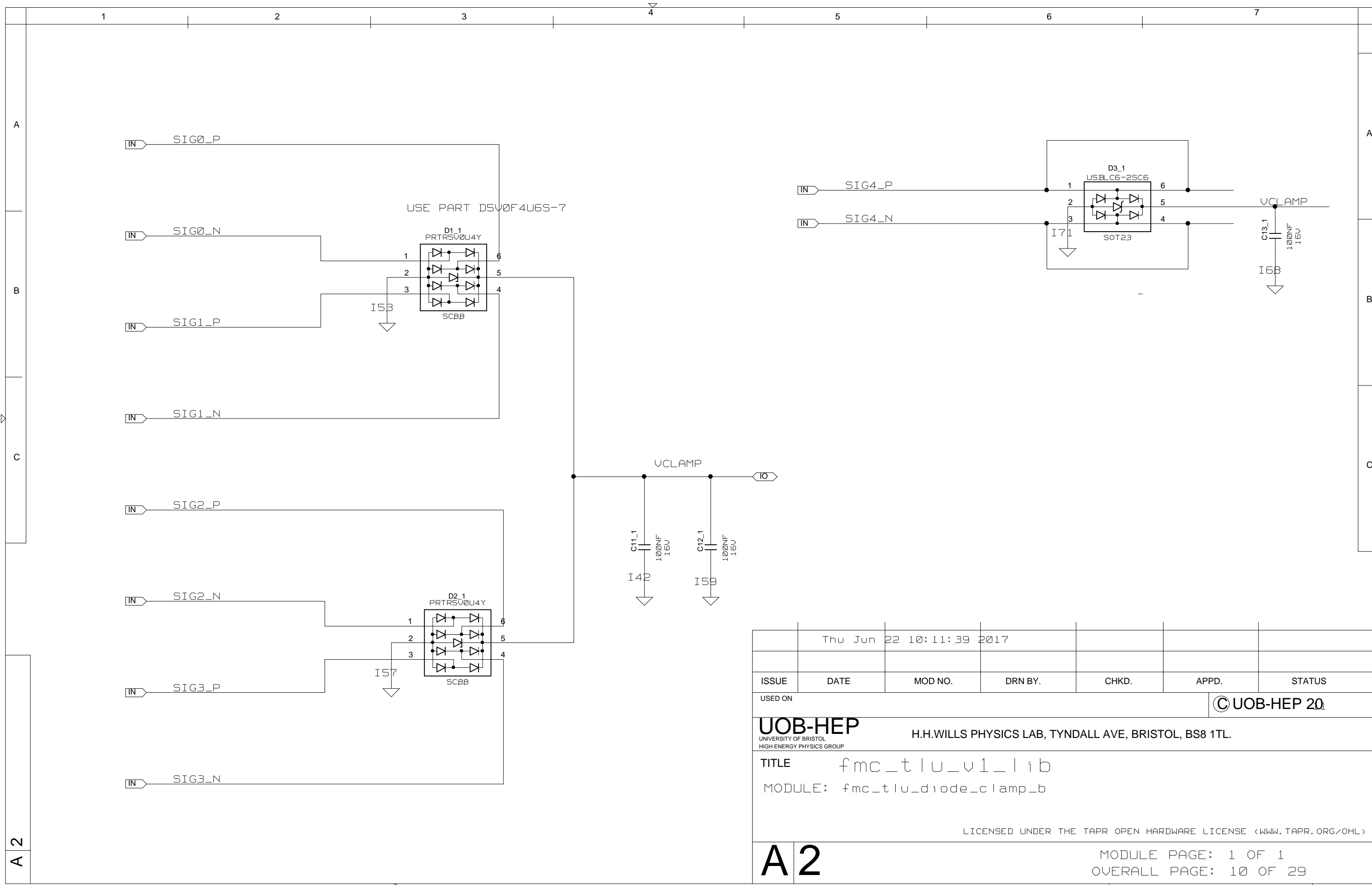
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TITLE `fmc_tlu_v1_lib` HDMI FRONT PANEL CONNECTOR
MODULE: `fmc_tlu_hdmi_dut_connector`

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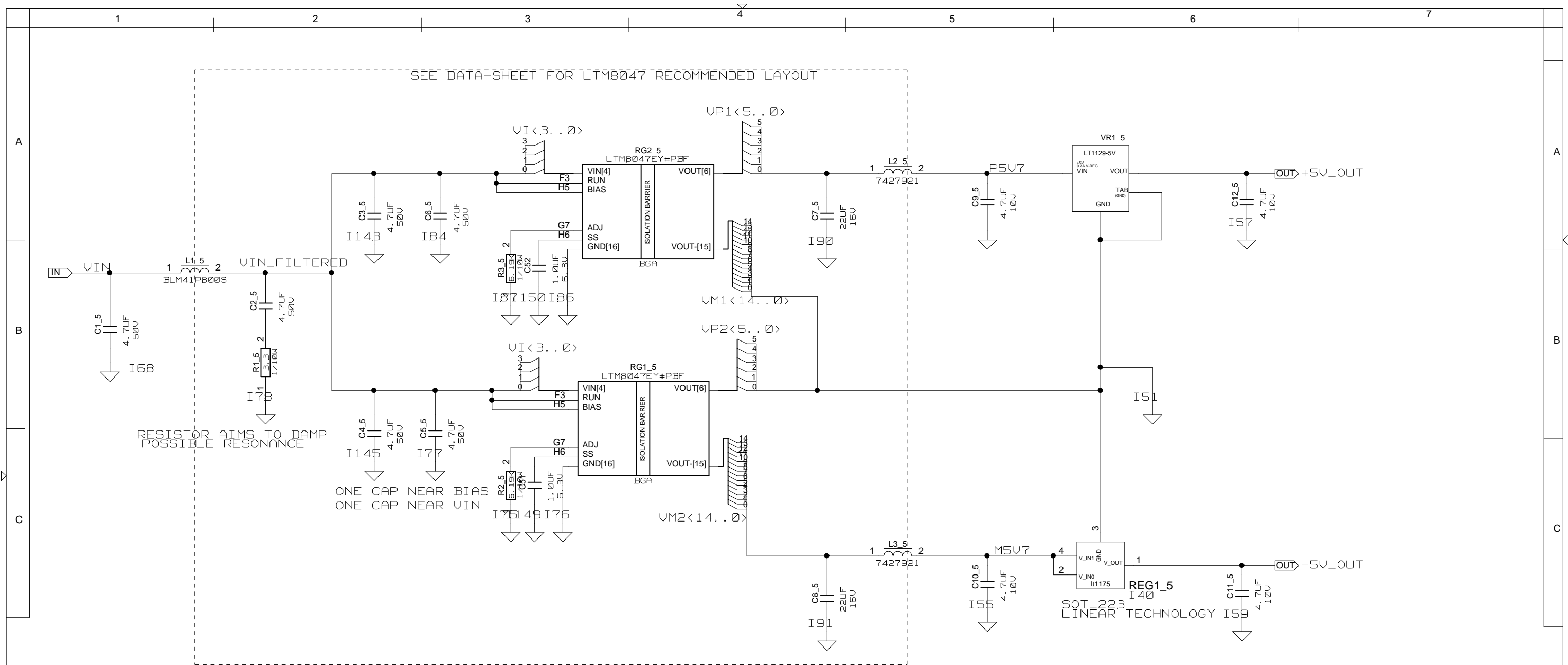
		Thu Jun 22 10:11:39 2017				
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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HIGH ENERGY PHYSICS GROUP H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE `fmc_tlu_v1_lib`
MODULE: `fmc_tlu_diode_clamp_b`

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SEE DATA-SHEET FOR LTMB047 RECOMMENDED LAYOUT

RESISTOR AIMS TO DAMP POSSIBLE RESONANCE

ONE CAP NEAR BIAS
ONE CAP NEAR VIN

PUT DC-DC MODULES ON
COPPER AREA SURROUNDED BY
A MOAT (SPLIT IN PLANES)
CROSS THE MOAT IN ONE PLACE
WITH VIN , +5V , -5V AND GROUND

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
	Fri May 05 14:39:22 2017					

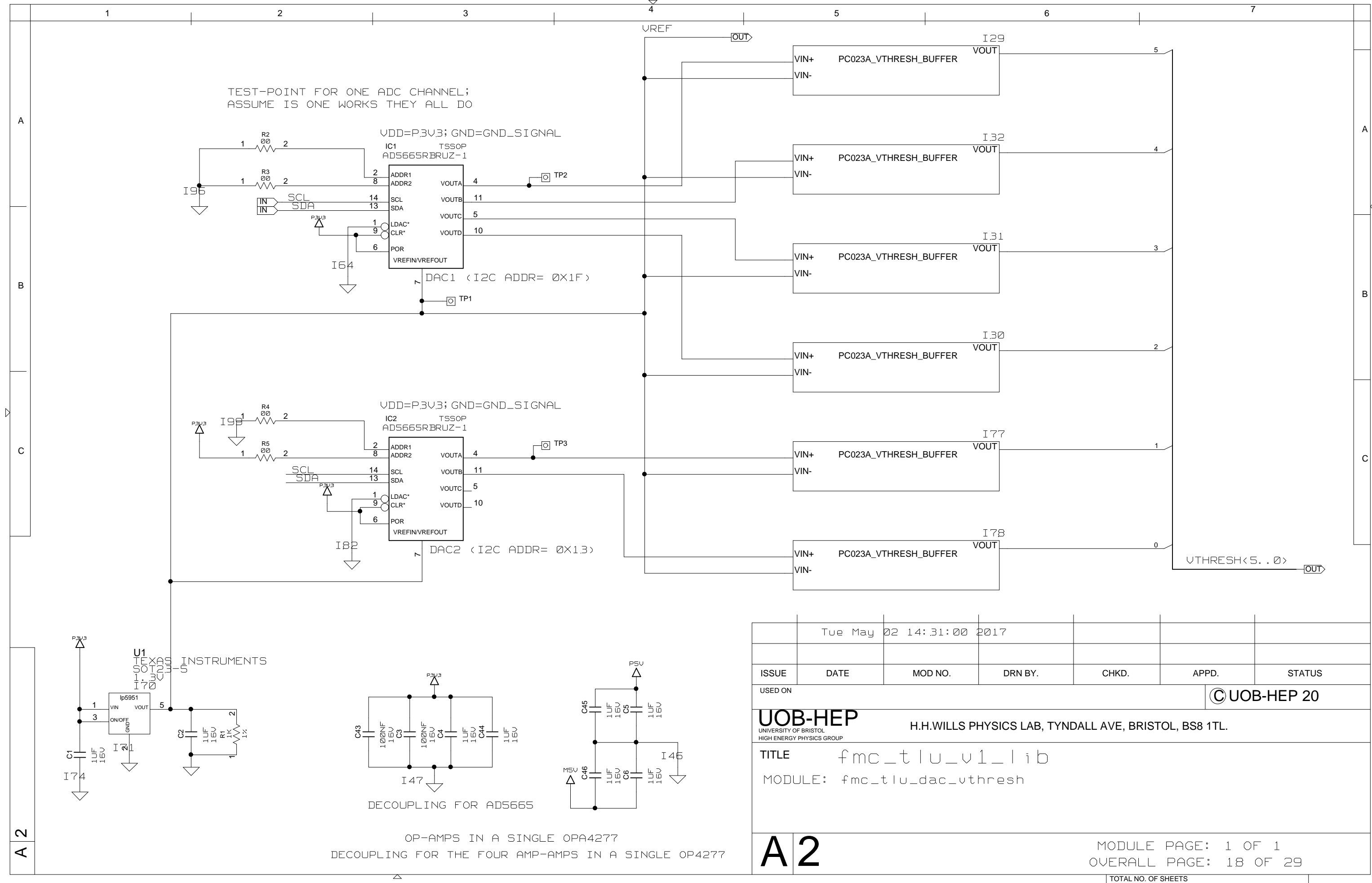
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TITLE fmc_tlu_v1_lib
MODULE: fmc_tlu_vsupply5v

SUPPLY_DIGITAL
OVERALL PAGE: 17 OF 29

A2 MODULE PAGE: 1 OF 1



TEST-POINT FOR ONE ADC CHANNEL;
ASSUME IS ONE WORKS THEY ALL DO

VDD=P3V3; GND=GND_SIGNAL

IC1 TSSOP
AD5665RBRUZ-1

ADDR1 2
ADDR2 8
SCL 14
SDA 13
LDAC* 9
CLR* 10
POR 6
VREFIN/VREFOUT 7

DAC1 (I2C ADDR= 0X1F)

VDD=P3V3; GND=GND_SIGNAL

IC2 TSSOP
AD5665RBRUZ-1

ADDR1 2
ADDR2 8
SCL 14
SDA 13
LDAC* 9
CLR* 10
POR 6
VREFIN/VREFOUT 7

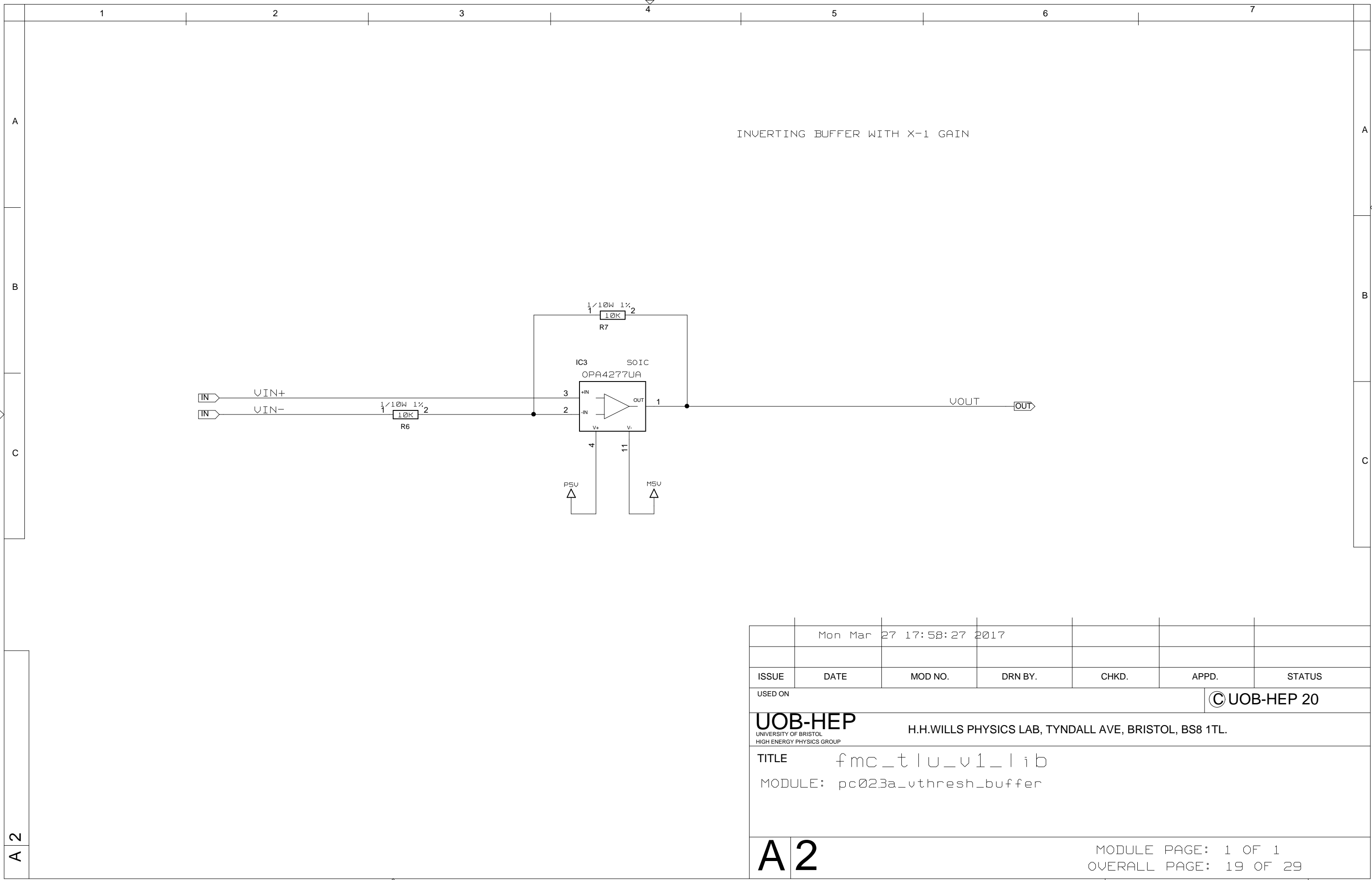
DAC2 (I2C ADDR= 0X13)

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
	Tue May 02 14:31:00 2017					

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TITLE fmc_tlu_v1_lib
MODULE: fmc_tlu_dac_vthresh



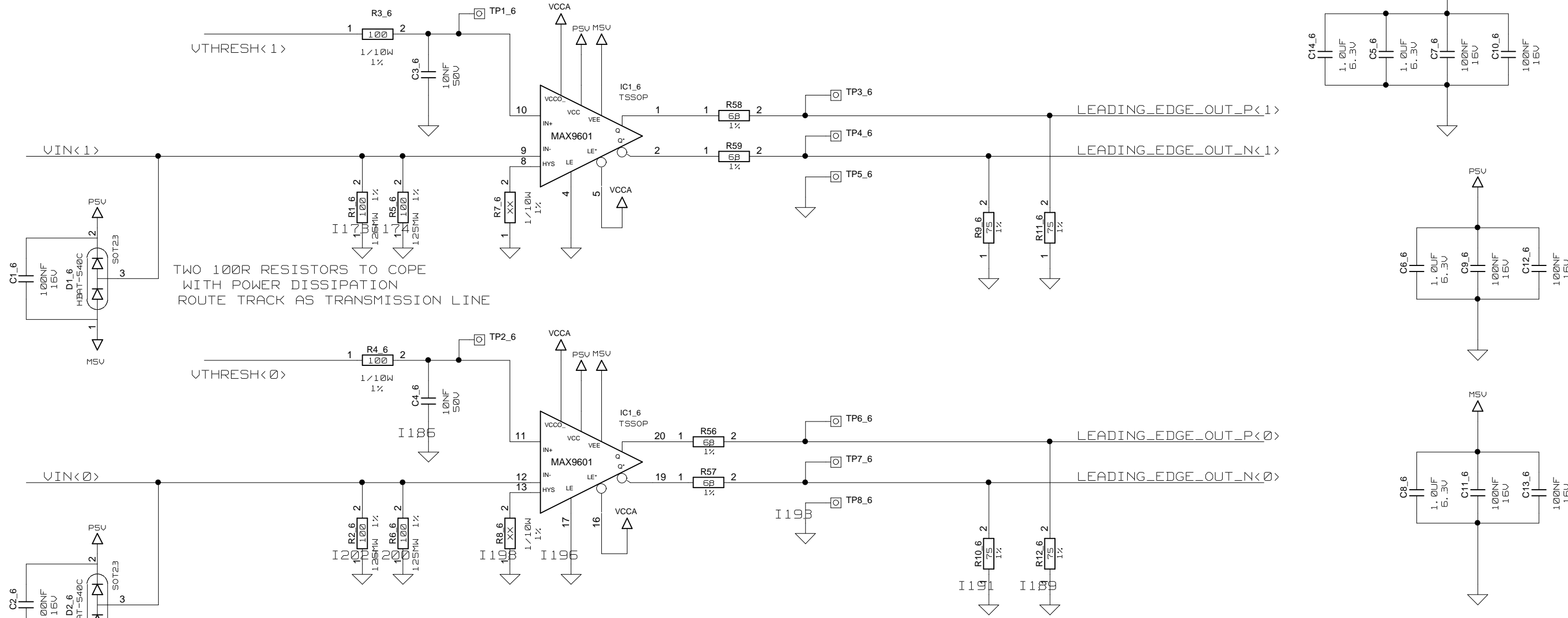
	Mon Mar 27 17:58:27 2017					
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TITLE `fmc_tlu_v1_lib`
MODULE: `pc023a_vthresh_buffer`

SPECIFY RESISTORS TO WITHSTAND PERMANENT 5V INPUT AT VIN



TWO 100Ω RESISTORS TO COPE WITH POWER DISSIPATION
ROUTE TRACK AS TRANSMISSION LINE



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	Thu Mar 30 12:08:36 2017					

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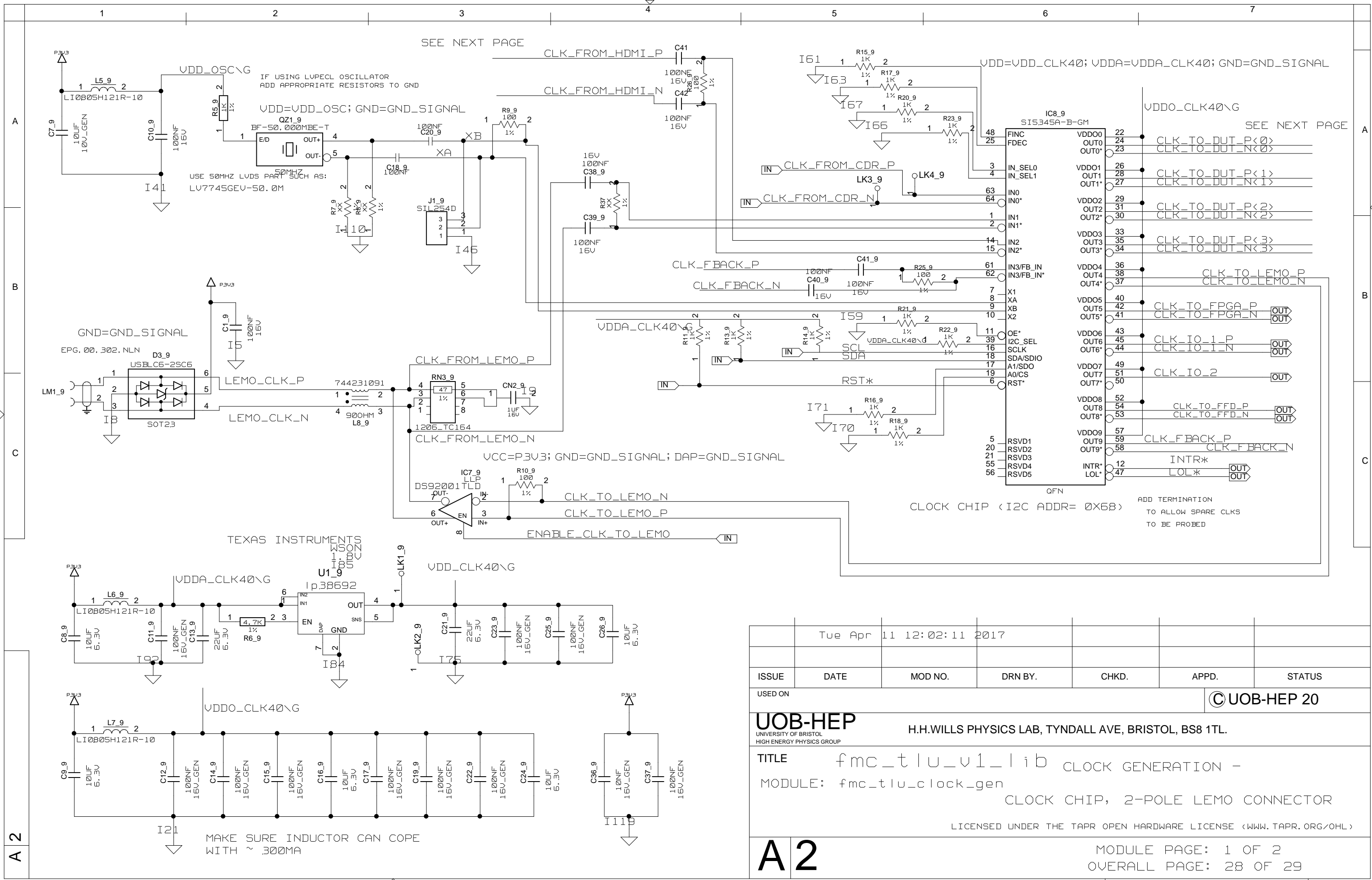
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE `fmc_tlu_v1_lib`
`MODULE: fmc_tlu_threshold_discriminator_dual`

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A 2 MODULE PAGE: 1 OF 1
OVERALL PAGE: 25 OF 29

TOTAL NO. OF SHEETS



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	Tue Apr 11 12:02:11 2017					

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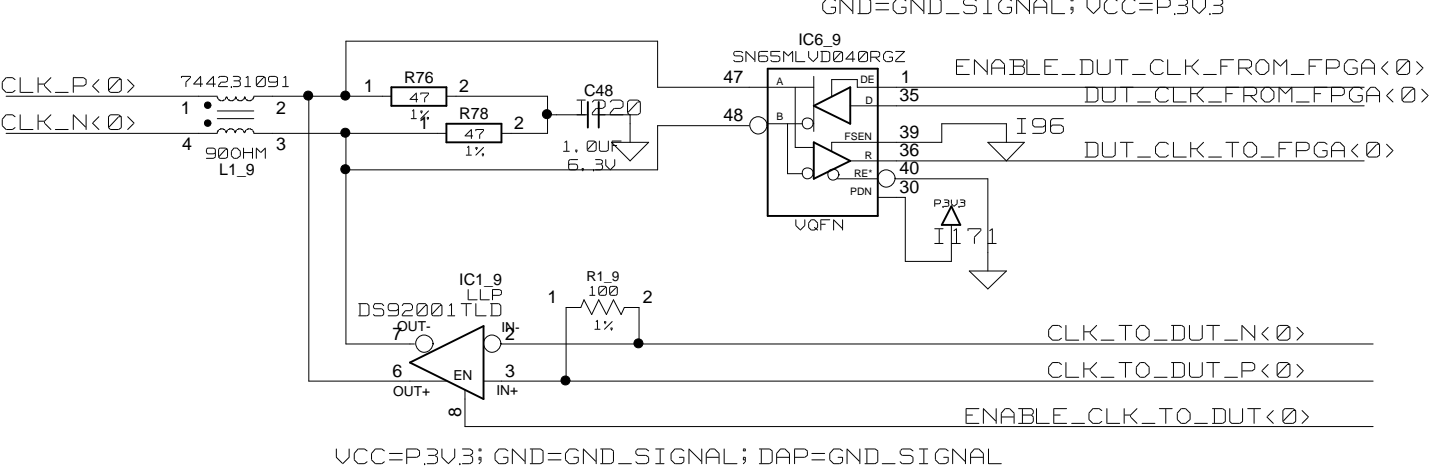
TITLE `fmc_tlu_v1_lib` CLOCK GENERATION -
 MODULE: `fmc_tlu_clock_gen`
 CLOCK CHIP, 2-POLE LEMO CONNECTOR

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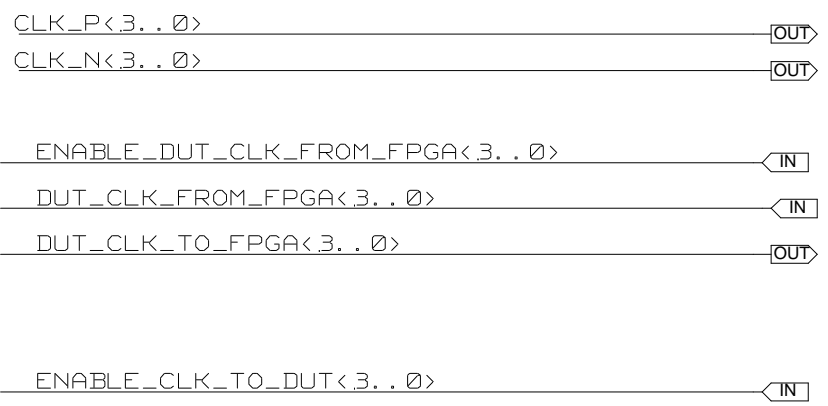
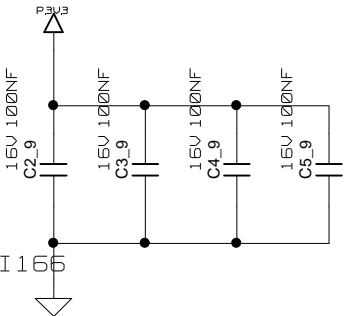
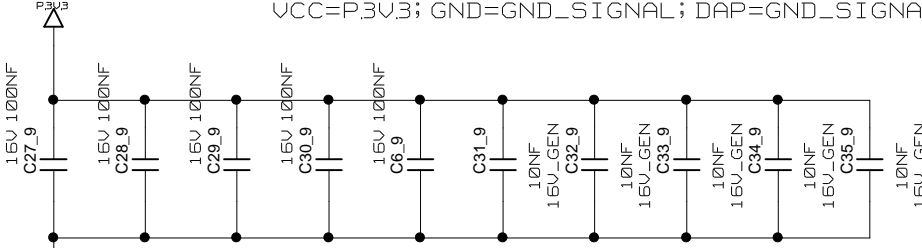
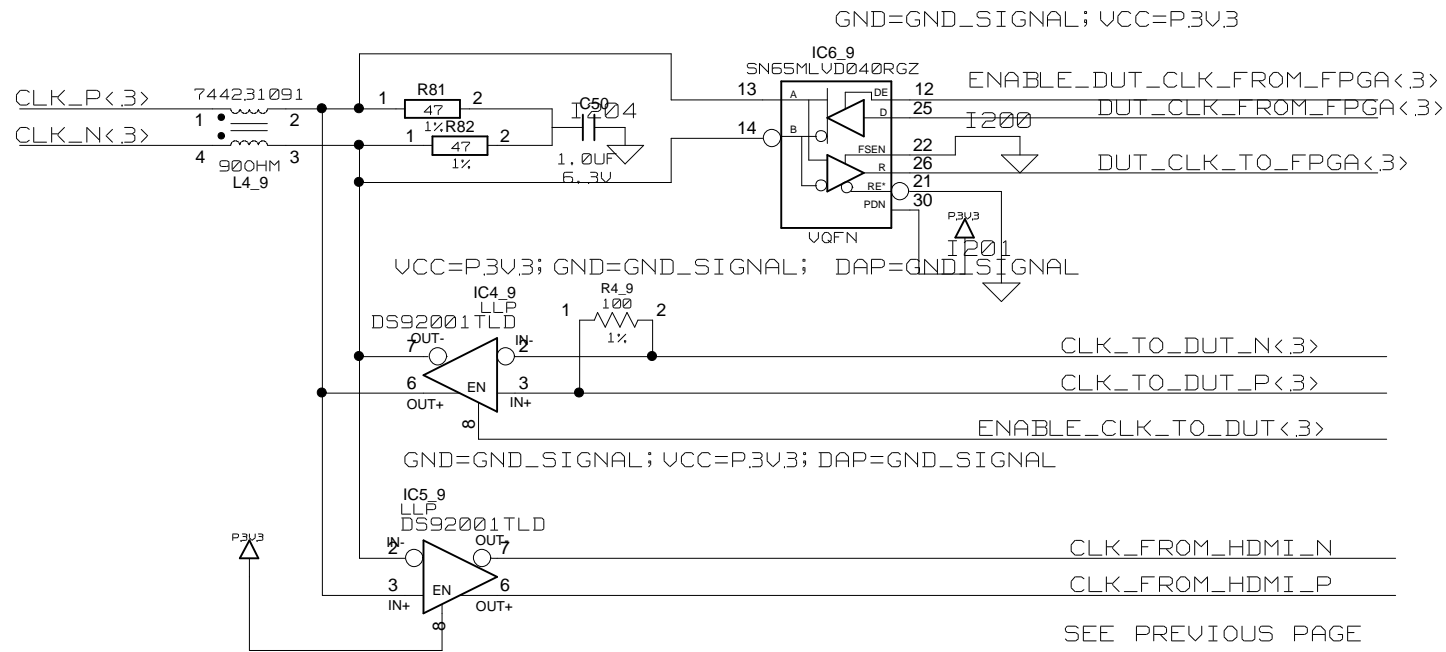
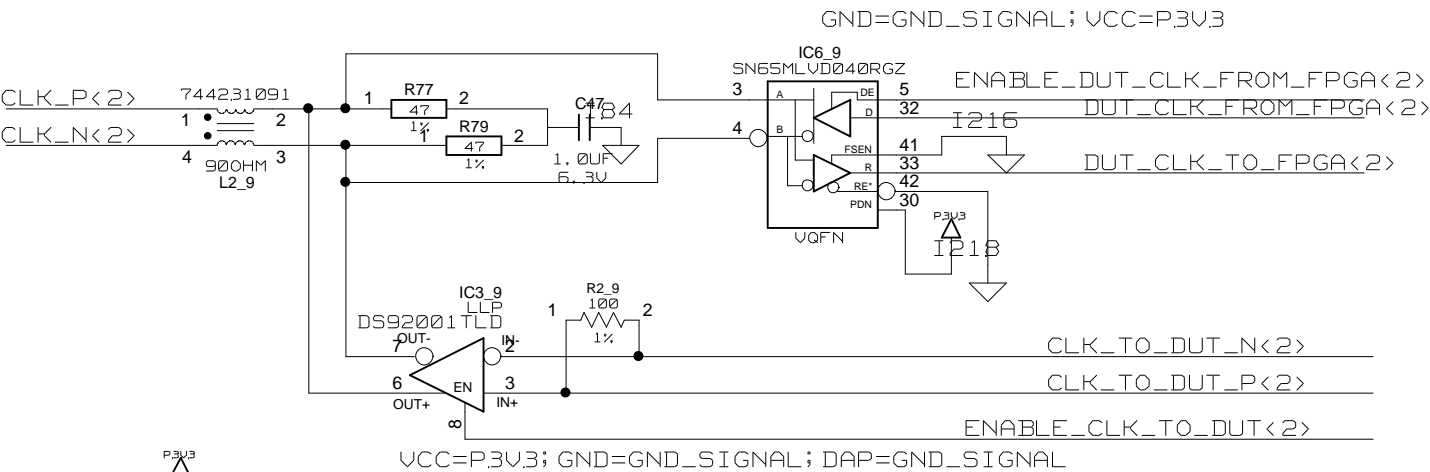
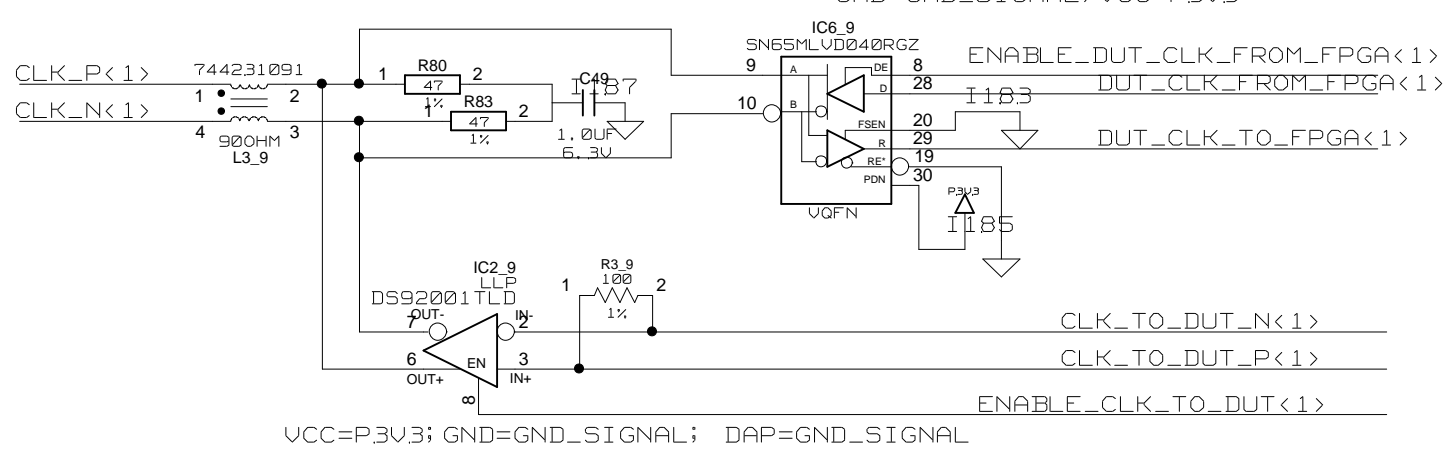
A2

TOTAL NO. OF SHEETS

USE_GNM214R61A105MEA2D
IF_GNM214B_ISN'T_AVAILABLE.



CONFIGURE SN65MLVD040
AS TYPE-1 RECEIVER (FSEN LOW)



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	Fri May 05 14:48:32 2017					

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TITLE `fmc_tlu_v1_lib` CLOCK GENERATION -
MODULE: `fmc_tlu_clock_gen`
I/O BUFFERS AND LEVEL TRANSLATORS
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