Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;

LIBRARY work;
USE work.ipbus.all;
USE work.emac_hostbus_decl.all;

USE work.fmcTLU.all;
LIBRARY unisim;
USE unisim.vcomponents.all;

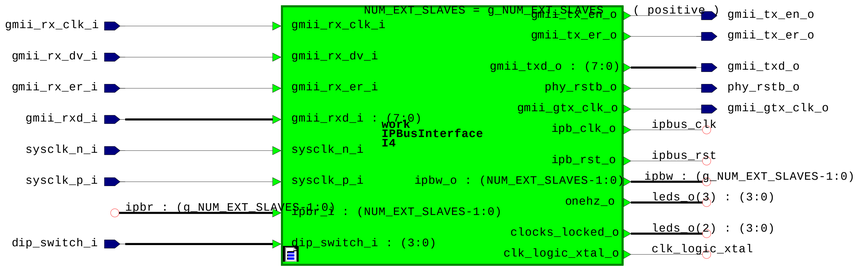
Declarations
Ports:

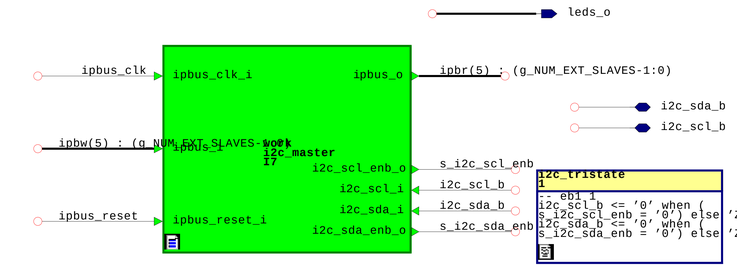
busy_n_i	: std_logic_vector(g_NUM_DUTS-1 DOWNTO 0)
busy_p_i	: std_logic_vector(g_NUM_DUTS-1 DOWNTO 0) --! Busy lines from DUTs (active high)
cfd_discr_n_i	: std_logic_vector(g_NUM_TRIG_INPUTS-1 DOWNTO 0)
cfd_discr_p_i	: std_logic_vector(g_NUM_TRIG_INPUTS-1 DOWNTO 0)
dip_switch_i	: std_logic_vector(3 DOWNTO 0)
dut_clk_n_i	: std_logic_vector(g_NUM_DUTS-1 DOWNTO 0)
dut_clk_p_i	: std_logic_vector(g_NUM_DUTS-1 DOWNTO 0)
gmii_rx_clk_i	: std_logic
gmii_rx_dv_i	: std_logic
gmii_rx_er_i	: std_logic
gmii_rxd_i	: std_logic_vector(7 DOWNTO 0)
sysclk_n_i	: std_logic --! 200 MHz xtal clock
sysclk_p_i	: std_logic
threshold_discr_n_i	: std_logic_vector(g_NUM_TRIG_INPUTS-1 DOWNTO 0)
threshold_discr_p_i	: std_logic_vector(g_NUM_TRIG_INPUTS-1 DOWNTO 0)
gmii_gtx_clk_o	: std_logic
gmii_tx_en_o	: std_logic
gmii_tx_er_o	: std_logic
gmii_txd_o	: std_logic_vector(7 DOWNTO 0)
gpio_hdr	: std_logic_vector(7 DOWNTO 0)
leds_o	: std_logic_vector(3 DOWNTO 0)
phy_rstb_o	: std_logic
reset_or_clk_n_o	: std_logic_vector(g_NUM_DUTS-1 DOWNTO 0)
reset_or_clk_p_o	: std_logic_vector(g_NUM_DUTS-1 DOWNTO 0)
triggers_n_o	: std_logic_vector(g_NUM_DUTS-1 DOWNTO 0)
triggers_p_o	: std_logic_vector(g_NUM_DUTS-1 DOWNTO 0) --! Trigger lines to DUT
extclk_n_b	: std_logic
extclk_p_b	: std_logic --! either external clock in, or a clock being driven out
i2c_scl_b	: std_logic
i2c_sda_b	: std_logic

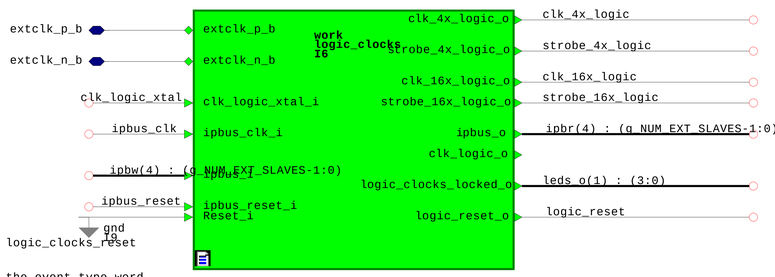
Diagram Signals:

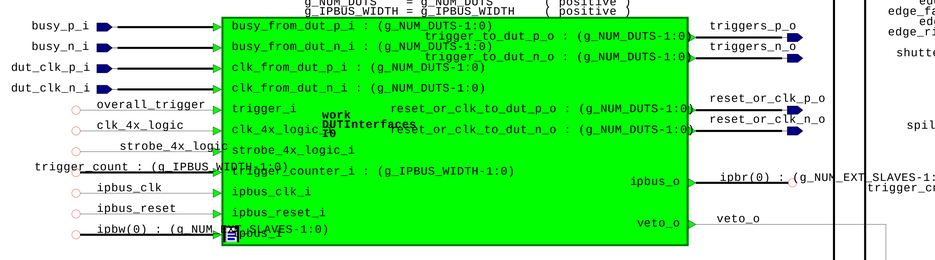
SIGNAL buffer_full_o	: std_logic --! Goes high when event buffer almost full
SIGNAL clk_16x_logic	: std_logic -- 640MHz clock
SIGNAL clk_4x_logic	: std_logic --! normally 160MHz
SIGNAL clk_logic_xtal	: std_logic -- ! 40MHz clock from onboard xtal
SIGNAL data_strobe	: std_logic -- goes high when data ready to load into event buffer
SIGNAL edge_fall_i	: std_logic_vector(g_NUM_EDGE_INPUTS-1 DOWNTO 0) -- ! High when falling edge
SIGNAL edge_fall_time_i	: t_triggerTimeArray(g_NUM_EDGE_INPUTS-1 DOWNTO 0) -- Array of edge times (w.r.t. logic_strobe)
SIGNAL edge_rise_i	: std_logic_vector(g_NUM_EDGE_INPUTS-1 DOWNTO 0) -- ! High when rising edge
SIGNAL edge_rise_time_i	: t_triggerTimeArray(g_NUM_EDGE_INPUTS-1 DOWNTO 0) -- Array of edge times (w.r.t. logic_strobe)
SIGNAL event_data	: std_logic_vector(g_EVENT_DATA_WIDTH-1 DOWNTO 0)
SIGNAL event_number_o	: std_logic_vector(g_IPBUS_WIDTH-1 downto 0) -- starts at one. Increments for each post_veto_trigger
SIGNAL ipbr	: ipb_rbus_array(g_NUM_EXT_SLAVES-1 DOWNTO 0) --! IPBus read signals
SIGNAL ipbus_clk	: std_logic
SIGNAL ipbus_clk_i	: std_logic
SIGNAL ipbus_reset	: std_logic
SIGNAL ipbus_rst	: std_logic -- ! IPBus reset to slaves
SIGNAL ipbw	: ipb_wbus_array(g_NUM_EXT_SLAVES-1 DOWNTO 0) --! IBus write signals
SIGNAL logic_clocks_reset	: std_logic -- Goes high to reset counters etc. Sync with clk_4x_logic
SIGNAL logic_reset	: std_logic -- Goes high to reset counters etc. Sync with clk_4x_logic
SIGNAL overall_trigger	: std_logic --! goes high to load trigger data
SIGNAL overall_veto	: std_logic --! Halts triggers when high
SIGNAL s_i2c_scl_enb	: std_logic
SIGNAL s_i2c_sda_enb	: std_logic
SIGNAL shutter_cnt_i	: std_logic_vector(g_SPILL_COUNTER_WIDTH-1 DOWNTO 0)
SIGNAL shutter_i	: std_logic
SIGNAL spill_cnt_i	: std_logic_vector(g_SPILL_COUNTER_WIDTH-1 DOWNTO 0)
SIGNAL spill_i	: std_logic
SIGNAL strobe_16x_logic	: std_logic --! Pulses one cycle every 4 of 16x clock.
SIGNAL strobe_4x_logic	: std_logic -- one pulse every 4 cycles of clk_4x
SIGNAL trigger_cnt_i	: std_logic_vector(g_IPBUS_WIDTH-1 DOWNTO 0)
SIGNAL trigger_count	: std_logic_vector(g_IPBUS_WIDTH-1 DOWNTO 0)
SIGNAL trigger_times	: t_triggerTimeArray(g_NUM_TRIG_INPUTS-1 DOWNTO 0) -- ! trigger arrival time (w.r.t. logic_strobe)
SIGNAL triggers	: std_logic_vector(g_NUM_TRIG_INPUTS-1 DOWNTO 0)
SIGNAL veto_o	: std_logic --! goes high when one or more DUT are busy

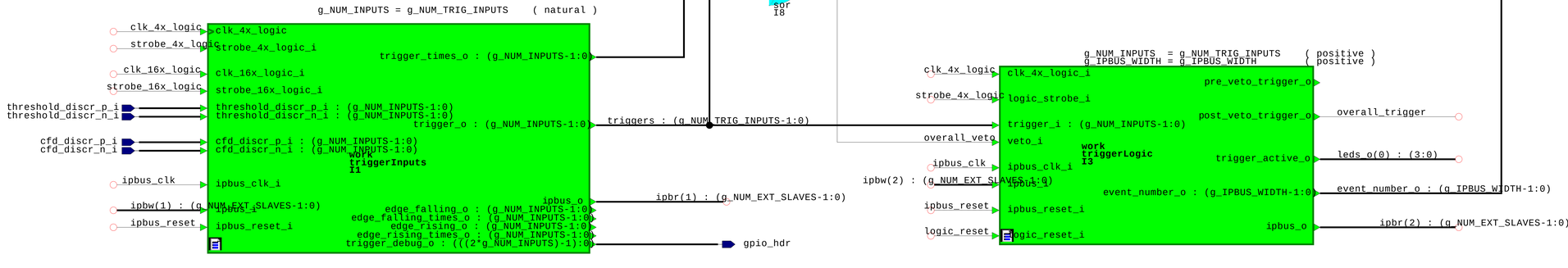
Post User:











University of Bristol High Energy Physics	Project fmc_mTLU Top level of AIDA Mini-TLU (double-height FMC coupled to Xilinx SP60X)
Title top_extphy	
Path: work/top_extphy/struct	
Edited by phdgc on 24 Jan 2014	