Schematic side			FPGA Side				
NET NAME	**FMC_LA**	**J4**	**FMC NAME**	**PACKAGE_PIN**	**VDHL NAME**	**FPGA IN/OUT**	**CONSTRAINT INSTRUCTION**
BEAM_TRIGGER_P<0>	FMC_LA<32>	H37	LA32_P	B1	threshold_discr_p_i[0]	In	set_property PACKAGE_PIN B1 [get_ports {threshold_discr_p_i[0]}]
BEAM_TRIGGER_P<1>	FMC_LA<33>	G36	LA33_P	C4	threshold_discr_p_i[1]	In	set_property PACKAGE_PIN C4 [get_ports {threshold_discr_p_i[1]}]
BEAM_TRIGGER_P<2>	FMC_LA<30>	H34	LA30_P	K2	threshold_discr_p_i[2]	In	set_property PACKAGE_PIN K2 [get_ports {threshold_discr_p_i[2]}]
BEAM_TRIGGER_P<3>	FMC_LA<31>	G33	LA31_P	C6	threshold_discr_p_i[3]	In	set_property PACKAGE_PIN C6 [get_ports {threshold_discr_p_i[3]}]
BEAM_TRIGGER_P<4>	FMC_LA<28>	H31	LA28_P	J4	threshold_discr_p_i[4]	In	set_property PACKAGE_PIN J4 [get_ports {threshold_discr_p_i[4]}]
BEAM_TRIGGER_P<5>	FMC_LA<29>	G30	LA29_P	H1	threshold_discr_p_i[5]	In	set_property PACKAGE_PIN H1 [get_ports {threshold_discr_p_i[5]}]
BEAM_TRIGGER_N<0>	FMC_LA*<32>	H38	LA32_N	A1	threshold_discr_n_i[0]	In	set_property PACKAGE_PIN A1 [get_ports {threshold_discr_n_i[0]}]
BEAM_TRIGGER_N<1>	FMC_LA*<33>	G37	LA33_N	B4	threshold_discr_n_i[1]	In	set_property PACKAGE_PIN B4 [get_ports {threshold_discr_n_i[1]}]
BEAM_TRIGGER_N<2>	FMC_LA*<30>	H35	LA30_N	K1	threshold_discr_n_i[2]	In	set_property PACKAGE_PIN K1 [get_ports {threshold_discr_n_i[2]}]
BEAM_TRIGGER_N<3>	FMC_LA*<31>	G34	LA31_N	C5	threshold_discr_n_i[3]	In	set_property PACKAGE_PIN C5 [get_ports {threshold_discr_n_i[3]}]
BEAM_TRIGGER_N<4>	FMC_LA*<28>	H32	LA28_N	H4	threshold_discr_n_i[4]	In	set_property PACKAGE_PIN H4 [get_ports {threshold_discr_n_i[4]}]
BEAM_TRIGGER_N<5>	FMC_LA*<29>	G31	LA29_N	G1	threshold_discr_n_i[5]	In	set_property PACKAGE_PIN G1 [get_ports {threshold_discr_n_i[5]}]
				P17	enclustra_clk	In	
CLK_TO_FPGA_P	FMC_CLK0_M2C_P	H4	CLK0_M2C_P	T5	sysclk_40_i_p	In	set_property PACKAGE_PIN T5 [get_ports {sysclk_40_i_p}]
CLK_TO_FPGA_N	FMC_CLK0_M2C_N	H5	CLK0_M2C_N	T4	sysclk_40_i_n	In	set_property PACKAGE_PIN T4 [get_ports {sysclk_40_i_n}]
CLK_FROM_FPGA_P	FMC_CLK1_M2C_P	G2	CLK1_M2C_P	E3	sysclk_50_o_p	Out	set_property PACKAGE_PIN E3 [get_ports {sysclk_50_o_p}]
CLK_FROM_FPGA_N	FMC_CLK1_M2C_N	G3	CLK1_M2C_N	D3	sysclk_50_o_n	Out	set_property PACKAGE_PIN D3 [get_ports {sysclk_50_o_n}]
SDA				P18			
SCL				N17			
I2C_RESET_N	FMC_LA<21>	H25	LA21_P	C2	i2c_reset	Out	set_property PACKAGE_PIN C2 [get_ports {i2c_reset}]
GPIO	FMC_LA*<24>	H29	LA24_N	F6	gpio	In/Out	set_property PACKAGE_PIN F6 [get_ports {gpio}]
CLK_GEN_RST_N	FMC_LA*<21>	H26	LA21_N	C1	clk_gen_rst	Out	set_property PACKAGE_PIN C1 [get_ports {clk_gen_rst}]
CLK_GEN_LOL_N	FMC_LA<24>	H28		G6		In	
SFP_LOS_FPGA	FMC_LA*<26>	D27		G2		In	
SFP_TX_FAULT_FPGA	FMC_LA<26>	D26		H2		In	
SFP_TX_DISABLE_FPGA	FMC_LA<25>	G27		H6		Out	
CDR_LOL	FMC_LA*<22>	G25		D7		In	
CDR_LOS	FMC_LA<22>	G24		E7		In	
DATA_FROM_CDR_P	FMC_LA<27>	C26		J3		In	
DATA_FROM_CDR_N	FMC_LA*<27>	C27		J2		In	
DATA_TO_FFD_P	FMC_LA<23>	D23		F1			
DATA_TO_FFD_N	FMC_LA*<23>	D24		E1		Out	
CONT_TO_FPGA<0>	FMC_LA*<0>	G7	LA00_N_CC	P5	cont_i[0]	In	set_property PACKAGE_PIN P5 [get_ports {cont_i[0]}]
CONT_TO_FPGA<1>	FMC_LA*<1>	D9	LA01_N_CC	P3	cont_i[1]	In	set_property PACKAGE_PIN P3 [get_ports {cont_i[1]}]
CONT_TO_FPGA<2>	FMC_LA*<2>	H8	LA02_N	N6	cont_i[2]	In	set_property PACKAGE_PIN N6 [get_ports {cont_i[2]}]
CONT_TO_FPGA<3>	FMC_LA*<3>	G10	LA03_N	L5	cont_i[3]	In	set_property PACKAGE_PIN L5 [get_ports {cont_i[3]}]
SPARE_TO_FPGA<0>	FMC_LA*<4>	H11	LA04_N	M1	spare_i[0]	In	set_property PACKAGE_PIN M1 [get_ports {spare_i[0]}]

SPARE_TO_FPGA<1>	FMC_LA*<5>	D12	LA05_N	N4	spare_i[1]	In	set_property PACKAGE_PIN N4 [get_ports {spare_i[1]}]
SPARE_TO_FPGA<2>	FMC_LA*<6>	C11	LA06_N	N1	spare_i[2]	In	set_property PACKAGE_PIN N1 [get_ports {spare_i[2]}]
SPARE_TO_FPGA<3>	FMC_LA*<7>	H14	LA07_N	M2	spare_i[3]	In	set_property PACKAGE_PIN M2 [get_ports {spare_i[3]}]
TRIG_TO_FPGA<0>	FMC_LA*<8>	G13	LA08_N	R5	triggers_i[0]	In	set_property PACKAGE_PIN R5 [get_ports {triggers_i[0]}]
TRIG_TO_FPGA<1>	FMC_LA*<9>	D15	LA09_N	R2	triggers_i[1]	In	set_property PACKAGE_PIN R2 [get_ports {triggers_i[1]}]
TRIG_TO_FPGA<2>	FMC_LA*<10>	C15	LA10_N	T1	triggers_i[2]	In	set_property PACKAGE_PIN T1 [get_ports {triggers_i[2]}]
TRIG_TO_FPGA<3>	FMC_LA*<11>	H17	LA11_N	V1	triggers_i[3]	In	set_property PACKAGE_PIN V1 [get_ports {triggers_i[3]}]
BUSY_TO_FPGA<0>	FMC_LA*<12>	G16	LA12_N	T6	busy_i[0]	In	set_property PACKAGE_PIN T6 [get_ports {busy_i[0]}]
BUSY_TO_FPGA<1>	FMC_LA*<13>	D18	LA13_N	U3	busy_i[1]	In	set_property PACKAGE_PIN U3 [get_ports {busy_i[1]}]
BUSY_TO_FPGA<3>	FMC_LA*<14>	C19	LA14_N	T8	busy_i[2]	In	set_property PACKAGE_PIN T8 [get_ports {busy_i[2]}]
BUSY_TO_FPGA<2>	FMC_LA*<15>	H20	LA15_N	L4	busy_i[3]	In	set_property PACKAGE_PIN L4 [get_ports {busy_i[3]}]
DUT_CLK_TO_FPGA<0>	FMC_LA*<16>	G19	LA16_N	L3	dut_clk_i[0]	In	set_property PACKAGE_PIN L3 [get_ports {dut_clk_i[0]}]
DUT_CLK_TO_FPGA<1>	FMC_LA*<17>	D21	LA17_N_CC	F3	dut_clk_i[1]	In	set_property PACKAGE_PIN F3 [get_ports {dut_clk_i[1]}]
DUT_CLK_TO_FPGA<2>	FMC_LA*<18>	C23	LA18_N_CC	D2	dut_clk_i[2]	In	set_property PACKAGE_PIN D2 [get_ports {dut_clk_i[2]}]
DUT_CLK_TO_FPGA<3>	FMC_LA*<19>	H23	LA19_N	G3	dut_clk_i[3]	In	set_property PACKAGE_PIN G3 [get_ports {dut_clk_i[3]}]
CONT_FROM_FPGA<0>	FMC_LA<0>	G6	LA00_P_CC	N5	cont_o[0]	Out	set_property PACKAGE_PIN N5 [get_ports {cont_o[0]}]
CONT_FROM_FPGA<1>	FMC_LA<1>	D8	LA01_P_CC	P4	cont_o[1]	Out	set_property PACKAGE_PIN P4 [get_ports {cont_o[1]}]
CONT_FROM_FPGA<2>	FMC_LA<2>	H7	LA02_P	M6	cont_o[2]	Out	set_property PACKAGE_PIN M6 [get_ports {cont_o[2]}]
CONT_FROM_FPGA<3>	FMC_LA<3>	G9	LA03_P	L6	cont_o[3]	Out	set_property PACKAGE_PIN L6 [get_ports {cont_o[3]}]
SPARE_FROM_FPGA<0>	FMC_LA<4>	H10	LA04_P	L1	spare_o[0]	Out	set_property PACKAGE_PIN L1 [get_ports {spare_o[0]}]
SPARE_FROM_FPGA<1>	FMC_LA<5>	D11	LA05_P	M4	spare_o[1]	Out	set_property PACKAGE_PIN M4 [get_ports {spare_o[1]}]
SPARE_FROM_FPGA<2>	FMC_LA<6>	C10	LA06_P	N2	spare_o[2]	Out	set_property PACKAGE_PIN N2 [get_ports {spare_o[2]}]
SPARE_FROM_FPGA<3>	FMC_LA<7>	H13	LA07_P	M3	spare_o[3]	Out	set_property PACKAGE_PIN M3 [get_ports {spare_o[3]}]
TRIG_FROM_FPGA<0>	FMC_LA<8>	G12	LA08_P	R6	triggers_o[0]	Out	set_property PACKAGE_PIN R6 [get_ports {triggers_o[0]}]
TRIG_FROM_FPGA<1>	FMC_LA<9>	D14	LA09_P	P2	triggers_o[1]	Out	set_property PACKAGE_PIN P2 [get_ports {triggers_o[1]}]
TRIG_FROM_FPGA<2>	FMC_LA<10>	C14	LA10_P	R1	triggers_o[2]	Out	set_property PACKAGE_PIN R1 [get_ports {triggers_o[2]}]
TRIG_FROM_FPGA<3>	FMC_LA<11>	H16	LA11_P	U1	triggers_o[3]	Out	set_property PACKAGE_PIN U1 [get_ports {triggers_o[3]}]
BUSY_FROM_FPGA<0>	FMC_LA<12>	G15	LA12_P	R7	busy_o[0]	Out	set_property PACKAGE_PIN R7 [get_ports {busy_o[0]}]
BUSY_FROM_FPGA<1>	FMC_LA<13>	D17	LA13_P	U4	busy_o[1]	Out	set_property PACKAGE_PIN U4 [get_ports {busy_o[1]}]
BUSY_FROM_FPGA<2>	FMC_LA<14>	C18	LA14_P	R8	busy_o[2]	Out	set_property PACKAGE_PIN R8 [get_ports {busy_o[2]}]
BUSY_FROM_FPGA<3>	FMC_LA<15>	H19	LA15_P	K5	busy_o[3]	Out	set_property PACKAGE_PIN K5 [get_ports {busy_o[3]}]
DUT_CLK_FROM_FPGA<0>	FMC_LA<16>	G18	LA16_P	K3	dut_clk_o[0]	Out	set_property PACKAGE_PIN K3 [get_ports {dut_clk_o[0]}]
DUT_CLK_FROM_FPGA<1>	FMC_LA<17>	D20	LA17_P_CC	F4	dut_clk_o[1]	Out	set_property PACKAGE_PIN F4 [get_ports {dut_clk_o[1]}]
DUT_CLK_FROM_FPGA<2>	FMC_LA<18>	C22	LA18_P_CC	E2	dut_clk_o[2]	Out	set_property PACKAGE_PIN E2 [get_ports {dut_clk_o[2]}]
DUT_CLK_FROM_FPGA<3>	FMC_LA<19>	H22	LA19_P	G4	dut_clk_o[3]	Out	set_property PACKAGE_PIN G4 [get_ports {dut_clk_o[3]}]