This block takes as input the N triggers from the threshold discriminators and provides, for each of them a fine timing of when the trigger occurs.

It has an IPBus block to provide configuration.

Inputs:

Clk\_4x\_logic

Clk\_16x\_logic\_i

Ipbus\_clk\_i

Ipbus\_i[ipbus\_addr] [31:0]

Ipbus\_i[ipbus\_strobe]

Ipbus\_i[ipb\_wdata] [31:0]

Ipbus\_i[ipb\_write]

Ipbus\_reset\_i

Reset\_i

Strobe\_4x\_logic\_i

Strobe\_16x\_logic\_i

Threshold\_discr\_n\_i[N-1:0]

Threshold\_discr\_p\_i[N-1:0]

Outpus:

Edge\_falling\_o[N-1:0]

Edge\_falling\_times\_o[0][4:0]

Edge\_falling\_times\_o[1][4:0]

Edge\_falling\_times\_o[…][4:0]

Edge\_falling\_times\_o[N-1][4:0]

Edge\_rising\_o[N-1:0]

Edge\_rising\_times\_o[0][4:0]

Edge\_rising\_times\_o[1][4:0]

Edge\_rising\_times\_o[…][4:0]

Edge\_rising\_times\_o[N-1][4:0]

Ipbus\_o[ipb\_ack]

Ipbus\_o[ipb\_err]

Ipbus\_o[ipb\_data][31:0]

Trigger\_o[N-1:0]

Trigger\_times\_o[0][4:0]

Trigger\_times\_o[1][4:0]

Trigger\_times\_o[…][4:0]

Trigger\_times\_o[N-1][4:0]

The