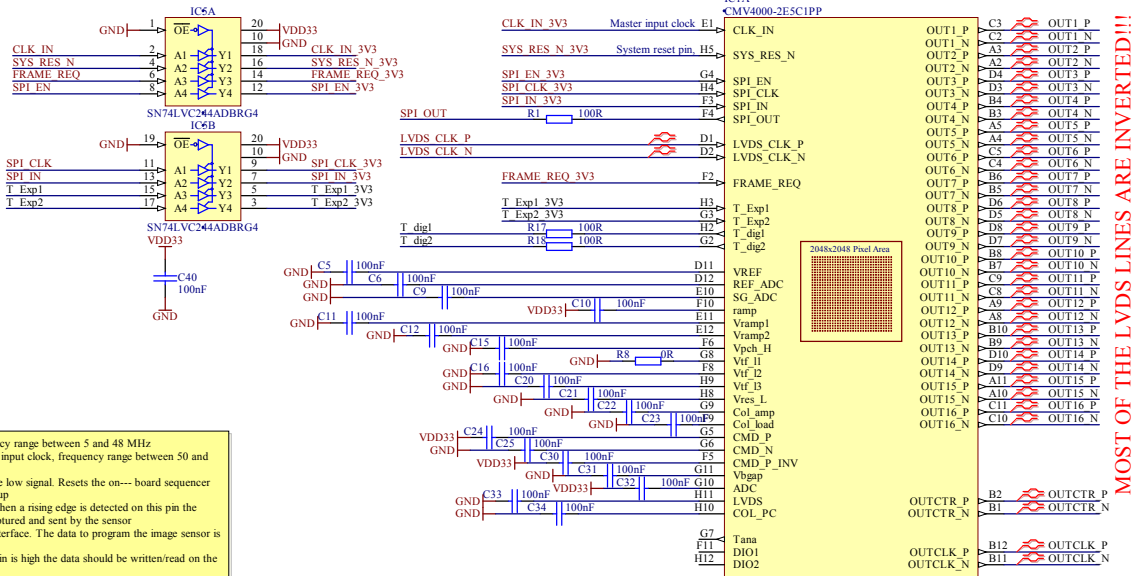


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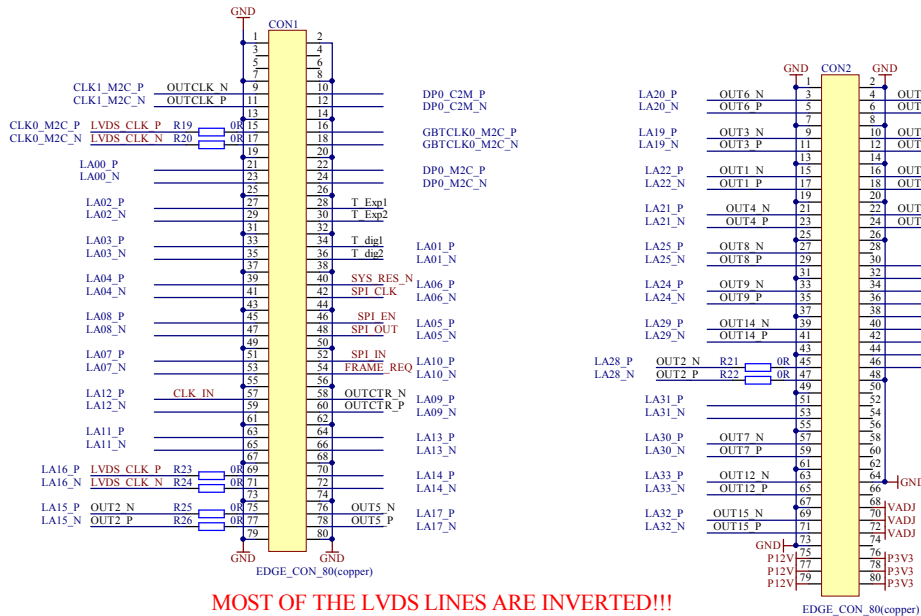
B1 ... B4
screw holes for attaching the
FMC to the carrier board.

Project/Equipment		FMC_DIO_16ch_LVDS		Designer			
Document		 Creotech Instruments S.A.		Drawn by			
CTI				Check by			
FMC Connector Fanout				Last Mod.		2014-10-29	
				File		fmc_connector SchDoc	
				Print Date		2014-10-29 16:02:46	
		Creotech Instruments S.A.		Sheet		4 of 5	
				A3		-	



CLK_IN Master input clock, frequency range between 5 and 48 MHz
 LVDS_CLK_N/P High speed LVDS input clock, frequency range between 50 and 480 MHz
 SYS_RES_N System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up
 FRAME_REQ Frame request pin. When a rising edge is detected on this pin the programmed number of frames is captured and sent by the sensor
 SPI_IN Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
 SPI_EN SPI enable pin. When this pin is high the data should be written/read on the SPI
 SPI_CLK SPI clock. This is the clock on which the SPI runs (max 48MHz)
 T_EXP1 Input pin which can be used to program the exposure time externally.
 Optional
 T_EXP2 Input pin which can be used to program the exposure time externally in interleaved high dynamic range mode. Optional

MOST OF THE LVDS LINES ARE INVERTED!!!



MOST OF THE LVDS LINES ARE INVERTED!!!

Supply name	Typical value	Range	Current nominal	Current peak
VDD20	2.0V	1.6V~2.1V	200mA	1A
VDD33	3.3V	3V~3.5V	100mA	0.5A
VDDpix	3.0V	2.3V~3.6V	20mA	0.6A
Vres_h	3.3V	3.0V~3.6V	NA	0.5A

