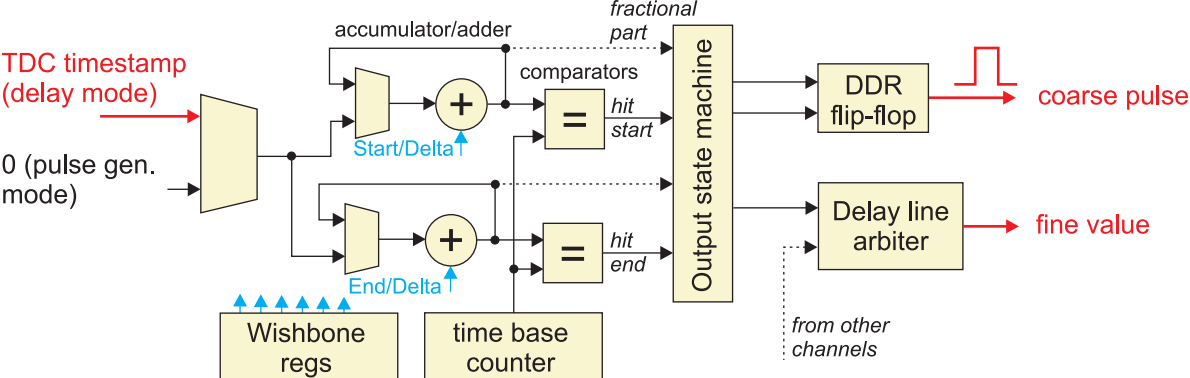
accumulator/adder
fractional part
TDC timestamp (delay mode)
comparators
hit start
Start/Delta
0 (pulse gen. mode)
Output state machine
DDR flip-flop
coarse pulse
Delay line arbiter
fine value
hit end
End/Delta
Wishbone regs
time base counter
from other channels