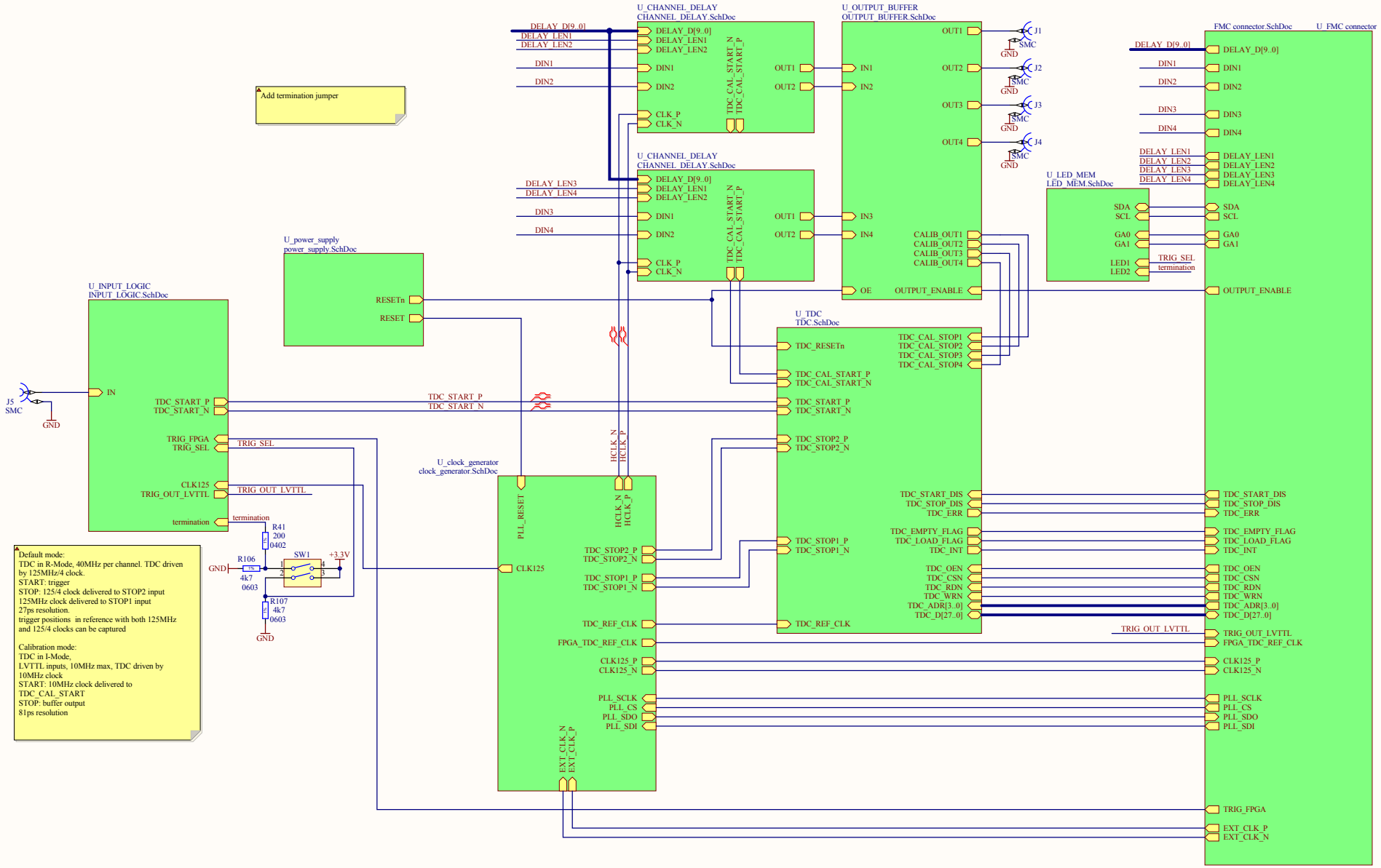
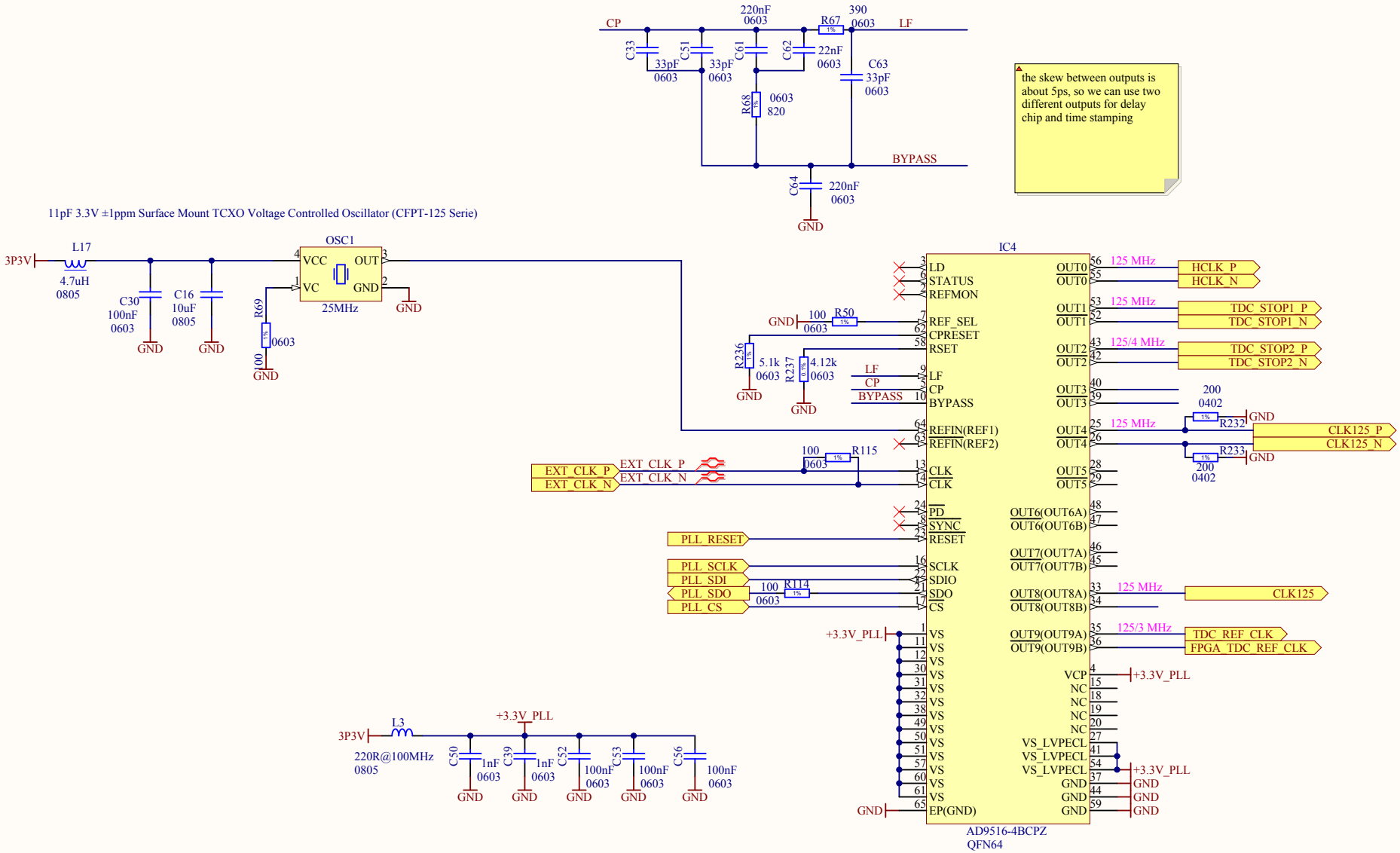
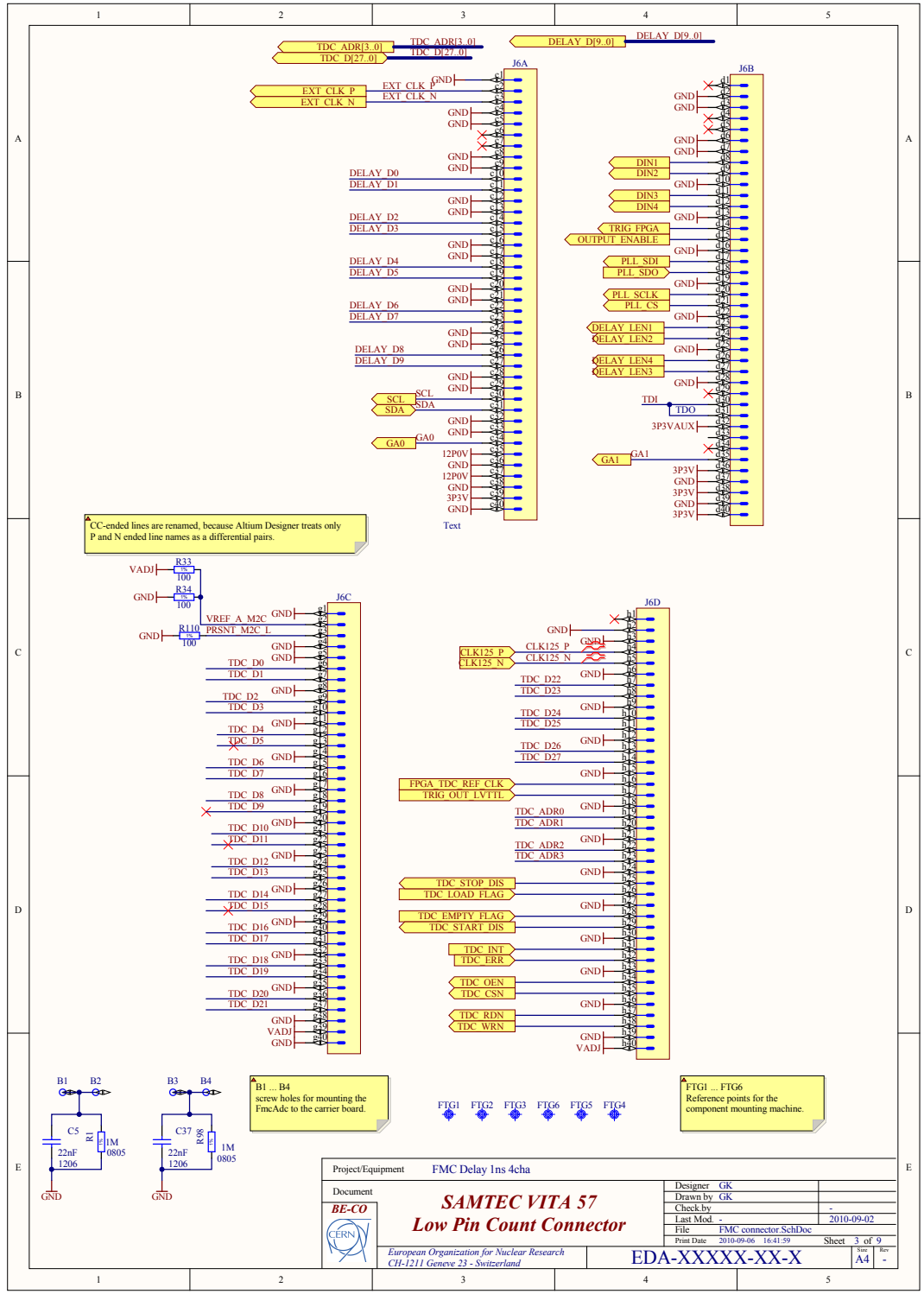
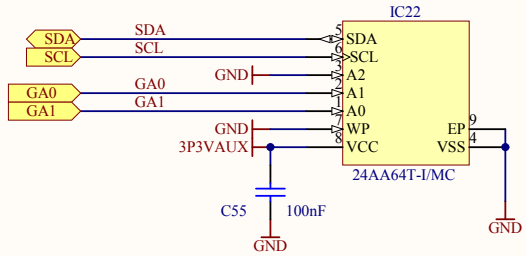
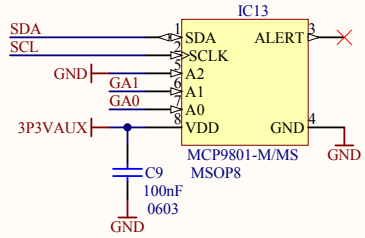

U_CHANNEL_DELAY
CHANNEL_DELAY.SchDoc
U_OUTPUT_BUFFER
OUTPUT_BUFFER.SchDoc
FMC connector.SchDoc
U_FMC connector
U_CHANNEL_DELAY
CHANNEL_DELAY.SchDoc
U_LED_MEM
LED_MEM.SchDoc
U_power_supply
power_supply.SchDoc
U_INPUT_LOGIC
INPUT_LOGIC.SchDoc
U_TDC
TDC.SchDoc
U_clock_generator
clock_generator.SchDoc
Add termination jumper
Default mode:
TDC in R-Mode, 40MHz per channel. TDC driven by 125MHz/4 clock.
START: trigger
STOP: 125/4 clock delivered to STOP2 input
125MHz clock delivered to STOP1 input
27ps resolution.
trigger positions in reference with both 125MHz and 125/4 clocks can be captured
Calibration mode:
TDC in I-Mode,
LVTTL inputs, 10MHz max, TDC driven by 10MHz clock
START: 10MHz clock delivered to TDC_CAL_START
STOP: buffer output
81ps resolution
Project/Equipment
FMC Delay 1ns 4cha
Document
FMC delay top
BE-CO
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by GK
Check.by -
Last Mod. -
2010-09-02
File FMC_Delay_1ns_4Cha.SchDoc
Print Date 2010-09-06 16:41:59
Sheet 1 of 9
EDA-XXXXX-VX-X
Size A3
Rev -

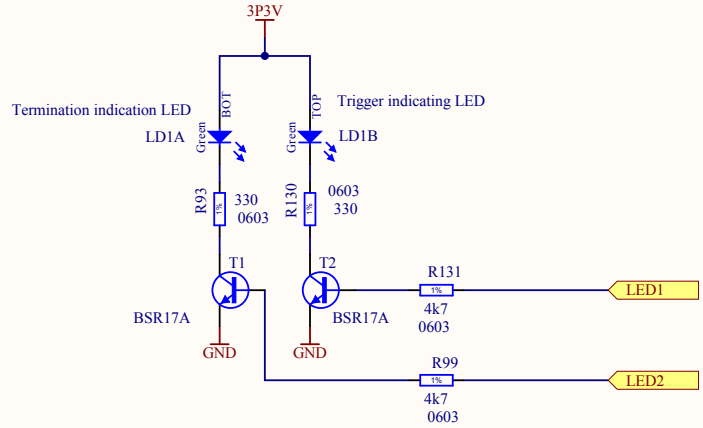


Project/Equipment	FMC Delay 1ns 4cha		
Document	ADC clock generator	Designer GK	
		Drawn by	
		Check.by -	-
		Last Mod. -	2010-09-02
		File clock_generator.SchDoc	
		Print Date 2010-09-06 16:41:59	Sheet 2 of 9
BE-CO	European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-VX-X	Size A4 / Rev -

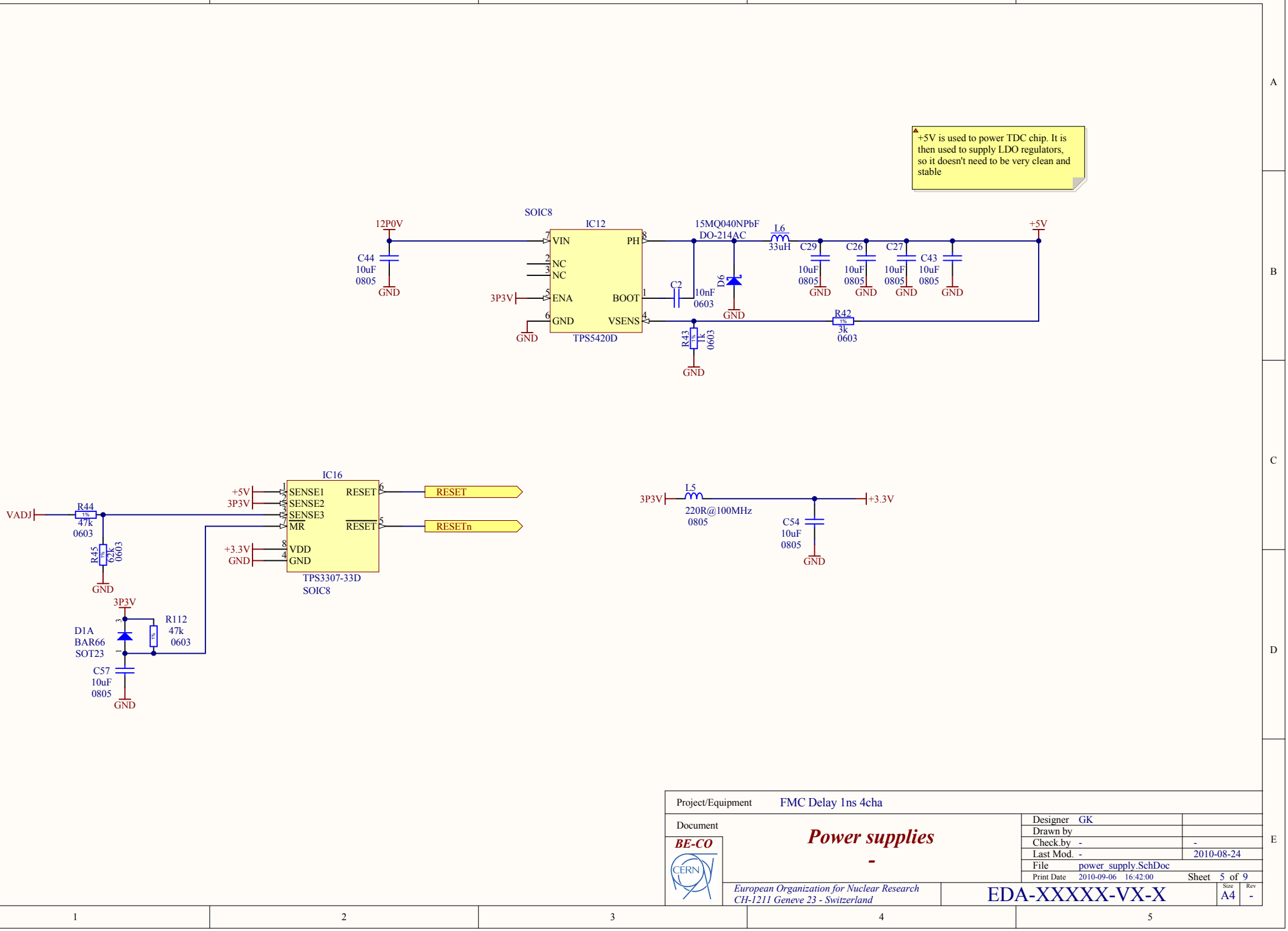

TDC_ADR[3..0]
TDC_D[27..0]
DELAY_D[9..0]
J6A
J6B
J6C
J6D
EXT_CLK_P
EXT_CLK_N
DELAY_D0
DELAY_D1
DELAY_D2
DELAY_D3
DELAY_D4
DELAY_D5
DELAY_D6
DELAY_D7
DELAY_D8
DELAY_D9
SCL
SDA
GA0
GA1
12P0V
3P3V
GND
DIN1
DIN2
DIN3
DIN4
TRIG_FPGA
OUTPUT_ENABLE
PLL_SDI
PLL_SDO
PLL_SCLK
PLL_CS
DELAY_LEN1
DELAY_LEN2
DELAY_LEN4
DELAY_LEN3
TDI
TDO
3P3VAUX
Text
CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.
VADJ
R33
100
R34
100
VREF_A_M2C
R110
PRSNT_M2C_L
TDC_D0
TDC_D1
TDC_D2
TDC_D3
TDC_D4
TDC_D5
TDC_D6
TDC_D7
TDC_D8
TDC_D9
TDC_D10
TDC_D11
TDC_D12
TDC_D13
TDC_D14
TDC_D15
TDC_D16
TDC_D17
TDC_D18
TDC_D19
TDC_D20
TDC_D21
CLK125_P
CLK125_N
TDC_D22
TDC_D23
TDC_D24
TDC_D25
TDC_D26
TDC_D27
FPGA_TDC_REF_CLK
TRIG_OUT_LVTTL
TDC_ADR0
TDC_ADR1
TDC_ADR2
TDC_ADR3
TDC_STOP_DIS
TDC_LOAD_FLAG
TDC_EMPTY_FLAG
TDC_START_DIS
TDC_INT
TDC_ERR
TDC_OEN
TDC_CSN
TDC_RDN
TDC_WRN
B1
B2
B3
B4
C5
22nF
1206
R1
1M
0805
C37
22nF
1206
R98
1M
0805
B1 ... B4
screw holes for mounting the FmcAdc to the carrier board.
FTG1
FTG2
FTG3
FTG6
FTG5
FTG4
FTG1 ... FTG6
Reference points for the component mounting machine.
Project/Equipment
FMC Delay 1ns 4cha
Document
SAMTEC VITA 57
Low Pin Count Connector
BE-CO
CERN
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by GK
Check by -
Last Mod. - 2010-09-02
File FMC_connector.SchDoc
Print Date 2010-09-06 16:41:59
Sheet 3 of 9
EDA-XXXXX-XX-X
Size A4
Rev -

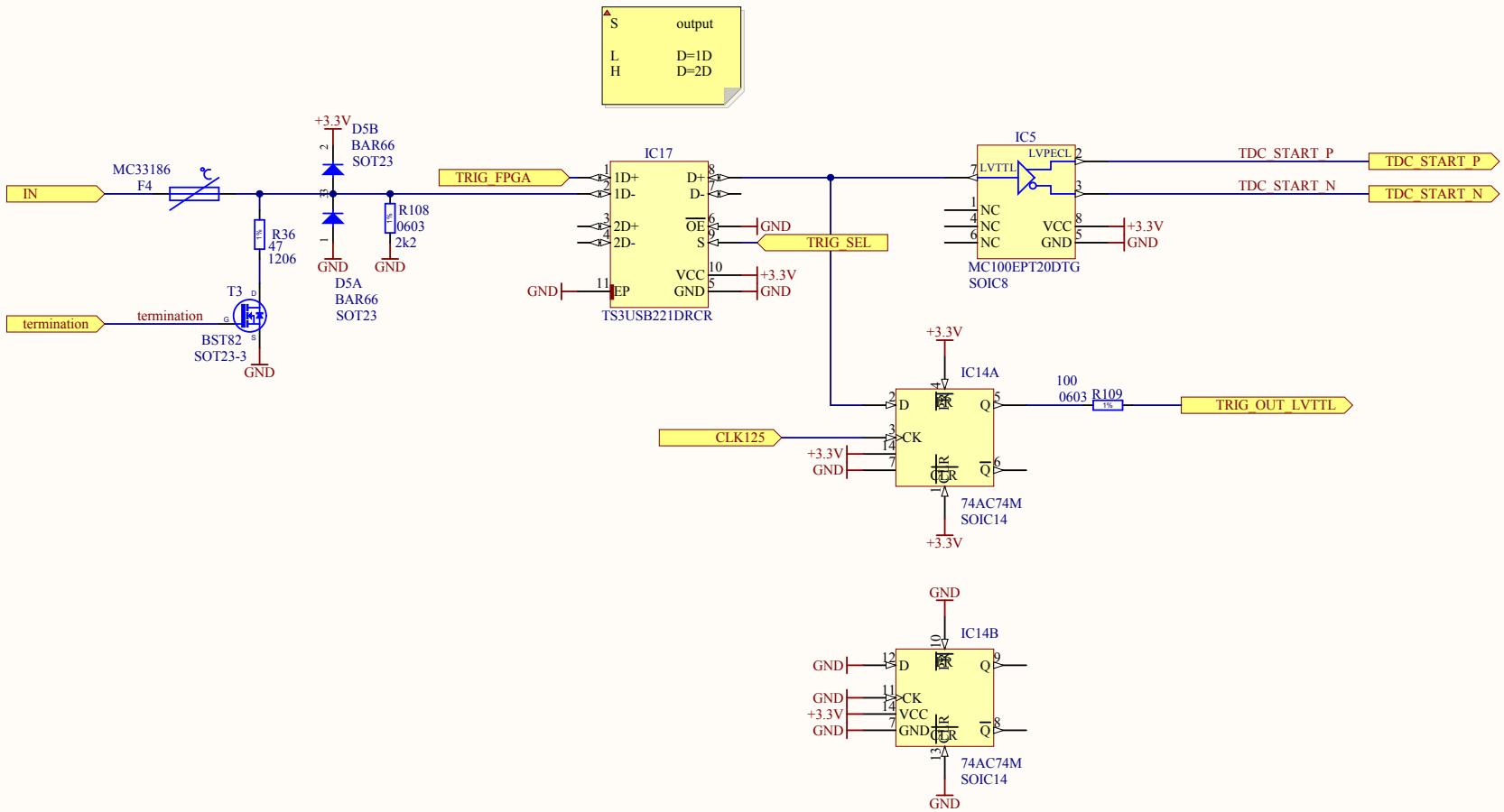




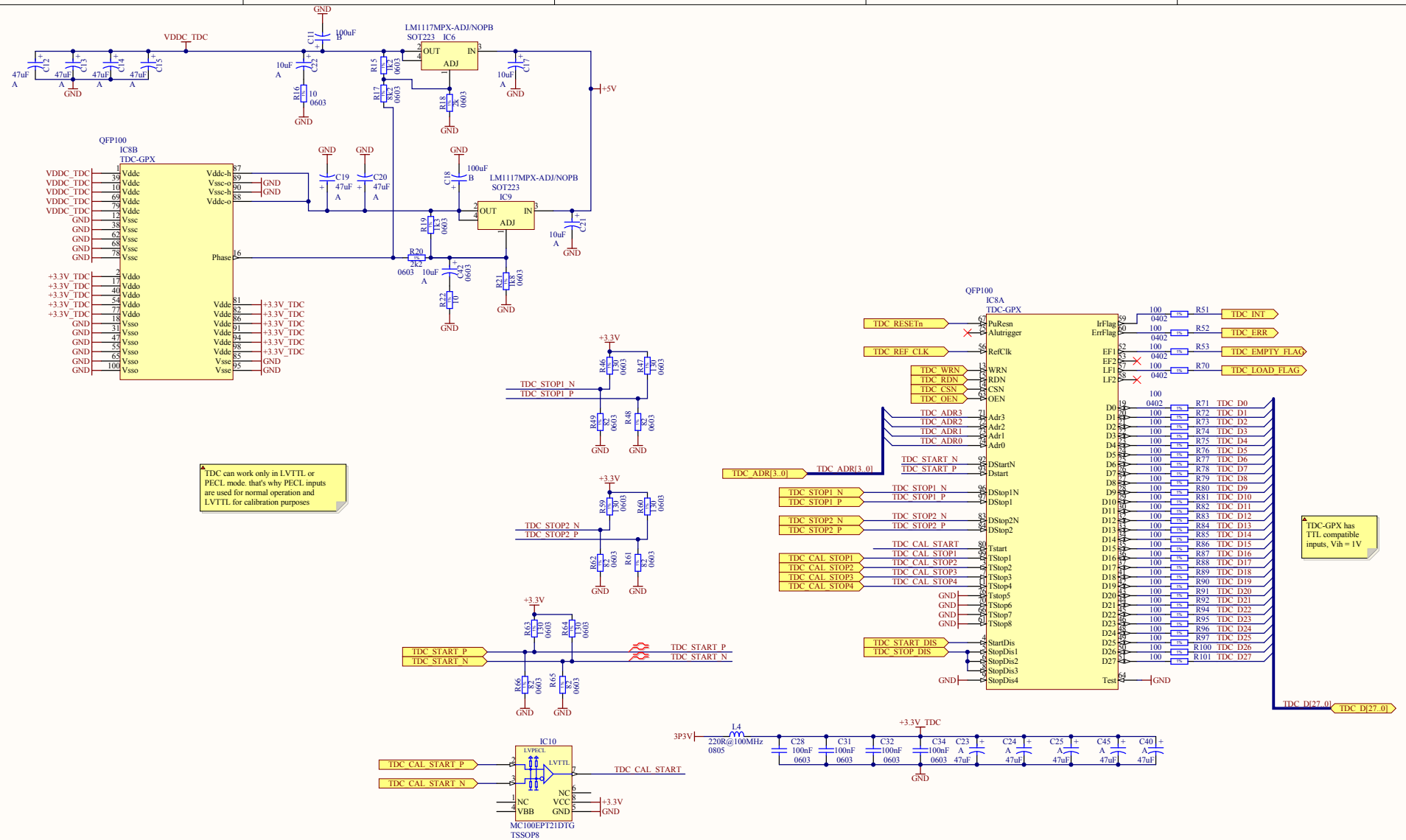


Project/Equipment	FMC Delay 1ns 4cha		
Document	**LED and MEMORY**	Designer GK	
		Drawn by GK	XX/XX/XXXX
		Check.by -	-
		Last Mod. -	2010-08-22
		File LED_MEM.SchDoc	
		Print Date 2010-09-06 16:41:59	Sheet 4 of 9
BE-CO	*European Organization for Nuclear Research* *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -

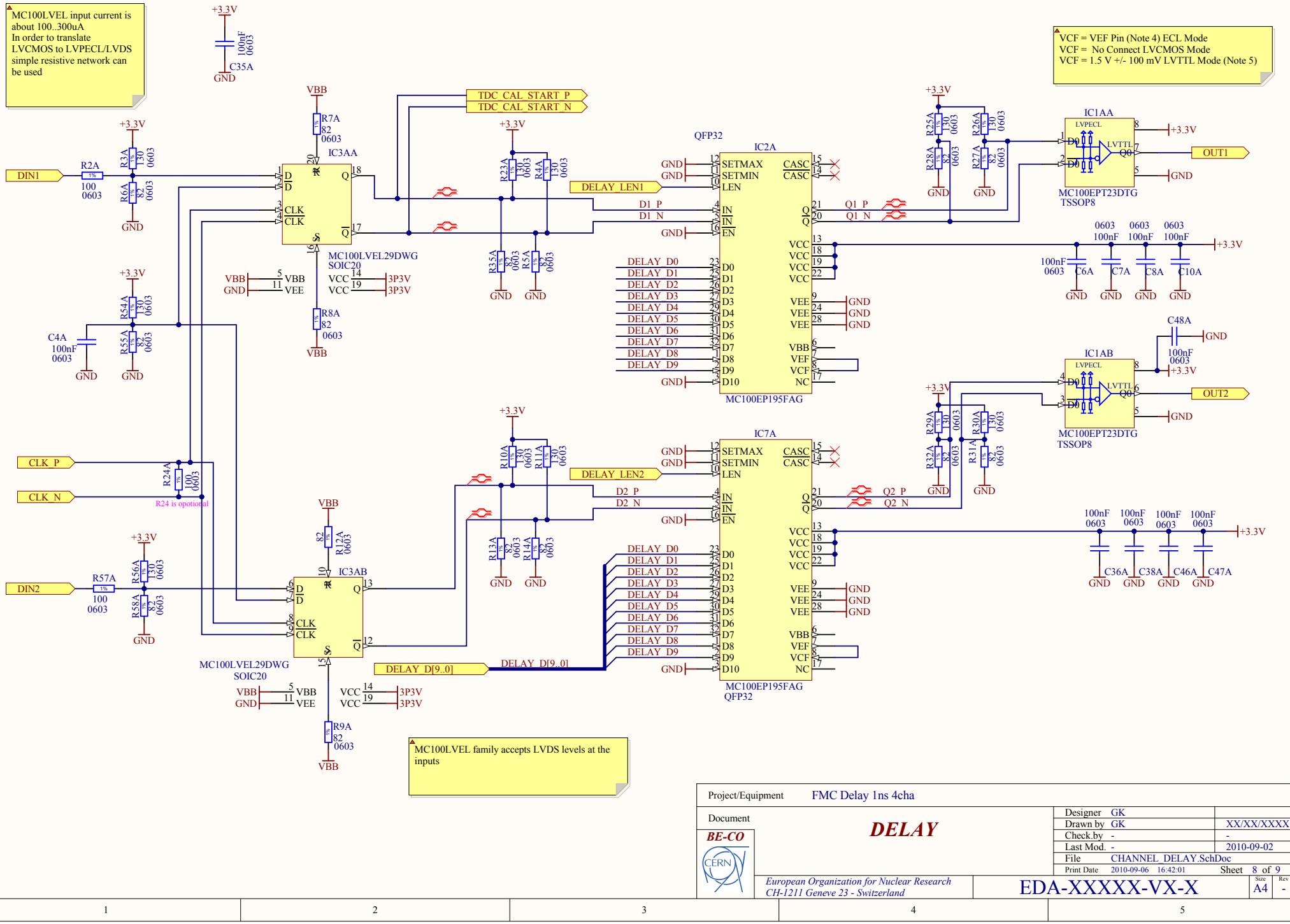

+5V is used to power TDC chip. It is then used to supply LDO regulators, so it doesn't need to be very clean and stable
SOIC8
IC12
12P0V
C44
10uF
0805
GND
VIN
NC
NC
ENA
GND
PH
BOOT
VSENS
TPS5420D
3P3V
C2
10nF
0603
15MQ040NPbF
DO-214AC
D6
L6
33uH
C29
C26
C27
C43
10uF
0805
+5V
R42
3k
0603
R43
1k
0603
IC16
VADJ
R44
47k
0603
R45
62k
0603
+5V
3P3V
SENSE1
SENSE2
SENSE3
MR
RESET
RESETn
+3.3V
VDD
TPS3307-33D
SOIC8
D1A
BAR66
SOT23
R112
47k
0603
C57
10uF
0805
L5
220R@100MHz
0805
C54
10uF
0805
+3.3V
Project/Equipment
FMC Delay 1ns 4cha
Document
Power supplies
-
BE-CO
CERN
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by
Check.by -
Last Mod. -
2010-08-24
File power_supply.SchDoc
Print Date 2010-09-06 16:42:00
Sheet 5 of 9
EDA-XXXXX-VX-X
Size A4
Rev -

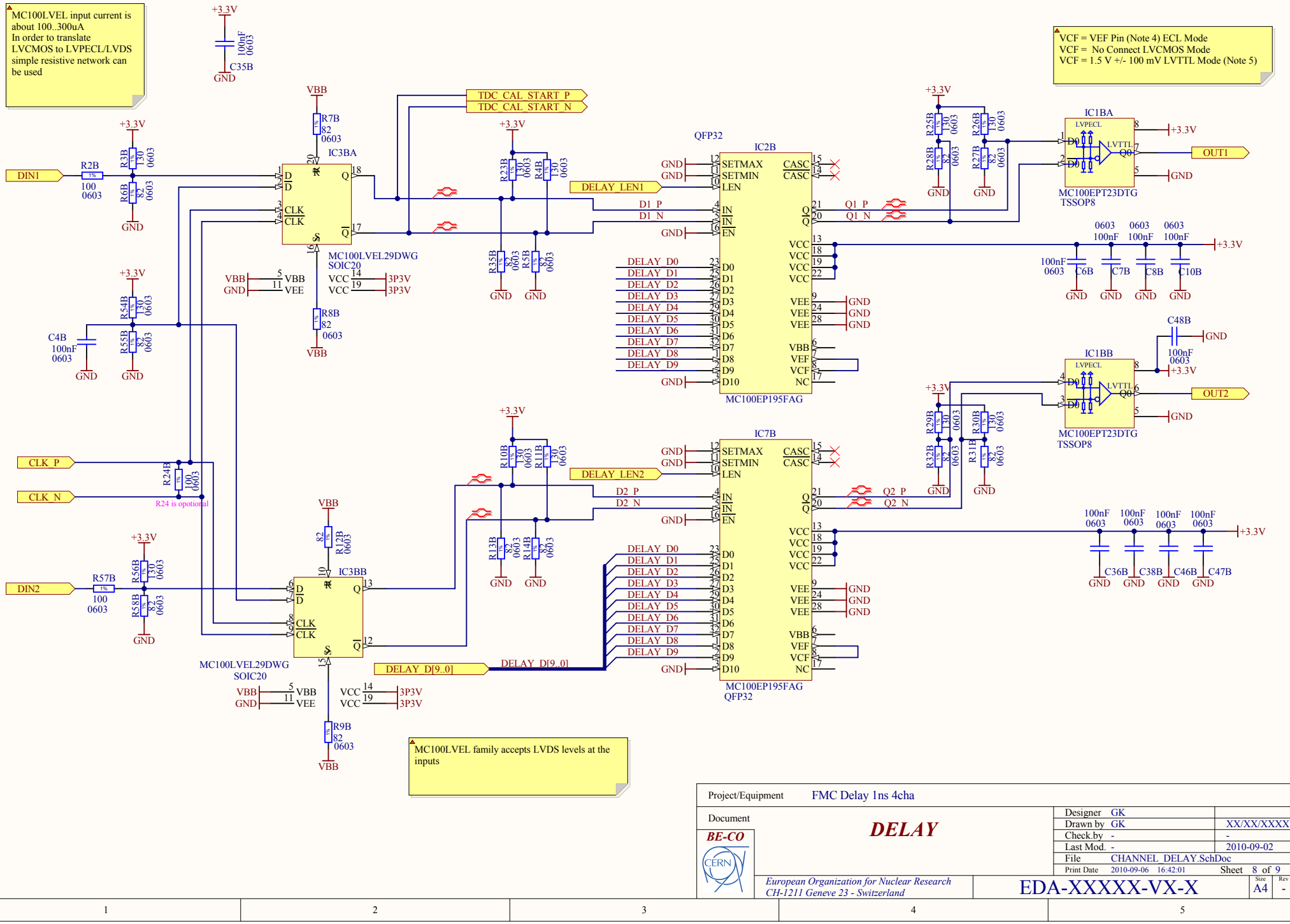


Project/Equipment	FMC Delay 1ns 4cha		
Document	**Input logic**	Designer GK	
	-	Drawn by	
		Check.by -	-
		Last Mod. -	2010-09-02
		File INPUT_LOGIC.SchDoc	
		Print Date 2010-09-06 16:42:00	Sheet 6 of 9
BE-CO	*European Organization for Nuclear Research* *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	TDC	Designer GK	
BE-CO		Drawn by GK	XX/XX/XXXX
		Check.by -	-
		Last Mod. -	2010-09-02
		File TDC.SchDoc	
		Print Date 2010-09-06 16:42:00	Sheet 7 of 9
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	Size A3 / Rev -


MC100LVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used
VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV LVTTL Mode (Note 5)
TDC_CAL_START_P
TDC_CAL_START_N
DIN1
DIN2
CLK_P
CLK_N
R24 is optional
DELAY_LEN1
DELAY_LEN2
DELAY_D[9..0]
D1_P
D1_N
D2_P
D2_N
Q1_P
Q1_N
Q2_P
Q2_N
OUT1
OUT2
QFP32
IC2A
IC7A
IC3AA
IC3AB
IC1AA
IC1AB
MC100EP195FAG
MC100LVEL29DWG
SOIC20
MC100EPT23DTG
TSSOP8
LVPECL
LVTTL
MC100LVEL family accepts LVDS levels at the inputs
Project/Equipment
FMC Delay 1ns 4cha
Document
DELAY
BE-CO
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by GK
Check.by -
Last Mod. -
File CHANNEL_DELAY.SchDoc
Print Date 2010-09-06 16:42:01
Sheet 8 of 9
EDA-XXXXX-VX-X
Size A4
Rev -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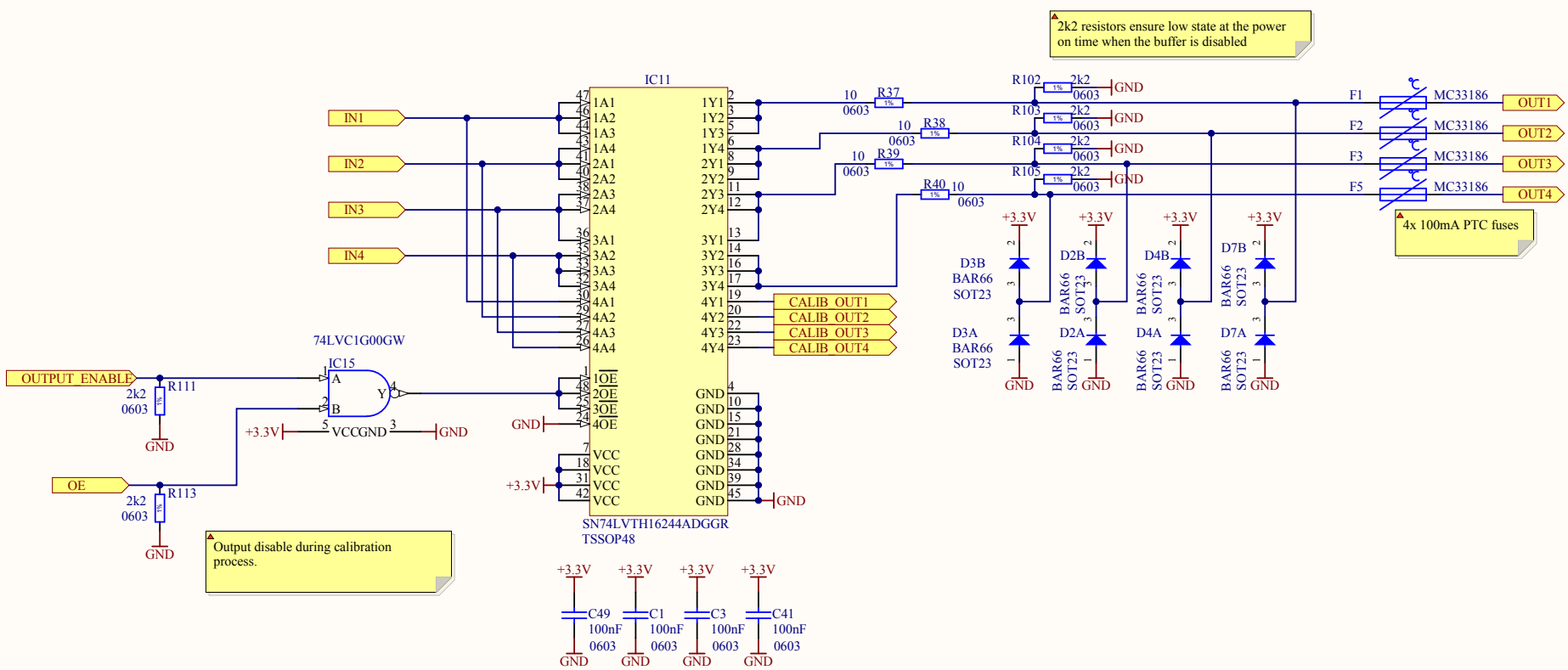
VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV LVTTL Mode (Note 5)
TDC_CAL_START_P
TDC_CAL_START_N
DIN1
DIN2
CLK_P
CLK_N
R24 is optional
DELAY_LEN1
DELAY_LEN2
DELAY_D[9..0]
D1_P
D1_N
D2_P
D2_N
Q1_P
Q1_N
Q2_P
Q2_N
OUT1
OUT2
IC2B
IC7B
QFP32
MC100EP195FAG
IC3BA
IC3BB
MC100LVEL29DWG
SOIC20
IC1BA
IC1BB
MC100EPT23DTG
TSSOP8
LVPECL
LVTTL
MC100LVEL family accepts LVDS levels at the inputs
Project/Equipment
FMC Delay 1ns 4cha
Document
DELAY
BE-CO
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by GK
XX/XX/XXXX
Check.by -
Last Mod. -
2010-09-02
File CHANNEL_DELAY.SchDoc
Print Date 2010-09-06 16:42:01
Sheet 8 of 9
EDA-XXXXX-VX-X
Size A4
Rev -


2k2 resistors ensure low state at the power on time when the buffer is disabled
IC11
IN1
IN2
IN3
IN4
CALIB_OUT1
CALIB_OUT2
CALIB_OUT3
CALIB_OUT4
SN74LVTH16244ADGGR
TSSOP48
74LVC1G00GW
IC15
OUTPUT_ENABLE
OE
R111
R113
2k2
0603
Output disable during calibration process.
R37
R38
R39
R40
10
0603
R102
R103
R104
R105
2k2
0603
D3B
D3A
D2B
D2A
D4B
D4A
D7B
D7A
BAR66
SOT23
F1
F2
F3
F5
MC33186
OUT1
OUT2
OUT3
OUT4
4x 100mA PTC fuses
C49
C1
C3
C41
100nF
0603
+3.3V
GND
VCC
VCCGND
Project/Equipment
FMC Delay 1ns 4cha
Document
Output buffer
BE-CO
Designer GK
Drawn by GK
Check.by -
Last Mod. -
File OUTPUT_BUFFER.SchDoc
Print Date 2010-09-06 16:42:02
Sheet 9 of 9
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
EDA-XXXXX-VX-X
Size A4
Rev -