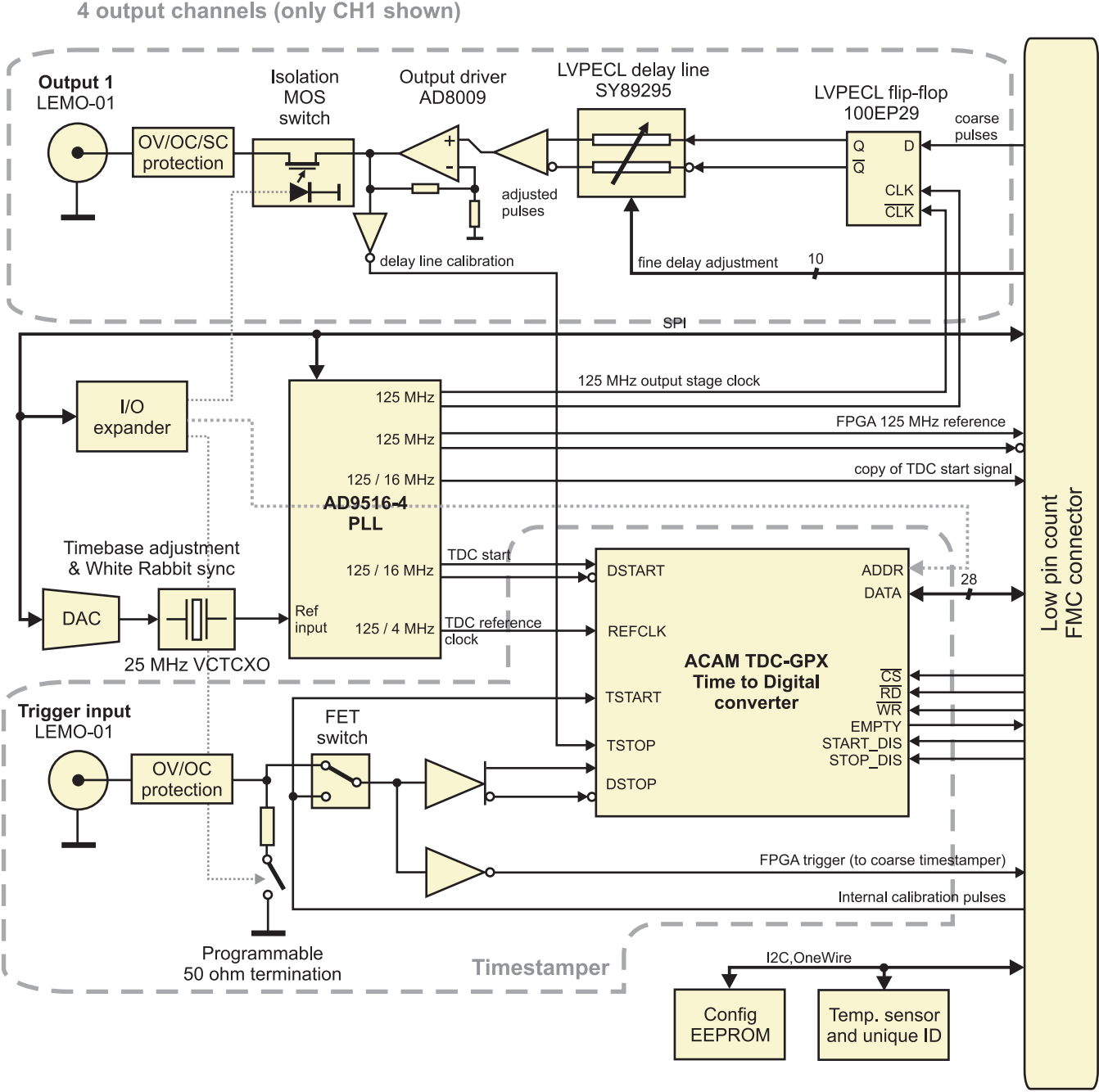
4 output channels (only CH1 shown)
Output 1
LEMO-01
OV/OC/SC protection
Isolation MOS switch
Output driver AD8009
LVPECL delay line SY89295
LVPECL flip-flop 100EP29
coarse pulses
Q
D
CLK
adjusted pulses
delay line calibration
fine delay adjustment
10
SPI
I/O expander
125 MHz
125 MHz
125 / 16 MHz
AD9516-4 PLL
125 / 16 MHz
Ref input
125 / 4 MHz
125 MHz output stage clock
FPGA 125 MHz reference
copy of TDC start signal
Timebase adjustment & White Rabbit sync
DAC
25 MHz VCTCXO
TDC start
TDC reference clock
DSTART
REFCLK
TSTART
TSTOP
DSTOP
ACAM TDC-GPX Time to Digital converter
ADDR
DATA
28
CS
RD
WR
EMPTY
START_DIS
STOP_DIS
Trigger input
LEMO-01
OV/OC protection
FET switch
FPGA trigger (to coarse timestamper)
Internal calibration pulses
Programmable 50 ohm termination
Timestamper
I2C,OneWire
Config EEPROM
Temp. sensor and unique ID
Low pin count FMC connector