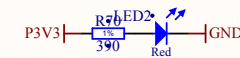


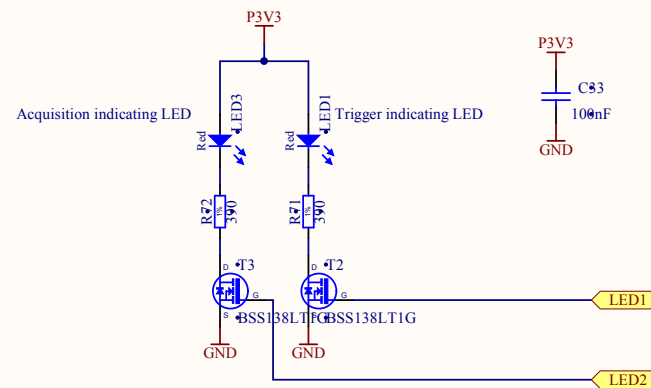
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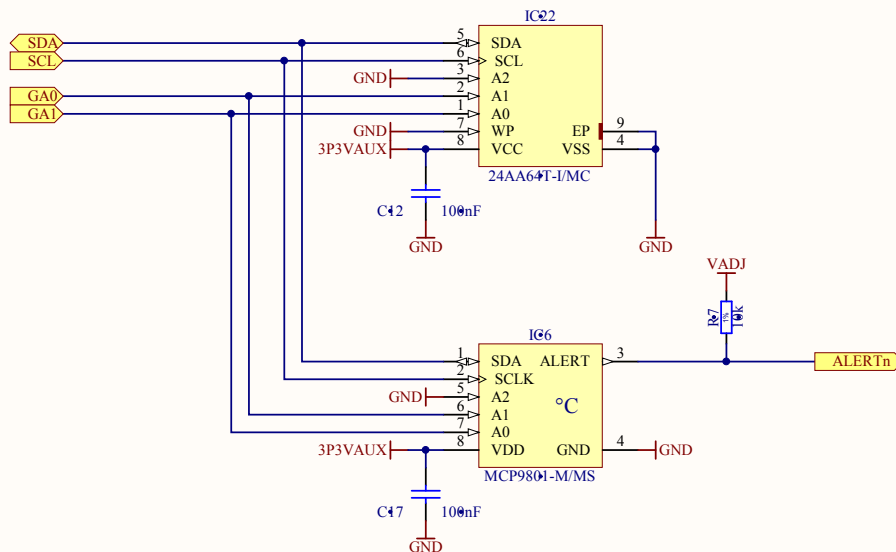
reversed LED polarity - schematic pins only



reversed LED polarity - schematic pins only



24AA64T = b"10100 GA0 GA1"
MCP9801 = b"10010 GA0 GA1"



Warning!
Following the VITA 57.1 standard:
GA0 goes to A1
GA1 goes to A0

FTG1 FTG2 FTG3 FTG6 FTG5 FTG4

FTG1 ... FTG6
Reference points for the
component mounting machine.

Project/Equipment FmcAdc100M14b4cha

Document

BE-CO



**Trigger input, EEPROM,
thermometer and LEDs**

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

Designer	Maciej Fimiarz	01/02/2010
Drawn by	Maciej Fimiarz	17/10/2011
Check by	B. Civel	2014-06-09
Last Mod.	Cattin, van der Bij	2014-06-09
File	I2C mem LED.SchDoc	
Print Date	2014-06-09 16:16:35	Sheet 2 of 11

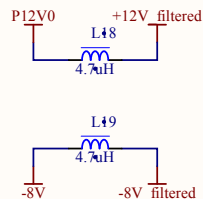
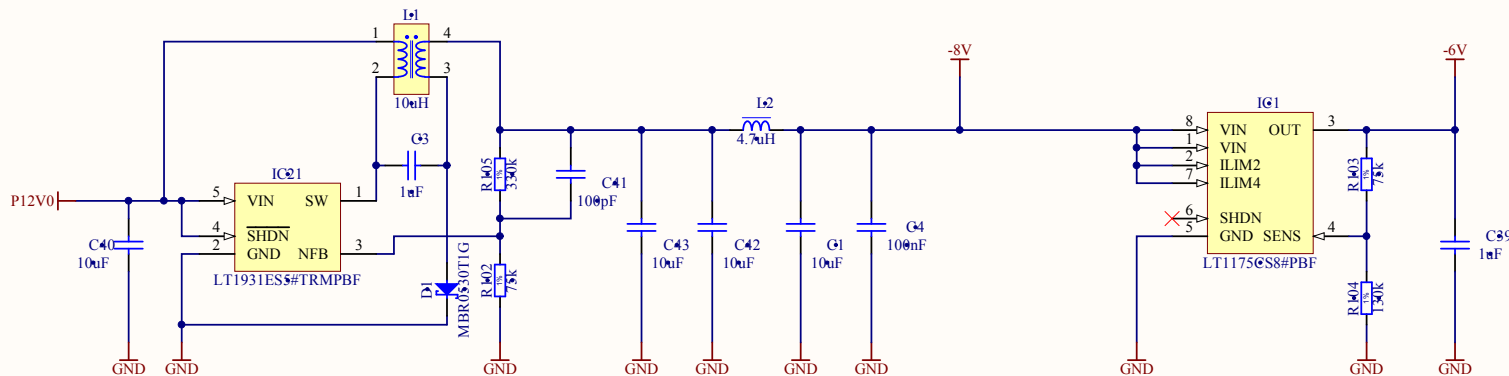
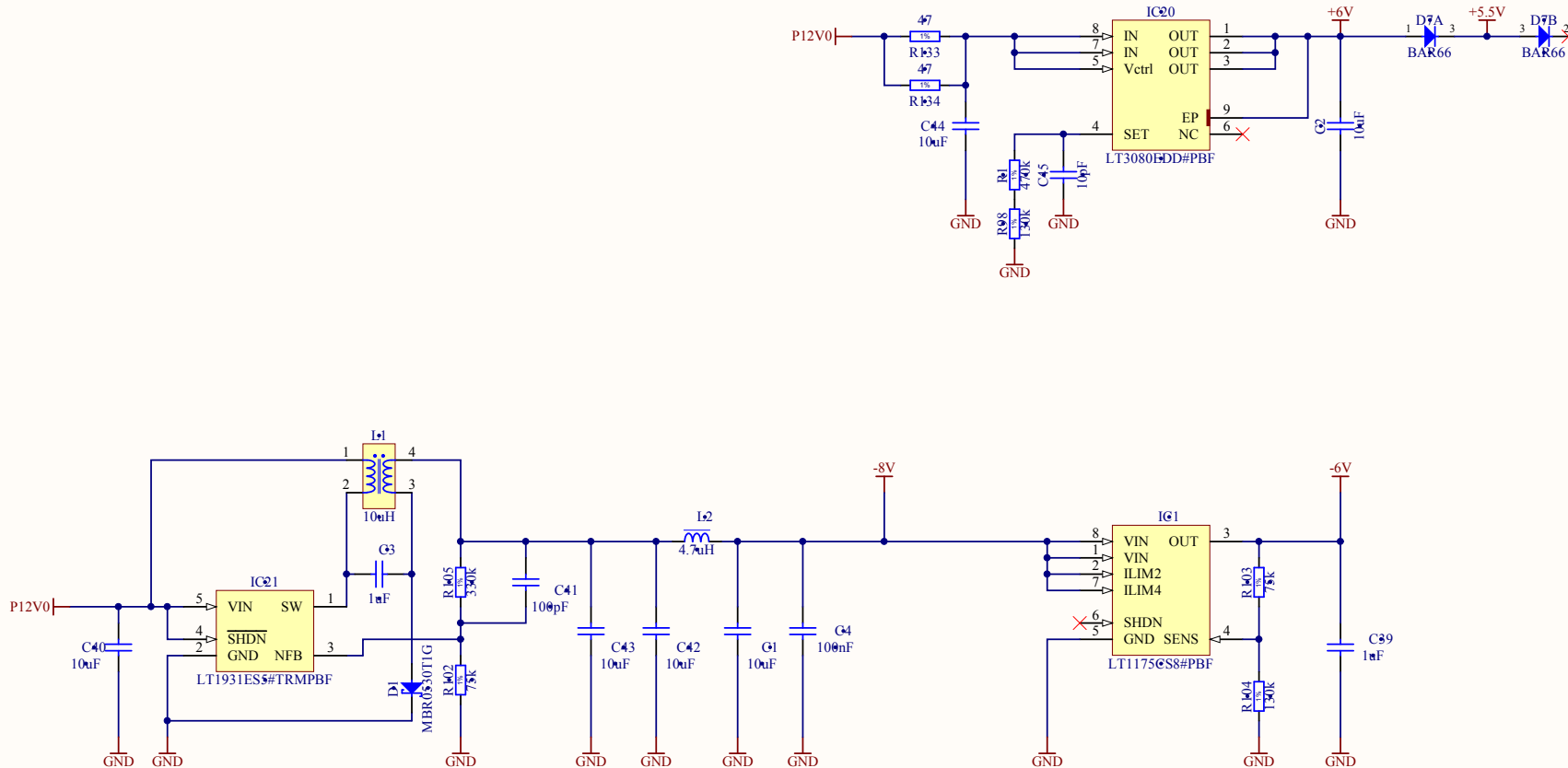
EDA-02063-V5-0

Site A4 Rev -

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▲ +5.5V is used as a power supply for offset DACs.
The real value is 6V - 0.6... 0.7V which gives 5.3... 5.4V.
It is lower than 5.5V; max. DAC voltage for normal operation.



Project/Equipment FmcAdc100M14b4cha

Document



Power supplies

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

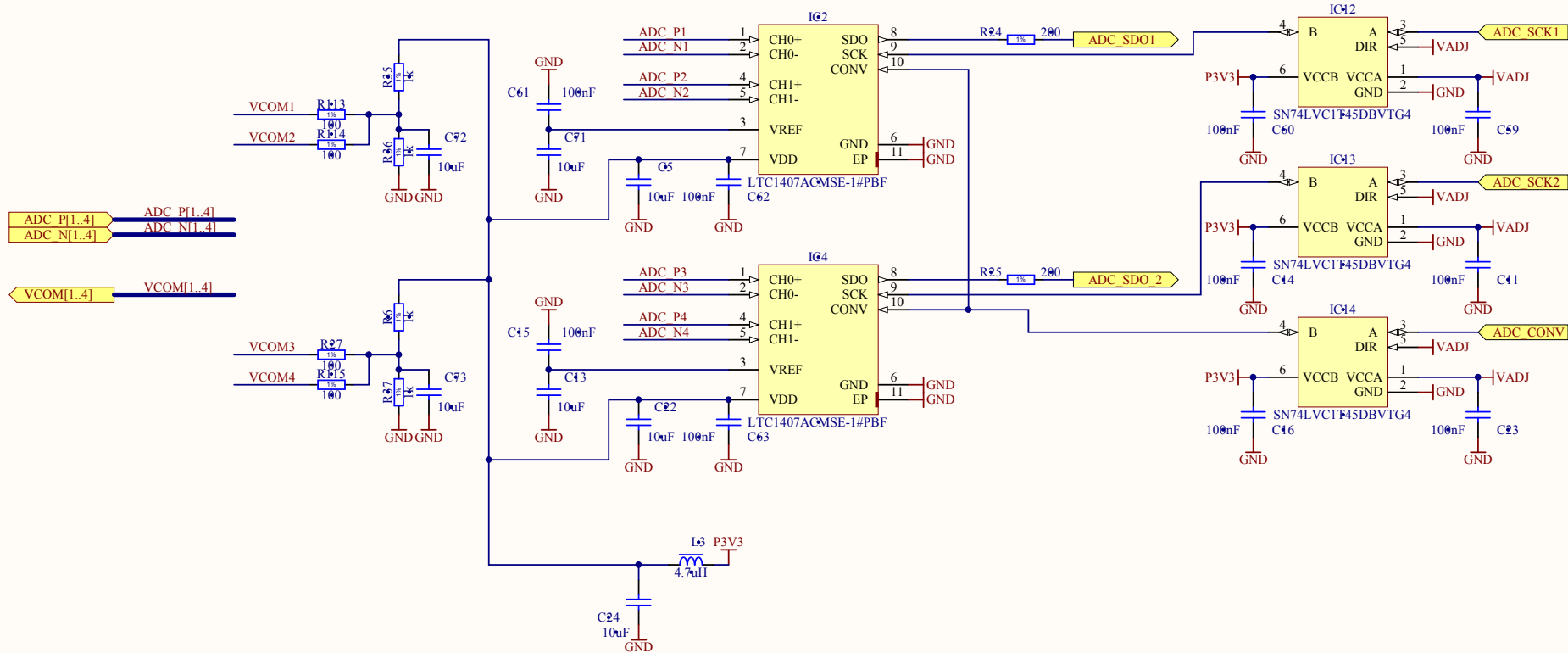
Designer	Maciej Fimiarz	01/02/2010
Drawn by	Maciej Fimiarz	17/10/2011
Check by	B. Civel	2014-06-09
Last Mod.	Cattin, van der Bij	2014-06-09
File	power_supply.SchDoc	
Print Date	2014-06-09 16:16:36	Sheet 3 of 11

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Size A4
Rev -

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Project/Equipment FmcAdc100M14b4cha

Document

BE-CO



**Linear Technologies' ADC
105MSPS 14b**

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

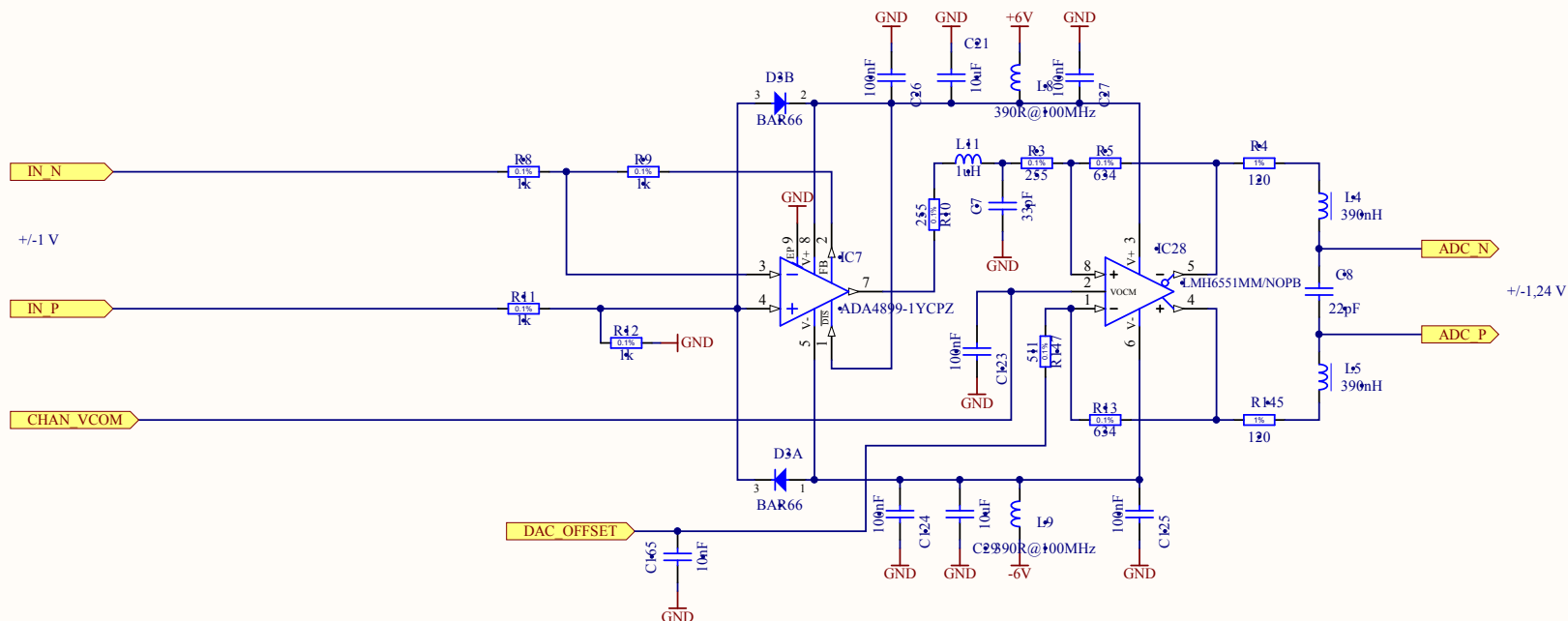
Designer	Maciej Fimiarz	01/02/2010
Drawn by	Maciej Fimiarz	17/10/2011
Check by	B. Civel	2014-06-09
Last Mod.	Cattin, van der Bij	
File	ADC.SchDoc	
Print Date	2014-06-09 16:16:36	Sheet 5 of 11

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Site Rev
A4 -

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Project/Equipment FmcAdc100M14b4cha

Document



Channel 1 Analogue front-end

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

Designer	Maciej Fimiarz	01/02/2010
Drawn by	Maciej Fimiarz	17/10/2011
Check by	B. Civel	2014-06-09
Last Mod.	Cattin, van der Bij	2014-06-09
File	input_stage.SchDoc	
Print Date	2014-06-09 16:16:36	Sheet 7 of 11

EDA-02063-V5-0

Size A4 Rev -

A

B

C

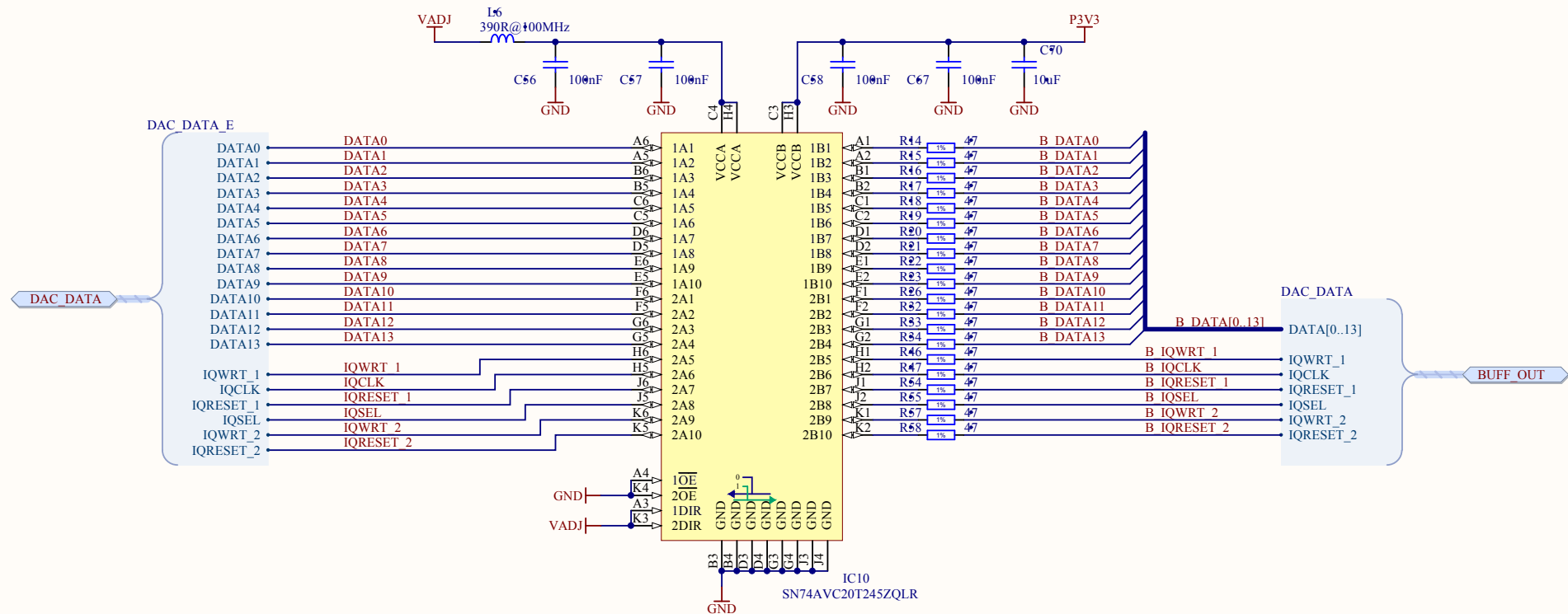
D

A

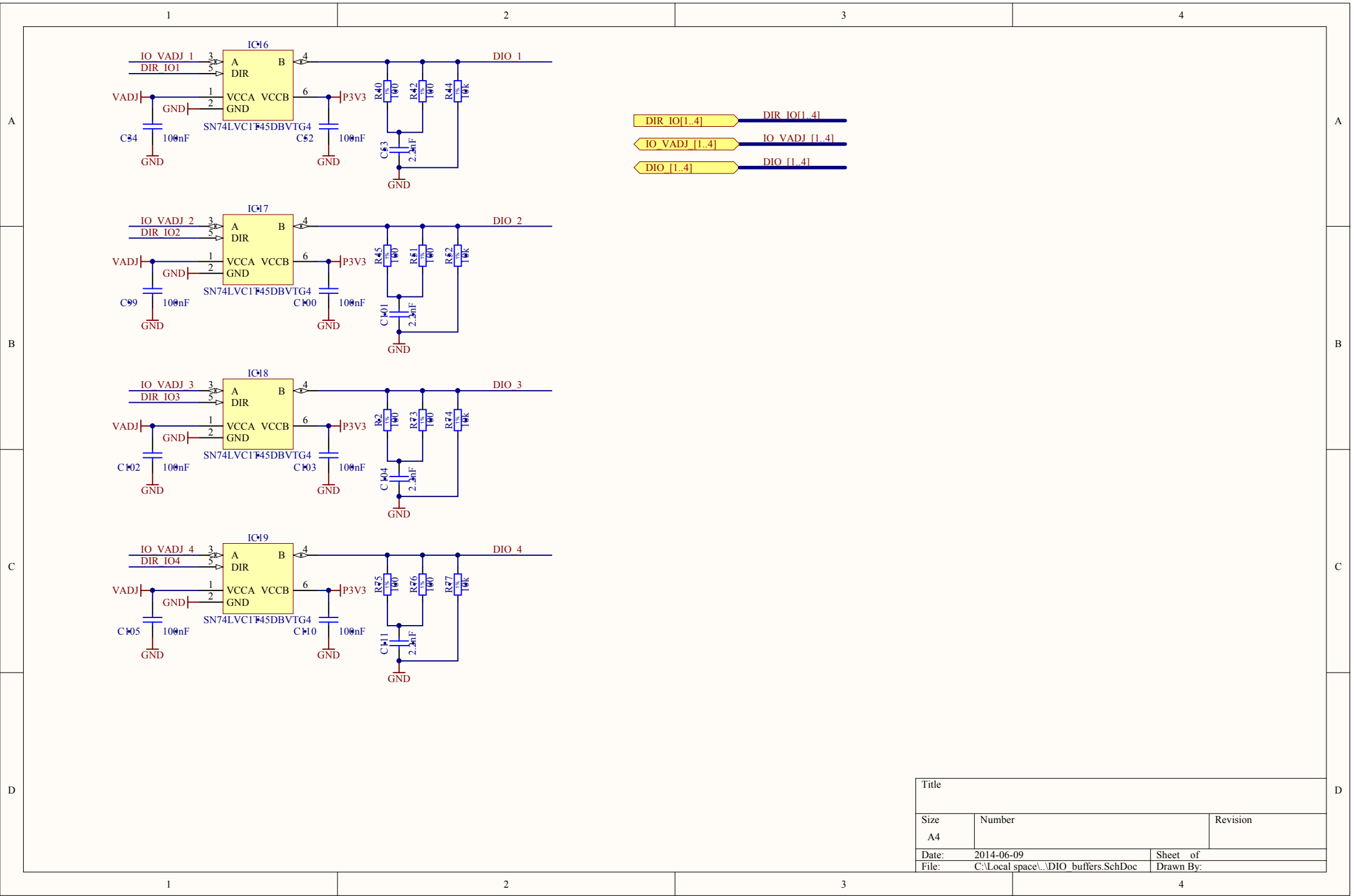
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C

D



Title		
Size	Number	Revision
A4		
Date:	2014-06-09	Sheet of
File:	C:\Local space\...\buffer.SchDoc	Drawn By:



IC16

SN74LVC1745DBVTG4

A

DIR

B

VCCA

VCCB

GND

6

P3V3

100nF

GND

100

100

2.2nF

GND

100

100

10k

DIO 1

IC17

SN74LVC1745DBVTG4

A

DIR

B

VCCA

VCCB

GND

6

P3V3

100nF

GND

100

100

2.2nF

GND

100

100

10k

DIO 2

IC18

SN74LVC1745DBVTG4

A

DIR

B

VCCA

VCCB

GND

6

P3V3

100nF

GND

100

100

2.2nF

GND

100

100

10k

DIO 3

IC19

SN74LVC1745DBVTG4

A

DIR

B

VCCA

VCCB

GND

6

P3V3

100nF

GND

100

100

2.2nF

GND

100

100

10k

DIO 4

DIR IO[1..4]

DIR IO1[..4]

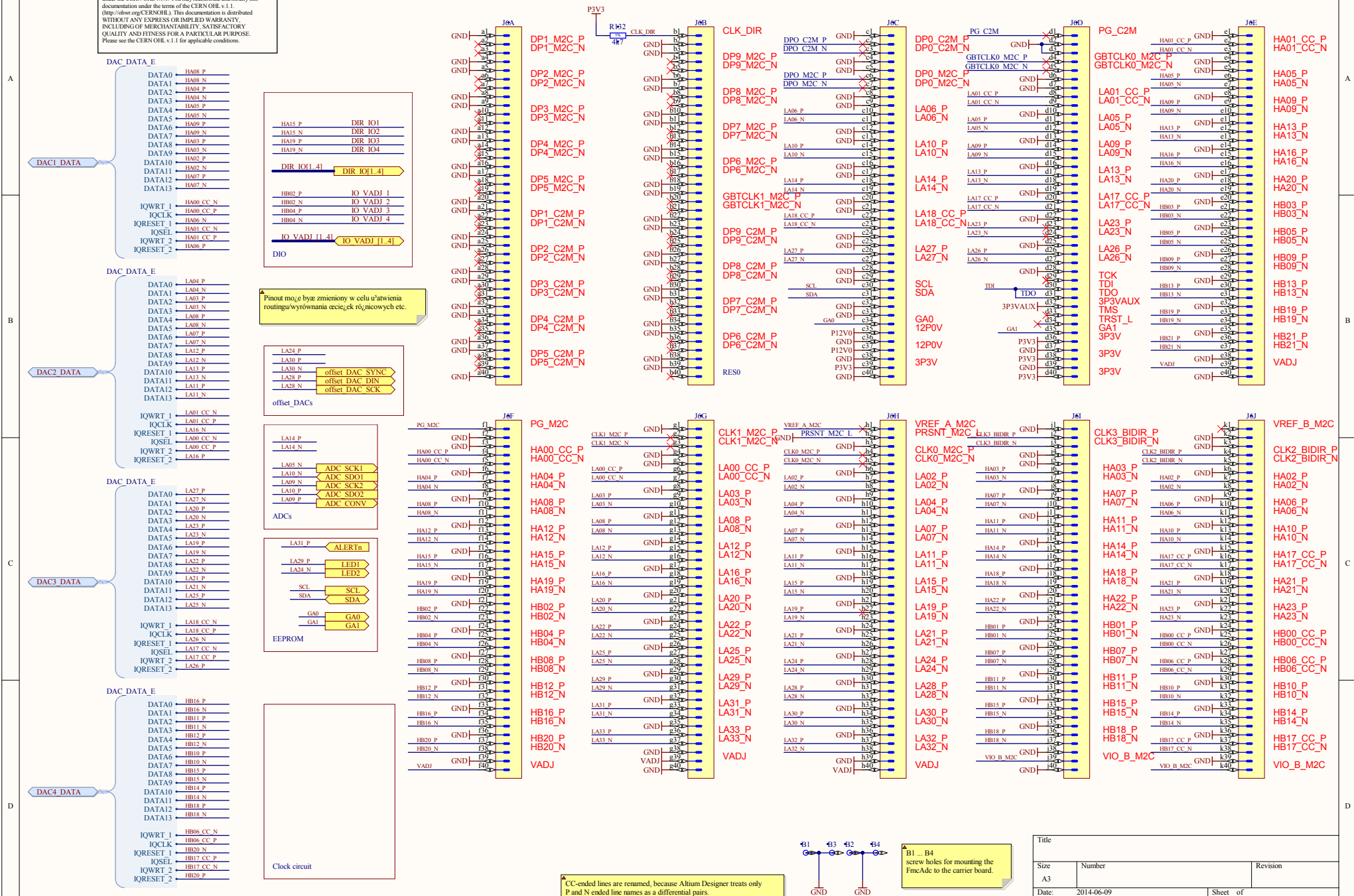
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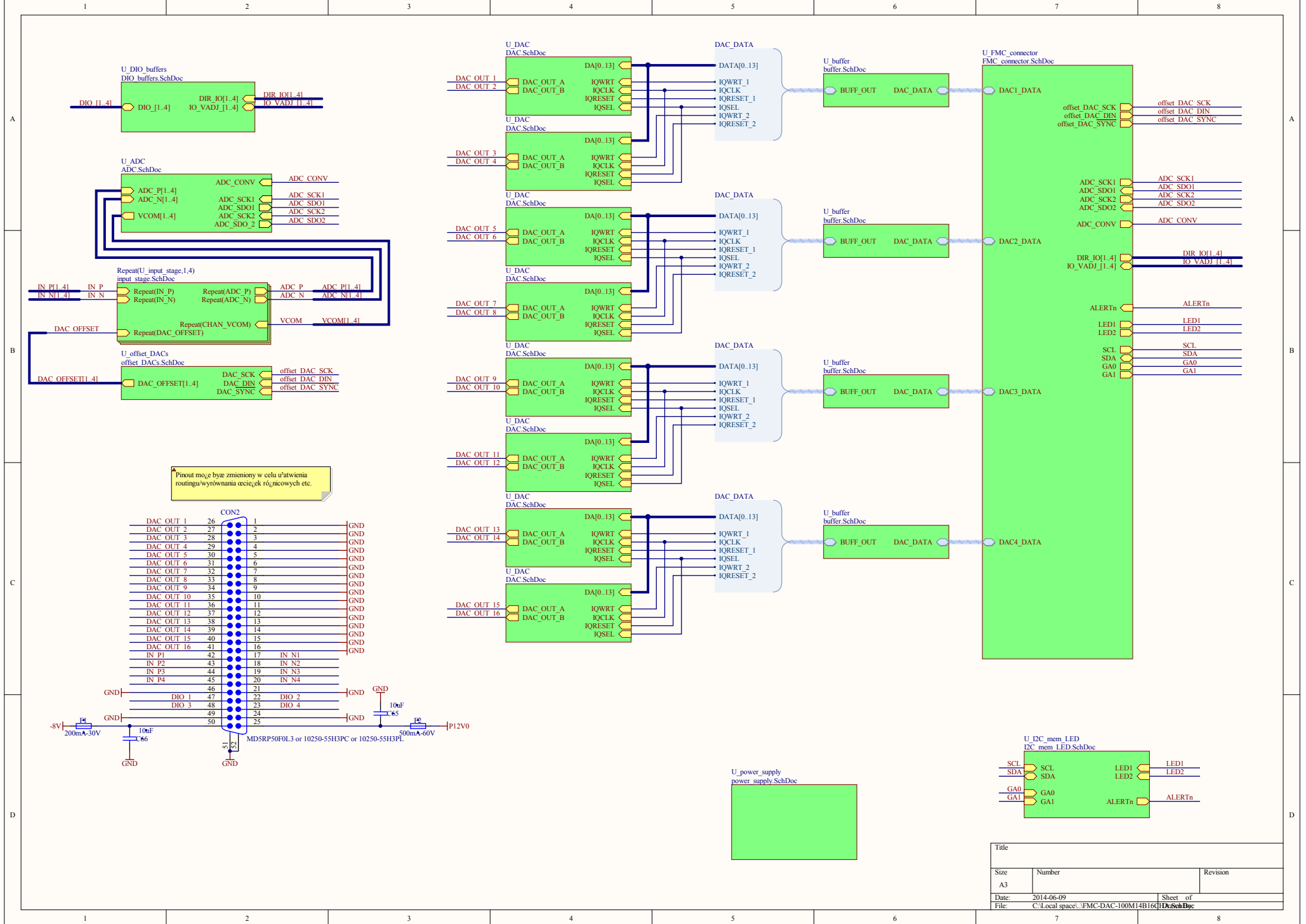
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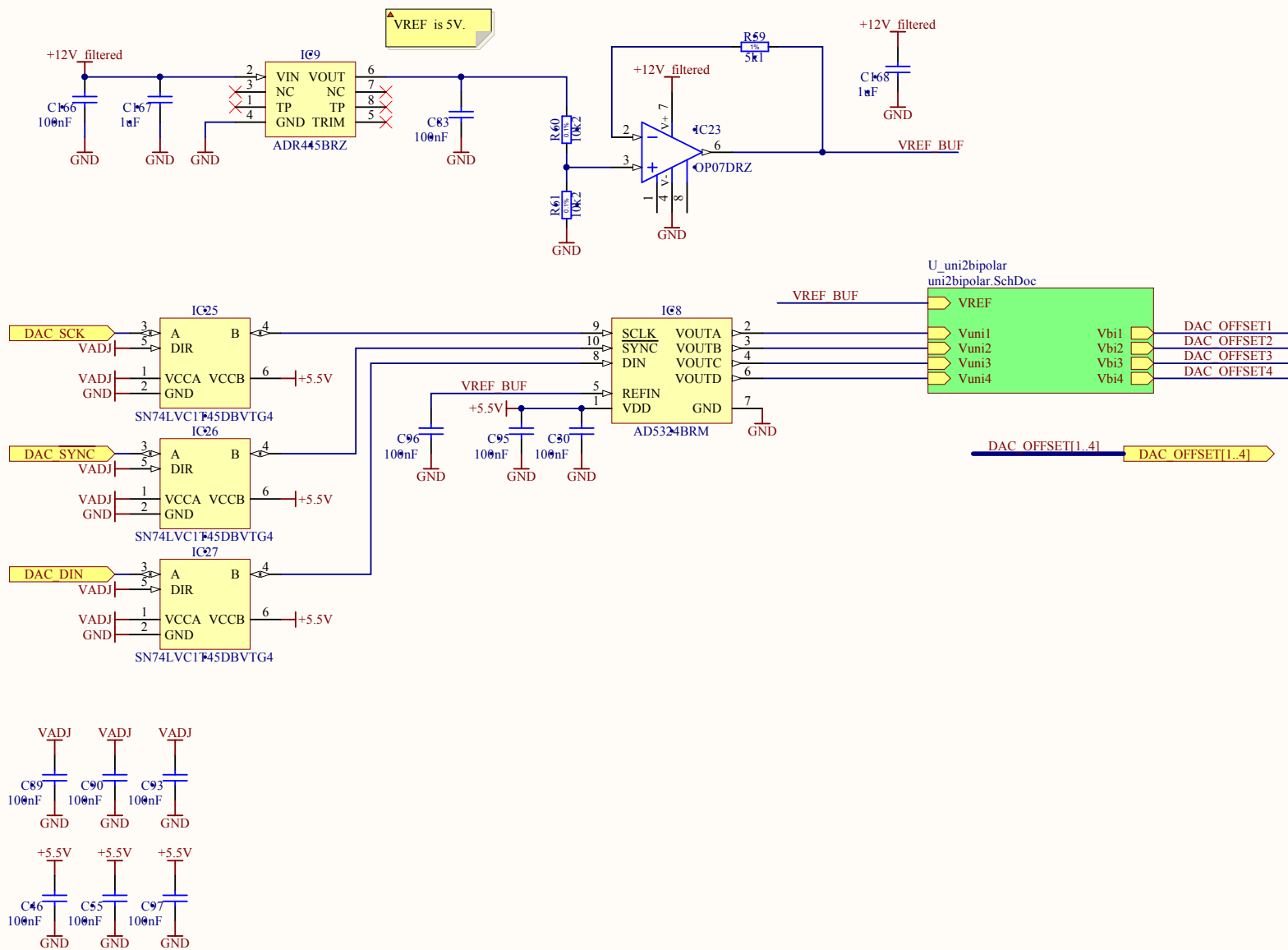
DIO [1..4]

DIO [1..4]

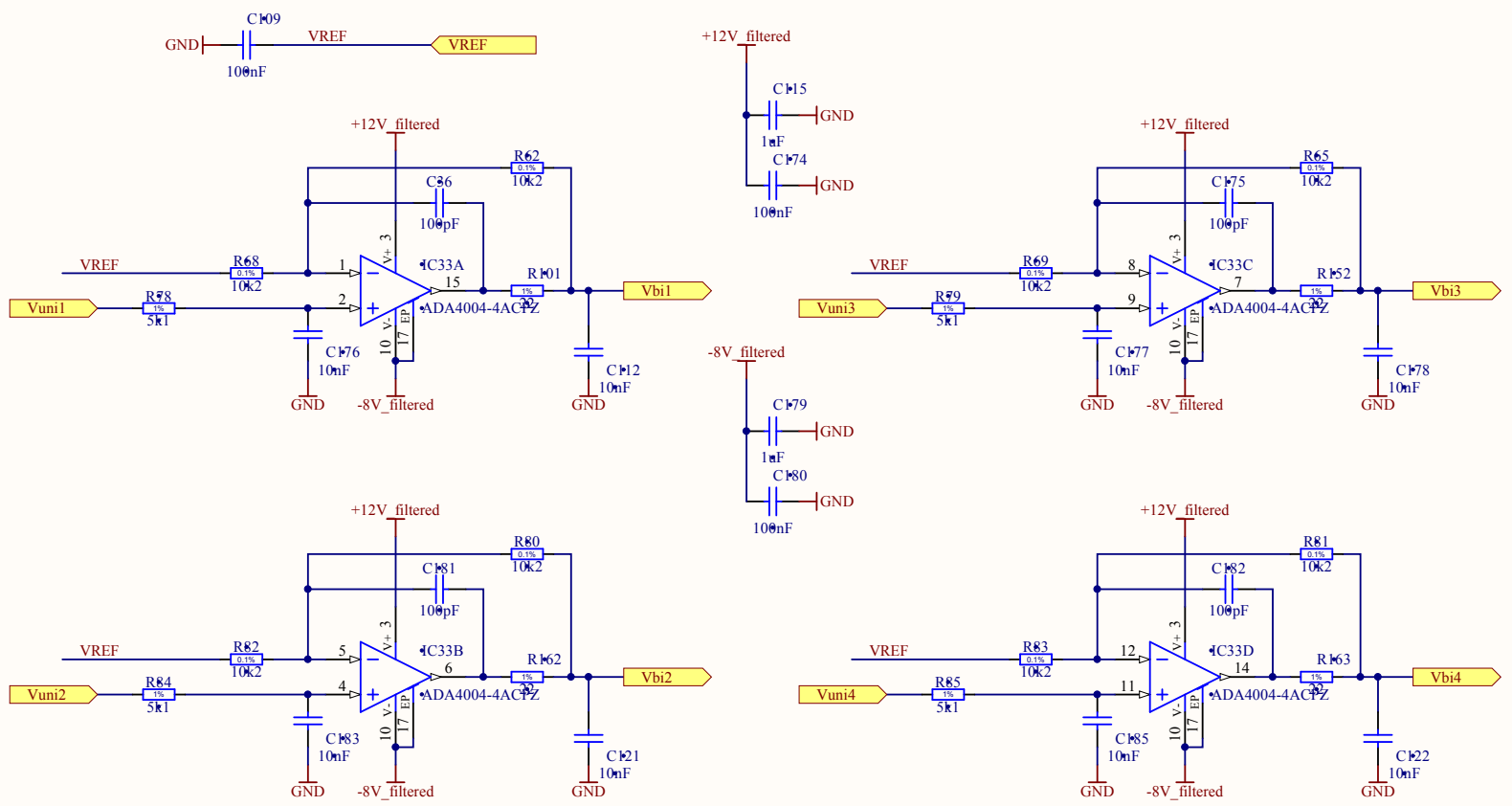
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Size	Number	Revision
A4		
Date:	2014-06-09	Sheet of
File:	C:\Local space\...\DIO_buffers.SchDoc	Drawn By:







Title		
Size	Number	Revision
A4		
Date:	2014-06-09	Sheet of
File:	C:\Local space\...\offset_DACs.SchDoc	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	2014-06-09	Sheet of
File:	C:\Local space\uni2bipolar.SchDoc	Drawn By: