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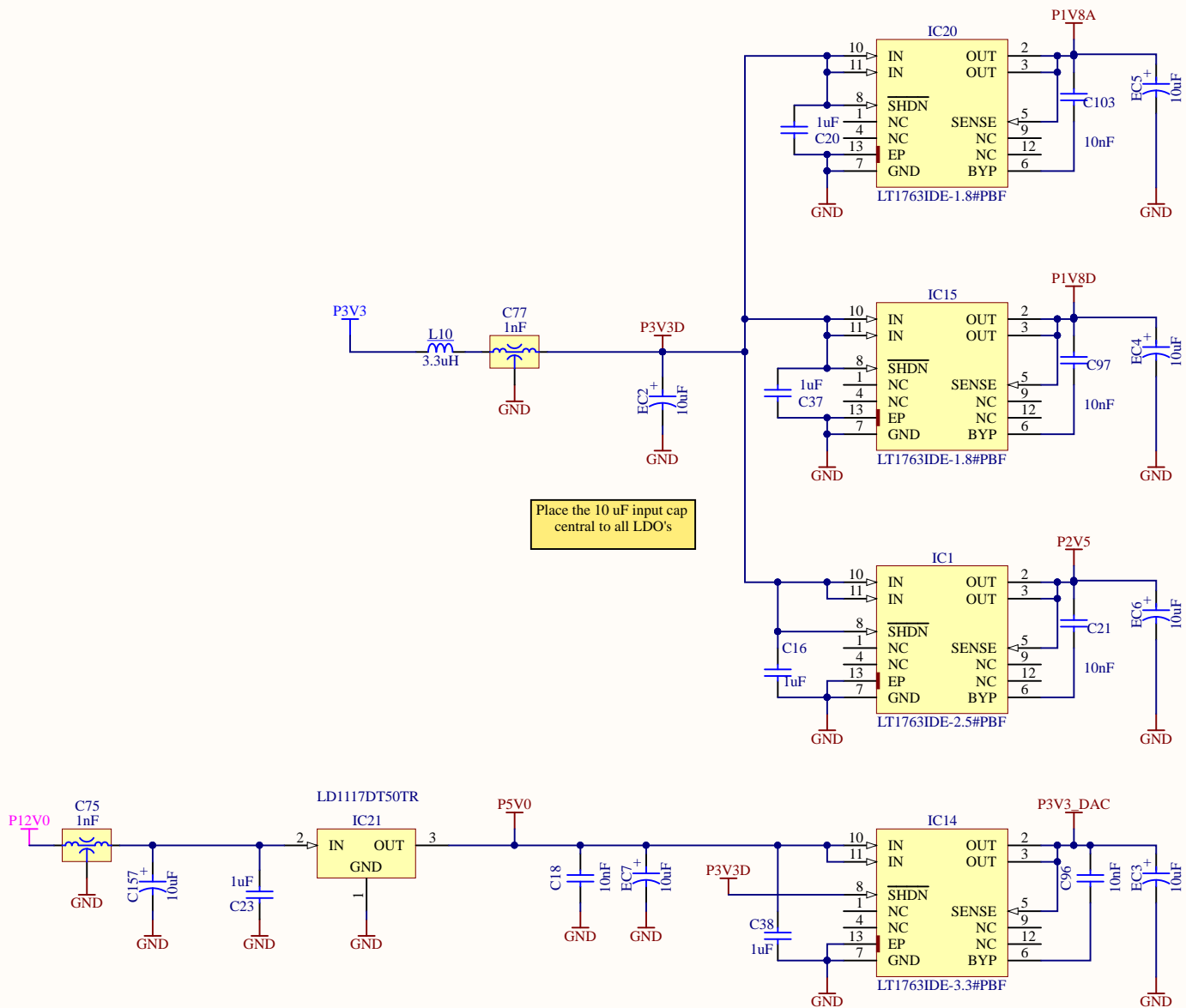
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Project/Equipment		FMC DDS v3 (FMCDDac600m12b1ChaDDS)	
Document		Designer	G.K., T.W.
		Drawn by	G.K., T.W.
		Check by	B. Civel
		Last Mod.	B. Civel
File		FMC DDS.SchDoc	
Print Date		04.01.2019 17:39:26	
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		Rev	-

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Project/Equipment		FMC DDS v3 (FMCdac600m12b1ChaDDS)	
Document		Designer	G.K., T.W.
<div>BE-CO</div> <div></div>	<div>FMC DDS v3</div> <div>- Power Supply Regulators -</div>	Drawn by	G.K., T.W.
		Check by	B. Civel
		Last Mod.	B. Civel
		File	Power.SchDoc
		Print Date	04.01.2019 17:39:26
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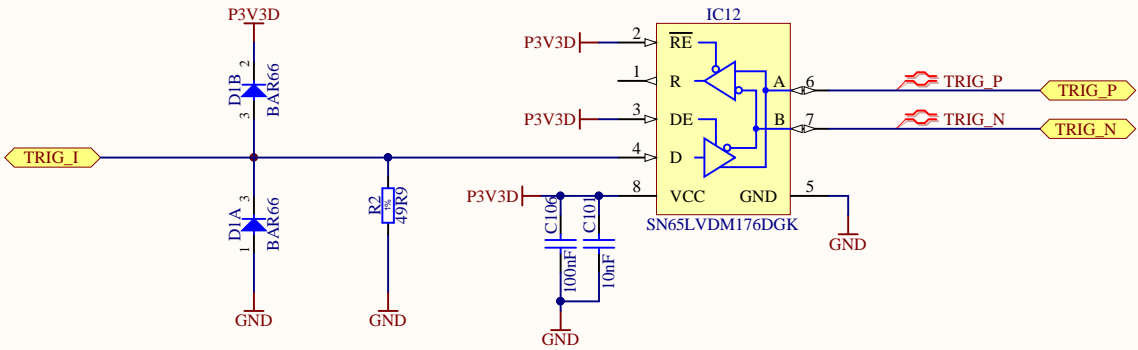



Place the 10 uF input cap
central to all LDO's

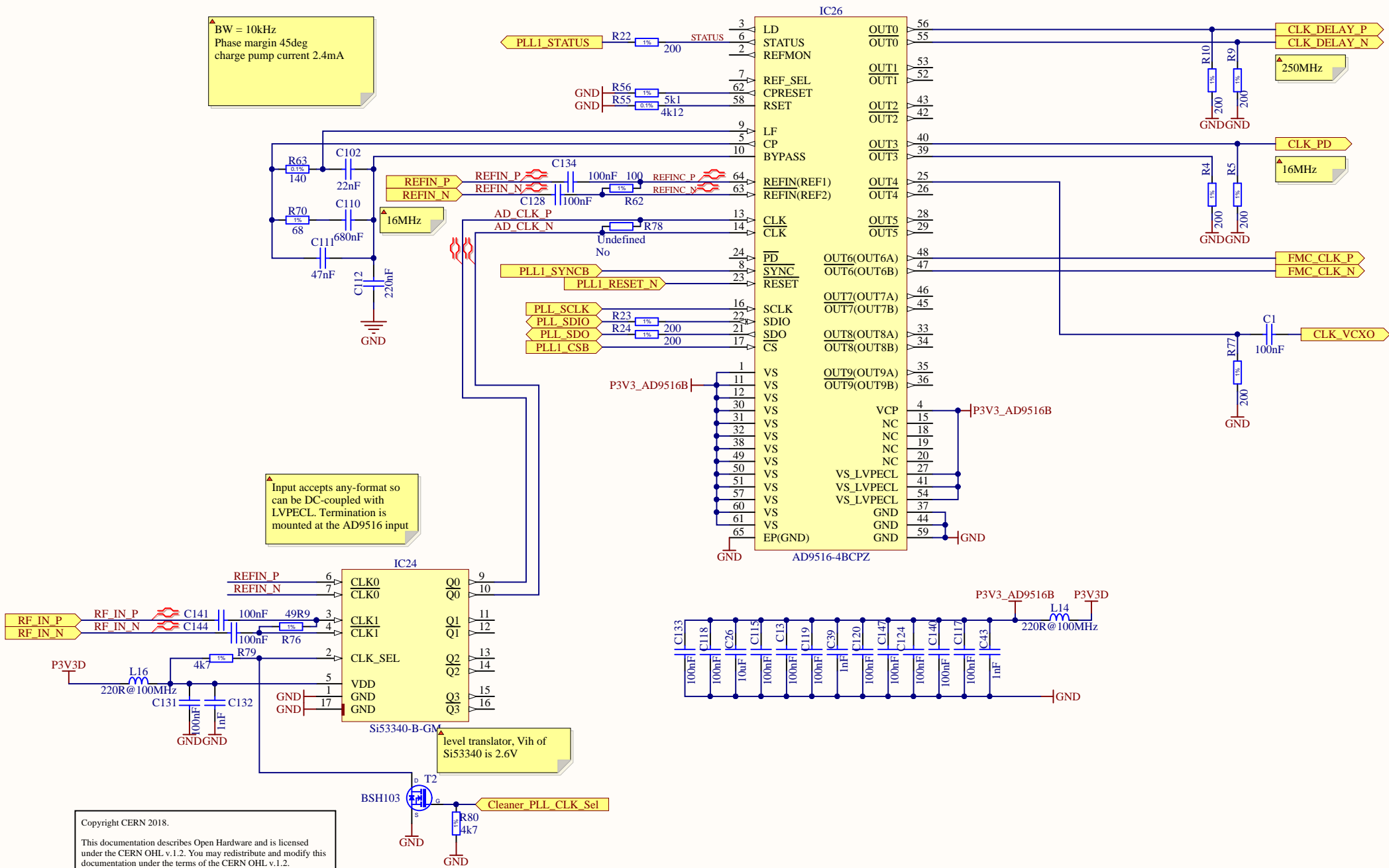
Place all LT1763's on 100 mm^2 (min)
pour. Device pad should have multiple
(>6) 0.5 mm vias connecting to all
ground planes, and be soldered to pour

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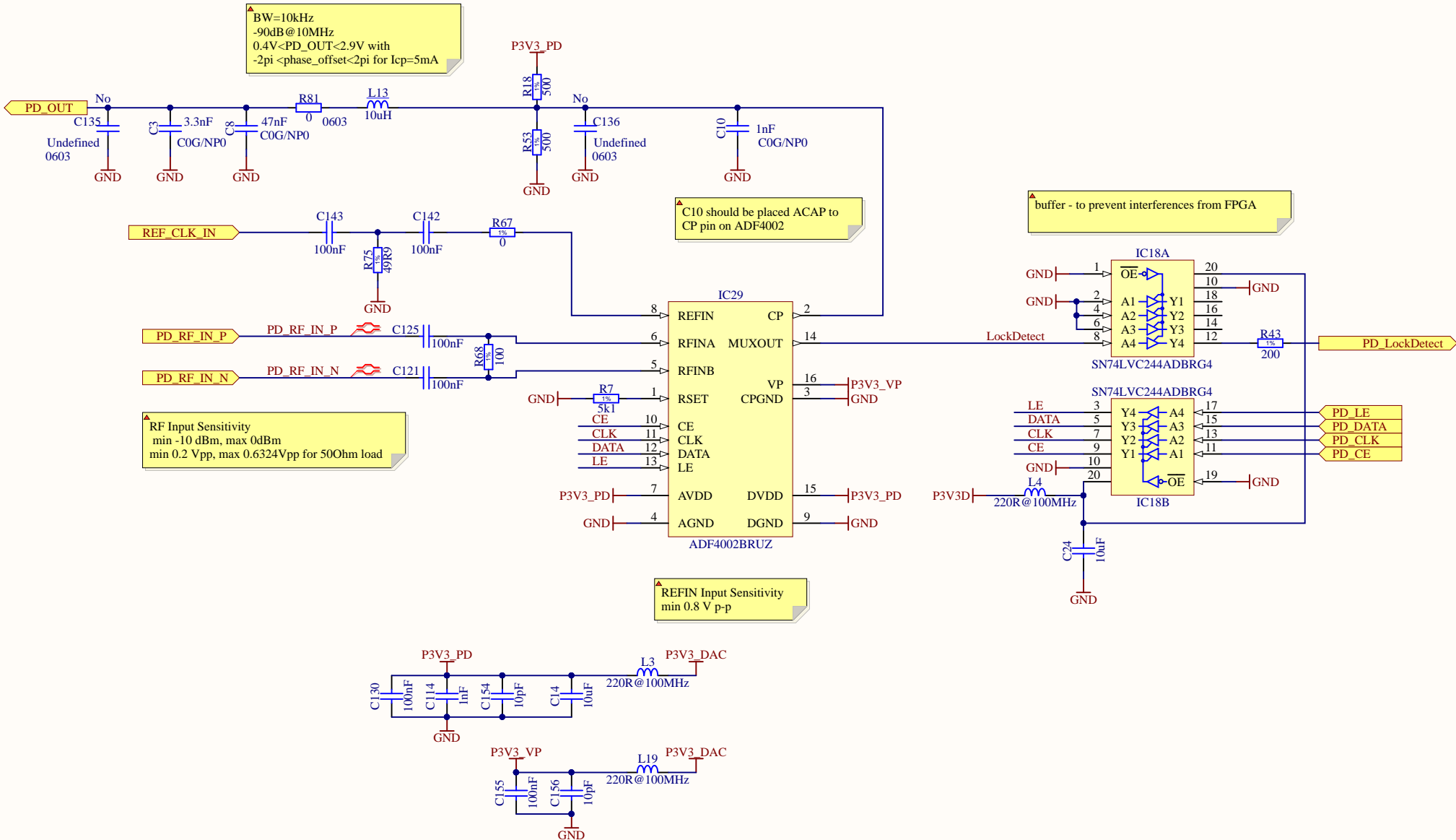


Project/Equipment		FMC DDS v3 (FMC DAC600m12b1ChaDDS)	
<div>Document</div> <div>BE-CO</div> <div></div>	Designer		G.K., T.W.
	Drawn by		G.K., T.W.
	Check by		B. Civel
	Last Mod.		B. Civel
	File		Trigger.SchDoc
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Size		A3	Rev -




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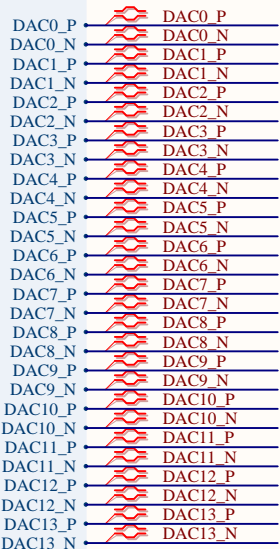
Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)	
Document		Designer	G.K., T.W.
<div>BE-CO</div> <div></div>	<div>FMC DDS v3</div> <div>- Phase Detector -</div>	Drawn by	G.K., T.W.
		Check.by	B. Civel
		Last Mod.	B. Civel
		File	Phase detector.SchDoc
		Print Date	04.01.2019 17:39:27
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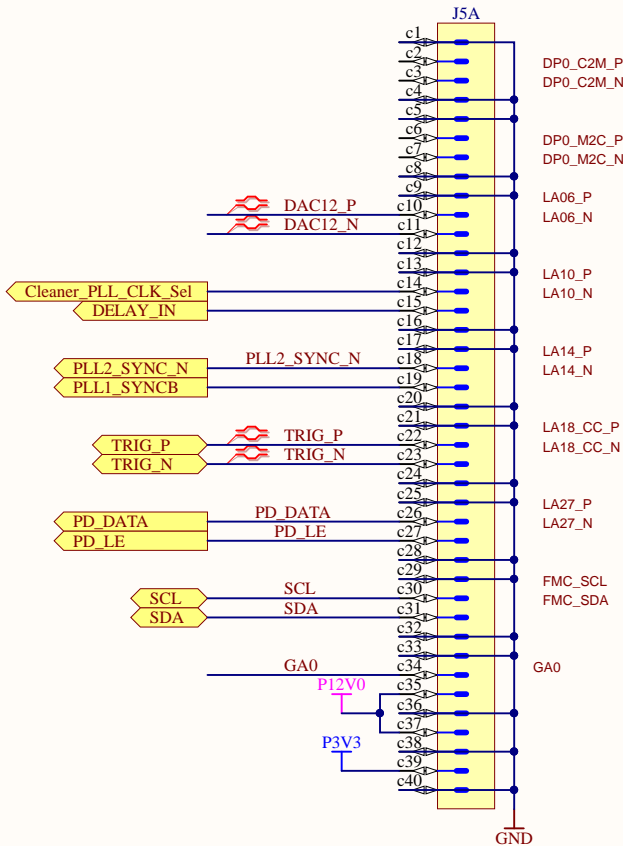
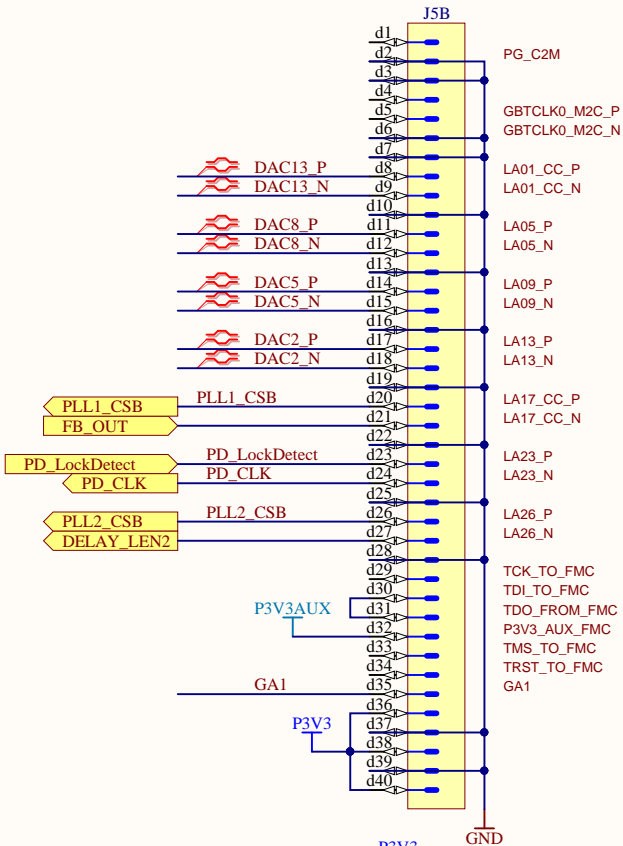
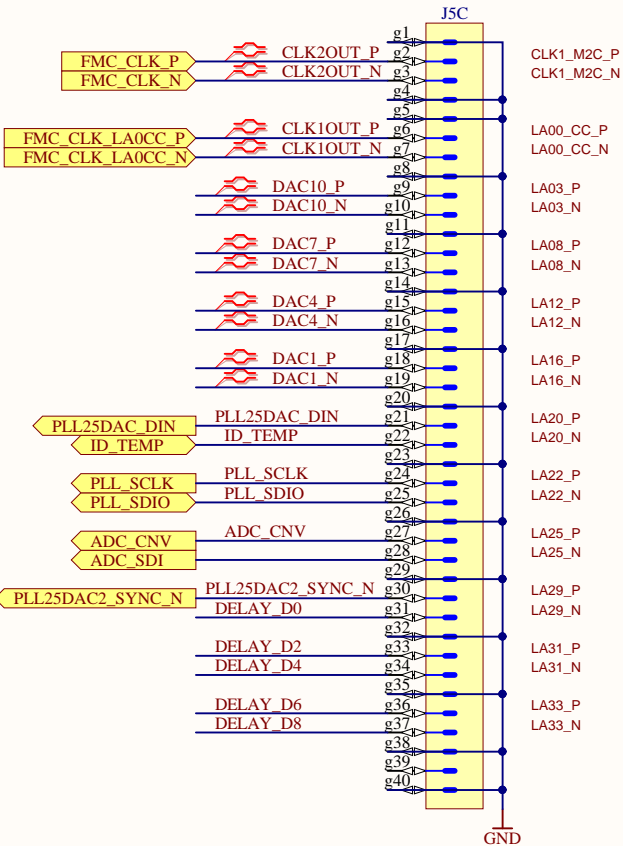
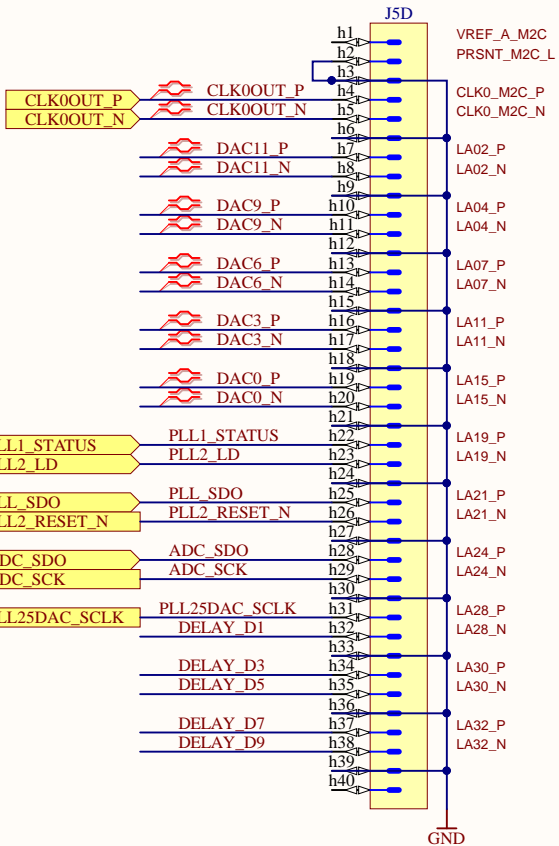
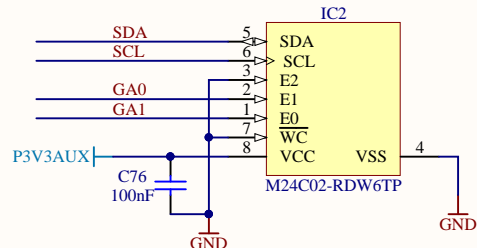
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Project/Equipment FMC DDS v3(FMCDac600m12b1ChaDDS)		
<div>Document</div> <div>BE-CO</div> <div></div>	Designer G.K., T.W.	
	Drawn by G.K., T.W.	04/07/2014
	Check by B. Civel	16/07/2014
	Last Mod. B. Civel	04.01.2019
	File ADC_filter.SchDoc	
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		Size A3 Rev -

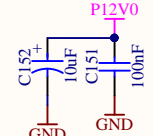
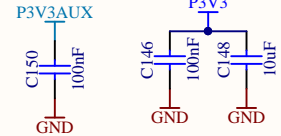
DAC_DAT



DAC_DAT



DELAY_D[9..0] DELAY_D[9..0]



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CERN		Check by B. Civel	
		Last Mod. B. Civel	
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		Print Date 04.01.2019 17:39:28	
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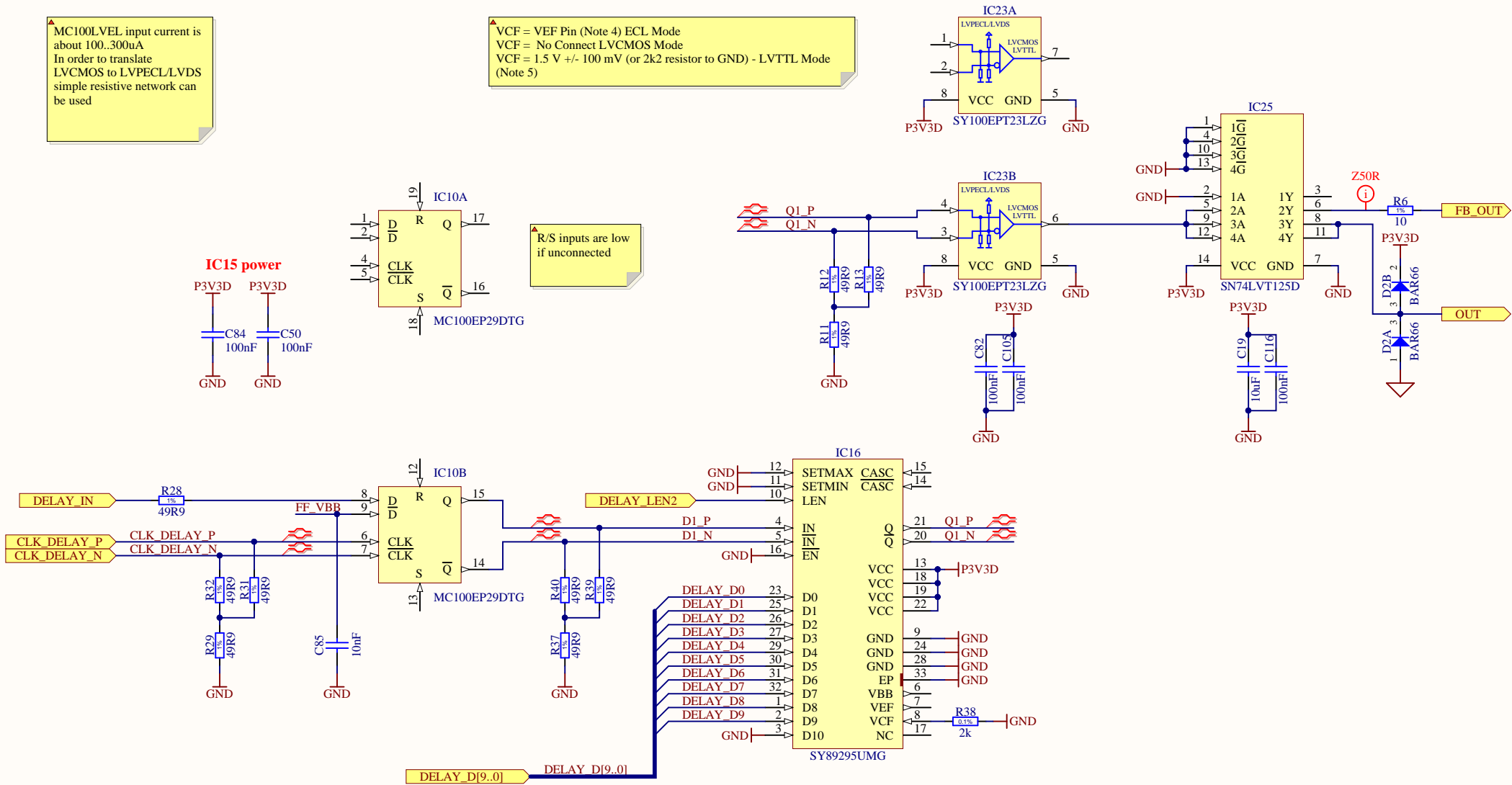
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FMC DDS v3
- FMC Connector & EEPROM -

EDA-03010-V3-0

▲ MC100LEVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used

▲ VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV (or 2k2 resistor to GND) - LVTTTL Mode (Note 5)



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