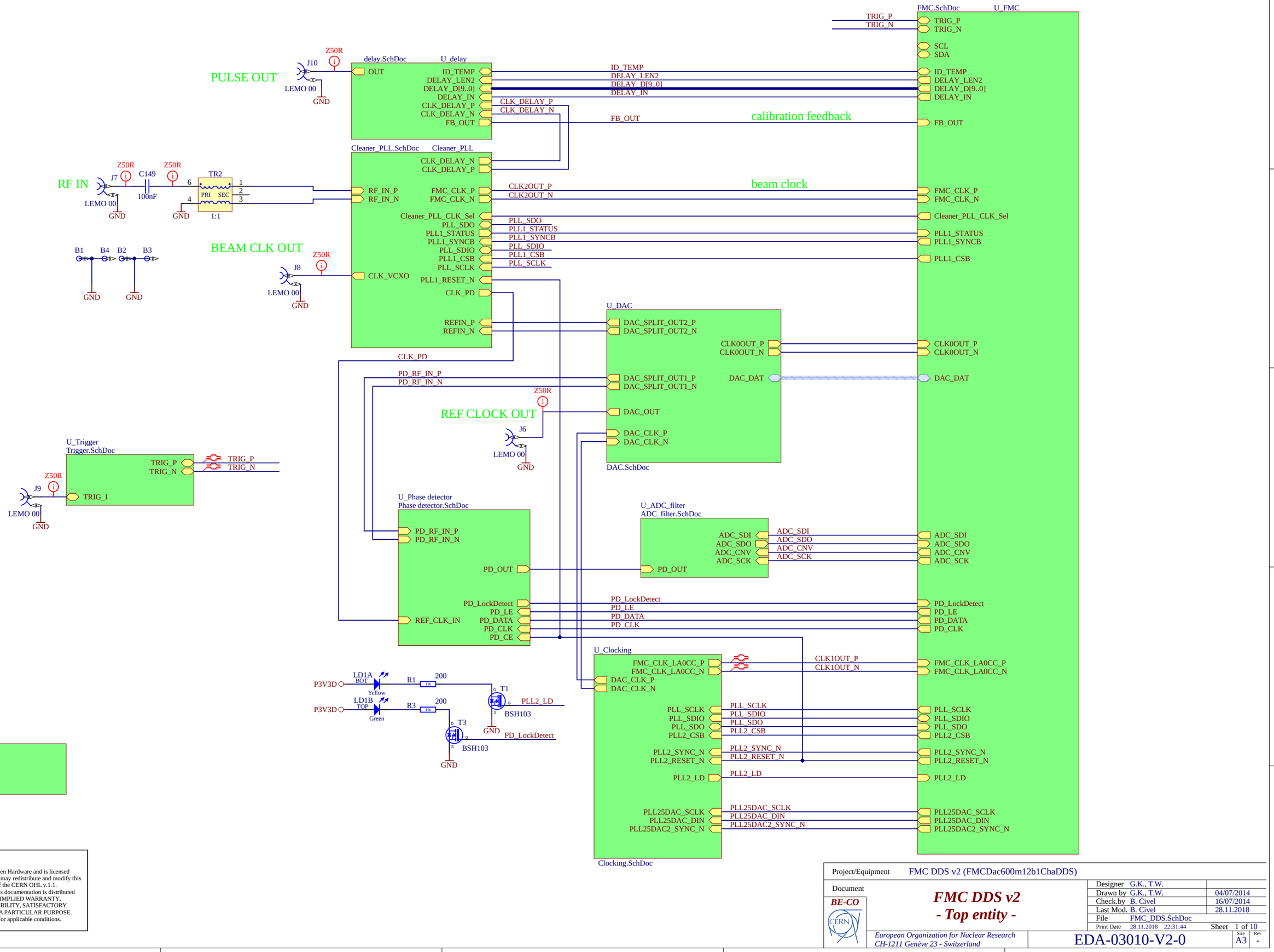

Project/Equipment	FMC DDS v2 (FMCDac600m12b1ChaDDS)
Document	**FMC DDS v2 - Top entity -**
Designer	G.K., T.W.
Drawn by	G.K., T.W. 04/07/2014
Check.by	B. Civel 16/07/2014
Last Mod.	B. Civel 28.11.2018
File	FMC_DDS.SchDoc
Print Date	28.11.2018 22:31:44
Sheet	1 of 10
Size	A3
Rev	-

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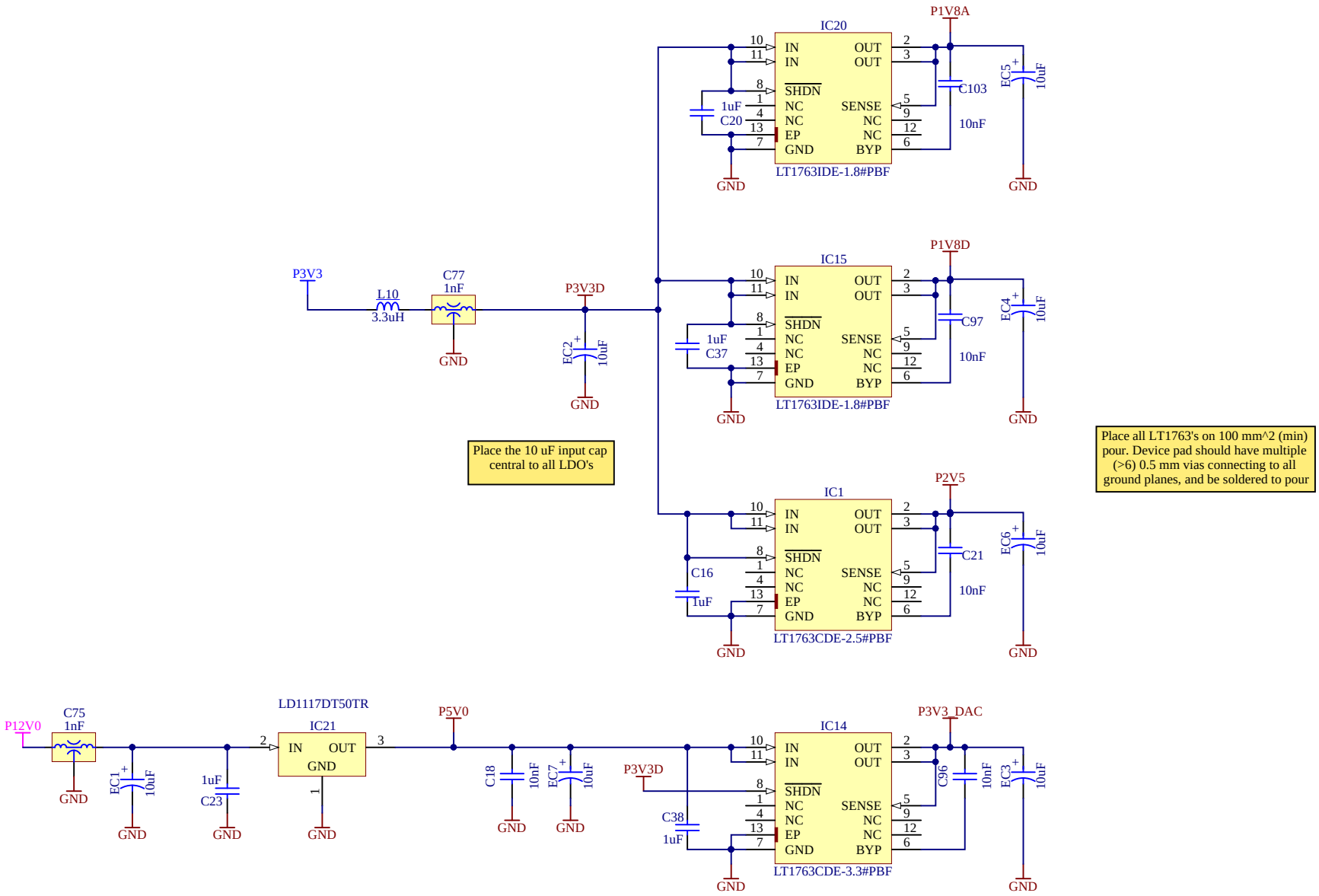

Place the 10 uF input cap central to all LDO's

Place all LT1763's on 100 mm^2 (min) pour. Device pad should have multiple (>6) 0.5 mm vias connecting to all ground planes, and be soldered to pour

Project/Equipment	FMC DDS v2 (FMCDac600m12b1ChaDDS)
Document	**FMC DDS v2 - Power Supply Regulators -**
Designer	G.K., T.W.
Drawn by	G.K., T.W. 04/07/2014
Check.by	B. Civel 16/07/2014
Last Mod.	B. Civel 28.11.2018
File	Power.SchDoc
Print Date	28.11.2018 22:31:44
Sheet	2 of 10
Size	A4
Rev	-

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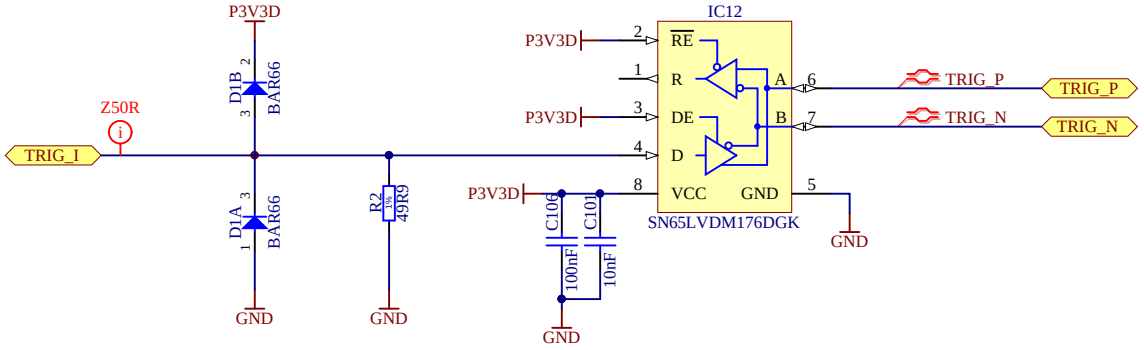

Project/Equipment: FMC DDS v2 (FMCDac600m12b1ChaDDS)

Document: **FMC DDS v2 - Trigger Input -**

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Designer	G.K., T.W.	
Drawn by	G.K., T.W.	04/07/2014
Check.by	B. Civel	16/07/2014
Last Mod.	B. Civel	28.11.2018
File	Trigger.SchDoc	
Print Date	28.11.2018 22:31:44	Sheet 3 of 10

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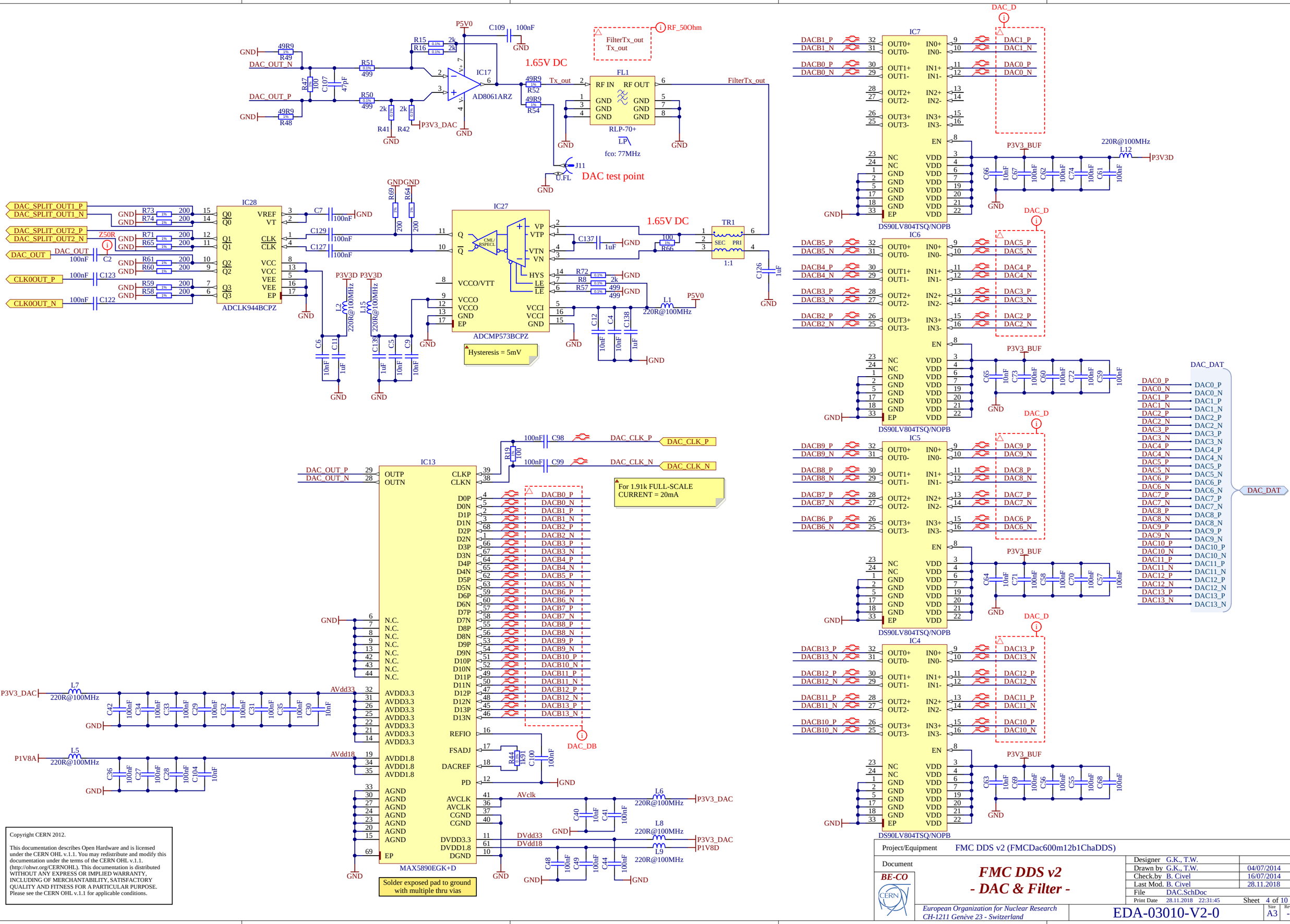
Size: A4 | Rev: -



Project/Equipment	FMC DDS v2 (FMCDac600m12b1ChaDDS)
Document	**FMC DDS v2 - DAC & Filter -**
Designer	G.K., T.W.
Drawn by	G.K., T.W. 04/07/2014
Check.by	B. Civel 16/07/2014
Last Mod.	B. Civel 28.11.2018
File	DAC.SchDoc
Print Date	28.11.2018 22:31:45
Sheet	4 of 10
Size	A3
Rev	-

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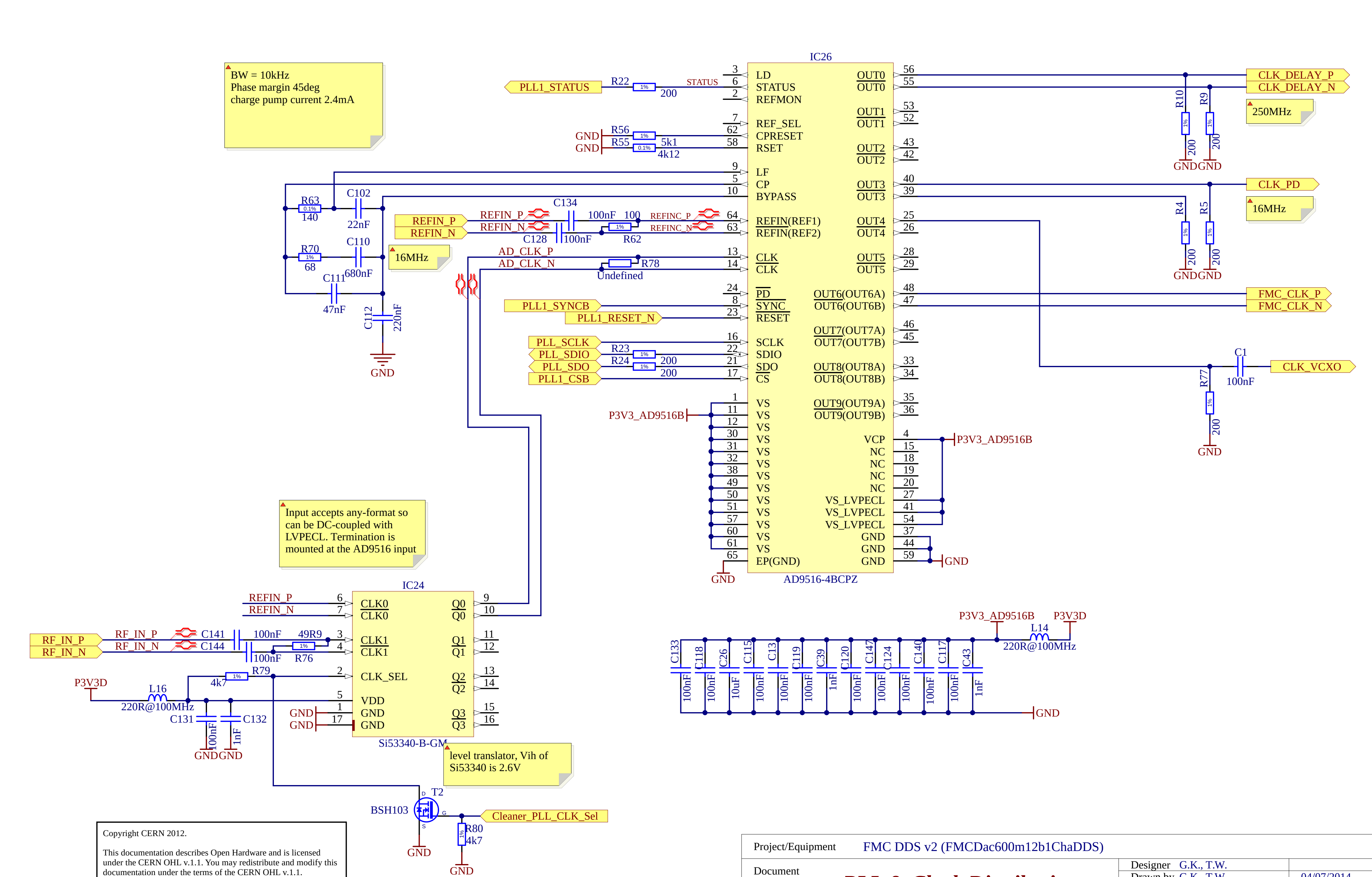

Project/Equipment: FMC DDS v2 (FMCDac600m12b1ChaDDS)

Document

PLL & Clock Distribution RF Divider

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Designer	G.K., T.W.	
Drawn by	G.K., T.W.	04/07/2014
Check.by	B. Civel	16/07/2014
Last Mod.	B. Civel	28.11.2018
File	Cleaner_PLL.SchDoc	
Print Date	28.11.2018 22:31:45	Sheet 5 of 10

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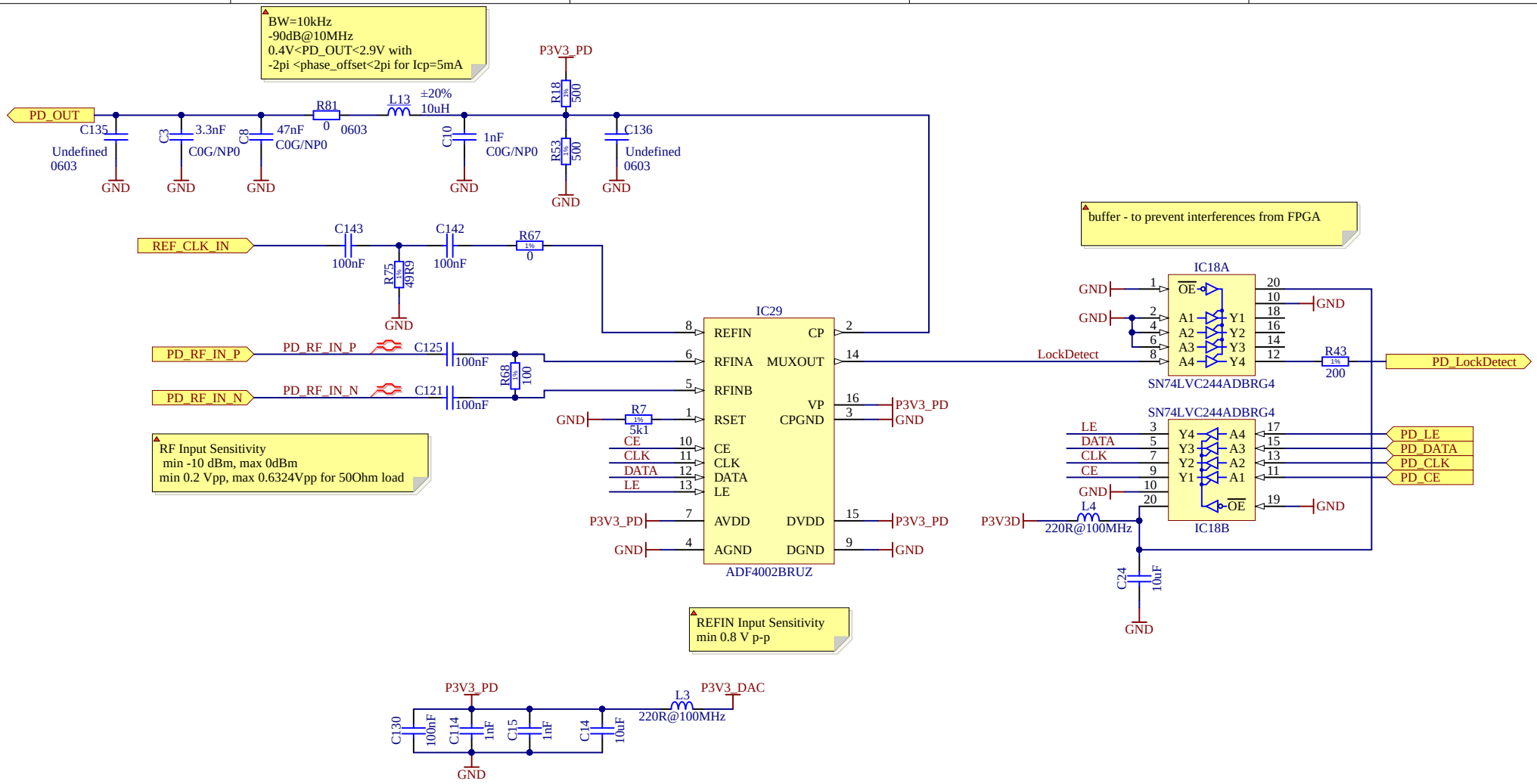
Size A4 Rev -



Project/Equipment	FMC DDS v2 (FMCDac600m12b1ChaDDS)
Document	**FMC DDS v2 - Phase Detector -**
Designer	G.K., T.W.
Drawn by	G.K., T.W. 04/07/2014
Check.by	B. Civel 16/07/2014
Last Mod.	B. Civel 28.11.2018
File	Phase detector.SchDoc
Print Date	28.11.2018 22:31:46
Sheet	6 of 10
Size	A4
Rev	-

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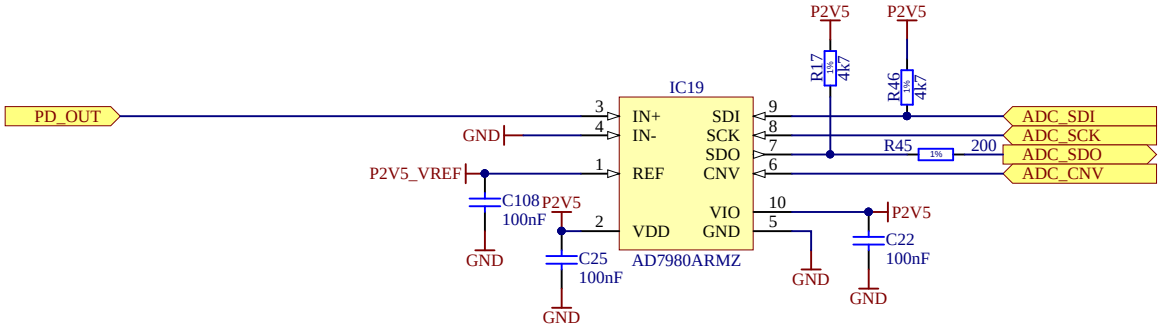
Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows. Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. CS mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low; if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.



Project/Equipment	FMC DDS v2 (FMCDac600m12b1ChaDDS)		
Document	**FMC DDS v2 - ADC -**	Designer	G.K., T.W.
		Drawn by	G.K., T.W. 04/07/2014
		Check.by	B. Civel 16/07/2014
		Last Mod.	B. Civel 28.11.2018
		File	ADC_filter.SchDoc
		Print Date	28.11.2018 22:31:46 Sheet 7 of 10

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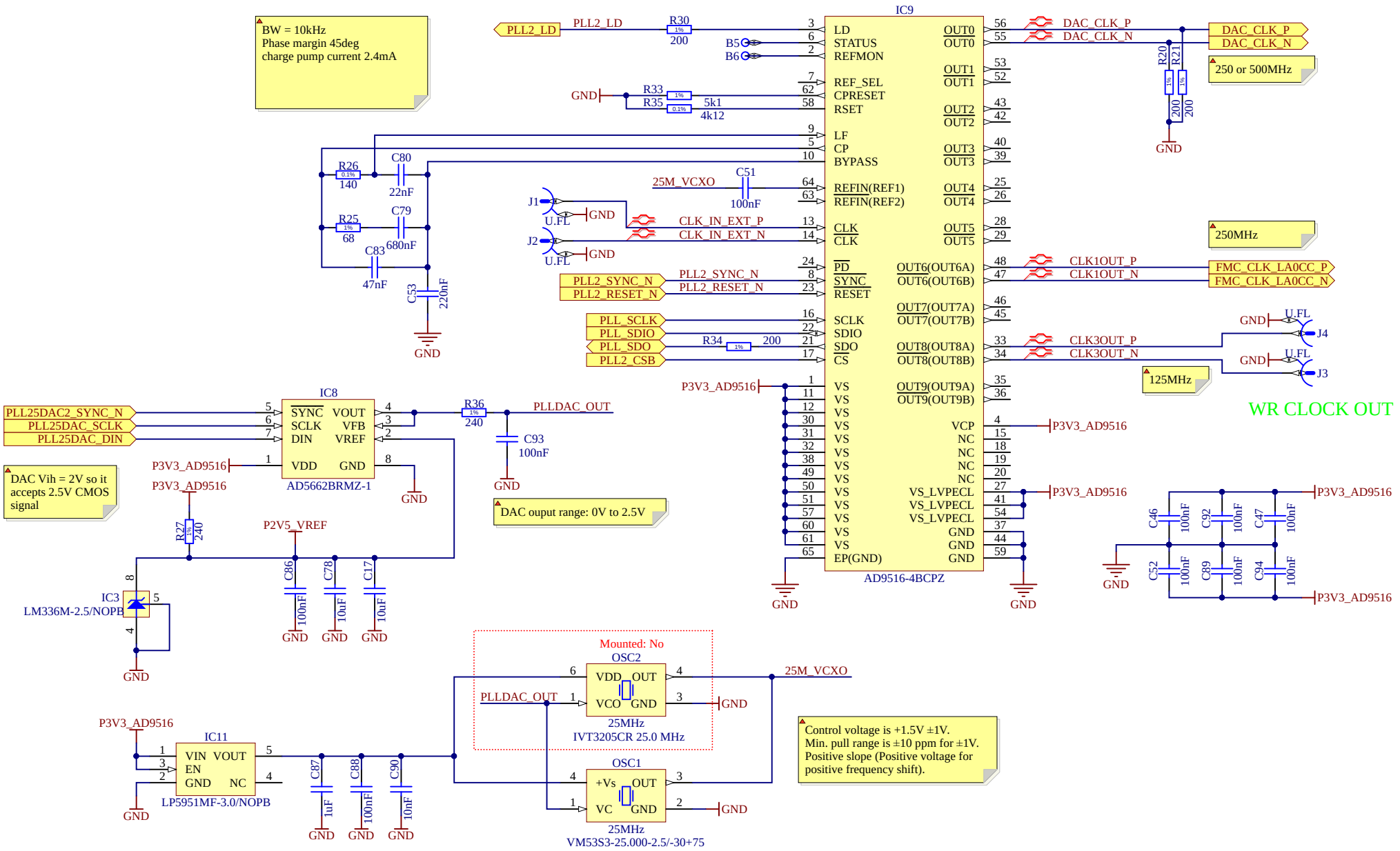

Project/Equipment	FMC DDS v2 (FMCDac600m12b1ChaDDS)
Document	**FMC DDS v2 - VCXO & PLL, WR Clock -**
Designer	G.K., T.W.
Drawn by	G.K., T.W. 04/07/2014
Check.by	B. Civel 16/07/2014
Last Mod.	B. Civel 28.11.2018
File	Clocking.SchDoc
Print Date	28.11.2018 22:31:46
Sheet	8 of 10
Size	A4
Rev	-

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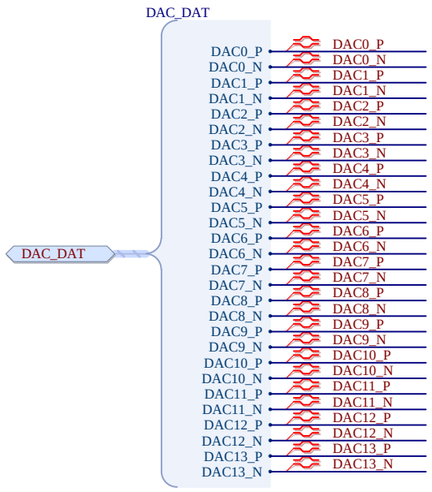

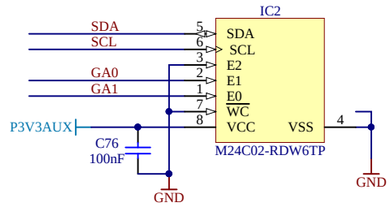

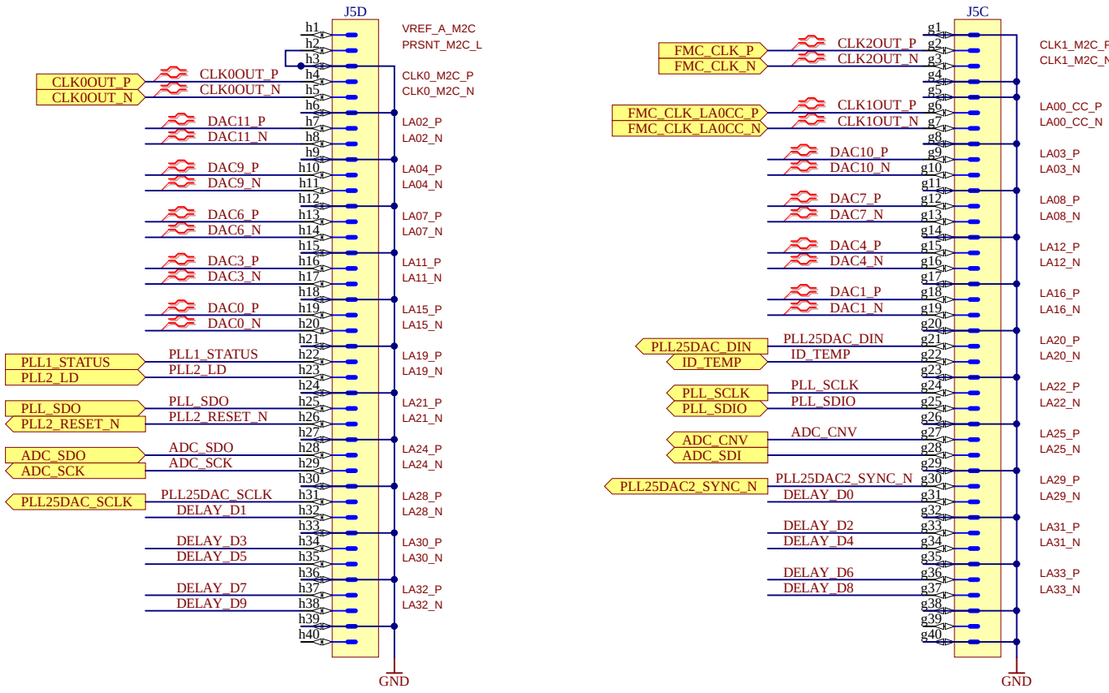

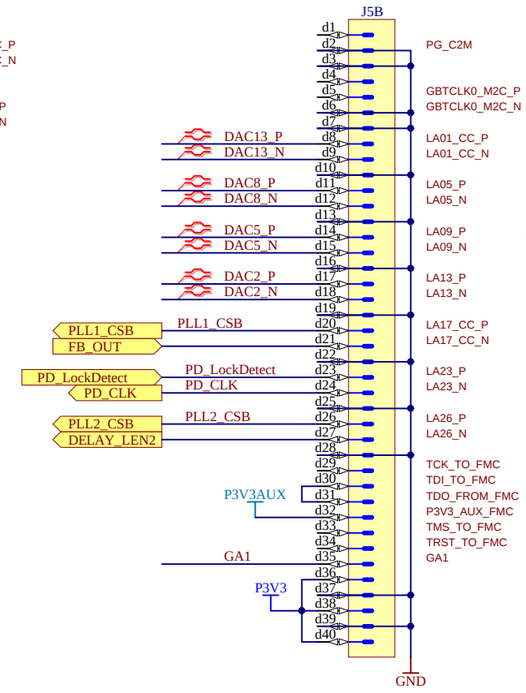

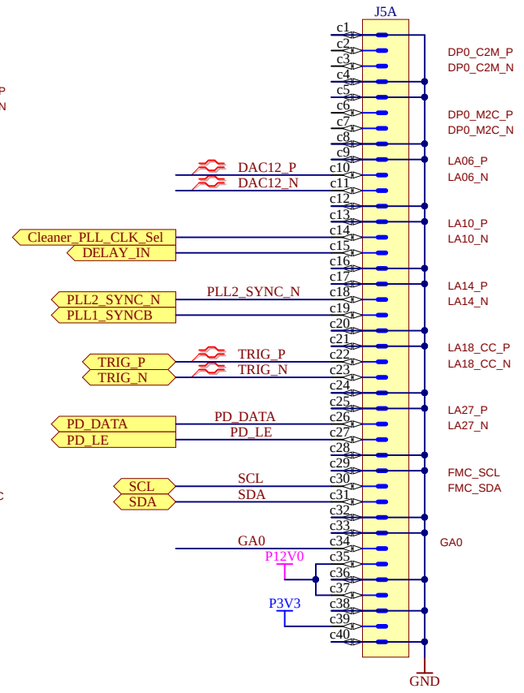

DELAY_D[9..0] DELAY_D[9..0]

FTG1 FTG6
FTG3 FTG4
FTG2 FTG5

Project/Equipment FMC DDS v2 (FMCDac600m12b1ChaDDS)

Document

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FMC DDS v2 - FMC Connector & EEPROM -

Designer	G.K., T.W.	
Drawn by	G.K., T.W.	04/07/2014
Check.by	B. Civel	16/07/2014
Last Mod.	B. Civel	28.11.2018
File	FMC.SchDoc	
Print Date	28.11.2018 22:31:46	Sheet 9 of 10

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MC100LVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used

VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV (or 2k2 resistor to GND) - LVTTL Mode (Note 5)

R/S inputs are low if unconnected

IC15 power

P3V3D P3V3D
C84 100nF C50 100nF
GND GND

IC10A
MC100EP29DTG

IC23A
SY100EPT23LZG

IC23B
SY100EPT23LZG

IC25
SN74LVT125D

Z50R
R6 10
FB_OUT
OUT
D2B BAR66
D2A BAR66

IC10B
MC100EP29DTG

IC16
SY89295UMG

DELAY_IN
CLK_DELAY_P
CLK_DELAY_N
FF_VBB
DELAY_LEN2
DELAY_D[9..0]

Temp sensor. Place under SY89295 chip.

ID_TEMP
IC22
DS18B20U+

Project/Equipment	FMC DDS v2 (FMCDac600m12b1ChaDDS)
Document	**FMC DDS v2 - Fine Delay, Output Buffers -**
Designer	G.K., T.W.
Drawn by	G.K., T.W. 04/07/2014
Check.by	B. Civel 16/07/2014
Last Mod.	B. Civel 28.11.2018
File	delay.SchDoc
Print Date	28.11.2018 22:31:47 Sheet 10 of 10

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