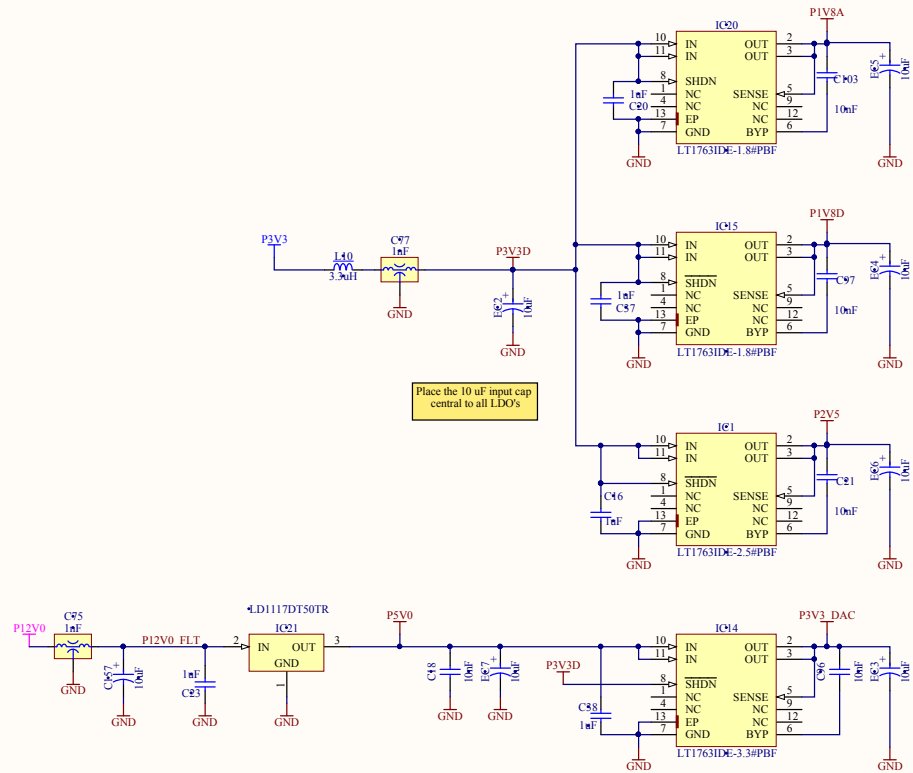


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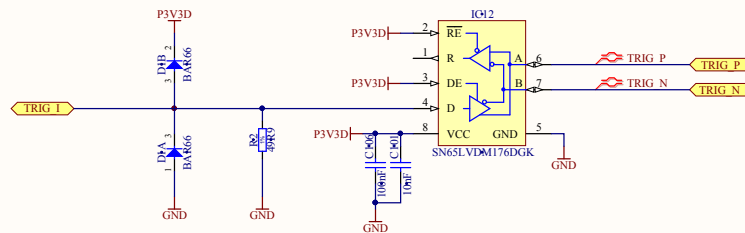
Place the 10 uF input cap central to all LDO's

Place all LT1763's on 100 mm² (min) pour. Device pad should have multiple (>6) 0.5 mm vias connecting to all ground planes, and be soldered to pour

Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)	
Document		Designer G.K. T.W.	
BE-CO		Drawn by G.K. T.W.	
CERN		Check by B. Civel	
		Last Mod. B. Civel	
		File Power SchDoc	
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		Sheet 2 of 10	
		A3	
		EDA-03010-V3-0	

FMC DDS v3
- Power Supply Regulators -

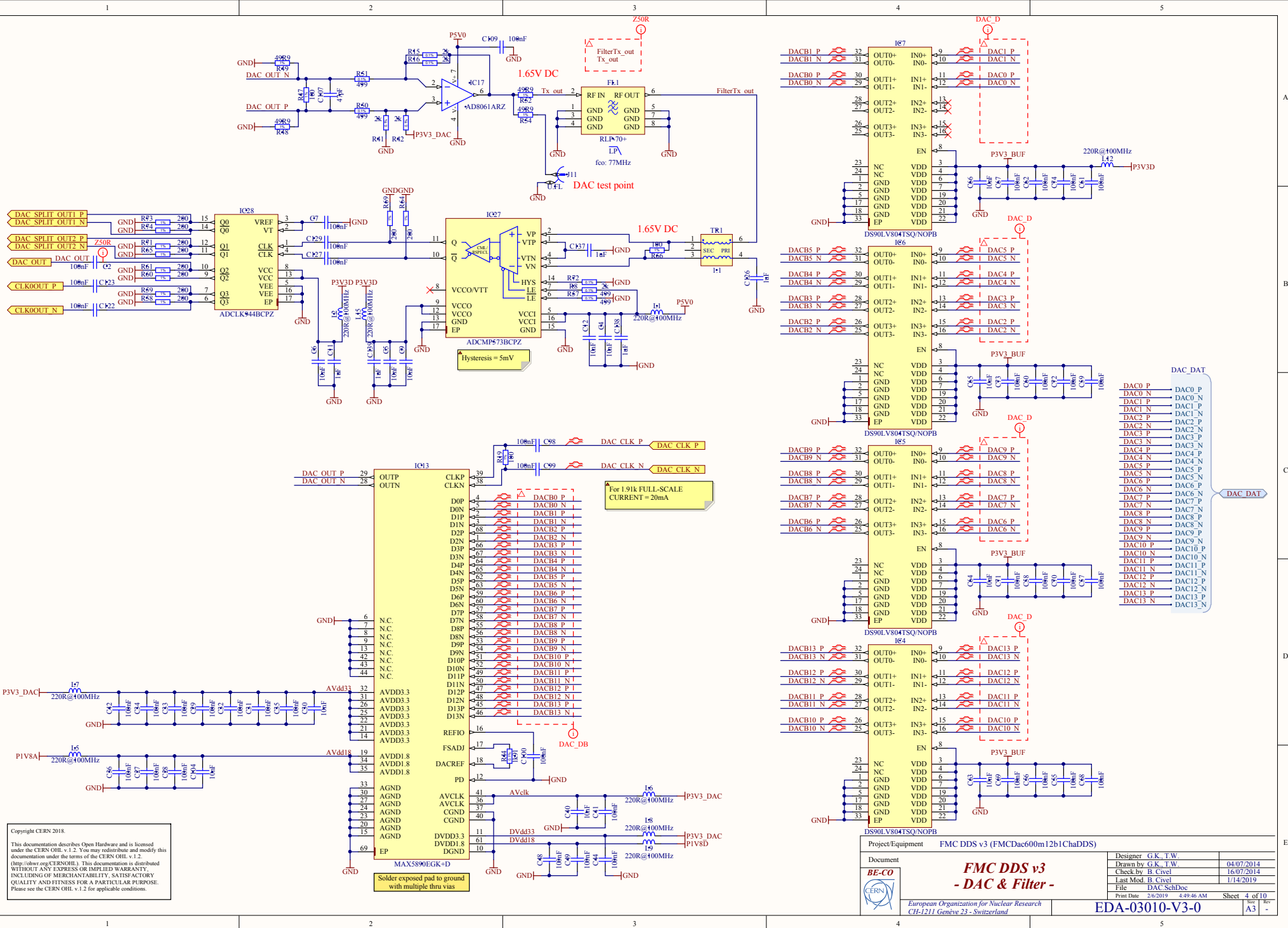
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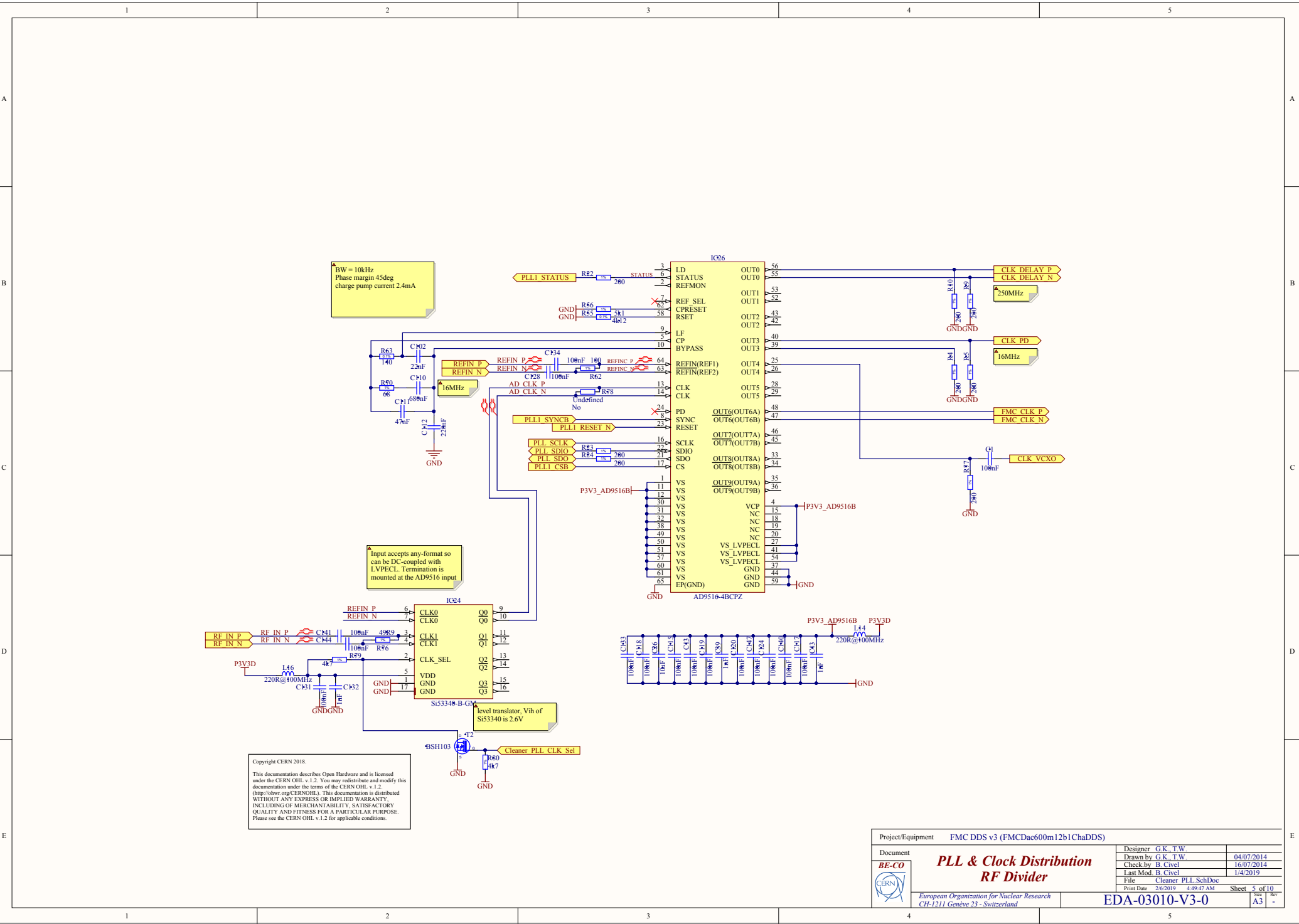


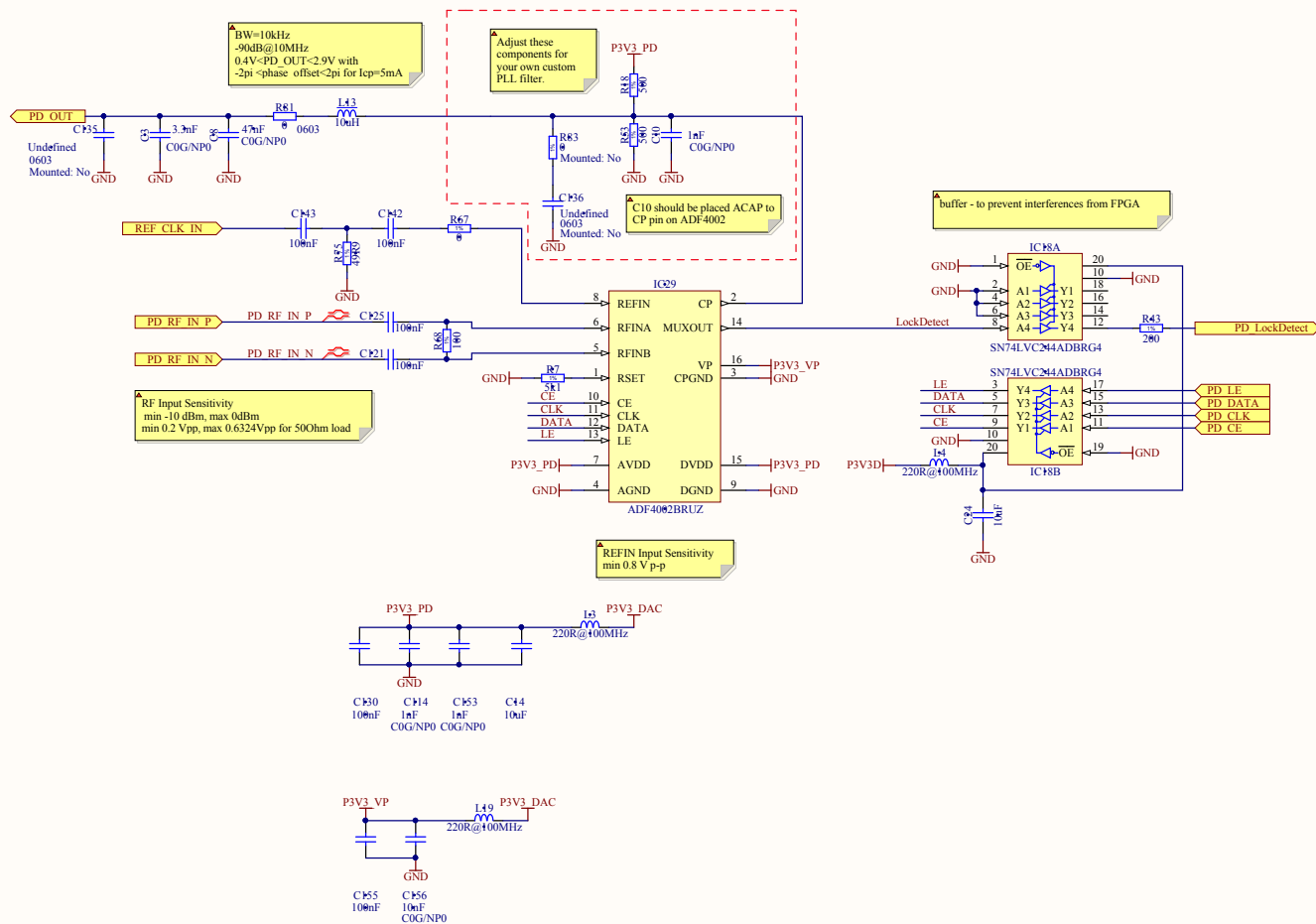
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Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)	
Document	Designer	G.K. T.W.	
	Drawn by	G.K. T.W.	04/07/2014
	Check by	B. Civel	16/07/2014
	Last Mod.	B. Civel	1/4/2019
	File	Trigger SchDoc	
Print Date		2/6/2019 4:49:46 AM	Sheet 3 of 10
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		A3	-





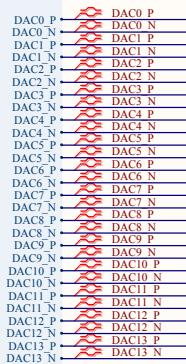


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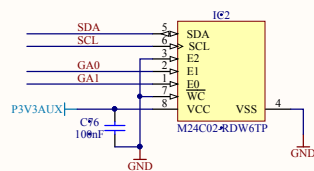
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Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)	
<div>Document</div> <div>BE-CO</div> <div>CERN</div>	Designer	G.K. T.W.	
	Drawn by	G.K. T.W.	04/07/2014
	Check by	B. Civel	16/07/2014
	Last Mod.	B. Civel	2/6/2019
	File	Phase detector SchDoc	
Print Date		2/6/2019 4:49:47 AM	Sheet 6 of 10
European Organization for Nuclear Research		CH-1211 Genève 23 - Switzerland	EDA-03010-V3-0
		A3	-

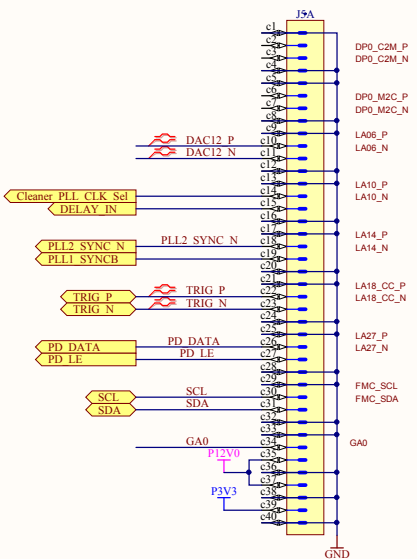
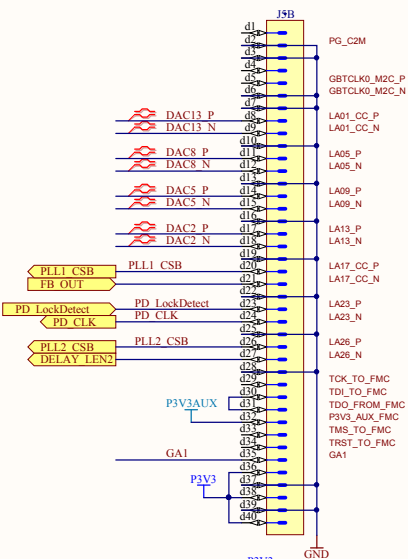
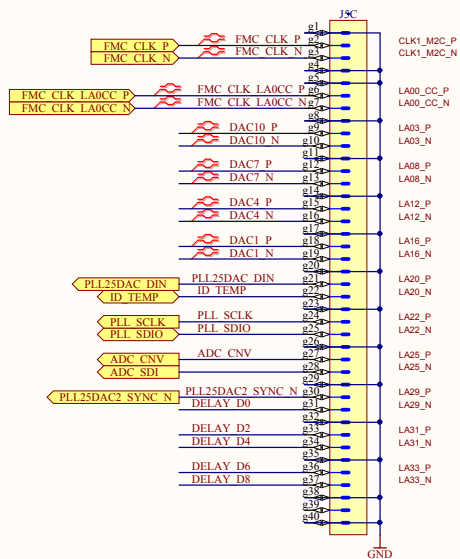
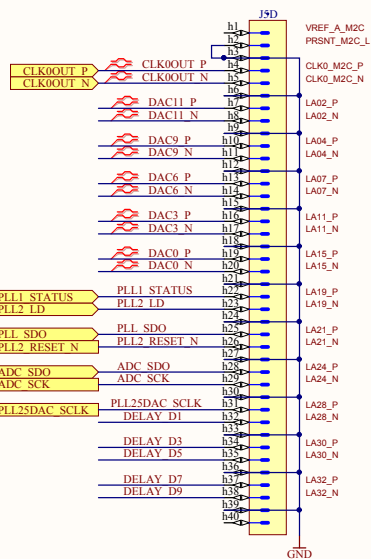
DAC DAT



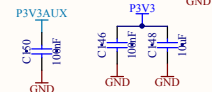
DAC DAT



Note on GA0, GA1 pins: they are connected IN REVERSE to the EEPROM address pins:
GA0->A1/E1
GA1->A0/E0.
This looks awkward, but so says the VITA FMC standard.



DELAY D[9:0] DELAY D[9:0]



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Project/Equipment	FMC DDS v3 (FMCDDac600m12b1ChaDDS)		
Document	BE-CO		
FMC DDS v3 - FMC Connector & EEPROM -		Designer	G.K. T.W.
		Drawn by	G.K. T.W.
		Check by	B. Civel
		Last Mod.	B. Civel
		File	FMC SchDoc
		Print Date	2/6/2019 4:49:47 AM
		Sheet	9 of 10
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