FmcAdc100M14b4cha

An informal description of the design

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Abstract

FmcAdc100M14b4cha is a 4 channel 14 bit 100MS/s ADC board with internal/external triggering in FMC (FPGA Mezzanine Card) format

1. What is it it?

FmcAdc100M14b4cha is 4 channel 14 bit ADC board in FMC (FPGA Mezzanine Card) standard. The maximum sampling speed is 100MS/s. The gain of each channel can be chosen from three values: +/-50mV/full scale, +/-0.5V/full scale and +/-5V/full scale. Voltage offset range is +/-5V and the offset's value is independent on the gain. The ADC board can be either externally or internally triggered. The task was to create the ADC measuring board which could be very flexible, fast and having a low noise level to be sufficient for many acquisition needing applications.

Thank AA

2. Board features & parameters

Table 1.

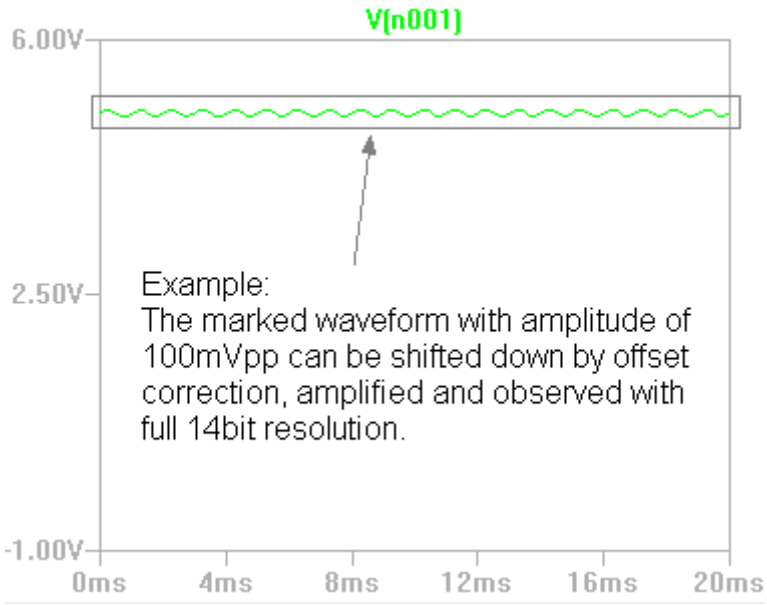
Parameter	**Value**
No. of channels	4
Input voltage ranges	+/-50mV, +/-0.5V, +/-5Vpp
Sampling speed	5 … 105MS/s
Analog bandwidth	25MHz
Offset range	+/-5V for all input voltage ranges
ADC resolution	14 bits
SNR for 100mVpp range	> 65dB
SNR for 1Vpp range	> 70dB
SNR for 10Vpp range	> 70dB
Input impedance	1kΩ / 50Ω (settable by software)
Maximum input voltage:	without termination: +/- 10V with 50Ω termination: +/- 7.5V
Maximum input overload (100ms):	without termination: +/- 25V with 50Ω termination: +/- 15V
Max. gain error calibrated	calibrated: < 0.5% Uncalibrated +/-50mV range: ~ 5% uncalibrated +/-0.5V range: ~ 1% uncalibrated +/-5V range: ~ 5%
Zero offset correction	Yes, may be done on request or after a power-on procedure, controlled by software
FMC to carrier interface	FMC high pin count connector with external clock FMC low pin count connector with internal clock
ADC to FPGA interface	Serial LVDS, 2 pairs for each channel
Internal sampling clock	Range: 10 … 105MHz, Jitter: 0.62ps
On-board thermometer	Present, therefore calibration or detecting the moment, when the board temperature is stable is possible.

3. What are the main goals we focused on?

The most important aim we focused on while creating this design was achieving the lowest possible noise level. Nowadays there is no problem with the bandwidth or slew rate parameter of operational amplifiers. Modern amplifier may have Gain Bandwidth Product over 1GHz, so speed requirement for analog stage hasn't been treated as a problem, as well as ADC sampling speed and resolution. Nowadays, ADCs following the sampling speed and the resolution requirements are available on the market. More attention was paid on the signal-to-noise ratio and power dissipation while choosing the best ADC for this board.

The need of adding a voltage offset correction in front of the board was a bit unusual because in most popular acquisition boards or oscilloscopes there is offset correction related to the input voltage range. It means that let's say +/- 5V can be added to the signal, but only in the 5V input offset range. When 50mV range is chosen, offset correction normally would be narrowed to +/- 50mV. In contrast in this design, the offset is independent on the input gain range and it is possible to magnify 100mVpp AC signal, on top of a DC base of +5V.

Requirement for that type of offset correction is its stability and high resolution. For example LSB of 16bit +/-5V offset correction is 0.15mV, typical zero error – 1mV. These values are easily visible on 100mV gain range. But remember, that DAC is just one from larger number of offset sources in this design.



The input peak-to-peak voltage range of FmcAdc100M14b4cha board can be chosen from three values (+/-50mV, +/-0.5V, +/-5V). This range can be changed by the software, which makes the board easy to use and adaptable to varying environment conditions.

The parameter, which determined the design structure mostly is the signal-to-noise ratio. Every amplifier choice and resistor value may degrade the SNR parameter. Flexibility and ease of use need to give up to SNR, if these parameters are against the noise. In FmcAdc100M14b4cha project, all the parameters could be achieved by proper analog stage idea and using modern, fast and very low noise components. The base of first idea was to create oscilloscope-like card, and therefore, to make it compatible with standard, input impedance should be equal 1MΩ. But because of resistor's and following amplifier's noise level, it was decided to make it lower – 1kΩ. This is one of the places, where compromise had to be made.

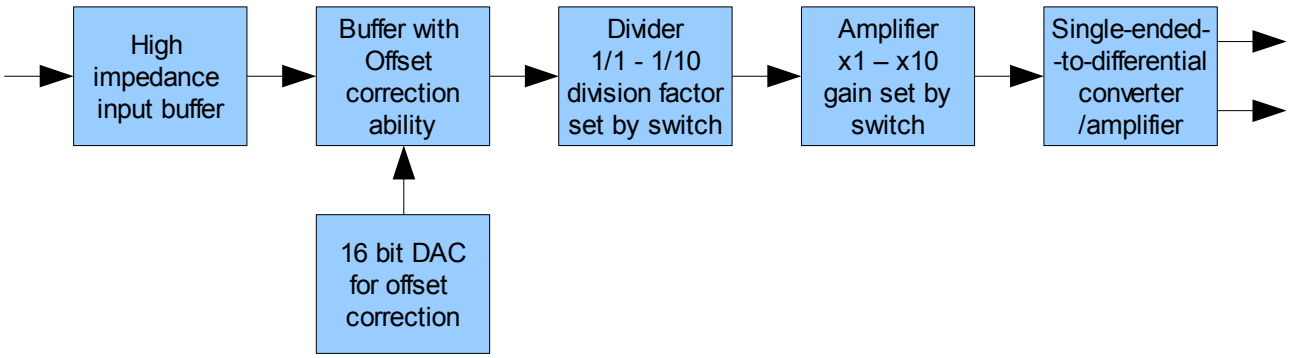
4. Closer look at the board structure

How to correlate low noise level, variable gain and offset correction at the input?

At first look, it seems to be impossible to reconcile parameters shown above. I also need to mention about high input impedance which is always nicely seen in measurement devices.

The first FmcAdc – the unsuccessful effort of matching the specification

Block schematic of the old architecture

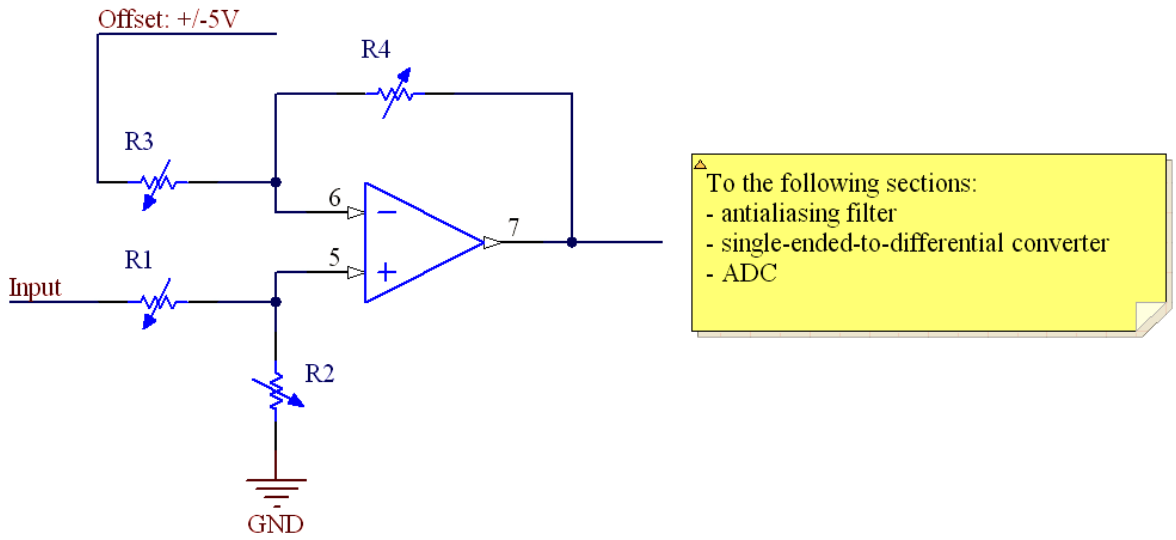


Even if the idea is clean and follows the common sense, there is a problem with noise level, large signal linearity and supply strategy. High impedance input buffer can base on fast JFET input amplifier. But voltage noise level is poor in comparison to bipolar amplifiers (5.4nV/√Hz vs. 0.9nV/√Hz). OK, so why do not use bipolar amplifier at the input? Theoretically it is possible, but its polarisation current of more than 5µA (typical for high linearity and fast opamps) will cause large input offset because of voltage drop on input resistor. It is possible to use another type very modern opamp, AD4899 made by Analog Devices, but it's supply voltage is limited to +/- 6V. Therefore it is impossible to include +/-5V input voltage range with +/-5V offset correction (maximum input voltage can reach +/-10V in that condition).

Buffer with offset correction, divider and following amplifier add unnecessary noise and nonlinearities. Estimated SNR for 100mVpp range is 45dB. It means that effective-number-of-bits (ENOB) parameter is almost... 8bits. Too bad for 14 bit resolution system.

Final idea, which bases on differential amplifier at the input.

Simplified schematic below explains the structure.



All the resistors are have the resistance switchable between 2 values, for ex. 100 & 1000Ω. If proportion the R3/R4 follows the R1/R2, the gain of the amplifier exactly equals R2/R1. So with these variable resistors it is possible to set the gain of the amplifier like shown below:

R1 = R3 value	R2 = R4	gain
100Ω	1000Ω	10 x
1000Ω	1000Ω	1 x
1000Ω	100Ω	0.1 x

Advantages of the new structure:

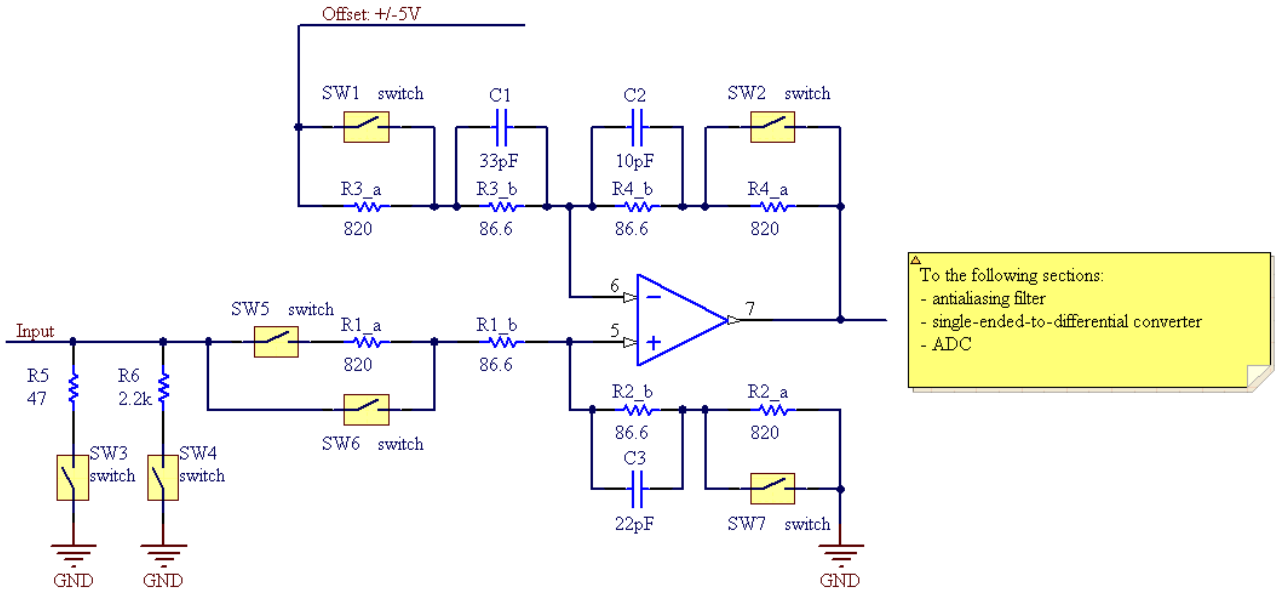
- lowest number of component possible to achieve,
- low noise level
- low distortion factor – opamp output voltage is lower than +/- 1V, so nonlinearities made by Slew Rate factor are reduced,
- thermal stability coming from symmetry of dividers,
- possibility of adding auto-calibration option,

- ability of changing gain by software,
- opamp doesn't need to be powered from high voltage. Input common mode voltage is always kept +/- 5V range. This make two main advantages:
    - supply strategy is simpler – only one switching supply (for creating negative voltage) is needed,
    - it is easier to find low noise, high speed, very linear opamp powered from +/- 6V (unlike the +/-15V).

Disadvantages:

- Only real disadvantage of the new input stage structure is restricted input resistance. There is no buffer preceding the resistors, so if low noise level is important (in this case, that goal is on the top of the list), resistor's values cannot be high. Example shown above well matches to the real values.
- Input impedance is varying while switching the gain. Needs to be corrected by additional parallel resistor (activated when 1x gain is set).

OK, the idea seems to be clear and easily adaptable in real design. But how to switch the resistors values and still keep it small, simple and stable? The following picture shows the solution used in FmcAdc card.

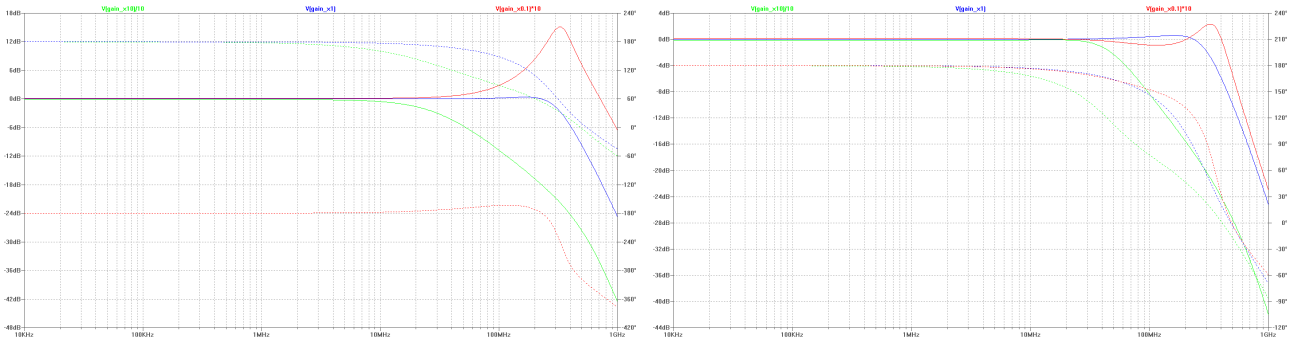


Switches SW1, SW2, SW6, SW7 are used to change the gain as mentioned above. Additional SW5 switch allow user to disconnect the amplifier from the input socket (SW6 must be turned-off too). This option is used to proceed the auto-calibration. SW4 activates R6 resistor, which corrects the input resistance to make it constant in spite of gain changes. SW3 allow user to activate 50Ω termination.

As the switches, AQY221N3M, MOSFET-based optocouplers are used. They are activated by LED light and shall work well in this conditions. Main parameters list is shown in the table below.

Dimensions	2.95 x 2.2 x 1.4
Max. current	150mA
Max. voltage	25V
Typ. resistance	5.5Ω
Max. resistance	7.5Ω
Typ. capacitance	1.1pF
Max. capacitance	1.5pF

Capacitors in parallel with resistors are put here for compensation of the frequency characteristic of the amplifier to increase the stability. Following pictures show the frequency response of the input stage.



a) input channel without compensation b) input channel with compensation

Going back to the switches and the stability issues... One thing that need to be explained more carefully is the initial precision, thermal stability of the input stage and what is the autocalibration option.

Let's treat the switches as the buttons with series resistance of about 5.5Ω. In the datasheet there is information, that max. switch resistance is 7.5Ω. Lets also imagine, that

in the worst condition, some of the switches will have the top possible resistance, some other – the lowest. The lowest possible resistance is not given in datasheet, so let's estimate it – 4Ω should be OK. Resistor's precision in signal path is 0.1%. Following table shows the precision of uncalibrated FmcAdc board for the worst possible case.

Gain range	**Gain precision [%]**	**Offset correction precision [mV] at the output @ 5V of offset at the input**
100mVpp	-2.8 / +0.65	-176 / +166
1Vpp	-0.2 / +0.1	-6.8 / +2.8
10Vpp	-1 / +3.3	-18.5 / +17.7

Gain accuracy is very satisfying even without doing any calibration and achieves the best value for 1Vpp input voltage range. This happens, because for this case, only one setting gain switch (**SW5**), main source of resistance mismatch, is activated.

The worse news is, that offset correction accuracy does not follow the gain precision and should be calibrated. It was simulated for 5V of voltage offset at the input corrected by 5V internal offset correction (for this estimation DAC for offset correction gives exactly 5V). If the components were ideal, there should be 0V at the output. Shown above output voltage should be related to the maximum expected voltage value which is +/- 1V.

Maximum input voltage

Limitation of maximum input voltage is caused by:

- Resistors' power dissipation ability. There is not much place on the board, so every component needs to be as small as possible. Heat dissipated by resistors makes the long term overload limit. Limit is 7.5V with 50Ω
- MOSFET switches maximum voltage. It is limited to 25V. Even short overload may cause switch damage, so this voltage is a hard limit.
- MOSFET switches maximum current is 150mA. It is makes limits only, if 50Ω termination is activated (highest current in input path is flowing through the SW3

and R5). Otherwise, limits mentioned in upper points are more important. Datasheet informs that for 100ms period, maximum current is 300mA, so such short period of time, even 15V could be attached to the 50Ω-terminated input.

Word about static electricity...

Input impedance of 1kΩ makes the limit of maximum voltage that can appear at the input. For maximum tolerable voltage of MOSFET switches, which is 25V, the current in this condition is exactly 25mA and not really possible to be generated by static charges. That's why for example resistors are not static charges sensitive. On the other hand, when board is not powered, and all the switches are turned-off, input impedance is made by R1_a, R1_b, R2_a, R2_b connected in series, which gives approximately 1.8kΩ. Not much higher, and rather also not problematic.

So how the idea of autocalibration will be looking like?

Our first idea was to avoid any initial calibration procedure, for making the fabrication process easier. Imagine, if you have hundred of boards to test, and they cannot be tested automatically (you need to install some cables, set some voltages), you try to make everything as precise as possible. Just plug the FmcAdc into the carrier, turn the power on, check, if there is communication between boards – the board is then tested.

After preceding estimation, it became clear, that autocalibration is necessary. The procedure is divided into points.

a) **SW5** and **SW6** is switched off, so the input socket is disconnected from the input amplifier. The DAC value (for offset calibration) should be set to 0V. Then, after measurement the voltage by internal ADC, it is possible to save the digital and analogue input offset of the amplifier. The ADC value should be stored into memory.

b) Very precise voltage source should be connected to the input (it may be done before doing **a)** point). For the 1Vpp input voltage range, to achieve the best precision, the voltage should be close to the half of the max. input peak-to-peak value but not exceeding the +/- input voltage limit, when the worst initial gain

condition occurs (in this case, the 0.4V will be OK). Then you can measure the overall gain of the amplifier with the internal amplifier, DAC and ADC offset reduced. This measurement gives the gain of whole chain – the voltage scale factor. This value should also be stored into memory.

c) The last thing to do is calibrating offset DAC. Voltage value of precise voltage source should be changed to the 5V. Then, the DAC output voltage is regulated until the ADC measures the value closest to zero (including the correction made in point **a)**). Now you know, that DAC gives exactly the same voltage, as the calibration voltage source and DAC voltage scale factor can be stored into memory.

The calibration procedure should be repeated for all the four channels and for all three amplifier gain factors.

Now, during every start-up it is possible to measure and reduce offset just by disconnecting the input socket from the amplifier (switching-off **SW5** and **SW6**).

Offset sources in FmcAdc:

- operational amplifier voltage offset, current offset and polarisation current,
- DAC voltage offset,
- offset made by following stage (single-ended-to-differential converter, ADC).

Shown above parameters will vary during the changing temperature condition and ageing process. That's why initial, main, calibration should be repeated let's say once a year, or two years. Offset reduction needs to be involved into the start-up procedure, or repeated in every ten hours, or after every user request.

Estimated performance can be read from the table. After doing the initial calibration procedure, and offset reduction every time, when the card is being turned on, gain precision should come to about +/-0.2%.

Choice of operational amplifier

Unfortunately there are not many options to choose in the market. Below, there is the list of parameters, which need to be fulfilled by the opamp. They are mutually exclusive mostly.

- low voltage and current noise level (focus on bipolar input amplifiers),
- low voltage offset (the same situation as above),
- low polarisation current (it makes voltage drop on input impedance which increase the voltage offset – JFET and CMOS type would be the best),
- high speed (25MHz bandwidth * 10 gives GBW = 250MHz and 157V/µs),
- unity gain stable,
- low distortion level (must be accurate for 14bit system),
- overloads and static electricity resistance (CMOS type is not allowed here),
- inputs needs tolerate up to +/- 5V, which forces supply voltage to be higher than at least +/-5V (in case of using rail-to-rail input opamp).

The best choice was the ADA4899 from Analog Devices. There were no real opponent for this part, so following table contains parameters only for this device not related for any other.

Parameter	**value**
Voltage noise	1 nV/sqrt(Hz)
Current noise	5.2 pA/sqrt(Hz)
Polarisation current	100 nA
GBW	600 MHz
Slew rate	310 V/µs
Max. supply voltage	+/- 6V
Distortion level	-80 dB@10MHz

Some noise estimation for the most sensitive gain

Maximum input in this case AC voltage is 100mVpp, which gives 35mV of RMS value. At the output, there will be 350mV of RMS voltage. Bandwidth is 25MHz and it is cut

sharply, so for the noise estimation, we can use this value as equivalent noise bandwidth.

Noise equation for differential amplifier related to the output:

$$\sqrt{2\,(i_n * R2)^2 + \left(e_n\left(\frac{R_1+R_2}{R_1}\right)\right)^2 + 8\,k\,T\,R_2\left(\frac{R_1+R_2}{R_1}\right)} * \sqrt{BW}$$

The equation is valid, when R1 = R3 and R2 = R4.

R1 = 90Ω

R2 = 900Ω

i_n = 5.2pA/sqrt(Hz) - opamp current noise

u_n = 1nV/sqrt(Hz) - opamp voltage noise

k= 1.33*10^23 - Boltzmann constant

BW = 25MHz - equivalent noise bandwidth

RMS noise level is 105μV, so the dB SNR is:

350mV / 105μV = $3.33 * 10^3$ => 70.5dB

The performance is great for this gain range, and will be better for two others. For estimation of the whole chain, we need to take into consideration the single-ended-to-differential converter's noise and the ADC's SNR.

What is single-ended-to-differential converter (or amplifier) for?

Well, most of high speed ADC are equipped with differential inputs to avoid problem of thermal instability and interference (which could appear on ground layer). Simplest idea of wiring one of inputs to the ground and driving the left one by input signal is unfortunately prohibited here. Usually ADCs need to have the input common mode voltage kept in the middle between supply lines, so special converter is needed.

The table shows the key parameters of fully differential amplifiers usually used for such conversion.

Type	**BW (MHz)**	**Slew Rate (V/us)**	**DC offset (mV)**	**SFDR (dBc)**
AD8138	320	1150	1	-94 @ 5MHz
THS4131	225	51	2	-88 @ 1MHz
THS4141	205	450	7	-84 @ 1MHz
LMH6551	370	2400	0.5	-94 @ 5MHz

In this design, LMH6551 has been used because of it's performance.

About noise level added by this stage... internal noise is very small (6nV / sqrt(Hz) and 1.5pA / sqrt(Hz)), as well as gain and resistances, so its addition to the overall noise is negligible.

OK – what to do with antialiasing filter? The max. sampling speed is 100MS/s so, if the cut off frequency (25MHz) is not very close to the Nyquist frequency, the edges of the filter may not be very sharp. It has been decided to use 4 pole LC filter. The easiest way of filtering is making this filter as a simple compact single-ended filter in front of the single-ended-to-differential converter. Lowest number component is achieved (just two capacitors and two inductors). But the wideband noise made by differential amplifier is not filtered and reduces performance (ADC's bandwidth is usually much higher than sampling frequency). So from this point of view, filter should be located at the output of the amplifier and be differential (4 inductors instead of two). The compromise is to divide filter into 2 parts, and put a half of it in front of amplifier, and a another half – at the output of amplifier. It is then both simple and effective.

Finally the ADC!

This is the key element of the FmcAdc board. Nowadays it is possible to buy even 16bit ADC with sampling speed two times higher than in the FmcAdc spec. But don't became to enthusiastic. There is a lot of disadvantages of pipelined architecture (every ADC type with that sampling speed). Those thing are listed below with some remarks to make you feel the problem better.

- Pipelined architecture, which is still not perfect, even if it's the best you can get.

  What does it mean? It means, that in the body of ADC there is couple (three or four) 4 or 5 - bit ADCs and this number minus one (two or three) DACs. In fact, internal architecture is more complicated, but just for explanation, imagine that our ADC is 16-bit, and contains 4 small ADCs and 3 DACs.

  First ADC does very grainy (only 4-bit resolution) measurement, stores it and sent the value to the following DAC. ADC's measurement gives 4 most significant bits of all 16 bits of final value. The DAC output voltage is subtracted from the original sampled voltage, so after the subtraction, there is the result – small voltage containing 12 bit, from full 16 bit resolution. This “rest” is amplified in analog way and measured by another ADC. Now we know another 4 bits, so in summary – 8 bits have been measured. Measurement done by second ADC is sent to second DAC and the voltages are subtracted once again, and then amplified. The queue works until the last bits became known. Collecting stored bits together gives the whole measurement. Now its clean what does the name of the architecture come from.

  As you can see, the measurement process is very complicated. The subtraction results are stored as a charge in the capacitors, amplified, converted etc. It is not simple, so as the result, output performance measured by Effective Number Of Bits factor is far from the 14 of 16 bits read in the ADC description. There are some methods of making the transition characteristic more linear and to improve the measure ability, if you are doing operation in frequency domain. But for normal acquiring system – ENOB factor (converted to the SINAD) is the most important and reliable parameter (in case of 14 bit ADC, ENOB is more or less 12 bits).

- SINAD (Signal-to-Noise-and-Distortion ratio)

  parameter that collects distortion and noise together and therefore gives most truthful information about ADC performance. It may be converted to the ENOB. As it was stated above, for time-domain single shot sampling system, this is the most imported property.

  $$ENOB = \frac{SINAD - 1.76\text{dB}}{6.02}$$

- Number of channels

  It is of course related to the simplicity of the design, and amount of place taken in the board. But it is mostly about clock providing to avoid jitter and phase shift between clock edges for ADCs. If four-channel type is chosen, these problems are solved by internal connections in package.

- Power consumption.

  Boards in FMC format are small are there is no forced cooling, so power dissipation should be kept in low level.

- Sampling speed and bandwidth

  It's clear, that ADC for this particular application should match the spec.

- Digital interface

  Because of the number of channels, using ADC with parallel 14-bit output for each channel would be problematic. On the other side, fully serial interface needs fast interface on the carrier side and may make problems with electrical compatibility and noises. We choose the serial one to try to keep in low pin count connector standard and make the on-board connections simpler. This concern of choosing connector will be explained later.

Type	Sampling speed (MS/s)	SNR (dBc)	INL / DNL typical (bits)	Power dissipation (mW)	Interface	Number of ADCs in package	Clock range min/max (MHz)
LTC2174	105	73	1 / 0.3	545	Serial LVDS	4	5 … 105
LTC 2267	105	73,1	1 / 0.3	300	Serial LVDS	2	5 … 105
ADC14DS105	105	73	1.5 / 0.5	1060	Serial LVDS	2	25 … 105
ADS6444	105	73	5 / 2.5	1350	Serial LVDS	4	5 … 105
AD9640	105	71,6	3 / 0.4	750	Serial LVDS	2	10 … 105

ADC on the top of the table is the winner. It's performance is great, current consumption small, and feature of containing four ADCs in one package is very nicely seen. It is communicating with the FPGA by serial interface, but for each channel there is two line pairs for communication. It makes transmission speed lower. Overall necessary number of lines is still small.

Clock source... sounds simple, so where is the problem?

At the beginning – indeed, there is a problem. It is not about the frequency stability or interface type but mainly about the jitter. If you want to keep the voltage noise level lower then 0.5 LSB even if the highest possible frequency is being sampled, for this conditions (25MHz, 14bit) clock jitter has to be lower than 0.388 ps. This is the result of simple equation:

$$t_j = \frac{1}{\Pi * f_{sig} * 2^{N+1}}$$

For being aware how hard it may be to achieve such parameters, take into consideration that normal (but looking solid and stable) quartz based generator has jitter of about 1.3ps – to bad to be sampling time base for this system. According to the board spec, FmcAdc is designed to have ability of being clocked either externally, or internally. So to make it easy, kind of multiplexer should be included in the board. But even best

available muxes add jitter of more or less 1ps to the signal. That's why there is no multiplexer on the board and the clock source is chosen during fabrication process simply by mounting coupling capacitors in proper place (they function as a jumpers).

External clock is delivered by dedicated clock lines of SAMTEC connector. Clock signal is generated by special PLL generator on carrier board. Carrier board specification guarantees that phase noise, jitter and frequency stability will be appropriate for ADC driving.

For internal clock, Si570 is working. This is integrated circuit looking like normal crystal based oscillator. But it has I2C interface which allows user to choose the clock frequency from the range from 10 to 280MHz (software will restrict the upper frequency to 100MHz). Frequency value can be set very precisely because of internal DDS in the generator core. Its clock jitter is 0.62ps and because of troubles with finding much better source with lower jitter, it is decided to use it as is.

External trigger

FmcAdc card will be working with carrier board containing FPGA and SRAM memory. This set of devices allow user to make measurements on request. External or internal trigger can begin or finish measurement process. For external triggering, digital single-ended-to-LVDS interface is included into the FmcAdc board.

The idea bases on LVDS buffer, which is in fact kind of differential amplifier. Inverting input is connected to stable voltage and non-inverting input is driven by the trigger signal. This stable voltage sets the threshold. Four resistors and two diodes are for the input protection, so the input will not be damaged even if constant overload of +/-7.5V (or higher, but for short term) occurs.

Normally, the input should be connected to 50Ω line terminated on both sides, so if driving logic is powered from 3.3V, logic “one” will be 1.65V (3.3V divided by two). For logic powered from 5V – it is 2.5V. Threshold is set in the middle between halves of these values. You can imagine, that will be nice, if trigger could tolerate normal CMOS logic powered from 5V, which could be occasionally connected here. For normal condition, input voltage should not exceed +5V/-0.9V. Otherwise will be clamped by protecting diodes.

Power supply

Analog part of the design needs negative voltage to work, so at least one switching

power supply must be on board. The good news is, that one is enough. All other necessary voltages are created by linear regulator from the available voltages.

Supply voltages list with loads

Value	Load	Method of obtaining voltage
+12V	-	From carrier board
+6V	140mA	From 12V, reduced by linear regulator
+3.3V	-	From carrier board
+1.8V	300mA	From carrier: VADJ set to the 2.5V and reduced by LDO regulator
-8V	40mA	Switching supply
-6V	140mA	From -8V, reduced by linear regulator

Estimated power dissipation on linear regulators

Voltage	Power
+1.8V	210mW
+6V	840mW
-6V	280mW

Regulator used in FmcAdc

- for +6V
  LT3080, small package, voltage set by single resistor

- for -6V
  LT1175, small package, output current and power dissipation is sufficient for this application

- for +1.8V

  LT1763, small low voltage LDO regulator. We could use just VADJ voltage set to 1.8V and do some filtering, but some carrier boards do not support variable voltage option, and the VADJ is fixed (like in case of Xilinx FPGA test boards – 2.5V). So it was decided to use small LDO regulator to keeps the compatibility with larger number of carrier boards (which doesn't cost much).

- for -8V

  For creating negative voltage from available positive, switching supply was used. LT1931 is a regulator working in CUK configuration. Great advantage of CUK converter is possibility of reaching very low noise level. According to the datasheet, output ripple level is about 1mVpp. Switching frequency is high (approx. 2.2MHz) so output capacitor is small (because it's ceramic type) as well as inductor.

Mezzanine-To-Carrier interface

FmcAdc communicte with carrier board by SAMTEC VITA-57 connector. I/O voltage for normal, single ended lines (SPI and I2C interface, MOSFET switches etc.) are in 2.5V CMOS standard (it is forced by VADJ voltage). Differential pairs (ADC output, clock lines, trigger) are in the LVDS standard.

Following table contains the list of all the lines used in project with the description about the purpose.

Description	Line name	Logic standard
SPI – SCK	LA31_P	CMOS 2.5V
SPI – DIN	LA31_N	CMOS 2.5V
SPI – SDO	LA06_N	CMOS 2.5V
SPI – DAC_RST	LA30_N	CMOS 2.5V
SPI – CS_ADC	LA30_P	CMOS 2.5V
SPI – CS_DAC_CH1	LA32_P	CMOS 2.5V
SPI – CS_DAC_CH2	LA32_N	CMOS 2.5V
SPI – CS_DAC_CH3	LA33_P	CMOS 2.5V
SPI – CS_DAC_CH4	LA33_N	CMOS 2.5V

LED_TOP	LA28_P	CMOS 2.5V
LED_BOTTOM	LA28_N	CMOS 2.5V
CLOCK_ENABLE	LA06_P	CMOS 2.5V
SCL_2	LA01_P_CC	CMOS 2.5V
SDA_2	LA01_N_CC	CMOS 2.5V
CLOCK_OUT_P	CLK2_BIDIR_P	LVDS
CLOCK_OUT_N	CLK2_BIDIR_N	LVDS
TRIG_P	LA00_P_CC	LVDS
TRIG_N	LA00_N_CC	LVDS
ADC_DCO_CLK_P	CLK0_M2C_P	LVDS
ADC_DCO_CLK_N	CLK0_M2C_N	LVDS
ADC_FR_CLK_P	CLK1_M2C_P	LVDS
ADC_FR_CLK_P	CLK1_M2C_N	LVDS
ADC_OUT_1_A_P	LA27_P	LVDS
ADC_OUT_1_A_N	LA27_N	LVDS
ADC_OUT_1_B_P	LA26_P	LVDS
ADC_OUT_1_B_N	LA26_N	LVDS
ADC_OUT_2_A_P	LA23_P	LVDS
ADC_OUT_2_A_N	LA23_N	LVDS
ADC_OUT_2_B_P	LA14_P	LVDS
ADC_OUT_2_B_N	LA14_N	LVDS
ADC_OUT_3_A_P	LA13_P	LVDS
ADC_OUT_3_A_N	LA13_N	LVDS
ADC_OUT_3_B_P	LA10_P	LVDS
ADC_OUT_3_B_N	LA10_N	LVDS
ADC_OUT_4_A_P	LA09_P	LVDS
ADC_OUT_4_A_N	LA09_N	LVDS
ADC_OUT_4_B_P	LA05_P	LVDS
ADC_OUT_4_B_N	LA05_N	LVDS
SW1_CH1	LA21_P	CMOS2.5V
SW2_CH1	LA21_N	CMOS2.5V
SW3_CH1	LA25_P	CMOS2.5V
SW4_CH1	LA25_N	CMOS2.5V
SW5_CH1	LA24_P	CMOS2.5V
SW6_CH1	LA24_N	CMOS2.5V
SW7_CH1	LA29_P	CMOS2.5V

SW1_CH2	LA15_P	CMOS2.5V
SW2_CH2	LA15_N	CMOS2.5V
SW3_CH2	LA20_P	CMOS2.5V
SW4_CH2	LA20_N	CMOS2.5V
SW5_CH2	LA19_P	CMOS2.5V
SW6_CH2	LA19_N	CMOS2.5V
SW7_CH2	LA22_P	CMOS2.5V
SW1_CH3	LA07_P	CMOS2.5V
SW2_CH3	LA07_N	CMOS2.5V
SW3_CH3	LA12_P	CMOS2.5V
SW4_CH3	LA12_N	CMOS2.5V
SW5_CH3	LA11_P	CMOS2.5V
SW6_CH3	LA11_N	CMOS2.5V
SW7_CH3	LA16_P	CMOS2.5V
SW1_CH4	LA02_P	CMOS2.5V
SW2_CH4	LA02_N	CMOS2.5V
SW3_CH4	LA03_P	CMOS2.5V
SW4_CH4	LA03_N	CMOS2.5V
SW5_CH4	LA04_P	CMOS2.5V
SW6_CH4	LA04_N	CMOS2.5V
SW7_CH4	LA08_P	CMOS2.5V

Table shows the switch configuration for particular modes of operation.

Input voltage range	**SW1**	**SW2**	**SW3**	**SW4**	**SW5**	**SW6**	**SW7**
+/-50mV	ON	ON	OFF	-	OFF	ON	OFF
+/-0.5V	ON	OFF	OFF	-	ON	OFF	OFF
+/-5V	ON	OFF	OF	-	OFF	OFF	ON
Offset calibration	OFF	OFF	OFF	OFF	OFF	OFF	ON
50Ω termination				ON			

ON – line driving the switch in HIGH state

OFF – line driving the switch in LOW state