Sampling clock domain

System clock domain

Ch. 1
Ch. 2
Ch. 3
Ch. 4

Trigger unit

Sync FIFO

Trigger time-tag

Data

Trigger

Single-shot

Multi-shot

DPRAM 0

DPRAM 1

Acq. FSM

Commands

Pre-trig cnt

Post-trig cnt

Shots cnt

Addr. cnt A

Addr. cnt B

addr_a @ trig
addr_a @ post_done

Flow control FIFO

Wishbone master interface