Abstract

Obsolescence of the negative supply inductor ref L1, has forced a production component change. These measurements quantify the impact of this change on the performance of the ADC. This work follows on from the previous report which quantified all aspects of the performance of the ADC.
## Revision History

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<th>Changes Made</th>
<th>Date</th>
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<td>1</td>
<td>First issue</td>
<td>12-Sep-19</td>
<td>SEC</td>
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<td>2</td>
<td>Update of results with Wurth &amp; Sumida inductors</td>
<td>04-Oct-19</td>
<td>SEC</td>
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<td>3</td>
<td>Update of results with Bourns &amp; Eaton DRQ73 inductors</td>
<td>21-Oct-19</td>
<td>SEC</td>
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1 References

1. “CERN Integration & Measurement Results 04.doc”, dated 4th October 2017, authors Steve Carpenter & Alex Carpenter, company Sundance Multiprocessor Technology Ltd.

2. “CERN ADC Development 02.doc”, dated 29th November 2017, author Steve Carpenter, company Sundance Multiprocessor Technology Ltd.

2 Foreword

Obsolescence of the negative supply inductor L1 has forced a production component change. These measurements quantify the impact of this change on the performance of the ADC. This work follows on from the previous report which quantified all aspects of the performance of the ADC.

Eaton / Cooper Bussman have made the CTX10-1A-R which is specified for the negative voltage generator inductor L1 obsolete. To be specific, they have made the -1A, -2A, -3A versions of the CTX10 obsolete. The following is an extract from an email from Incaa computers which details the production issue and recommended solution, dated 18th July 2019:

“We looked at it and Rene came with the following:


<table>
<thead>
<tr>
<th>Part</th>
<th>Parallel open circuit inductance [uH]</th>
<th>Parallel full load current [A (dc)]</th>
<th>Parallel DC resistance [Ohm (max)]</th>
<th>Series open circuit inductance [uH]</th>
<th>Series full load current [A(dC)]</th>
<th>Series DC resistance [Ohm (max)]</th>
<th>Height [mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTX10-1A-R</td>
<td>10.58</td>
<td>2.5</td>
<td>0.046</td>
<td>42.30</td>
<td>1.25</td>
<td>0.183</td>
<td>4.19</td>
</tr>
<tr>
<td>CTX10-2R</td>
<td>10.58</td>
<td>2.5</td>
<td>0.031</td>
<td>42.30</td>
<td>1.25</td>
<td>0.125</td>
<td>5.97</td>
</tr>
<tr>
<td>CTX10-1R</td>
<td>10.00</td>
<td>1.9</td>
<td>0.044</td>
<td>40.00</td>
<td>0.95</td>
<td>0.176</td>
<td>4.19</td>
</tr>
<tr>
<td>CTX10-1P-R</td>
<td>9.62</td>
<td>1.8</td>
<td>0.052</td>
<td>38.48</td>
<td>0.85</td>
<td>0.227</td>
<td>4.19</td>
</tr>
</tbody>
</table>
The big difference between the CTX10-1A-R and the CTX10-2-R, CTX10-1-R or CTX10-1P-R is the used core material. De CTX10-1A-R is an OCTA-PAC PLUS, the CTX10-2-R and CTX10-1-R are an OCTA-PAC, and the CTX10-1P-R is a ECONO-PAC.

OCTA-PAC's are designed around high frequency, low loss core material. ECONO-PAC's are a lower cost version of OCTAPAC’s offering high saturation flux density, Iron powder core material. OCTA-PAC PLUS's offer higher current ratings and higher saturation flux densities than OCTAPAC and ECONO-PAC, Amorphous metal core material.

The advantage of the ‘higher current ratings and higher saturation flux densities’ for the originally used CTX10-1A-R in a lower size device can be replaced by the higher size CTX10-2-R device which has about the same specifications. Het problem of the CTX10-2-R is however its height. The FMC specification states that the height of the part located in component envelope (see ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard, Figure 3) can only be 4.7mm high (see Figure 9), so the CTX10-2-R is not allowed, as it is situated on the EDA-02063 Fmc Adc 100M 14b 4cha within that area.

The next best is the CTX10-1-R which has a slightly lower inductance and a slightly lower full load current specification.

The power circuit of the EDA-02063 Fmc Adc 100M 14b 4cha, using the inductor as L1 and the LT1931ES5 (IC21) as switching regulator, can only provide 350mA. The LT1931 datasheet states: "When using coupled inductors, choose one that can handle at least 1A of current without saturating, and ensure that the inductor has a low DCR (copper-wire resistance) to minimize I^2R power losses." The datasheet even suggests the CTX10-1.

So you could ask yourself why in the original design the CTX10-1A-R was chosen and not the CTX10-1-R. This seems to have been a choice based on tests. The EDA-02063 Fmc Adc 100M 14b 4cha V1.0 used a SDQ12-4R7-R which is 4.7uH. If a 10uH equivalent should have been the better value, a SDQ12-100-R could have been a drop in replacement. As of the V2.0 version of the design the CTX10-1A-R is used and not the CTX10-1-R. There are no design review documents available on the ohwr site regarding this design change to V2.0, so it is unknown why this part is changed.

A change from the CTX10-1A-R to the CTX10-1-R for the V5.0 version could have some potential influence on the characteristics of the LT1931ES5 circuit, which could be shown in the form of a difference noise floor or a different amplitude of spurious frequencies in the measured signals. This can only be checked by an investigation by means of measurements.

Met vriendelijke groet, / Best regards, / 謹致问候,

Bart Sijbrandij

This report details measurements of the noise floor of different boards fitted with the CTX10-1A-R and with the CTX10-1-R.
The report uses techniques developed in reference 1, and builds on the reported results.
3 System Integration

3.1 Installation

The working installation was created by installing Ubuntu 19.04 on a Dell Dimension 5150 with a clean 1G Byte hard disc. Thanks go to Dimitris Lampridis for assistance with the installation, and for updating the following installation instructions:

https://www.ohwr.org/project/fmc-adc-100m14b4cha-sw/wikis/Software-setup-from-scratch

Here are the details of the 3 FMC-ADC-100M and 1 SPEC6 carrier boards used:

1. FMC-ADC-100M with CTX10-1A-R fitted at L1, Sn: HCCFFIA000-CR000228
2. FMC-ADC-100M with CTX10-1-R fitted at L1, Sn: HCCFFIA000-CR000208
3. FMC-ADC-100M with CTX10-1-R fitted at L1, Sn: HCCFFIA000-CR000229
4. SPEC6 carrier board, Sn: HCCFEIA_-CR000142

The test equipment and software used is basically unchanged from reference 1. In particular the 4MHz crystal filter is exactly as used in reference 1. Please refer to this reference for details of the test equipment and experimental setup.
4 ENOB and SNR measurements

4.1 Description

Reference 1 found that the noise floor on channel 1 is higher than on the other channels, and is dominated by a signal at 1.091MHz. The optimum ENOB of 10.73 was measured with a signal level at 4MHz of 86.72dB in figure 2. The largest noise peak was measured at 1.091MHz at 5.601dB in figure 3. This gives a signal to noise ratio of 81.119dB, ignoring 4MHz test signal harmonics. The ENOB for channels 2-4 was in excess of 11 bits.

The negative supply DC-DC generator that uses L1 is driven by IC21 which is LT1931ES5#TRMBF. The data sheet for this device specifies a switching frequency between 1.0 and 1.4MHz at 25°C, so a figure of 1.091MHZ is well within this range.

Reference 2 went on to describe the issue in detail and suggest possible improvements. It also showed that this noise issue only affects channel 1, so this report only considers the noise observed on channel 1.

In reference 2 section 2.3 the switching negative supply was replaced with an external linear supply, and the results showed that the reduction in ENOB on channel 1 was entirely due to the switching negative supply. With the switching supply the ENOB on channel 1 was measured at 10.73 bits, and with the linear supply this increased to 11.01 bits, which was similar to the other 3 channels.

4.2 Measurements ADC Sn: 228 Input range +/-0.5V

SPEC Sn: HCCFEIA__-CR000142
ADC Sn: HCCFFIA000-CR000228

This ADC board is fitted with the now obsolete CTX10-1A-R at L1.
Figure 1: FFT of ADC Sn: 228 Ch1 +/-0.5V Signal: 996mV pk-pk

Note 4MHz fundamental is at 86.59dB, so signal to noise at 1.115MHz (ignoring harmonics) is 79.197dB.

Comparison with reference 1 figure 2 SN: 139, shows harmonics are similar with 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonic strengths swapped.
Figure 2: FFT of ADC Sn: 228 Ch1 +/-0.5V Signal: 0mV pk-pk

- $\text{snr} = -11.2891$ dB
- $\text{enob} = -2.1676$ bits
- $\text{snr} = -11.2079$ dB
- pk-pk = 128
- mean = -20.6366
- RMS = 22.882
4.3 Measurements ADC Sn: 208 Input range +/-0.5V

SPEC Sn: HCCFEIA__-CR000142
ADC Sn: HCCFFIA000-CR000208

This ADC board is fitted with the replacement CTX10-1-R at L1.
Figure 3: FFT of ADC Sn: 208 Ch1 +/-0.5V Signal: 996mV pk-pk

Note 4MHz fundamental is at 86.56dB, so signal to noise at 1.114MHz (ignoring harmonics) is 71.63dB, a drop of 7.5dB.
Figure 4: FFT of ADC Sn: 208 Ch1 +/-0.5V Signal: 0mV pk-pk

Note noise 3rd harmonic at 3.336MHz is 6.927dB, 5th harmonic at 5.561MHz is 2.492dB
4.4 Measurements ADC Sn: 229 Input range +/-0.5V

SPEC Sn: HCCFEIA__-CR000142
ADC Sn: HCCFFIA000-CR000229

This ADC board is fitted with the replacement CTX10-1-R at L1.
Figure 5: FFT of ADC Sn: 229 Ch1 +/-0.5V Signal: 996mV pk-pk

Note 4MHz fundamental is at 86.56dB, so signal to noise at 1.114MHz (ignoring harmonics) is 68.37dB, a drop of 10.83dB.
Figure 6: FFT of ADC Sn: 229 Ch1 +/-0.5V Signal: 0mV pk-pk

Note noise 3rd harmonic at 3.139MHz is 8.996dB, 5th harmonic at 5.232MHz is 3.002dB
5 Conclusions

The average measured results for the 2 boards fitted with the replacement inductor, are an ENOB on channel 1 of 10.2. This is a significant reduction compared to an average ENOB on channel 1 of 10.7, for boards with the original inductor.

The noise fundamental on channel 1 at around 1MHz, is between 7 and 10dB worse with the replacement inductor.

It is likely that the mechanism of noise pickup on channel 1 is field related, because of the physical proximity of channel 1 to the inductor. There is no evidence to say if this field is electric or magnetic or both. The change in magnetic material in the inductor could result in greater magnetic field leakage, or it could result in a change in the slew rate of the driving waveform, causing a change in the electric field.

If the noise pickup mechanism is by electric field, it might be possible to reduce it by reducing the slew rate of the driving waveform with a snubber circuit as an add on to the existing pcb. However this option is not attractive for high volume production.

The input amplifiers all use a number of unshielded inductors as part of the signal conditioning. Channel 1 has inductor L4 only 5mm from L1, so L4 is the most likely component to pick up magnetic field leakage from L1. Additionally channel 1 component R4 is only 2mm from an L1 pcb pad, and there is no guard track or flood fill between them, so some electric field noise pickup is inevitable.

A survey of other fully shielded inductors with the same basic characteristics, found the following parts have similar but not identical mounting requirements to the Eaton CTX10:

1. Wurth 74489440100
2. Wurth 76889430100

The Wurth windings are arranged with inductor A on pins 1-4, and B on pins 2-3, with pins 1 & 3 the start of each winding. This compares to the Eaton pin assignments of A on pins 1-2, and B on pins 3-4, with pins 1 and 4 the start of each winding. Unfortunately there is no way to arrange the Wurth part so that it will fit the pcb directly, because of the difference in the pin allocated for the start of each winding. However it should be possible to design an adapter pcb to correct this pin out issue.

Other possible options to reduce the noise are to redesign the negative voltage DCDC to use a fully shielded inductor, located further away from an input amplifier. It might also be possible to modify the pcb to fit shields which enclose the input amplifiers, or to attach a low noise DCDC module to the existing pcb, instead of the built in DCDC circuit. See reference 2 for further details.
6 Results of Wurth and Sumida inductors

6.1 Wurth inductors
Both the suggested Wurth inductors 74489440100 and 76889430100 were fitted with cross over wires to correct for different pin out of these devices. Results were similar to the CTX10-1-R with channel 1 ENOB measured as:
ENOB = 10.14 bits for Wurth 74489440100
ENOB = 10.11 bits for Wurth 76889430100
It is possible the cross over wires increased field leakage and hence pickup. Production with these devices is unlikely to be practical because of the cross over wires.

6.2 Sumida inductor
Further research found a Sumida inductor with the correct pinout so that cross over wires are not required. However this inductor is slightly smaller than the CTX10-1-R, so that the pads do not align well with the existing pads on the pcb.

The Sumida inductor is CLS62NP-100NC.
Digikay URL:
Mouser URL:
https://www.mouser.co.uk/productdetail/sumida/cls62np-100nc?qs=LKI%2FVGYbYtjeQEka7uSo8w==
Figure 7: FFT of ADC Sn: 208 Ch1 with Sumida inductor +/-0.5V Signal: 996mV pk-pk

Note 4MHz fundamental is at 86.55dB, so signal to noise at 1.106MHz (ignoring harmonics) is 76.23dB, a drop of 2.96dB.
Figure 8: FFT of ADC Sn: 208 with Sumida inductor Ch1 +/-0.5V Signal: 0mV pk-pk

Note noise 2nd harmonic at 2.211MHz is 0.683dB, 3rd harmonic at 3.371MHz is -1.868dB
Figure 9: Zoomed FFT of ADC Sn: 208 with Sumida inductor Ch1 +/-0.5V Signal: 0mV pk-pk

Note: new noise frequency 0.0784MHz is bigger than oscillator noise at 1.1MHz.
This inductor has a noise level at 1.1MHz which is only 3dB worse than the original CTX10-1A-R. However the ENOB is only 10.3 bits, compared to 10.6 bits.

Careful examination of figures 7 and 8 revealed a new noise source at around 78kHz which is slightly bigger than the oscillator noise at 1.1MHz. This contributes to the total noise and reduces the ENOB. A search for this new noise source found that the -8V supply regulation in IC21 was unstable, resulting in bursts of oscillation at 1.1MHz, with a burst rate of 74 and 159kHz. See the scope screen shot below taken from IC21 pin 1 the switch output:

Figure 10: Scope screen shot of IC21 instability with C41=100pF
This circuit has a phase lead zero added by C41 at a frequency of:

\[
\frac{1}{2 \times \pi \times 330k \times 100pF} = 4822\text{Hz}.
\]

This is the most likely cause of the instability.

The LT1931 data sheet says the following about this:

“By choosing the appropriate values for the resistor and capacitor, the zero frequency can be designed to improve the phase margin of the overall converter. The typical target value for the zero frequency is between 20kHz to 60kHz.”

There is no evidence to say that setting C41 at 100pF was a design error. However it clearly does not follow the advice in the data sheet. For C41 to create a zero at 48kHz it should have a value of 10pF not 100pF.
Figure 12: Scope screen shot of IC21 instability with C41=10pF

With C41 removed completely the oscillation is stable.
Figure 13: FFT of ADC Sn: 208 with Sumida inductor Ch1 +/-0.5V Signal: 996mV pk-pk

Note 4MHz fundamental is at 86.42dB, so signal to noise at 1.124MHz (ignoring harmonics) is 67.44dB, a drop of 19.15dB.
Figure 14: FFT of ADC Sn: 208 with Sumida inductor Ch1 +/-0.5V Signal: 0mV pk-pk
Note noise 3\textsuperscript{rd} harmonic at 3.336MHz is 8.975dB, 5\textsuperscript{th} harmonic at 5.56MHz is 3.883dB
Figure 15: Zoomed FFT of ADC Sn: 208 with Sumida inductor Ch1 +/-0.5V Signal: 0mV pk-pk
The strength of EMI is often related to the rise and fall times of the signals. Slowing these down can reduce the EMI.

Measured IC21 pin 1 rise time at 7ns, fall time at 10ns.

Adding 33pF across D1 makes no difference to rise and fall times.

Adding 470pF across D1 changes the rise time to 18ns, the fall time remains 10ns. This reduces the ENOB to 9.5 because the higher harmonics of the 1.1MHz oscillation are increased significantly. This is probably due to increased switch on current required to discharge the 470pF capacitor.

7 Conclusions with Wurth and Sumida inductors

The best result was with the Sumida inductor with an ENOB of 10.32 in figure 13. The Sumida inductor does not require cross over wires, but is smaller than CTX10-1-R, so some manual intervention would be required for production.

Slowing down the rise and fall times of IC21 pin 1 (the switch output) with a capacitor, increases higher harmonics which decreases the ENOB.

This exhausts all possible avenues with the existing pcb layout.

It is recommended to change the pcb layout to fully correct this issue.
8 Results of Bourns and Eaton DRQ73 inductors

8.1 Bourns inductor

The Bourns SRF0703A-100M inductor has the start of both windings at the same physical end of the inductor, although the other ends of each winding are crossed.

It has been agreed to re-layout the pcb around this inductor, to make the layout closer to that recommended in the LT1931 data sheet. The winding cross over can be allowed for, although this does differ from the recommended layout.

The Bourns inductor was adapted to the existing pcb by cutting out suitable shapes of copper foil from a reel of adhesive copper tape. The foil was then soldered flat on the pcb, and the inductor soldered flat on top of the foil. This reduces the problem of having cross over wires travelling through the air and potentially increasing electric and magnetic field leakage.

Results were better with channel 1 ENOB measured as:

\[ \text{ENOB} = 10.46 \]

Production with these devices is only feasible on a modified pcb because of the pad positions and cross over.
Figure 16: FFT of ADC Sn: 208 Ch1 with Bourns inductor +/-0.5V Signal: 996mV pk-pk

Note 4MHz fundamental is at 86.60dB, so signal to noise at 1.07MHz (ignoring harmonics) is 71.8dB, a drop of 7.4dB.
Figure 17: FFT of ADC Sn: 208 with Bourns inductor Ch1 +/-0.5V Signal: 0mV pk-pk

Note noise 2\textsuperscript{nd} harmonic at 2.152MHz is 8.016dB, 3\textsuperscript{rd} harmonic at 3.228MHz is 1.843dB
8.2 Eaton DRQ73-100-R inductor

The Eaton DRQ73-100-R is physically very similar to the Bourns SRF0703A-100M measured above. The PCB layout can be designed to accommodate either of these.

The Eaton inductor was adapted to the existing pcb by cutting out suitable shapes of copper foil from a reel of adhesive copper tape. The foil was then soldered flat on the pcb, and the inductor soldered flat on top of the foil. This reduces the problem of having cross over wires travelling through the air and potentially increasing electric and magnetic field leakage.

Results were better with channel 1 ENOB measured as:

ENOB = 10.53

Production with these devices is only feasible on a modified pcb because of the pad positions and cross over.
Figure 18: FFT of ADC Sn: 208 Ch1 with Eaton DRQ73 inductor +/-0.5V Signal: 996mV pk-pk

Note 4MHz fundamental is at 86.54dB, so signal to noise at 1.127MHz (ignoring harmonics) is 73.91dB, a drop of 5.28dB.
Figure 19: FFT of ADC Sn: 208 with Eaton DRQ73 inductor Ch1 \(+/-0.5\)V Signal: 0mV pk-pk

Note noise 2\textsuperscript{nd} harmonic at 2.241MHz is 6.578dB, 3\textsuperscript{rd} harmonic at 3.361MHz is 2.264dB
9 Conclusions with Bourns and Eaton inductors

The best result was with the Eaton DRQ73-100-R inductor with an ENOB of 10.53 in figure 18.

This Eaton inductor requires a new pcb layout with cross over tracks.
The new pcb layout should implement the recommendations in the LT1931 data sheet as far as possible.

The inductor should be moved away from the channel 1 components as much as possible.

The inductor should be rotated so that the switched ends are furthest away from channel 1, with IC21 the LT1931 placed on the top of the pcb.