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CERN ADC Development report for FMC-ADC-100M

Abstract

Performance issues previously measured on the FMC-ADC-100M are fully analysed, and recommendations are made to correct these issues where practical.

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Revision History

Issue	Changes Made	Date	Initials
1	First draft	15-Nov-17	SEC
2	Added results of replacing SM negative supply with a linear supply	29-Nov-17	SEC
3	Added results of EMI near field measurements inside the PC. Formatting improvements	03-Dec-17	SEC

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1 Related Documents

1.1 Referenced Documents

1. “CERN Integration & Measurement Results 04.doc” dated 03-OCT-2017
2. “EDA-02063-V5-0_sch.pdf” dated 17-OCT-2011

Introduction

Document ref 1 measured the distortion and frequency response of the CERN FMC-ADC-100M, which revealed 4 separate less than ideal aspects of the performance:

- Channel 1 ENOB is lower than the other channels by between 2.5 and 5%
- The harmonic distortion on the 100mV range is around 11dB worse than the other ranges.
- The frequency response shows a rise of around 1.5dB below 10kHz.
- The frequency response is only -12dB at the Nyquist frequency of 50MHz.

This document attempts to analyse the reasons for the sub optimal performance and provide options to correct it where possible.

2 Channel 1 reduced ENOB

2.1 PCB Layout Description

Channel 1 ENOB is lower than the other channels by between 2.5 and 5%. On the 1V and 10V input ranges, there is a small measured increase in ENOB with channel number, across ALL channels. So it is likely that all channels are compromised by a localised noise source on the pcb.

Visual inspection of the pcb reveals the following:

- The input amplifiers are not shielded
- The PCB surface is not flood filled with ground shield
- Some signal traces are needlessly run on the pcb surface.
- There is a switching noise source (IC21, L1) adjacent to channel1

A switching DC-DC consisting of IC21, L1 and L2 converts +12V from the FMC connector to -8V, which is linear regulated by IC1 to -6V to supply the input amplifiers. IC21 is LT1931ES5 a 1.2MHz inverting DC-DC converter. L1 is a fully shielded transformer type “CTX10-1A-R” made by Coiltronics / Eaton, and is listed as “End Of Life”, and due to be discontinued. It has a saturation current rating of 2.5Amps.

The negative power output supplies 4 of each of the following devices:

ADA4004	2.2mA each	8.8mA total
ADA4899	16.2mA each	64.8mA total
LMH6551	8mA each	32mA total
TOTAL		105.6mA

L1 is currently a CTX10-1A-R with a saturation current of 2.5A, providing a DC power supply current estimated at around 105mA, with a peak demand estimated at 200mA. The output voltage is -8V, so the estimated peak power demand is 1.6 Watts.

This switching DC-DC is located nearest to channel 1 on the pcb.

Document ref 1 figure 3 clearly shows the dominant channel 1 noise frequency at 1.091MHz.

The measurement results show that the reduction in ENOB is roughly constant at all 3 gain settings, and is NOT gain dependant. This says that the noise is more likely to be induced in the output stage (IC4) of the channel 1 amplifier not the input stage (IC2).

The output stage of each amplifier includes a pair of inductors which provide some anti-alias filtering. These inductors are simple 390nH unshielded SM inductors, identified as L4 and L5 in channel1. Unfortunately L4 is located around 5mm from L1, and L5 is 8mm from L1. Any stray magnetic field from L1 is more likely to be coupled to L4 than any other inductor.

A large pcb trace from C3 to L1 passes within 1mm of R4, which carries the channel 1 negative signal output to L4. There is no copper ground shielding between them.

Each amplifier occupies 10mm by 36mm, so that all 4 occupy 40mm by 36mm.

2.2 Solution Analysis

Although no susceptibility testing has been performed, amplifier shielding would be expected to considerably improve the susceptibility to all EMI.

Each input amplifier should be located inside a metal shield to reduce noise pick up and cross channel interference. This is possible, but is a significant design challenge because of the lack of space. It is much easier to provide a single shield for all 4 amplifiers.

A possible shield with removable cover that will just fit the pcb, is BMI-S-230-F-R made by Laird. It is 50.8mm by 38.1mm, and available from Digikey:

https://www.digikey.co.uk/product-detail/en/laird-technologies-emi/BMI-S-230-F-R/903-1470-1-ND/3915244

The lid is BMI-S-230-C, also from Digikey:

https://www.digikey.co.uk/product-detail/en/laird-technologies-emi/BMI-S-230-C/903-1471-ND/3915247

This shield would cover all 4 amplifiers and the AtoD chip IC9. The DC-DC would be placed outside the shield.

There is a considerable amount of top and bottom surface pcb space that could be flooded with copper connected to ground. This should be done in conjunction with as many vias as possible to connect together all ground layers, as is normal practice in all high frequency RF circuits. In particular, each amplifier channel should be completely surrounded top and bottom with via connected ground flood fill. This process is aided by placing all possible signal traces on internal layers, sandwiched between ground planes, instead of running them without shielding on the pcb surface, as they are on the existing pcb.

In the unlikely event that fitting a metal shield is not considered practical, then the DC-DC switch mode inverter must be moved so that it is as far as possible from the signal carrying components. It should be moved to the other end of the FMC connector, where IC19 is currently located. This should increase the clearance to the nearest inductor to over 10mm.

The entire DC-DC switch mode inverter should be replaced with a monolithic inverter with shielded inductor. A monolithic solution does not induce any primary switching currents into the ground of the pcb since they are completely contained within the monolithic device.

A survey of a wide range of monolithic power supplies found the ideal choice is Texas Instruments LMZ34002:

http://www.ti.com/lit/ds/symlink/lmz34002.pdf

This device has a built in shielded inductor and is guaranteed to meet EN55022 class B emissions. The package size is 11 x 9 x 2.9mm which is smaller than the foot print of the CTX10-1A-R inductor alone.

The existing -8V supply is fed from the switch mode inverter and only filtered by a 4.7uH inductor L19. This supply may well be another source of input amplifier noise, since it is tracked all the way across the pcb to the other side. This -8V supply should be fed from a linear regulator, located close to the LMZ34002. The LMZ34002 output should be set to -9V to provide the linear regulation head room.

The unshielded signal filter inductors should be changed to shielded types. This will greatly reduce their ability to pick up stray interfering magnetic fields.

2.3 ENOB with SM supply replaced with linear

To determine the extent of the reduction in the EBOB caused by the existing Switch Mode negative power, it was disabled and replaced with an external linear supply of -8V. The table below shows the measured ENOB with both the SM and linear supplies, on the 1 Volt input range:

	Ch1 ENOB	Ch2 ENOB	Ch3 ENOB	Ch4 ENOB
SM PSU	10.73	11.02	11.08	11.13
Linear PSU	11.013	11.02	11.08	11.13

This result shows that the SM PSU does add noise to channel 1 only, as the other channels ENOB remains constant with the linear PSU.

The very small improvement in ENOB with channel number remains. This suggests that there is another position dependent noise source affecting all channels, which is closer to channel 1 than channel 4. There is no other noise source on the ADC board that is closer to channel 1 than another channel. On the SPECV4 carrier board there is a 25MHz oscillator nearer to channel 1, and channel 1 is nearer to the PC backplane, which is likely to be a source of EMI. Design changes that may reduce noise induced by external EMI are:

1. The addition of a metal shield around the amplifiers
2. Changing the unshielded amplifier filter inductors to shielded

2.4 EMI fields inside the PC

To provide evidence for or against the assertion “there is another position dependent noise source affecting all channels, which is closer to channel 1 than channel 4”, some simple uncalibrated RF field measurements were made. An RF probe consisting of 8 turns of wire on a ferrite core was attached to a 50 Ohm cable connected to the Oscilloscope channel 1. This was set for a gain of 1mv/cm, a sample rate of 100MHz, 500 point sample memory and FFT display with an average of 50.

Here is the baseline taken outside of the PC:

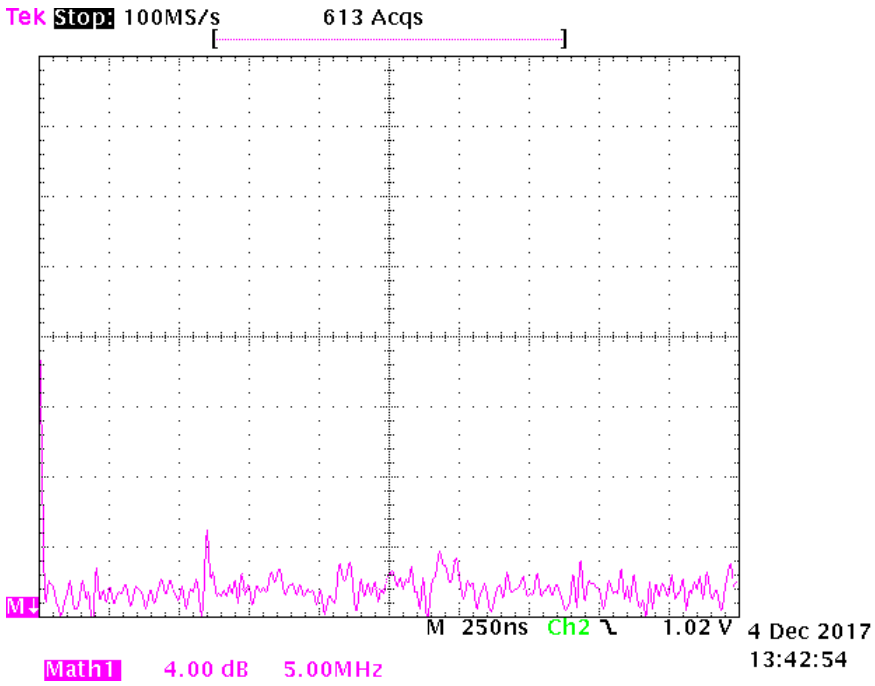

Figure 1: Baseline FFT of RF field outside the PC

Here is the result with the probe adjacent to ADC channel 1:

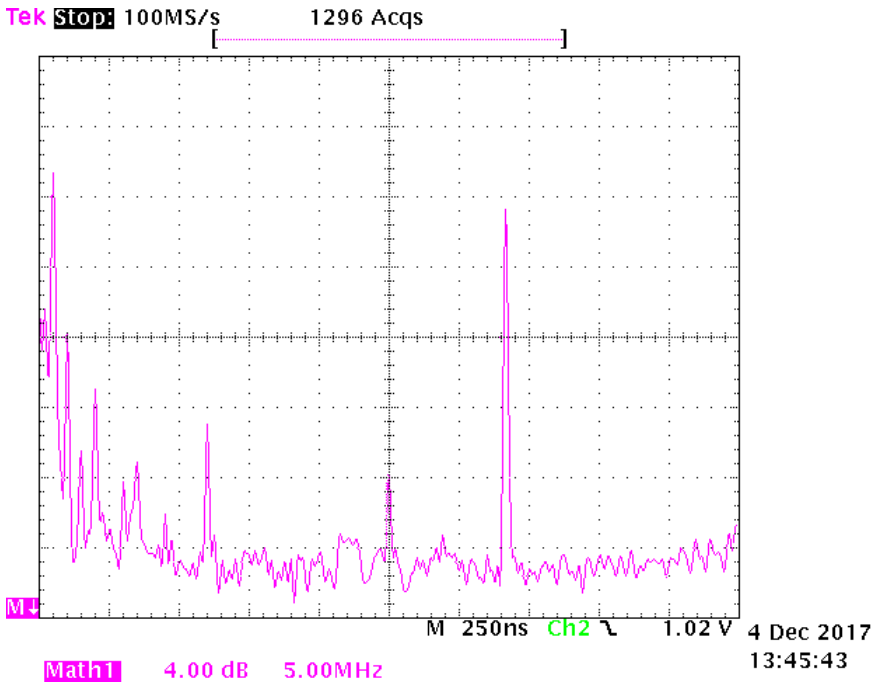

Figure 2: FFT of RF field adjacent to channel 1

Here is the result with the probe adjacent to ADC channel 4:

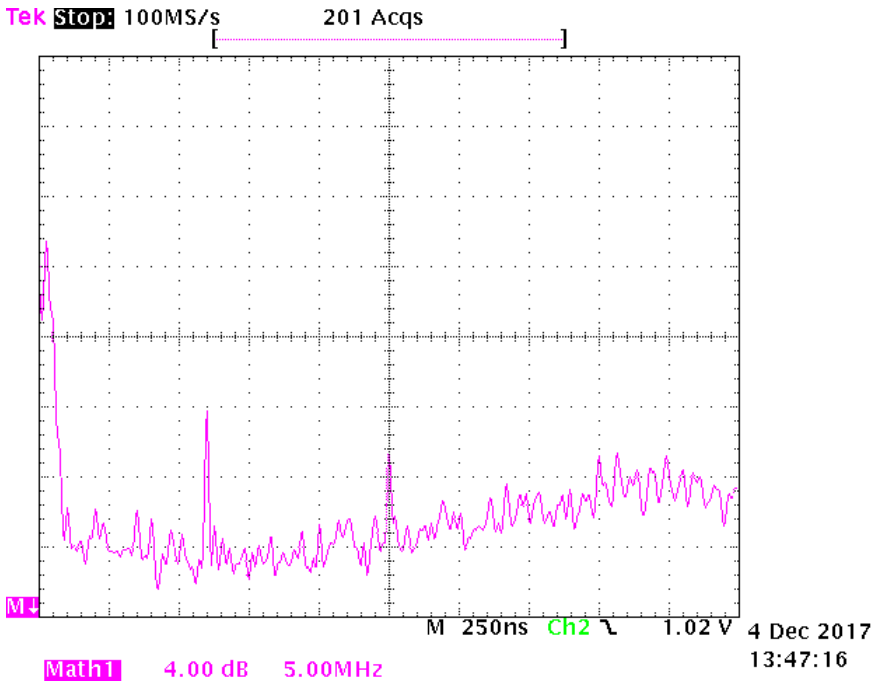

Figure 3: FFT of RF adjacent to channel 4

These result show the 2 most significant sources of noise inside the PC, relevant to the ADC, are:

1. The band below 2MHz which peaks at about 24dB above the baseline.
2. The spot frequency of 33MHz which is about 20dB above the baseline for channel 1 only.

Both are stronger at the channel 1 side of the ADC, compared to the channel 4 side. This is expected because channel 1 is nearest the PC back plane.

Note that because of the possibility of aliasing and other non linear mixing effects, these results are only provided to illustrate the location dependency issue.

3 100mV Range Harmonic Distortion

3.1 Distortion causes

The harmonic distortion on the 100mV range is around 11dB worse than the other ranges, when measured with a 4MHz test signal. Typical values of second harmonic distortion from ref 1 are:

100mV = -71dBc

1V = -82dBC

10V = -82dBc

Only the amplifier input stage is affected by changes in gain. The amplifier is Analog Devices part ADA4899. This device has a negative feed back path consisting of 4 resistors, 2 with high frequency bypass, and 2 opto switches which allow the amount of feed back to be changed. The partial schematic below shows how this is arranged:

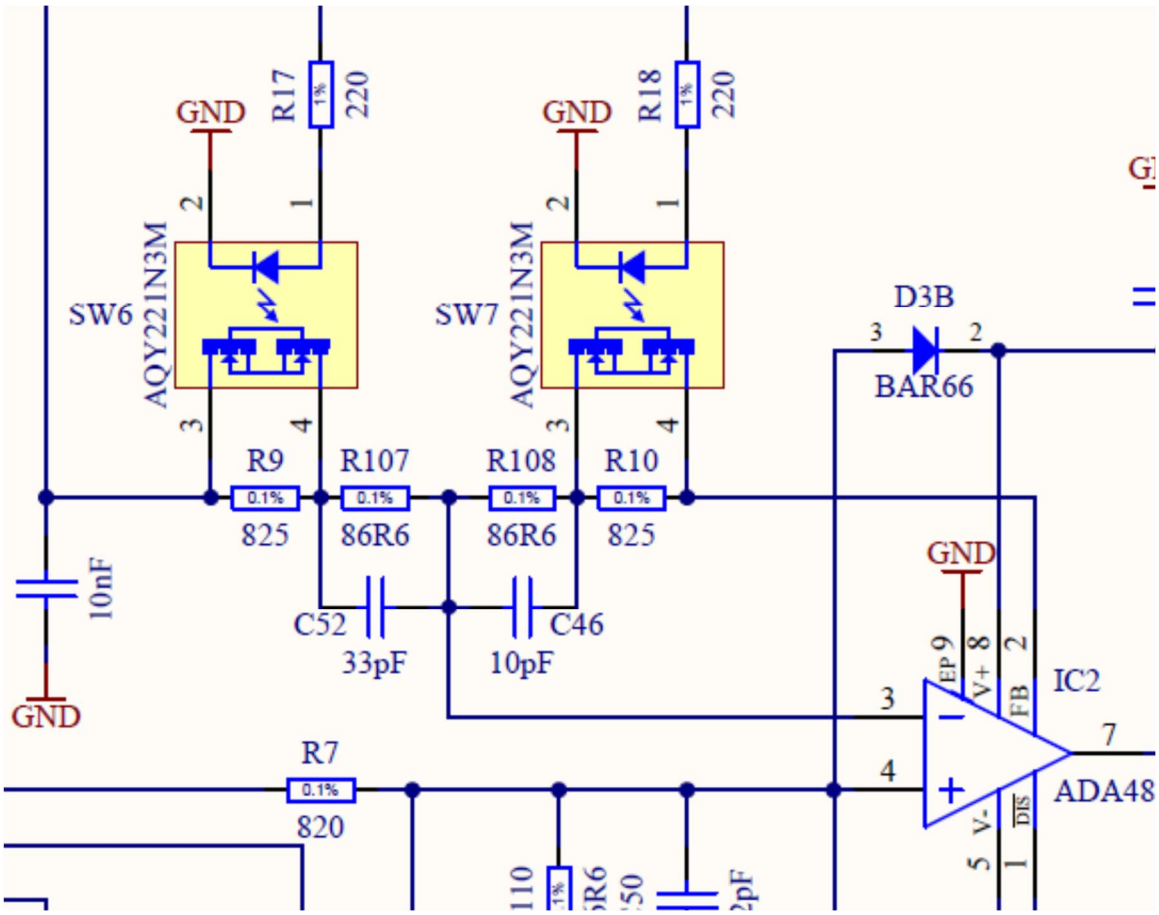

Figure 4: Partial schematic of Channel1

The amount of feed back for each gain setting and the expected band width is shown in the table below. Note that the band width is very load dependent, and the output is loaded by 242 Ohms and a series 1uH inductor. This means direct analysis from the data sheet can only be an estimate of band width:

Gain range	AC Feed back %	SW7	SW8	Gain at IC2 pin4	Estimated Bandwidth -3dB MHz
100mV	8.6	OFF	ON	11.6	32
1V	50	OFF	OFF	2	220
10V	91.3	ON	OFF	1.09	500

The data sheet figure 15 plots open loop gain, and clearly shows that at 20dB gain the band width is only 30MHz.

It is well known that the distortion in an amplifier is inversely proportional to the feed back, because greater feed back allows the amplifier to better correct any output error. It is less well understood that the effective feed back is proportional to its phase. So if the feed back is phase shifted at higher frequencies, then these frequencies will have higher distortion because the feed back is less effective. Increasing gain increases phase shift at high frequencies causing higher distortion.

The ADA4899 data sheet figure 22 plots distortion at a gain of 1, and figure 21 plots distortion at a gain of 5. The table below compares these figures with a source signal at 4MHz and a 100 Ohm load:

Harmonic MHz	Distortion with gain=1, 2V p-p	Distortion with gain=5, 2V p-p
8	-87dBc	-73dBc
12	-102dBc	-98dBc

This shows the second harmonic distortion at 8MHz can be 12dB worse at a gain of 5 compared to a gain 1, and is likely to be higher at higher gains.

3.2 Solution Analysis

The performance of a number of other types of amplifier were analysed for suitability in this circuit. A good option is the LMH6702 which offers a gain of 68dB at 30MHz, compared to the ADA4899 gain of 20dB at 30MHz. The table below details the differences, based on the data available in the data sheets:

Parameter	ADA4899	LMH6702
Gain at 30MHz	20dB	68dB
Slew rate	310V/us	3100V/us
HD2, G=1, 5MHz, load 100R	-87dBc	
HD2, G=2, 5MHz, load 100R		-100dBc
HD2, G=5, 5MHz, load 100R	-73dBc	
Feedback type	Voltage	Current

Because the LMH6702 uses current feed back, the gain switching topology would need to be changed to use a fixed feed back resistor (237 Ohms), and switched ground divider resistor.

The LMH6702 should offer some improvement in distortion performance on the 100mV range. However making this significant change to an existing design for a small improvement on one range does not seem to be a strong enough reason to take the risk.

The fundamental problem is setting a high gain of 11.6 in a single stage amplifier. The same gain could be obtained from a 2 stage amplifier with each stage set to a gain of just 3.4, which would have lower overall high frequency distortion. As the design already has 2 amplifier stages, the gain balance in the amplifier could be changed by increasing the output stage gain and reducing the input stage gain, so the net result is unchanged. This would reduce the distortion in the first stage and increase it in the second. The optimum gain balance would then have the same distortion in each stage. The problem with this approach is that the output stage distortion is then increased slightly for all 3 input ranges, making it less desirable.

An alternative solution is to add an additional amplifier stage. This could have a switched gain of 1 for the input ranges 1V and 10V, and a gain of 5.8 for the 100mV range. One of the optical relays that are used in the existing design to increase the first stage gain to 11.6 could be re-used to switch the gain on this additional stage, so the number of relays does not change. The problem with this approach is there is insufficient pcb space for the additional amplifier stage.

4 Low frequency response rise

4.1 Causes

The frequency response shows a rise of around 1.5dB below 10kHz. The graph below is taken from ref 1 figure 17, and shows the frequency response of channel 1 on the +/-0.5V range:

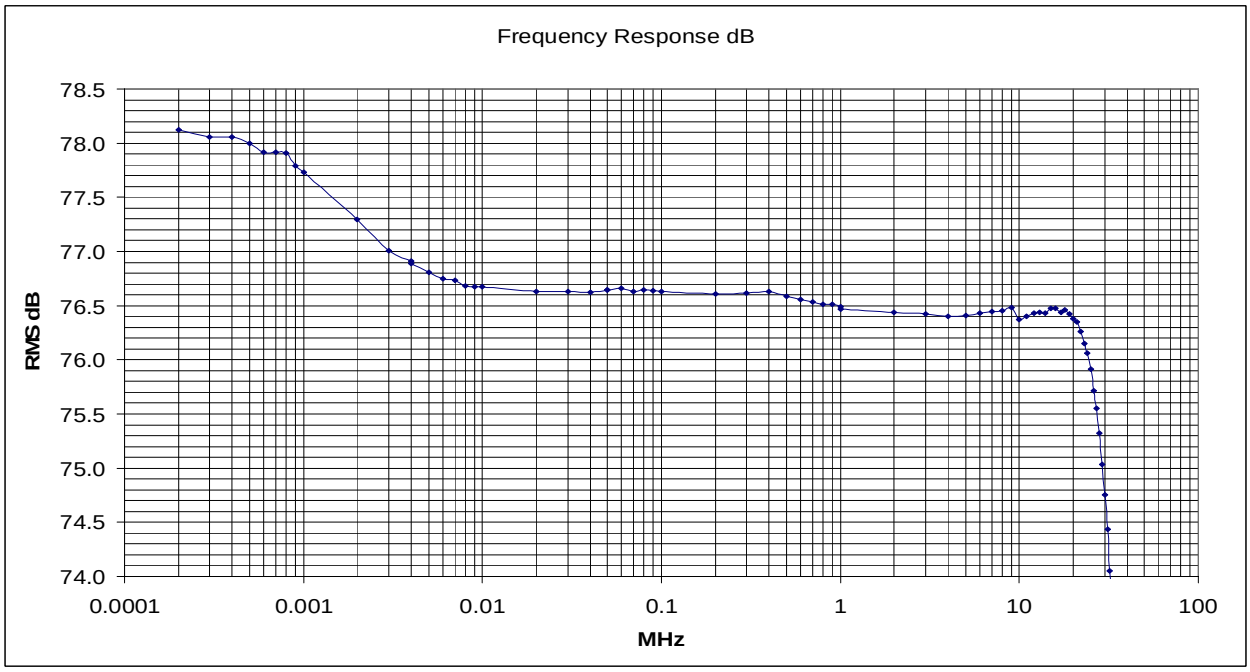

Figure 5: Ref 1 RMS dB Magnified Frequency Response of ADC Sn:139 Ch1 +/-0.5V

Below 10kHz the response rises by around 1.4dB.

To identify the source of this rise, an automatic Frequency Response Analyser was constructed. The FRA consists of a Tektronix TDS684 1GHz oscilloscope and a Systron Donner 1702 1GHz signal generator connected to a control PC over GPIB. The control PC runs Matlab where a program performs a frequency sweep, and analyses and compares the waveforms recorded on 2 of the scope channels. One channel is the reference or system input waveform and the other is the system output waveform. The program performs an FFT on both waveforms to extract the amplitude and phase of the test frequency only, and display their ratio, as a magnitude and phase plot.

This system has 2 very important advantages over other measurement systems:

- The FFT analysis is extremely frequency specific and ignores all noise and distortion
- The analysis is differential from channel to channel, and does not rely on the absolute accuracy of the oscilloscope.

During calibration the FRA accuracy was estimated as:

Amplitude better than +/-0.5%, or +/-0.044dB

Phase better than +/-1 degree

The scope is connected to ADC channel 1 using Tektronix P6245 FET probes with an input capacitance of less than 1pF. The scope reference channel is connected to the back of the ADC channel 1 Lemo connector. The scope measurement channel is

connected to the junction of L5 and C8, which is the ADC channel 1 output net titled “ADC_in1_P” on the schematic.

The graphs below show the measured response, which does NOT show the rise in response at low frequencies reported in ref1:

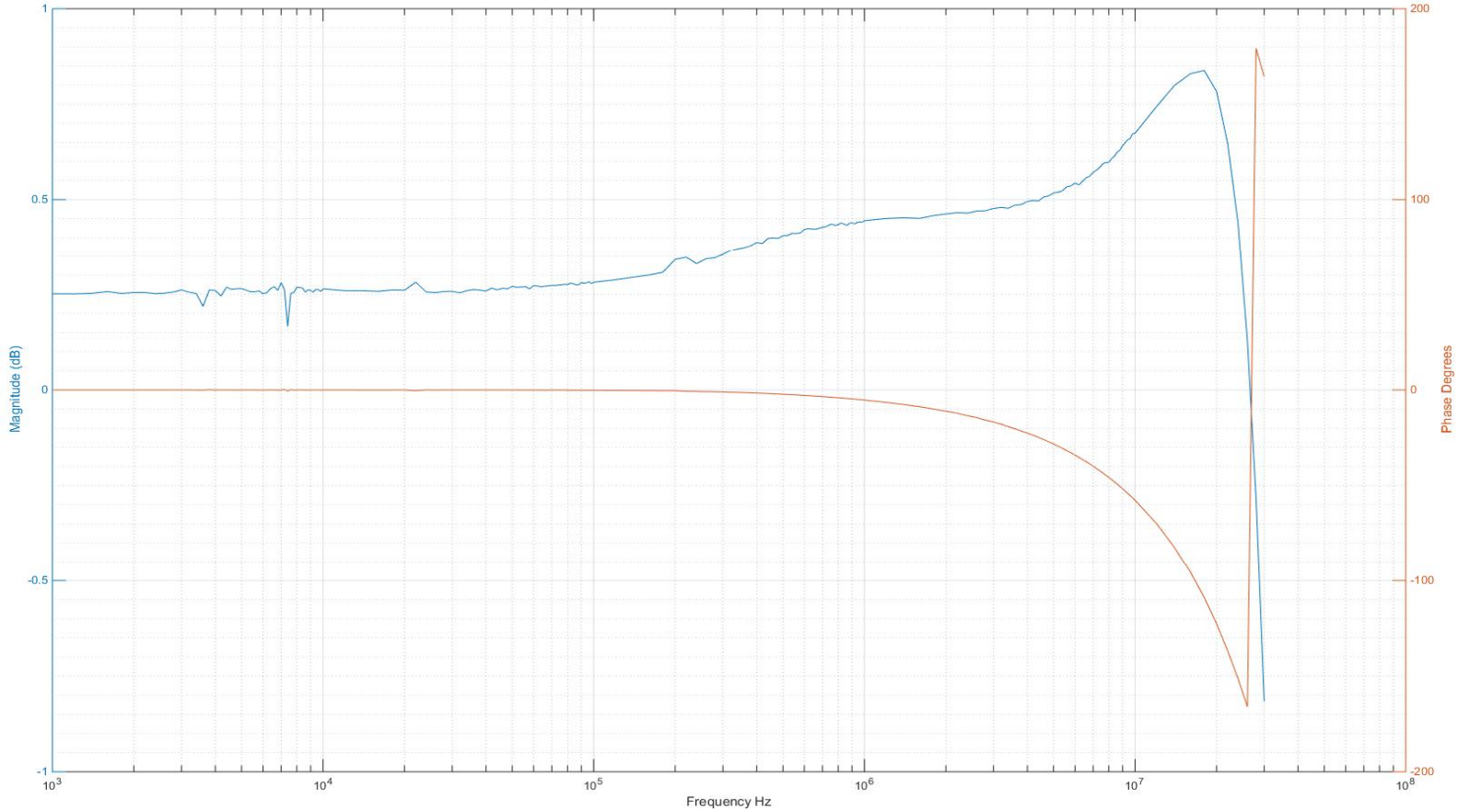

Figure 6: RMS dB Magnified Frequency Response of ADC Sn:139 Ch1 +/-0.5V

4.2 Analysis

Careful examination and repetition of the method used in ref 1 revealed that the rise in response was caused by the Analog Devices HMC1030 dual 3.9GHz RMS power detector, even though it was fed from a DC-microwave signal splitter. The HMC1030 is AC coupled with a 50 Ohm termination on chip. This means at low frequencies it presents an impedance which rises above 50 Ohms, and the signal level from the splitter increases. The signal level on the other output of the splitter also increases slightly. However with the oscilloscope connected to the output of the signal generator, it does not measure this small increase in the signal fed to the ADC. The result is a small measured rise in the response at low frequencies which is NOT caused by the ADC circuit.

5 Anti Alias Attenuation

5.1 Existing performance

The measured frequency response is only -12dB at the Nyquist frequency of 50MHz, so frequencies above this will be aliased.

The anti alias filter comprises 2 separate LC low pass filter stages. The first inter stage filter uses a 1uH inductor and a 33pF capacitor arranged as a low pass filter. The second output stage filter uses a pair of 390nH inductors and a single 22pF capacitor.

The first filter consists of 121 Ohm series resistor, 1uH series inductor, 33pF load, 121 Ohm load. Here are the results of modelling the first 1uH filter:

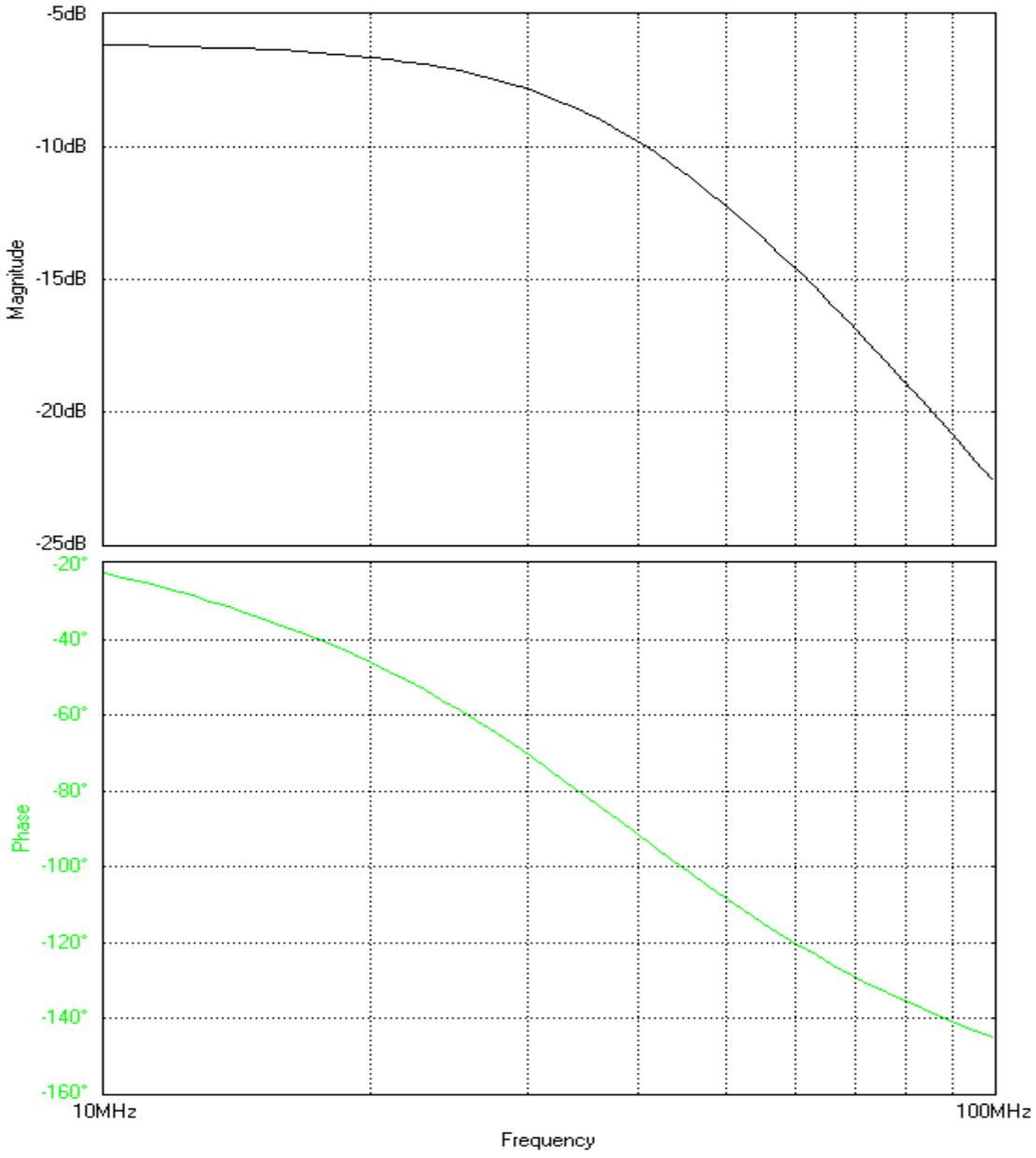

Figure 7: Frequency Response of existing inter stage filter

The roll off is:

27.8MHz = -1.5dB
36.5MHz = -3dB
50.0MHz = -6.2dB
100MHz = -16.5dB or 10dB/Octave
Phase:
30.0MHz = -71 degrees

The second filter consists of a differential input feeding series 121 Ohm resistor, series 390nH inductor, single 22pF output capacitor. Here are the results of modelling the second 390nH filter:

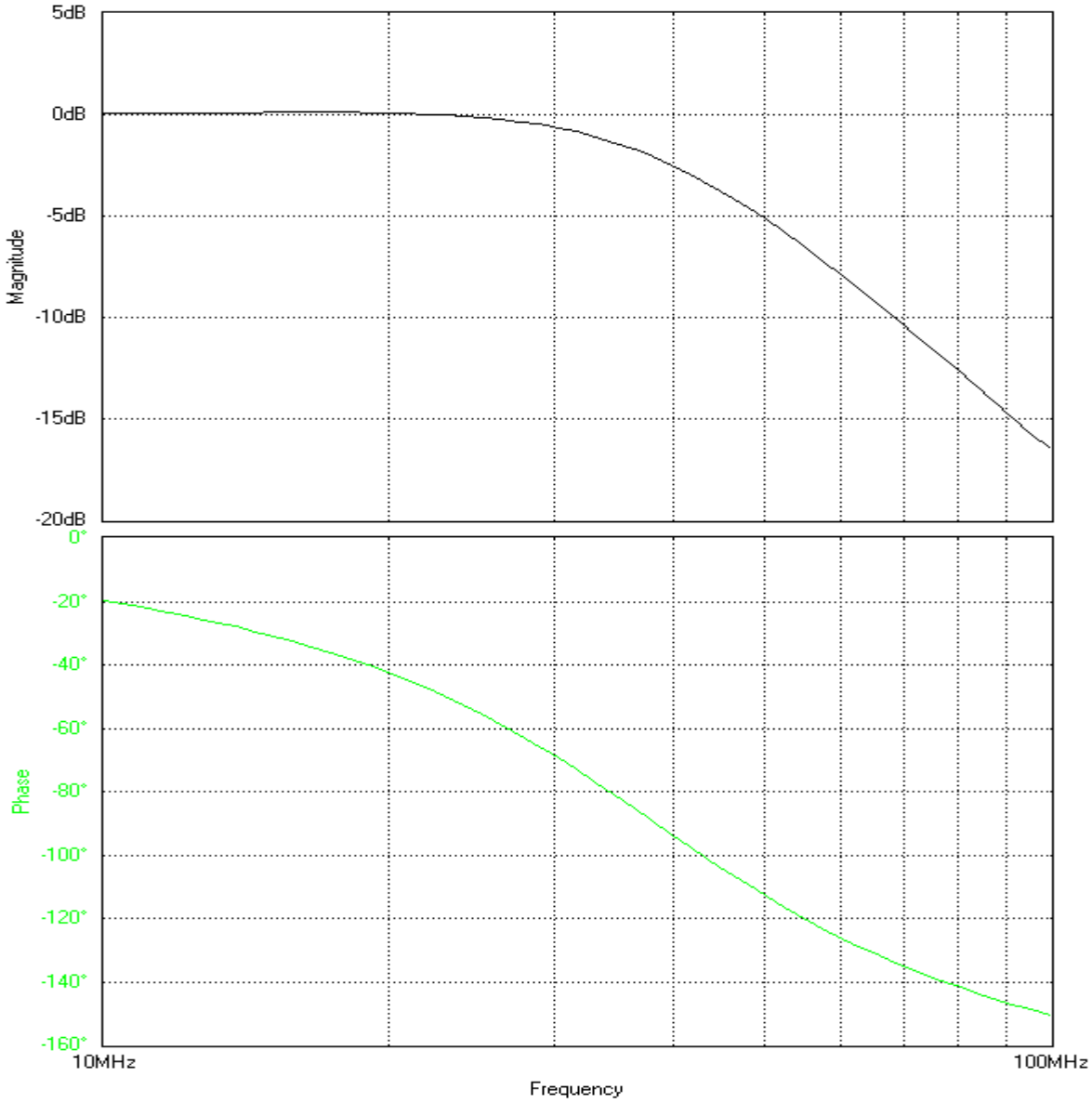

Figure 8: Frequency Response of existing output filter

The roll off is:
35.3MHz = -1.5dB
42.2MHz = -3dB
50.0MHz = -5.1dB

100.0MHz = -16.5dB or 11.4dB/Octave

Phase:

30.0MHz = -69 degrees

The 22pF output capacitor is in parallel with the ADC input capacitance, so the roll off frequencies will be slightly lower.

5.2 Solution analysis

The ideal anti alias filter would have a response of -3dB at 30MHz and -80dB at 50MHz, a roll off of more than 80dB per octave, which is not practical to design or build.

Below is a table of practical shunt type filters all with Butterworth characteristics, because only this type has maximal amplitude flatness in the pass band. All were designed with -3dB attenuation at 36.5MHz, so they have the same corner frequency as the existing inter stage filter:

Order	Inductors	Capacitors	Attenuation at 50MHz dB	Attenuation at 100MHz dB
2	1	1	-6.4	-17.6
3	1	2	-8.6	-26.3
5	2	3	-13.5	-43.8
7	3	4	-18.7	-61.3
9	4	5	-24	-79

Note that all of these filters actually divide the signal by 2, so they start with -6dB attenuation at low frequency. This has been corrected in the above table which shows the attenuation relative to that at DC.

The existing design of the inter stage filter has a single inductor and single capacitor so is order 2.

Phase distortion in the pass band increases with filter order, so a compromise needs to be made when choosing the optimum filter order for a given application. In this case all 4 inputs see the same phase distortion so the relative phase error between channels remains zero. For non continuous signals such as pulses, frequency dependent phase distortion in the pass band results in pulse shape distortion which must be modelled.

Component tolerance should also be taken into consideration, as this results in production variability in the accuracy of the filter. Higher order filters are more susceptible because they have more components.

As filter order increases the shielding requirements also increase, otherwise leakage from input to output effectively bypasses the filter.

If a high order filter is designed in to a pcb, it is easy to reduce the order by replacing inductors with zero ohm resistors and removing capacitors. It is very difficult to increase the order of a designed in filter.

Taking all this into account, it is recommended that the inter stage order 2 filter is replaced with an order 5 filter. The graphs below show the results of modelling a practical order 5 filter:

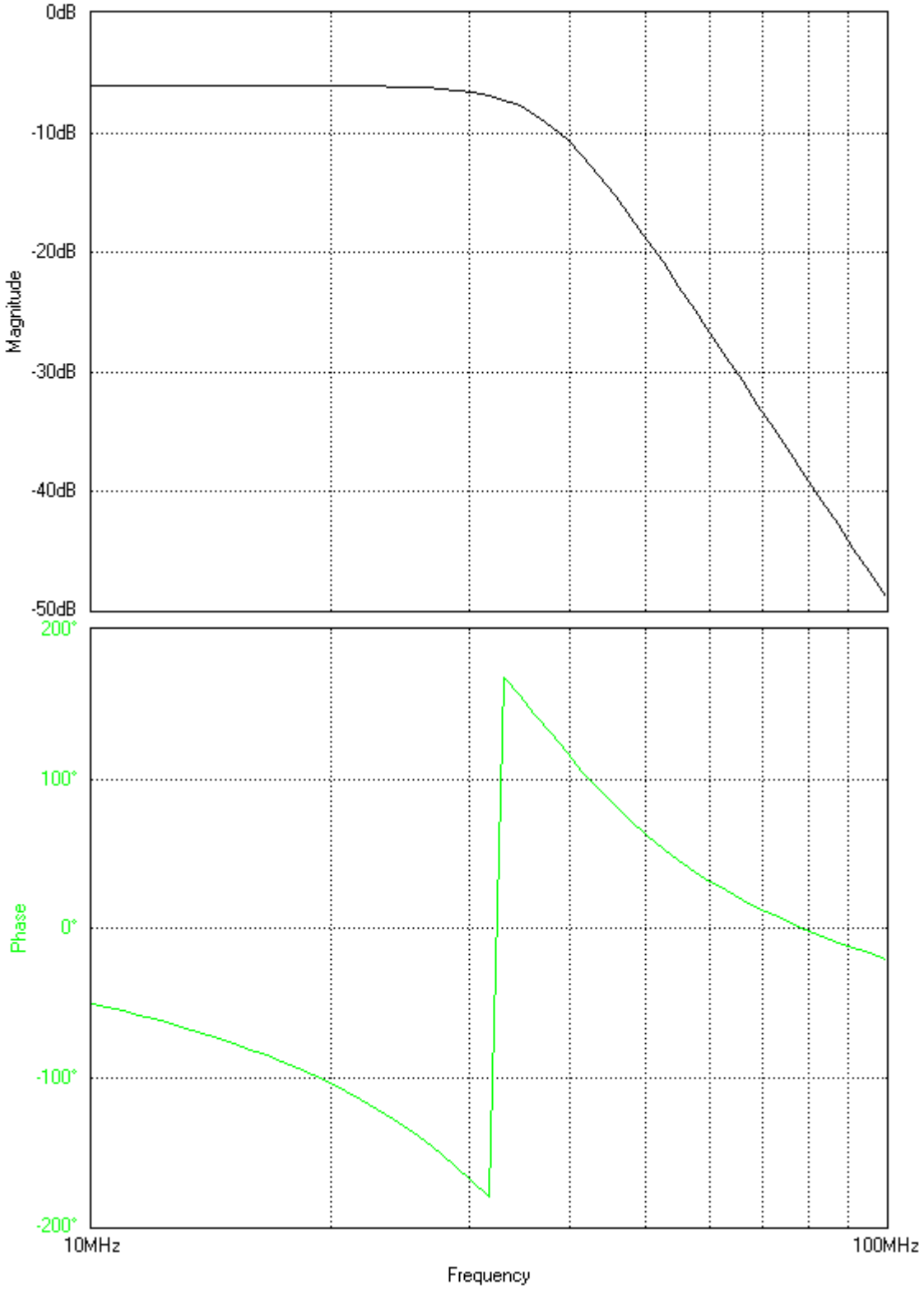

Figure 9: Frequency Response of proposed inter stage filter

6 Summary of recommendations

All four amplifiers should be located inside a metal shield to reduce noise pick up and cross channel interference. A possible shield with removable cover that will just fit the pcb, is BMI-S-230-F-R made by Laird. It is 50.8mm by 38.1mm, and available from Digikey.

There is a considerable amount of top and bottom surface pcb space that could be flooded with copper connected to ground. This should be done in conjunction with as many vias as possible to connect together all ground layers, as is normal practice in all high frequency RF circuits. In particular, each amplifier channel should be completely surrounded top and bottom with via connected ground flood fill. This process is aided by placing all possible signal traces on internal layers, sandwiched between ground planes, instead of running them without shielding on the pcb surface, as they are on the existing pcb.

The entire switch mode inverter should be replaced with a monolithic inverter with shielded inductor. A survey of a wide range of monolithic power supplies found the ideal choice is Texas Instruments LMZ34002.

The -8V supply should be fed from a linear regulator, located close to the switch mode inverter. This will increase the channel 1 ENOB to be the same as the other channels, however it will not improve channels 2/3/4.

The unshielded signal filter inductors should be changed to shielded types. This will greatly reduce their ability to pick up stray interfering magnetic fields.

Possible solutions to the increased distortion on the 100mV range do not offer sufficient advantage to be worth the risk of changing the design to accommodate them.

The inter stage anti-alias filter should be increased from order 2 to order 5, to improve the low pass filter response.