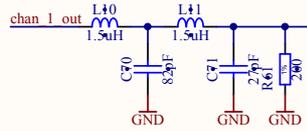
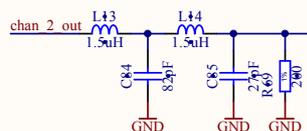


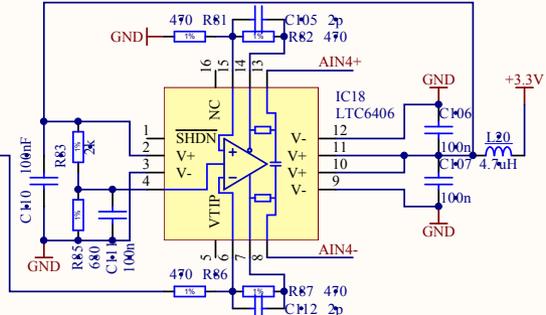
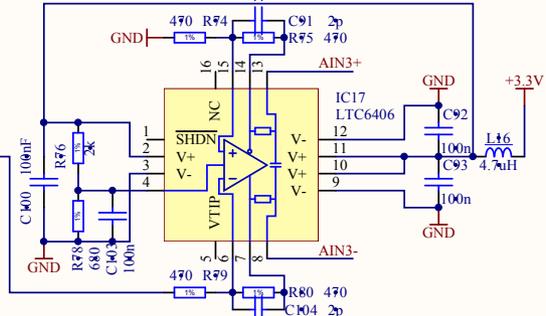
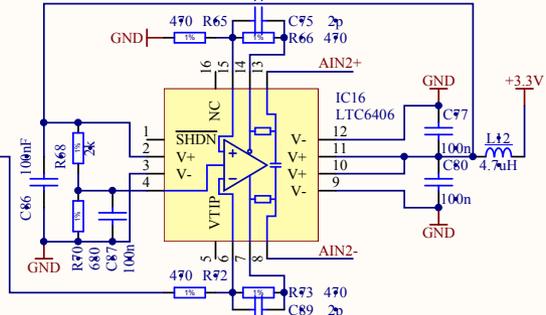
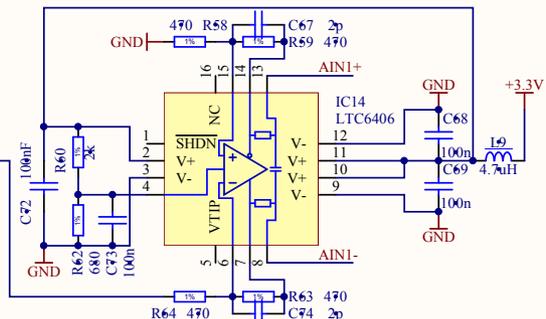
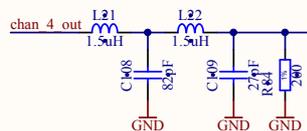
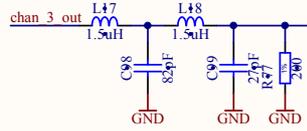
Input resistance seen by the filter: 1510hm



Antialiasing filter - Butterworth low-pass filter  
cut off frequency: 24MHz,  
att. at Nyquist frequency (50MHz): 34dB



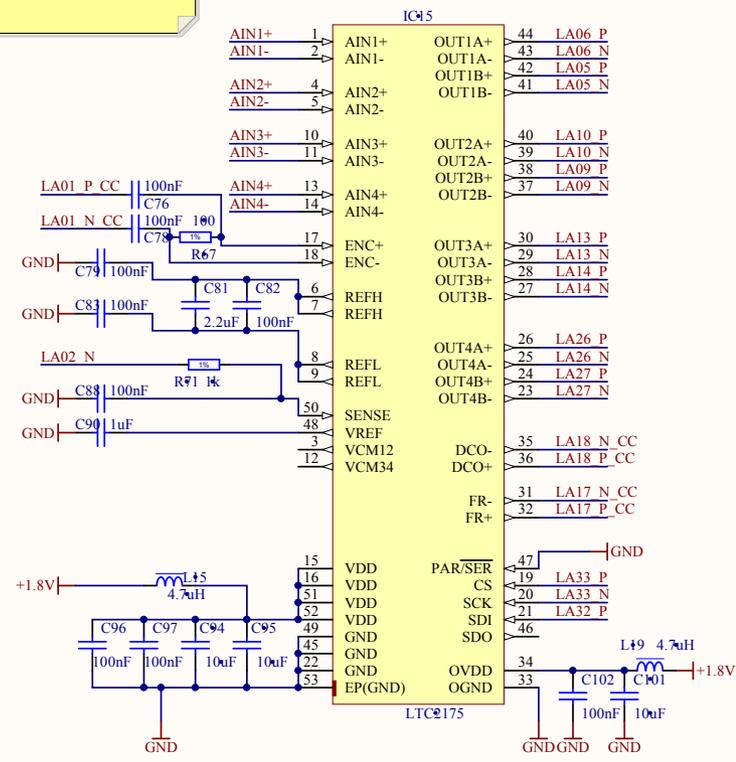
Large value of loopback resistors for differential amplifier are caused by need of protect amplifiers' inputs against overload. Preceding section is powered from +/- 15V and can deliver over 100mA (clamping diodes of differential amplifiers are 10mA tolerant).



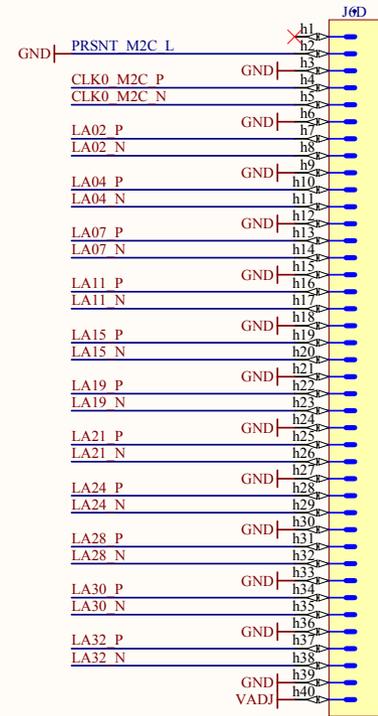
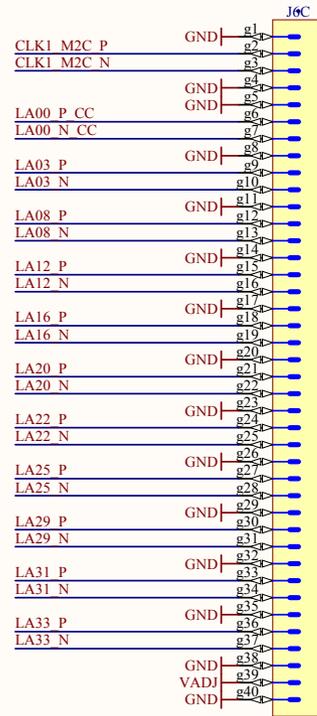
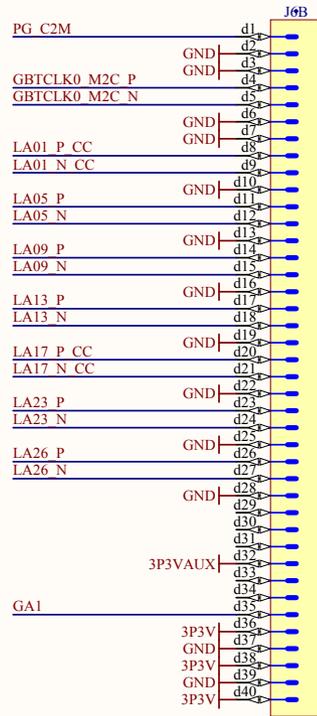
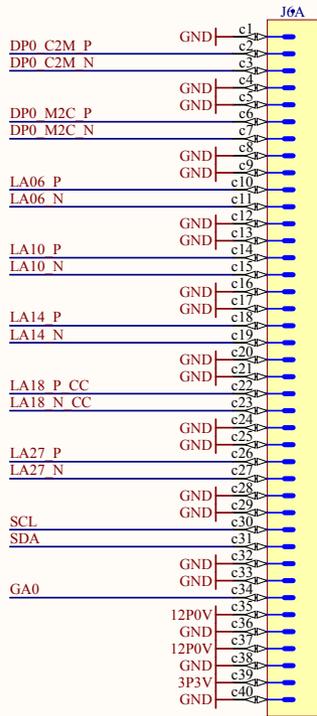
resistor divider creates potential of 0.9V for VOCM inputs (common mode output potential)

differential amplifier's output voltage range covers 0.9V +/-0.5V with single supply voltage

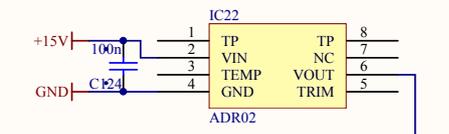
calculation for analog stage are valid for 1Vpp input voltage range of ADC.



Project/Equipment		-	
Document	EN-ICE	Designer	Designer
Check by	-	Drawn by	DrawnBy
Last Mod.	-	File	ADC_SchDoc
Print Date	12/18/2009 1:58:32 PM	Sheet	- of -
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		Size	A4
Title <b>Title2</b>		Rev	-
EDA-XXXXX-VX-X			



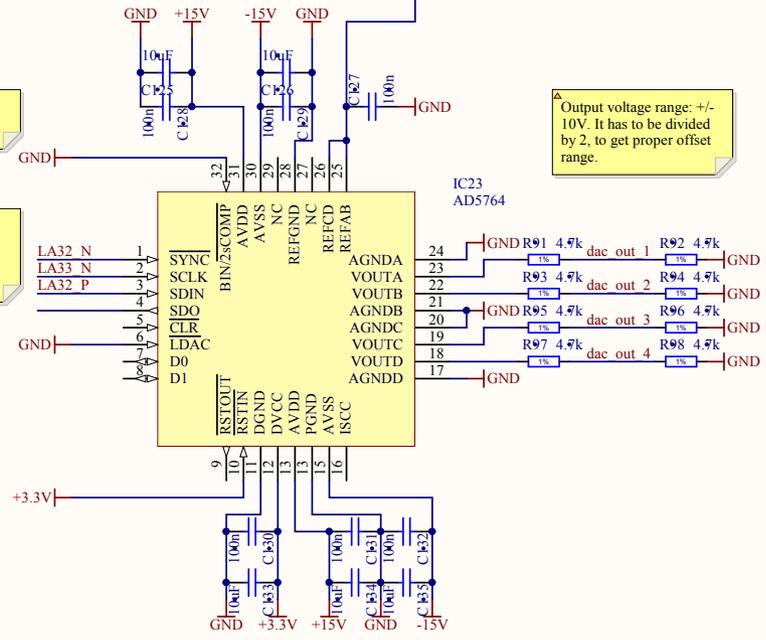
Project/Equipment -		Designer Designer	
Document		Drawn by DrawnBy	XX/XX/XXXX
 European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		Check by -	-
		Last Mod. -	12/18/2009
		File connector.SchDoc	
		Print Date 12/18/2009 1:58:32 PM	Sheet - of -
		EDA-XXXXX-VX-X	
		Size A4	Rev -



BIN/2sCOMP tied to GND: twos complement coding

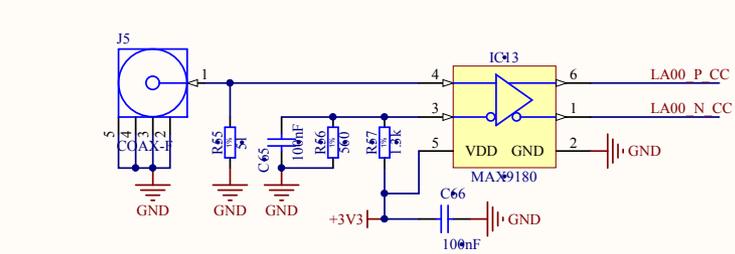
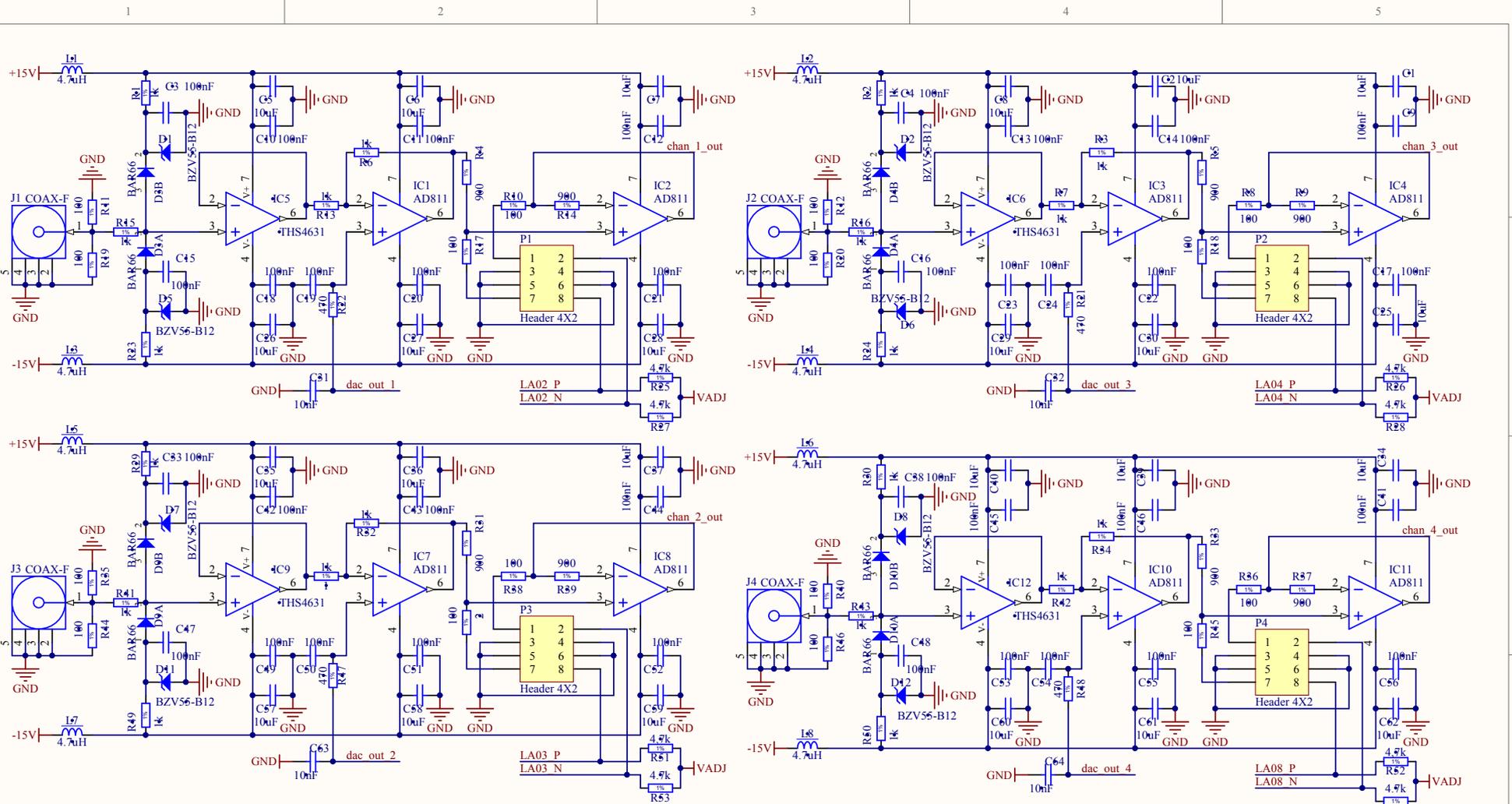
SPI interface shares data and clock lines between ADC and DAC except CS (/SYNC) line.

Output voltage range: +/- 10V. It has to be divided by 2, to get proper offset range.



IC23 AD5764

Project/Equipment		-	
Document	<p style="text-align: center;"><b>Title</b> <b>Title2</b></p> <p style="text-align: center;">European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland</p>		Designer Designer
 			Drawn by DrawnBy
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	Last Mod. -	12/18/2009	
	File DAC_SchDoc		
	Print Date 12/18/2009 1:58:32 PM	Sheet - of -	Size A4 Rev -
EDA-XXXXX-VX-X			



2x4 header:  
User is changing the gain by setting jumper position. Second jumper allows mainboard to determine jumper position and therefore the gain.

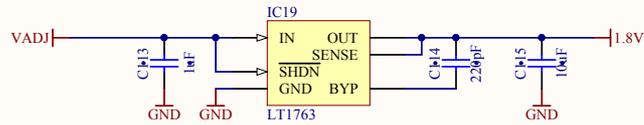
2 x 100 OHm resistors: 0.5W, 1206 - max. constant input voltage - 7.07V.

There is a problem with power (and value) of resistor for protecting clamping diodes at the inputs. Choosing high value and bypassing resistors by capacitors may cause phase problems (but it is commonly used in oscilloscopes).

Project/Equipment		Projekt	
Document		Designer	
EN-ICE		Drawn by	DrawnBy
CERN		Check by	-
		Last Mod.	12/18/2009
		File	input_stage.SchDoc
		Print Date	12/18/2009 1:58:33 PM
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		Size	A4
		Rev	-

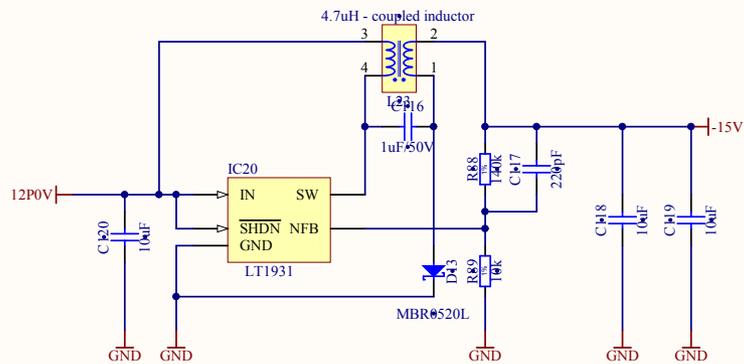
## Input stage Input buffers, PGAs, trigger buffer

EDA-XXXXX-VX-X

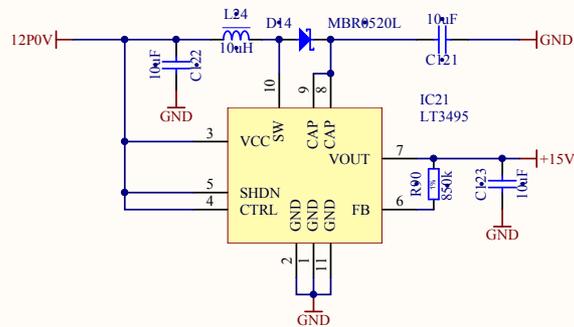


VADJ has to be set to 2.5V. Linear regulator makes 1.8V potential for supply the ADC.

With VADJ of 2.5V there is also no problem of level matching for DAC (logic one >= 2V). Otherwise level converter is needed.



CUK inverting DC/DC converter. According the datasheet - output ripple: 1mV.



standard low noise boost converter. According to the datasheet, output ripple approx. 10mV

Project/Equipment -		Designer Designer	
Document		Drawn by DrawnBy	XX/XX/XXXX
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CERN		Last Mod. -	12/18/2009
		File power_supply.SchDoc	
		Print Date 12/18/2009 1:58:33 PM	Sheet - of -
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	
		Size A4	Rev -