LogiCORE IP SelectIO Interface Wizard v1.4

DS746 July 23, 2010 **Product Specification**

Introduction

The LogiCORE™ IP SelectIO™ Interface Wizard simplifies the integration of the SelectIO technology into the system design in the Spartan®-6 and lower-power Spartan-6 devices, and the Virtex®-6 and lower power Virtex-6 devices. The Wizard creates an HDL file (Verilog or VHDL) that instantiates and configures I/O logic such as Input SERDES, Output SERDES and DELAY blocks configured to customer requirements. Additionally, it instantiates and configures the desired I/O clock primitive, connecting to the instantiated I/O logic.

Features

- Supports input, output or directional busses
- Creates clock circuitry required to drive I/O logic
- Supports up to a 16-bit wide data bus
- Supports optional data serialization of up to 10 bits for Virtex-6 devices and up to 8 bits for Spartan-6 devices bits
- Supports optional data and/or clock delay insertion
- Supports single and double data rate data
- Supports single-ended or differential standards for both clock and or data
- Implement phase detector functionality for Spartan-6 FPGA designs
- Output can be pulled into PlanAhead™ design tools for further I/O attribute setting
- Provides synthesizable example design and demonstration test bench to help with integration

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family (1)	Spartan-6 (2) Virtex-6 (3)				
Supported User Interfaces	None				
	Resources (4)				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Config1	82 (5)	0-68			
Provided with Core					
Documentation	Product Specification Getting Started Guide				
Design Files	Verilog and VHDL				
Example Design	Verilog and VHDL				
Test Bench	VHDL, Verilog				
Constraints File	User Constraints File				
Simulation Model	None				
Tested Design Tools					
Design Entry Tools	ISE® software 12.2 CORE Generator™ tool				
Simulation	ISim 12.2 Mentor Graphics ModelSim 6.5c and above Cadence IES 9.2 and above Synopsys VCS and VCS MX 2009.12 and above				
Synthesis Tools	XST 12.2				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the release notes for this Wizard.
2. For more information on the Spartan-6 devices, see the *Spartan-6 Family Overview* [Ref 1]
3. For more information on the Virtex-6 devices, see the *Virtex-6 Family Overview* [Ref 3]
4. These are the maximum resources used when phase detector is implemented.
5. These are the maximum resources used when phase detector is implemented.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The SelectIO Interface Wizard LogiCORE IP core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated by the Xilinx® ISE CORE Generator™ software, which is a standard component of the Xilinx ISE Design Suite. This version of the core can be generated using the ISE CORE Generator system v12.2 or higher. For more information, please visit the Architecture Wizards web page.

Information about additional Xilinx LogiCORE modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

References

1. DS160: *Spartan-6 Family Overview*
2. UG700: *LogiCORE IP SelectIO Interface Wizard v1.4 Getting Started Guide*
3. DS150: *Virtex-6 Family Overview*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/16/09	1.1	Initial Xilinx release.
12/02/09	1.2	Added Spartan-6 -1L (Lower Power) device support.
04/19/10	1.3	Updated Wizard and tools. Added Resources Used rows in the Facts table, "Support" and "Ordering Information."
07/23/10	1.4	Revised LogiCORE IP Facts table's format and content. Added support for Virtex-6 devices.

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