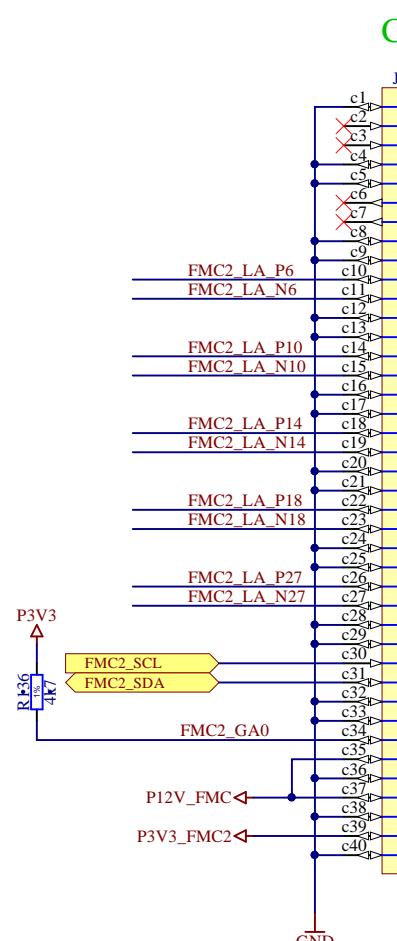
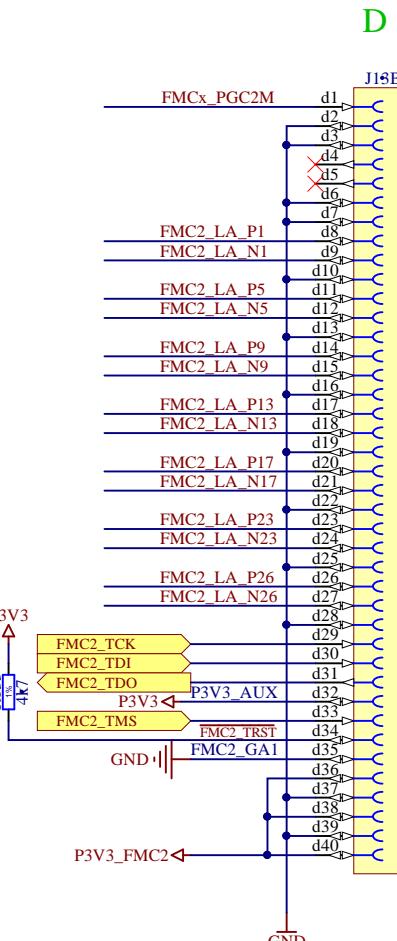
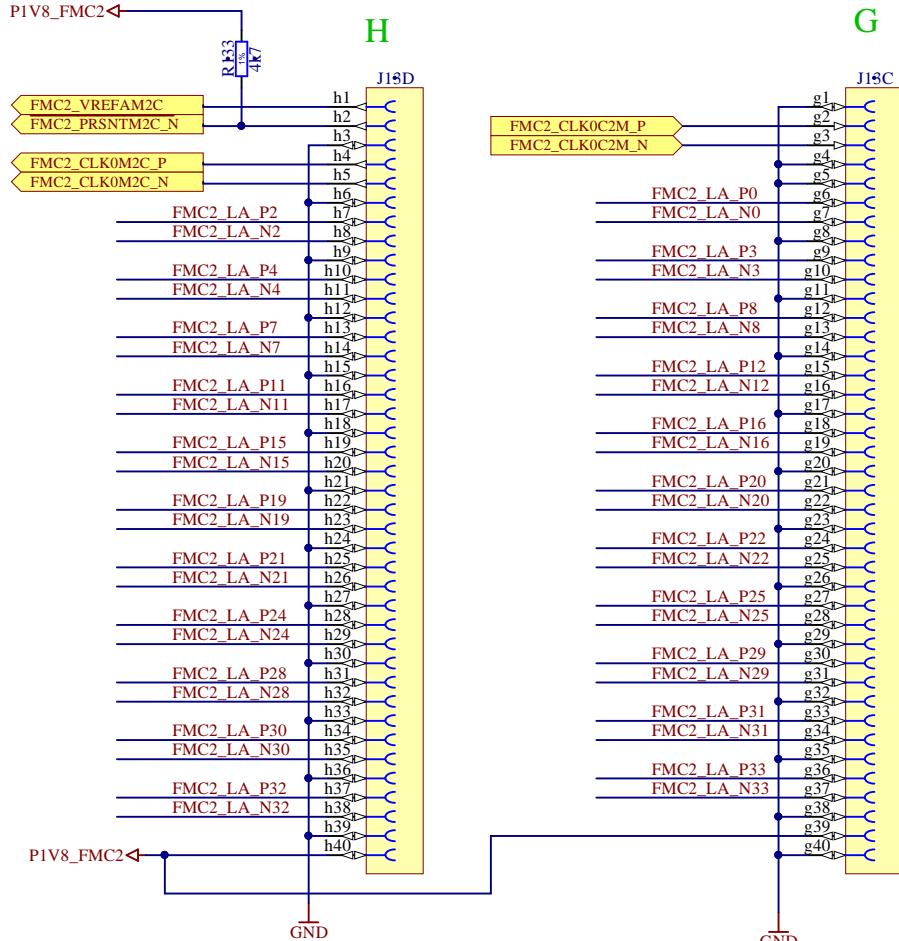
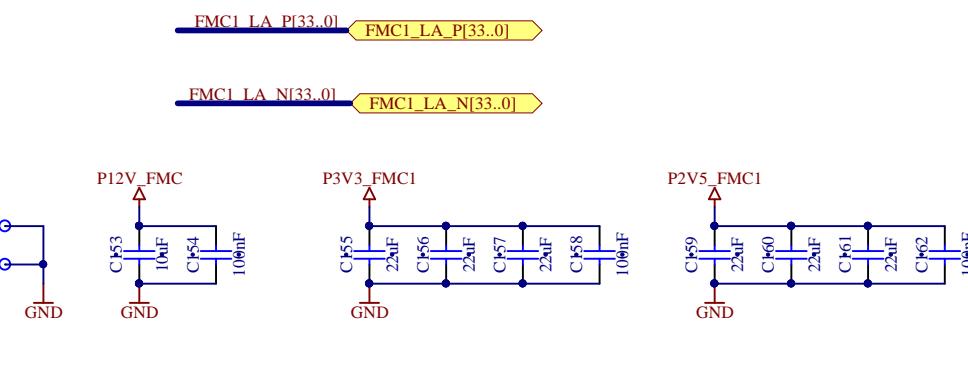
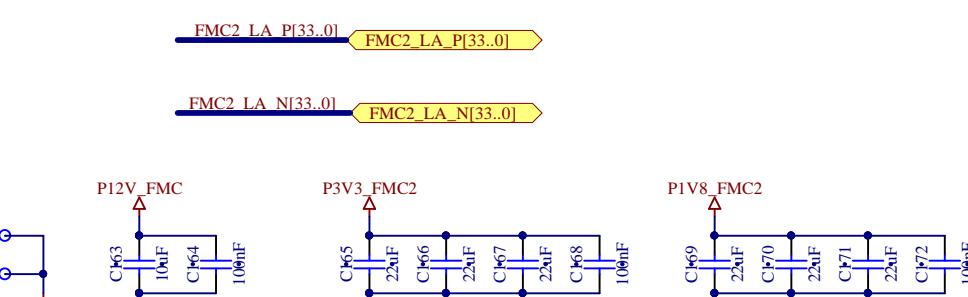


A V{ADJ} = 2.5V

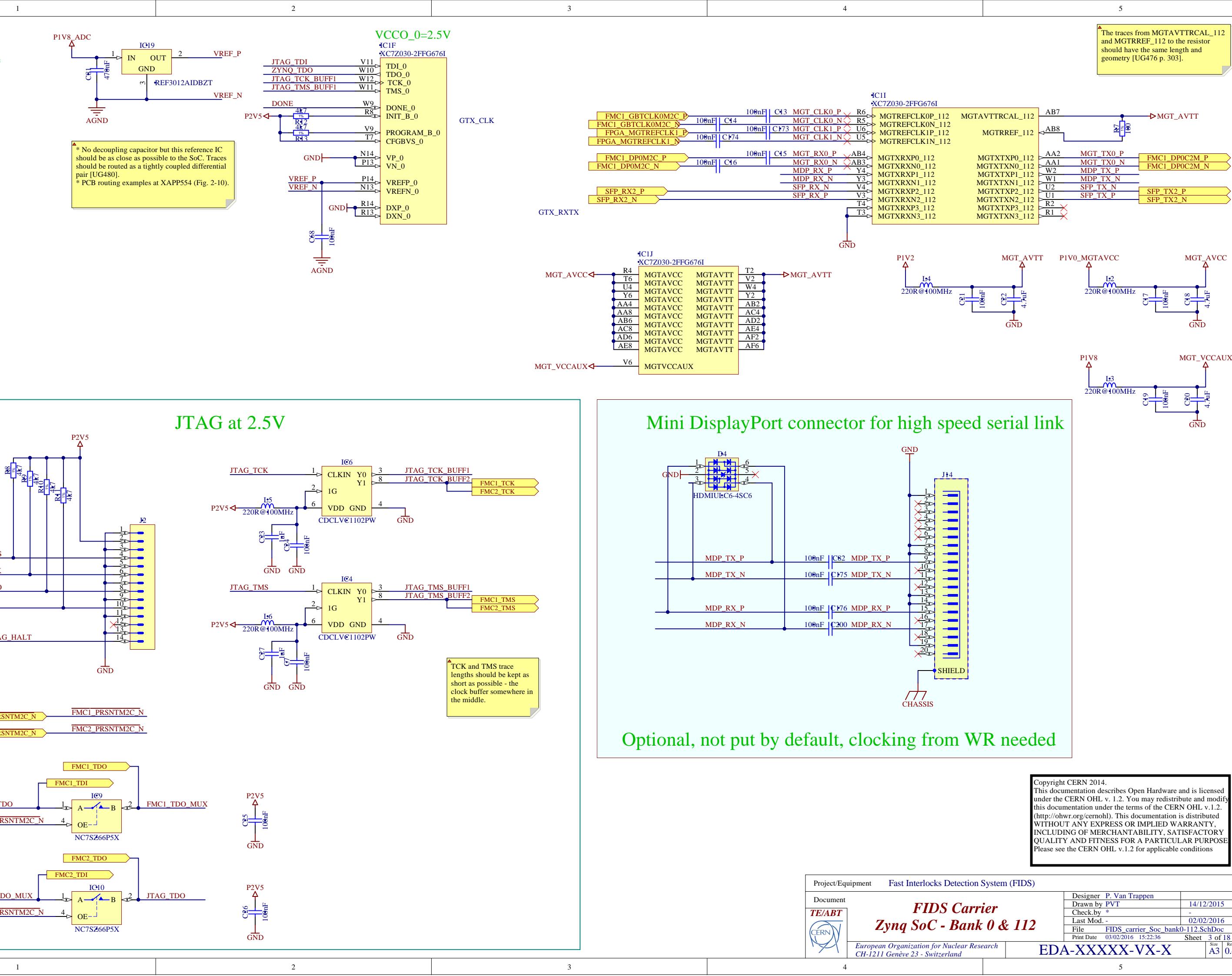
- ANSI/VITA 57.1:
 - For all differential pairs:
 - Recommendation 5.3: When signals are routed differentially each pair should provide a differential impedance of $100\Omega \pm 10\%$
 - For FMCx_CLK0M2C and FMCx_CLK0C2M pairs:
 - Rule 5.22: Clock traces shall provide a differential impedance of $100\Omega \pm 10\%$
 - Rule 5.23: The differential length mismatch on each differential clock pair shall be a maximum 11ps.
 - For the FMCx_DP0 pairs:
 - Rule 5.43: The differential length mismatch on each differential data pair shall 1ps.
 - For the FMCxGBTCLK0M2C pairs:
 - Rule 5.48: Clock traces shall provide a differential impedance of $100\Omega \pm 10\%$
 - Rule 5.49: The differential length mismatch on each differential clock pair shall 11ps.

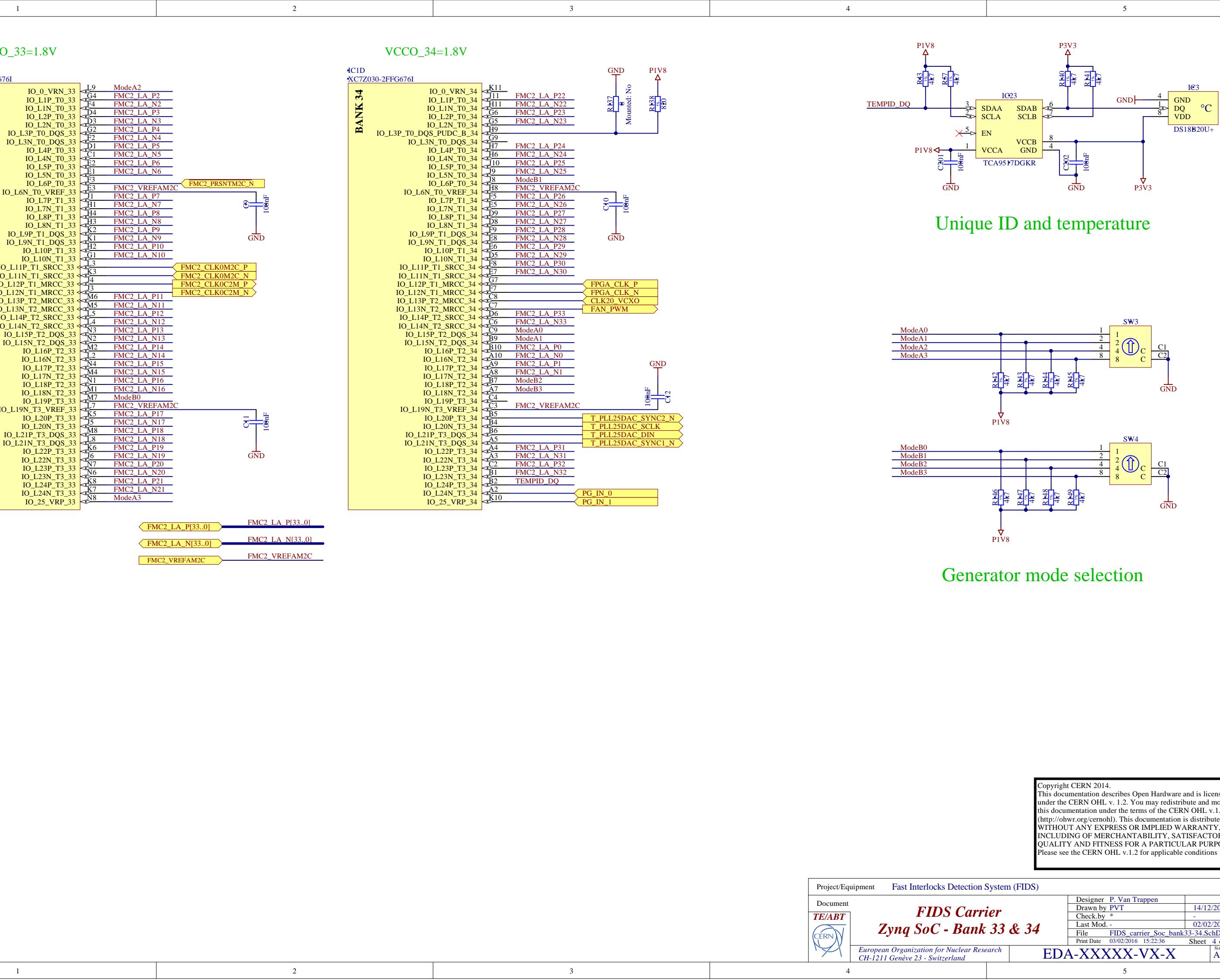


$V_{ADJ} = 1.8V$



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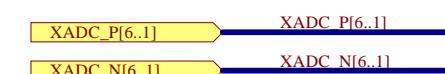
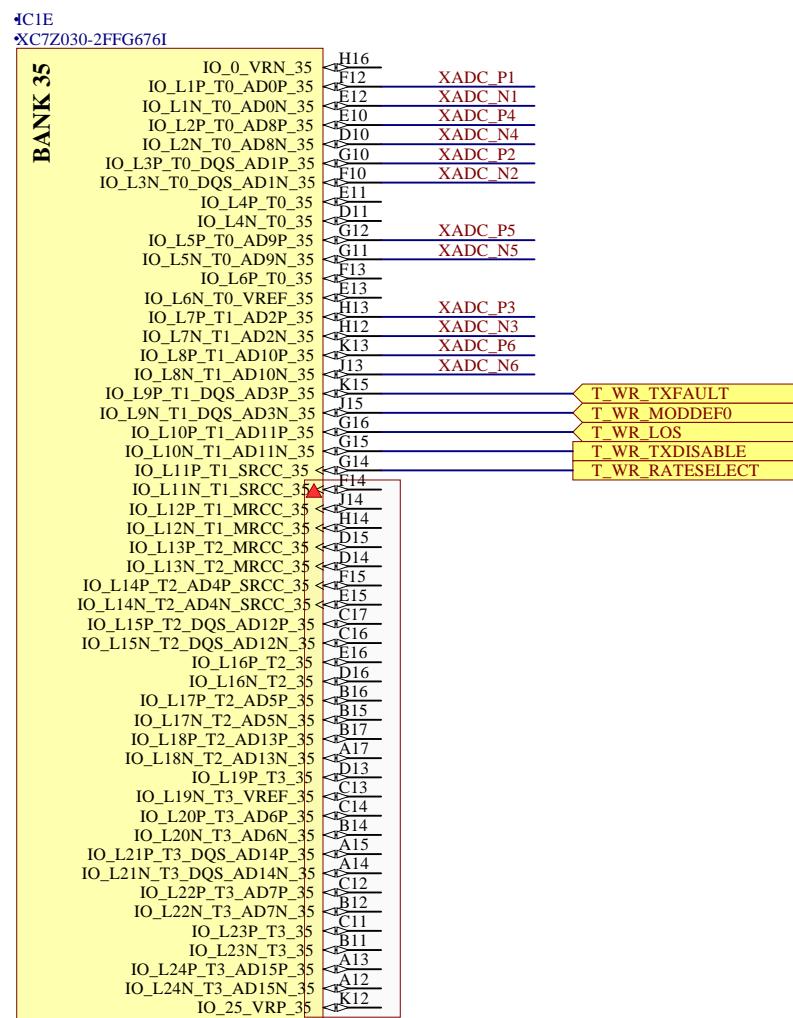


A

A

▲ No XADC pin swapping allowed! Input numbering doesn't follow package numbering but the order is important for full sampling rate support (i.e. simultaneous sampling mode).

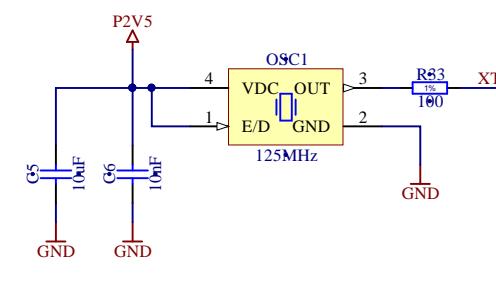
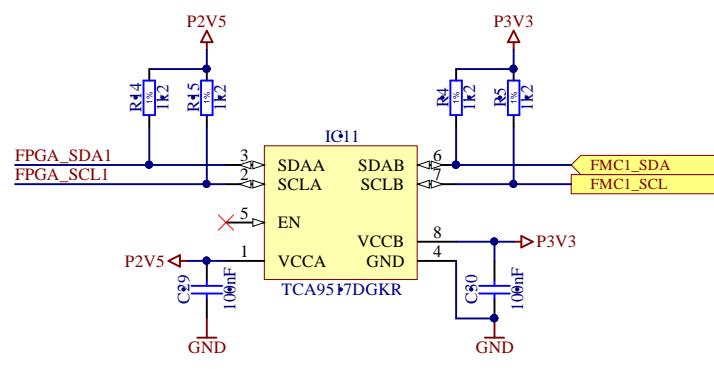
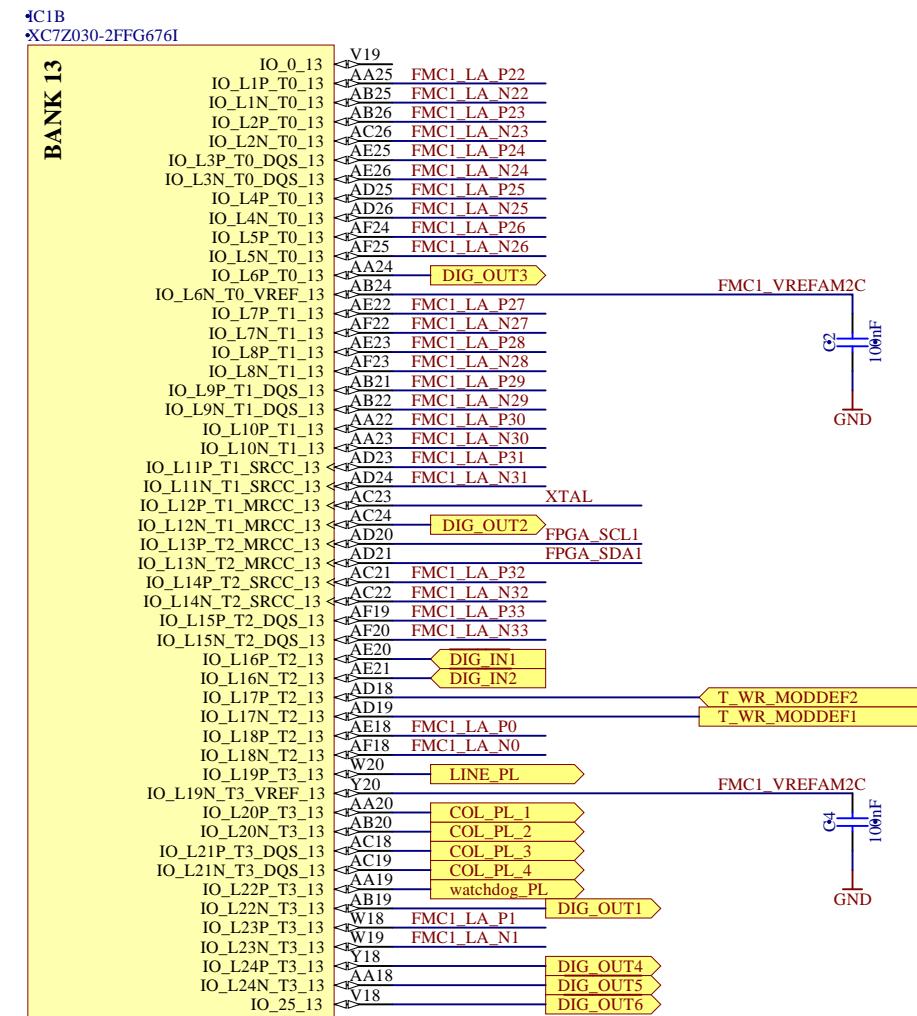
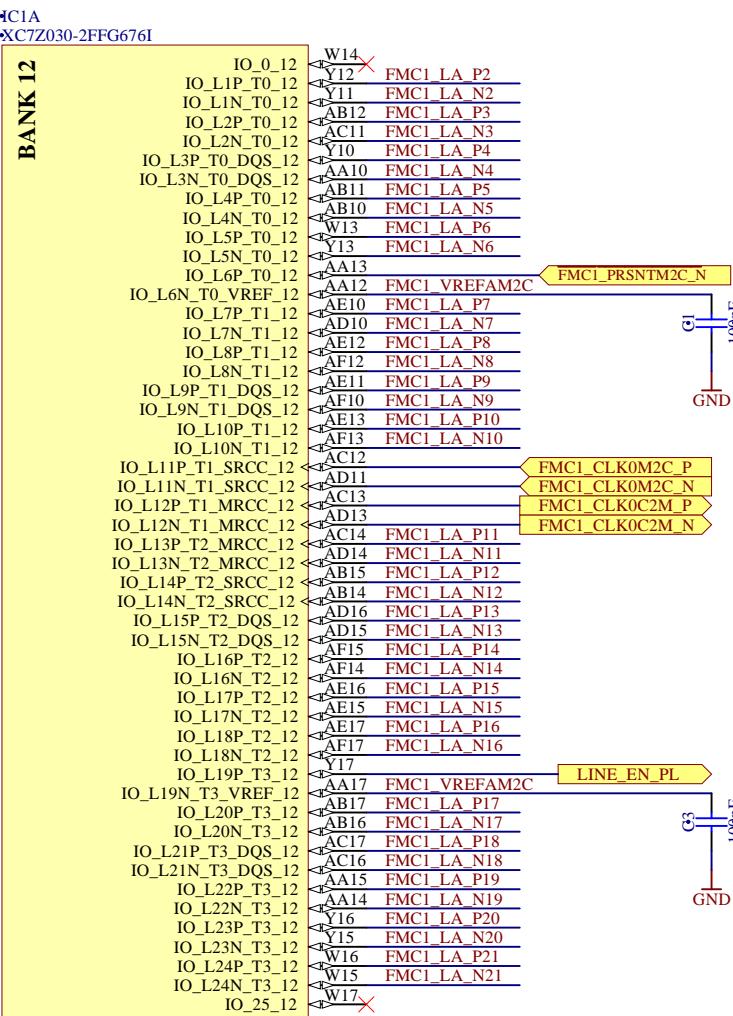
VCCO_35=1.8V



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Project/Equipment		Fast Interlocks Detection System (FIDS)		
Document	TE/ABT	<i>FIDS Carrier</i> <i>Zynq SoC - Bank 35</i>		EDA-XXXXX-VX-X
				Size A3 Rev 0.4
				5 of 18
				Print Date 03/02/2016 15:22:36
				File FIDS_carrier_Soc_bank35.SchDoc
				Last Mod. - 02/02/2016
				Check by * -
				Drawn by PVT 14/12/2015
				Designer P. Van Trappen

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Project/Equipment Fast Interlocks Detection System (FIDS)

Document

FIDS Carrier
Zynq SoC - Bank 12 & 13

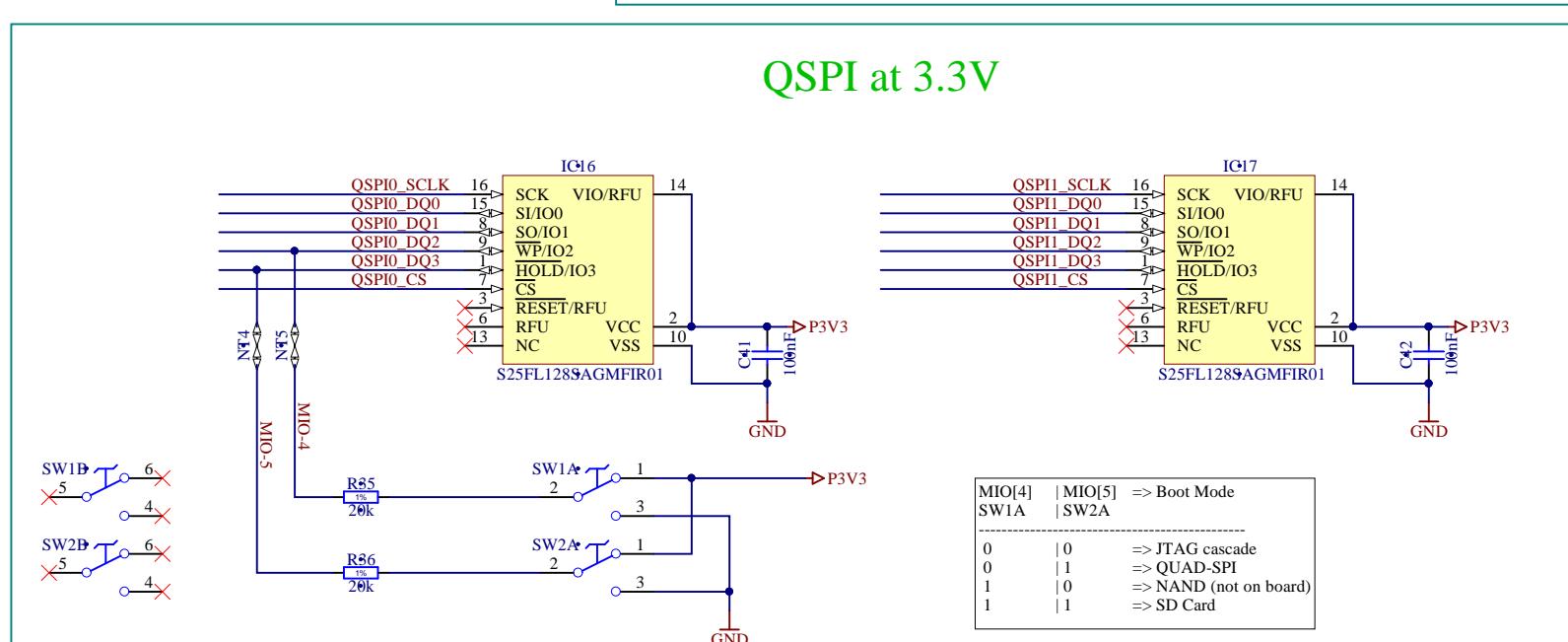
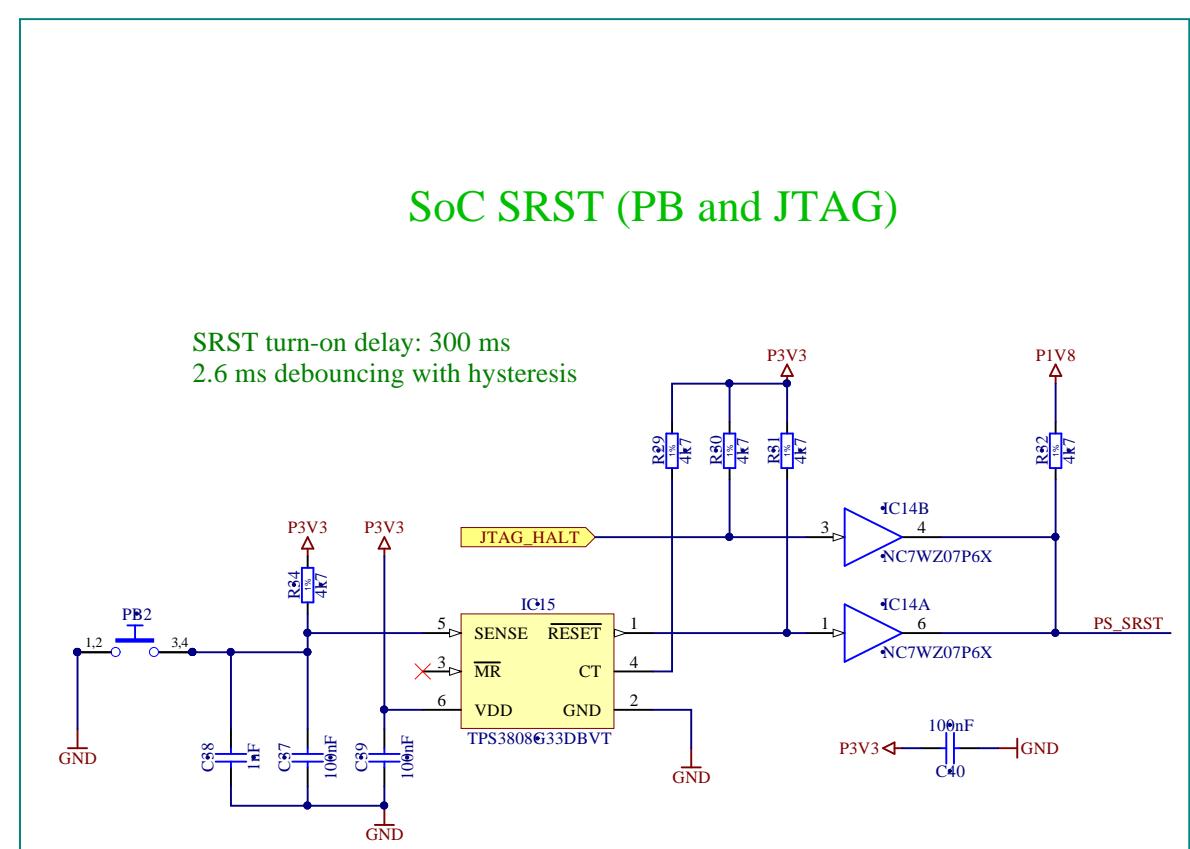
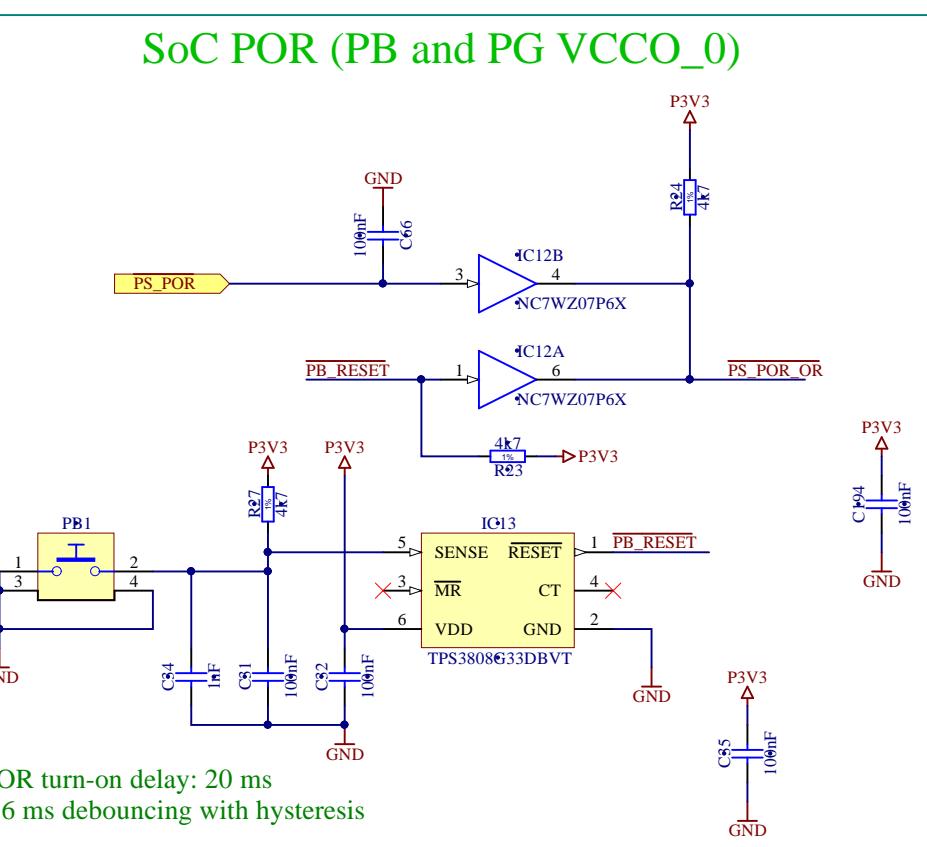
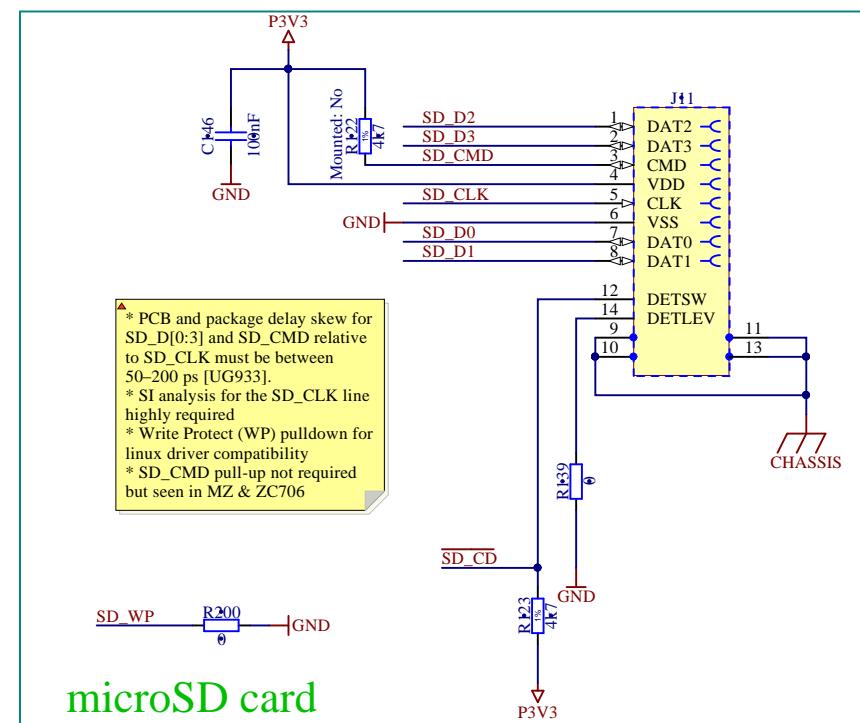
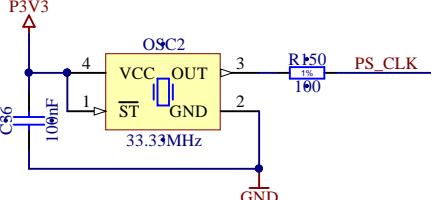
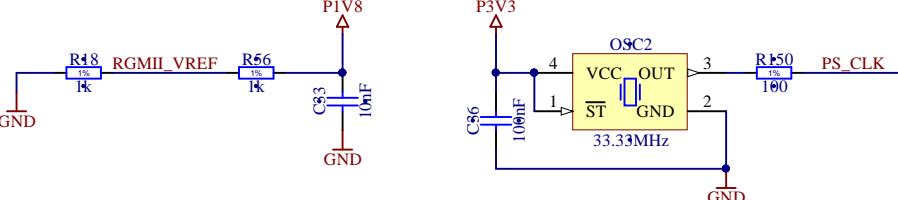
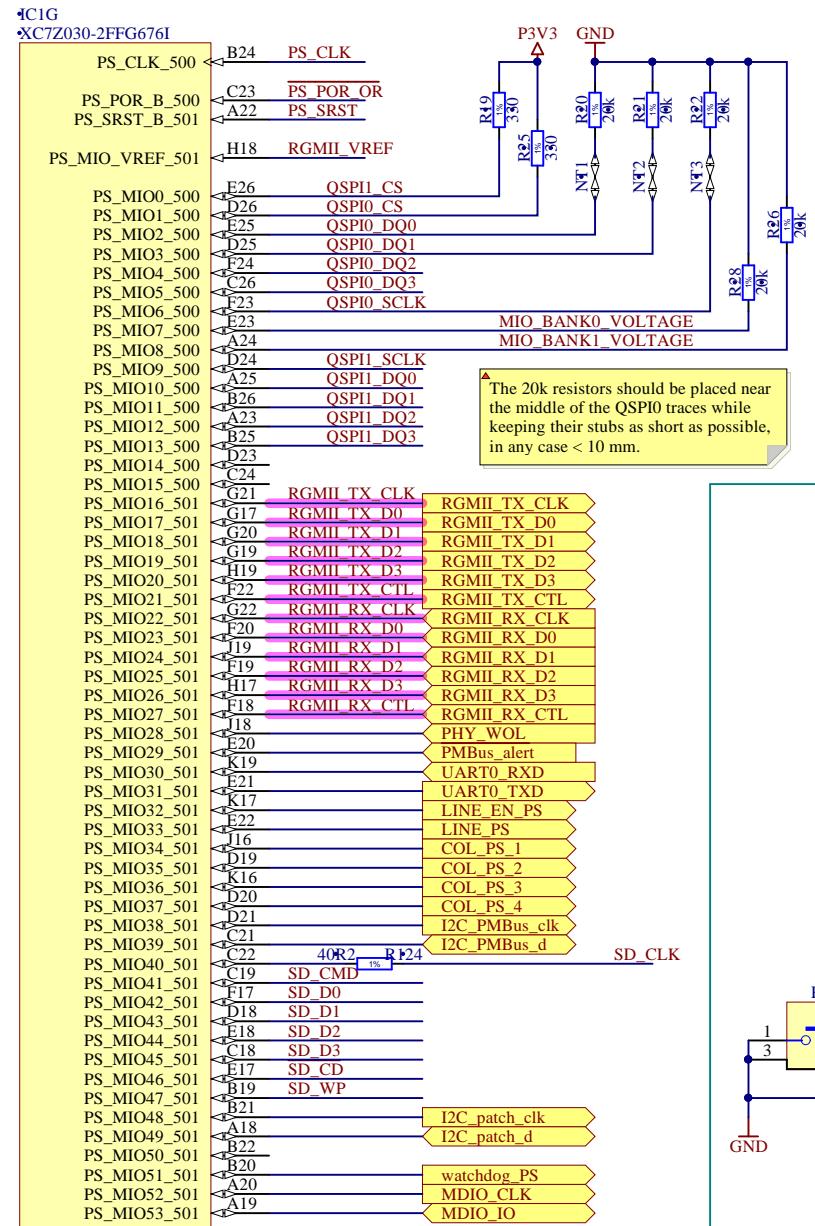
Designer	P. Van Trappen
Drawn by	PVT
Date	14/12/2015
Check by	*
Last Mod.	-
File	FIDS_carrier_Soc_bank12-13.SchDoc
Print Date	03/02/2016 15:22:36
Sheet	6 of 18

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EDA-XXXXXX-VX-X

Size A3 | Rev 0.4

VCCO_500=3.3V
VCCO_501=3.3V



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E

Project/Equipment Fast Interlocks Detection System (FIDS)
Document FIDS Carrier
Designer P. Van Trappen
Drawn by PVT
Check by *
Last Mod. 02/02/2016
File FIDS_carrier_Soc_bank500-501.SchDoc
Print Date 03/02/2016 15:22:36
Sheet 7 of 18

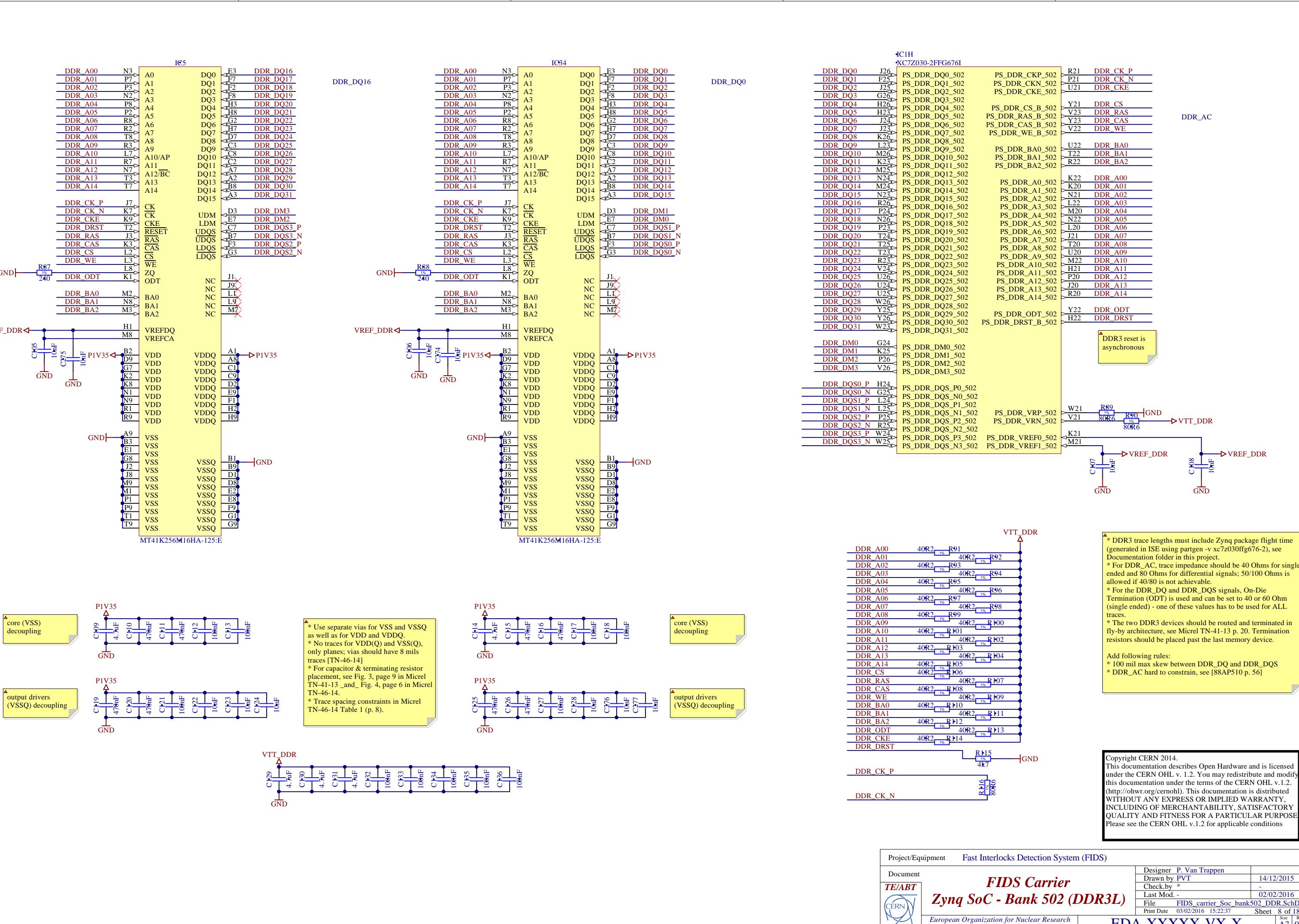
TE/ABT CERN

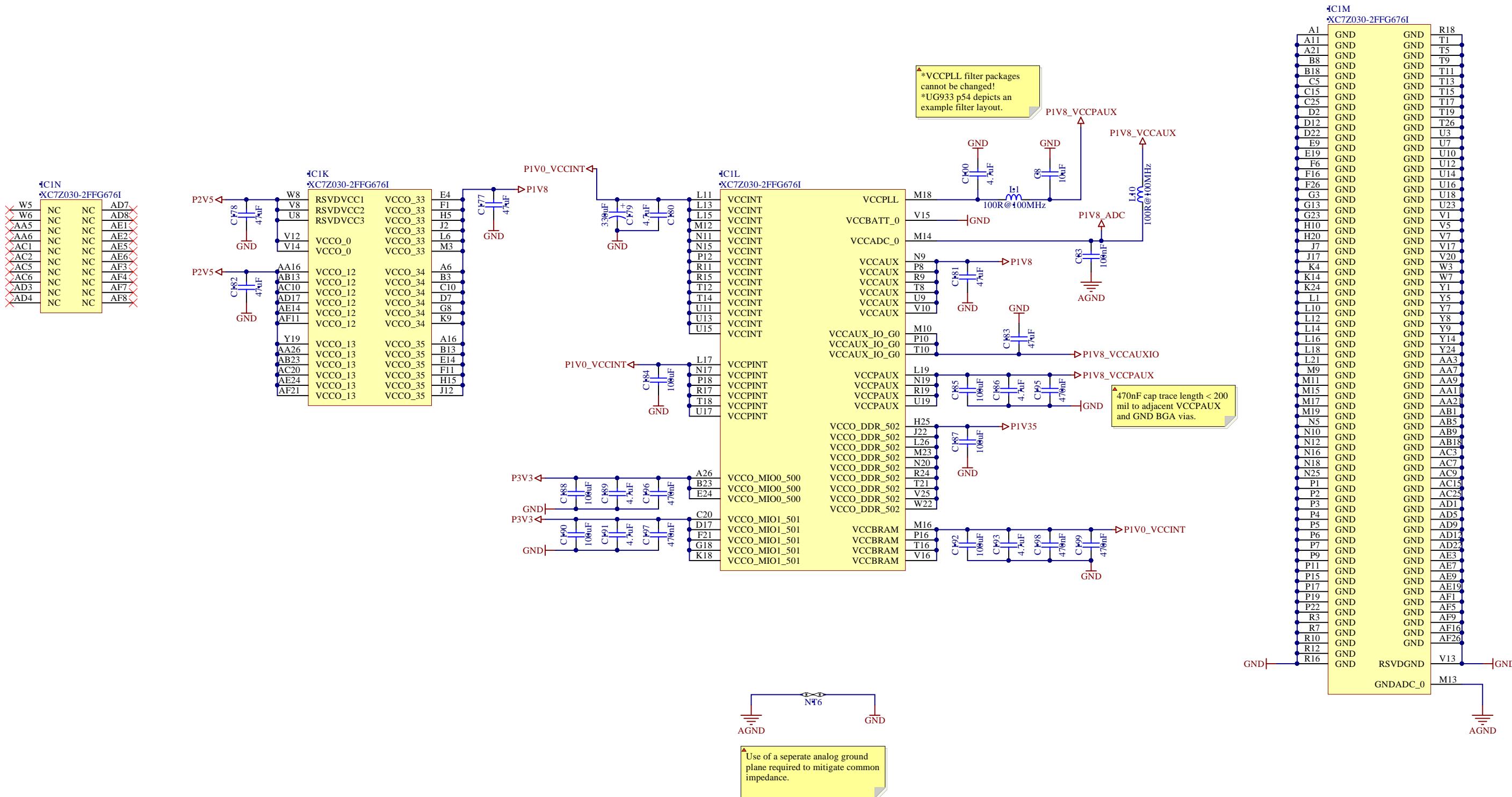
FIDS Carrier
Zynq SoC - Bank 500 & 501

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EDA-XXXXX-VX-X

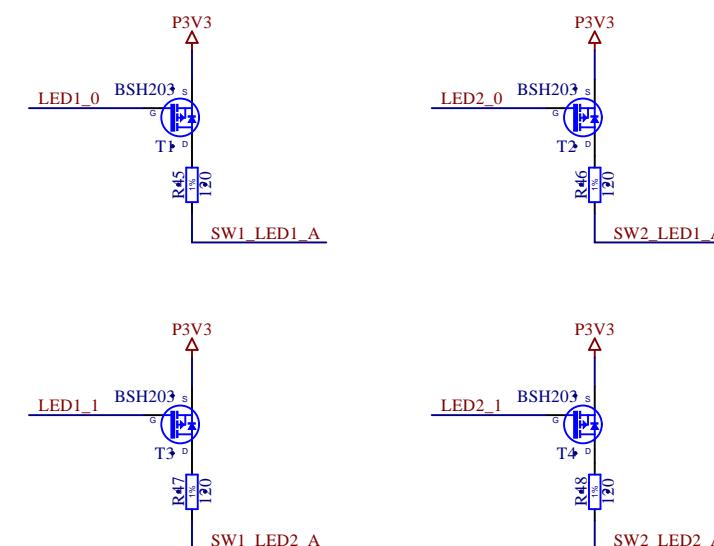
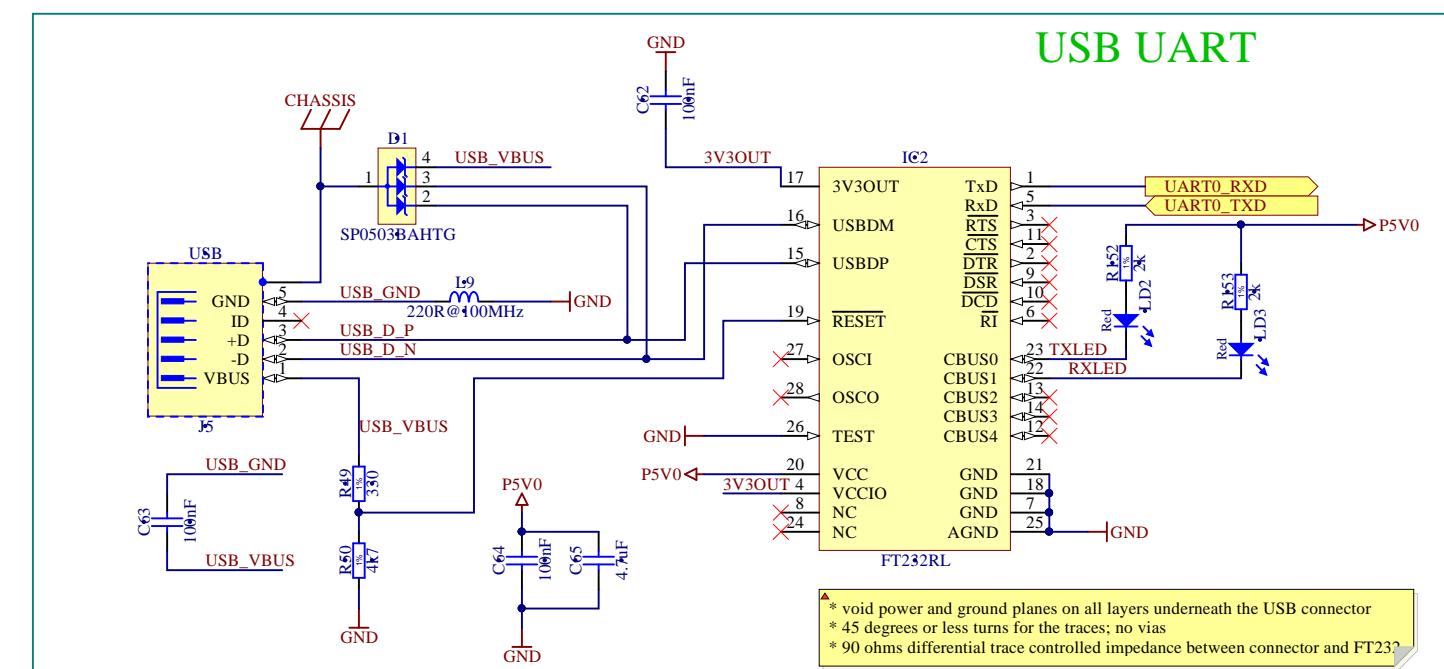
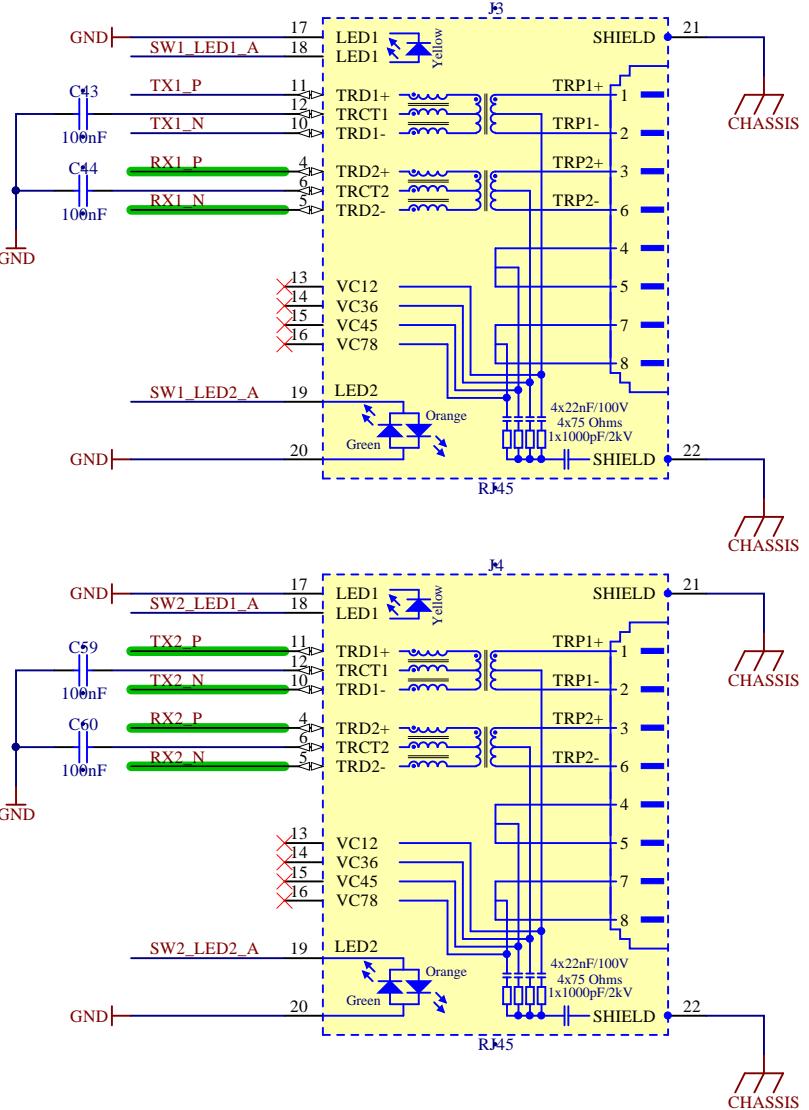
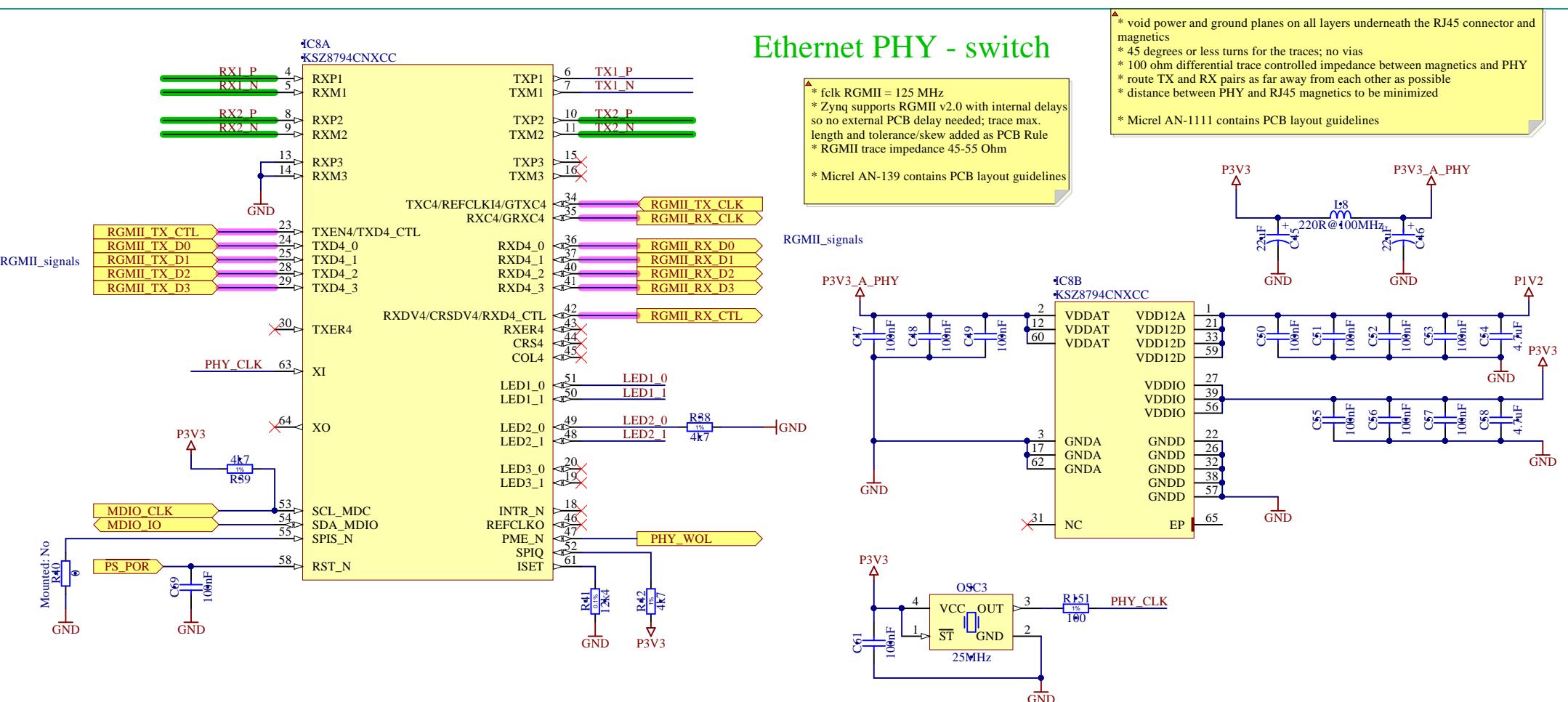
Size A3 Rev 0.4





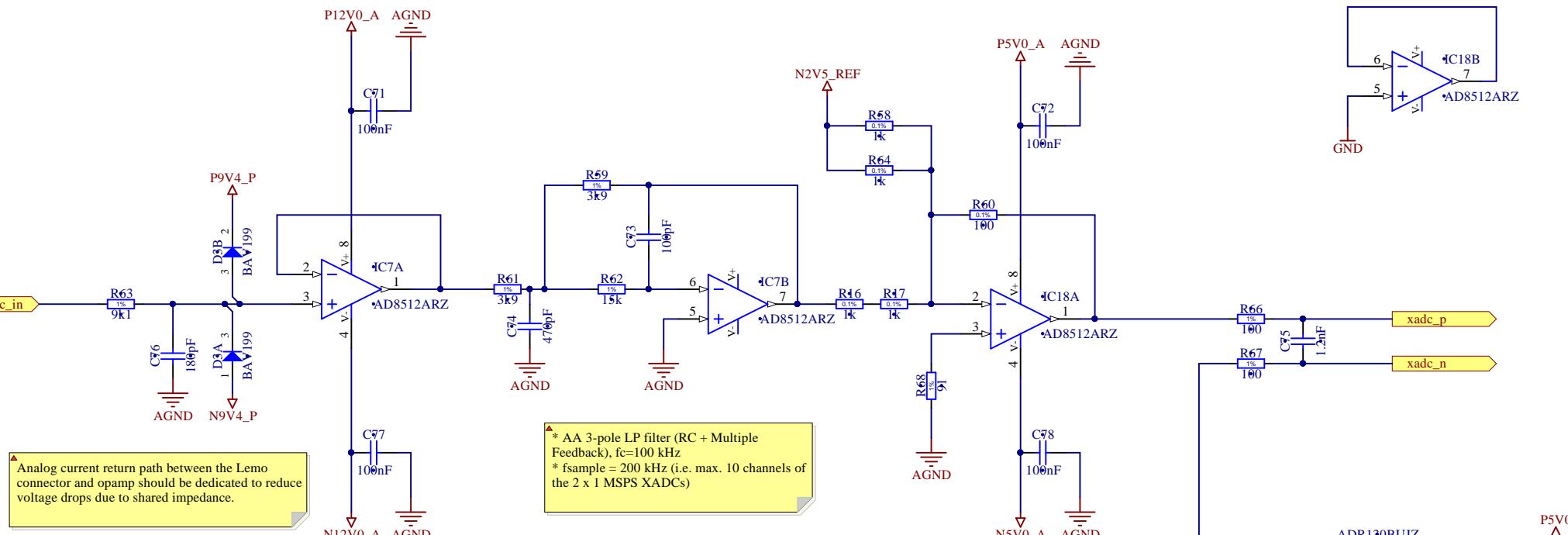
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Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	<i>FIDS Carrier Zynq SoC - Power</i>	Designer P. Van Trappen	
TE/ABT		Drawn by PVT	14/12/2015
		Check by *	-
		Last Mod. -	02/02/2016
		File FIDS_carrier_Soc_power.SchDoc	
		Print Date 03/02/2016 15:22:37	Sheet 9 of 18
			Size A3 0.4 Rev
	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	



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Project/Equipment		Fast Interlocks Detection System (FIDS)		
Document		<i>FIDS Carrier</i>		Designer P. Van Trappen
TE/ABT		<i>Ethernet, UART</i>		Drawn by PVT 14/12/2015
				Check by * -
				Last Mod. - 02/02/2016
				File FIDS_carrier_Ethernet_UART.SchDoc
				Print Date 03/02/2016 15:22:37 Sheet 10 of 18
European Organization for Nuclear Research CH-1211 Geneva 23 Switzerland			Size A3	Rev 0.4
EDA-XXXXX-VX-X				



Summing opamp: 1/20 input plus 0.5V offset addition to treat bipolar input signals.

AAF RC components to be placed as close as possible to SoC package! See xapp554 p. 5

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Project/Equipment Fast Interlocks Detection System (FIDS)

Document

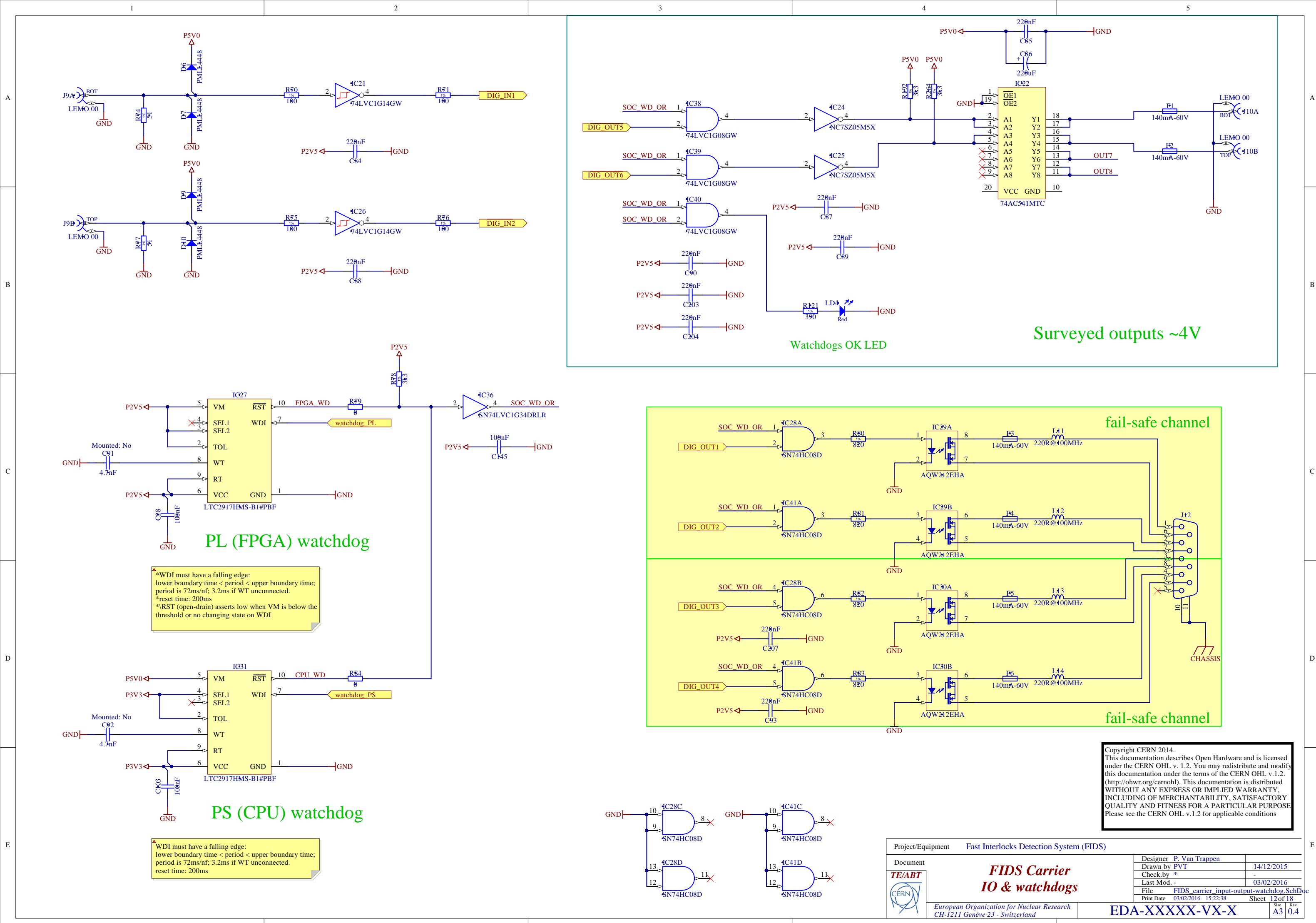


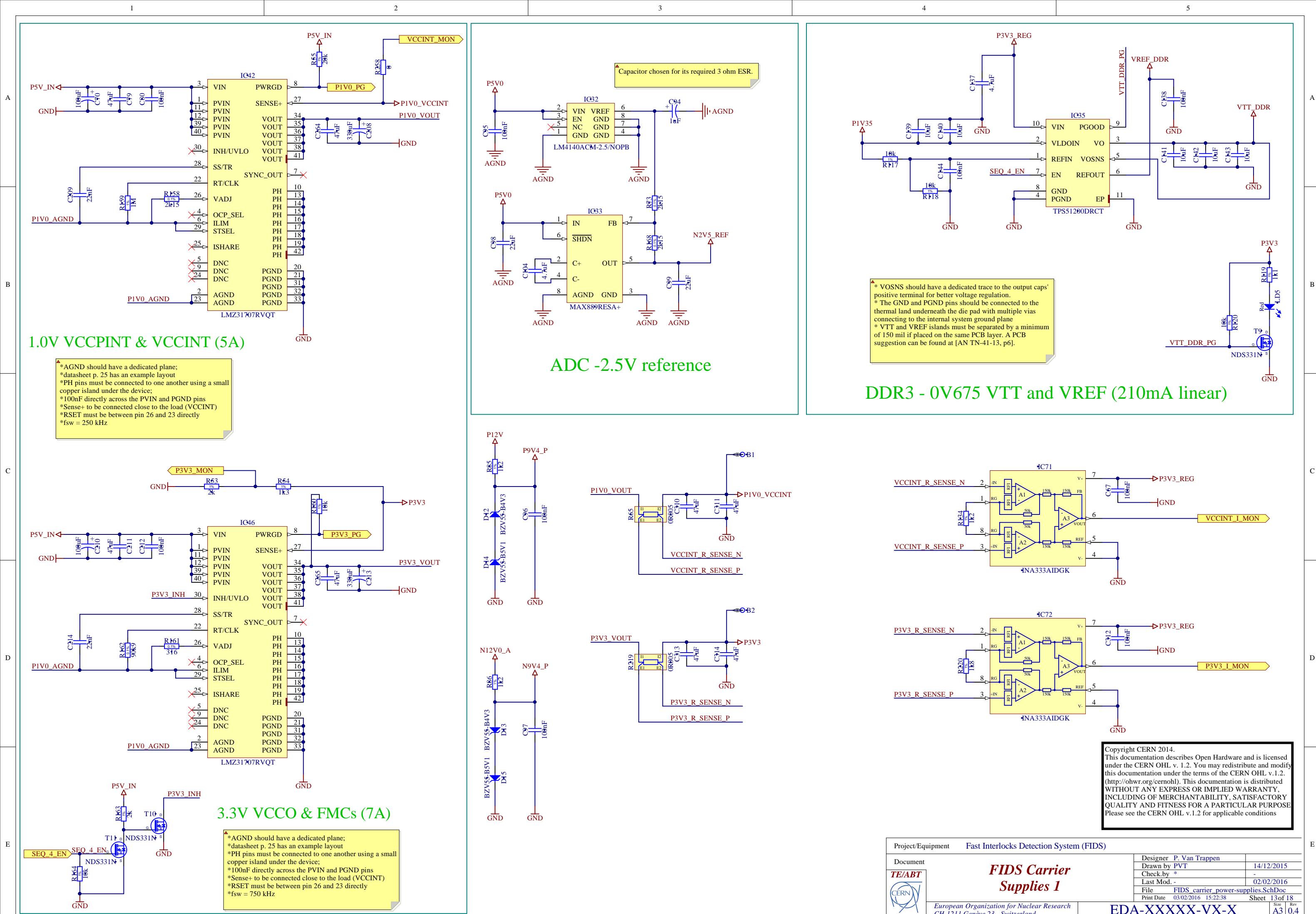
FIDS Carrier Analog input

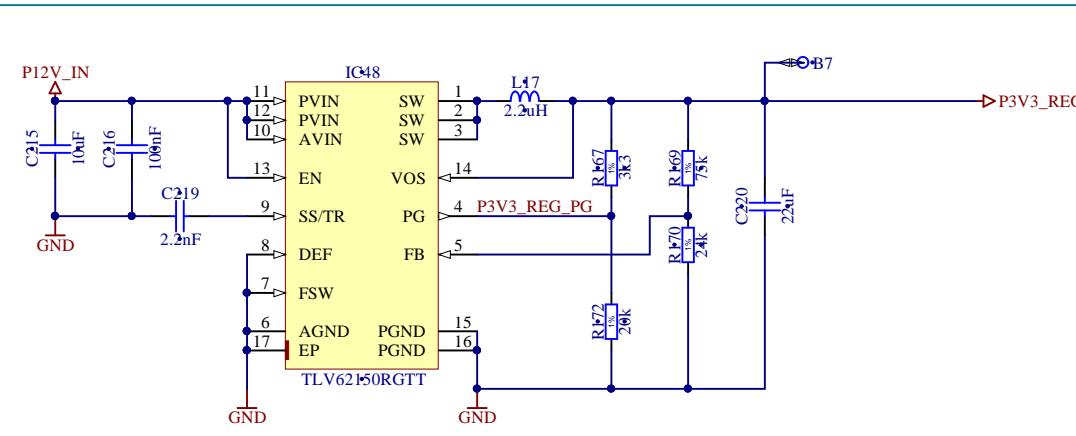
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-XXXXX-VX-X

Designer	P. Van Trappen
Drawn by	PVT
Check by	*
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File	FIDS_carrier_analog-input.SchDoc
Print Date	03/02/2016 15:22:38
Sheet	11 of 18
Size	A4
Rev	0.4

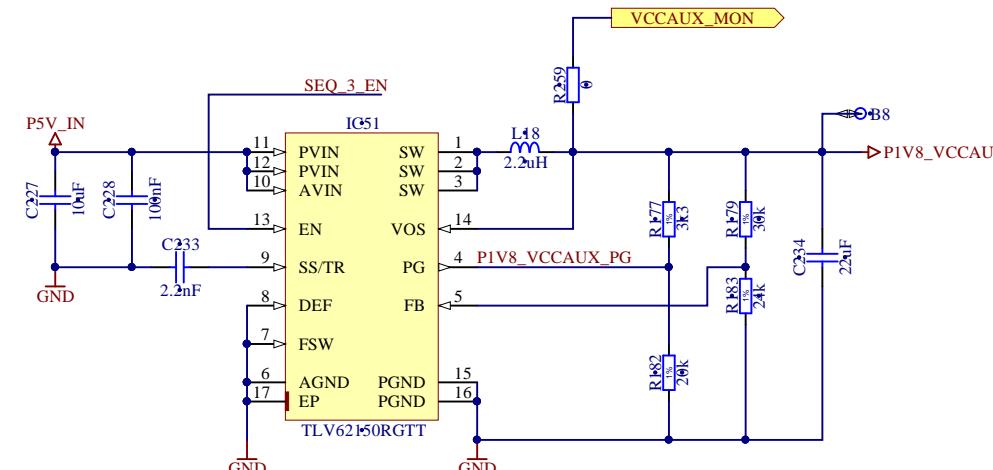






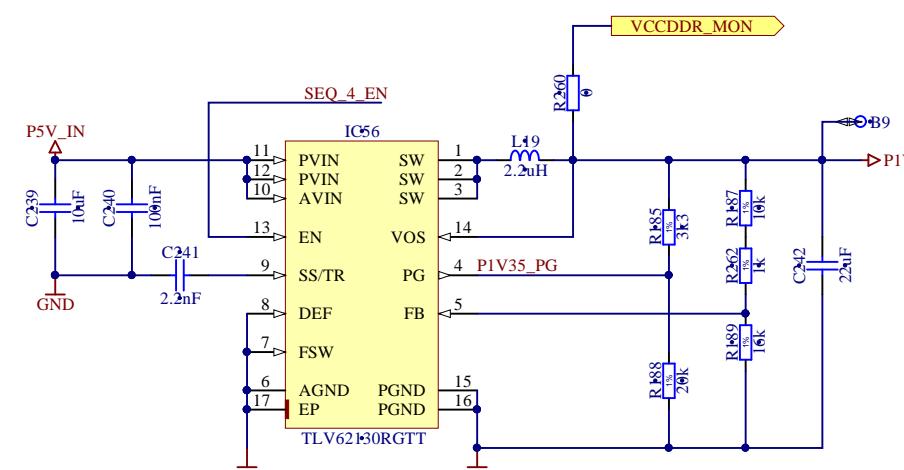
3.3V VREG (1A)

- *fsw = 2.5 MHz
- *layout example at datasheet p.21
- *100nF directly across the AVIN and AGND pins



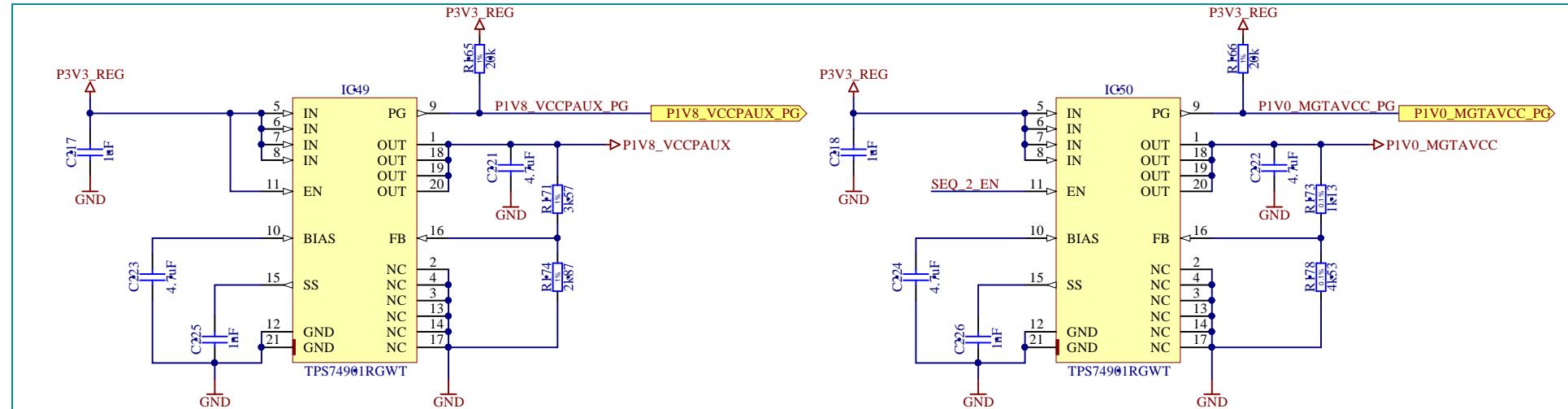
1.8V VCCAUX (800mA)

- *fsw = 2.5 MHz
- *layout example at datasheet p.21
- *100nF directly across the AVIN and AGND pins



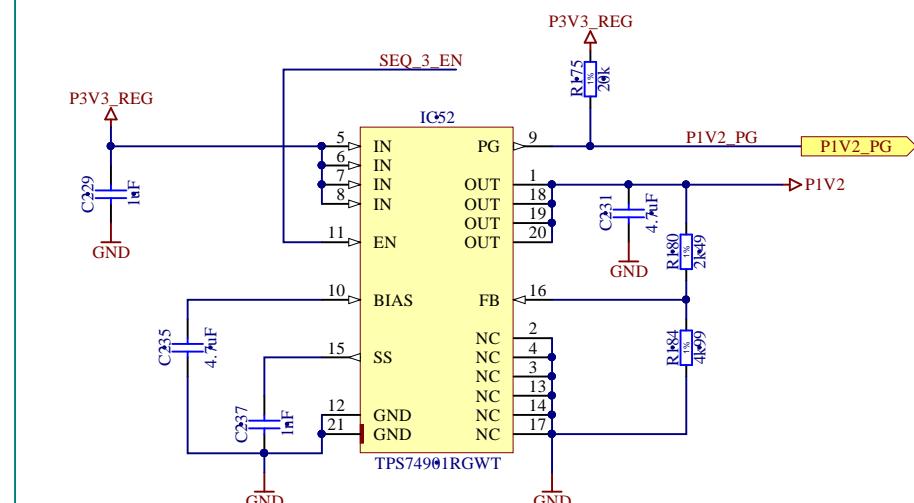
1.35V VCCDDR (1.1A)

*fsw = 2.5 MHz
*layout example at datasheet p.22
*100. Editing the μ controller AVIN and AGND pins



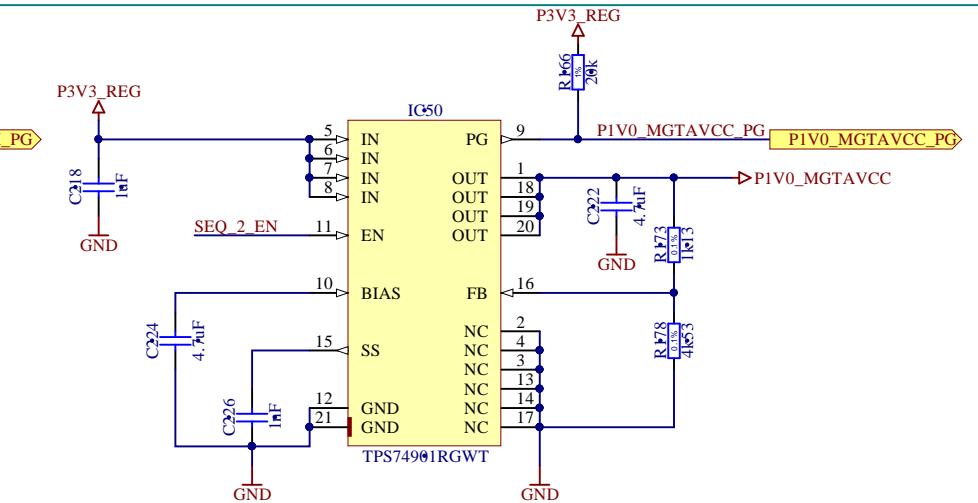
1.8V VCCPAUX (120mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; only 180 mW dissipation with a theta_{JA} of 120 °C/W.



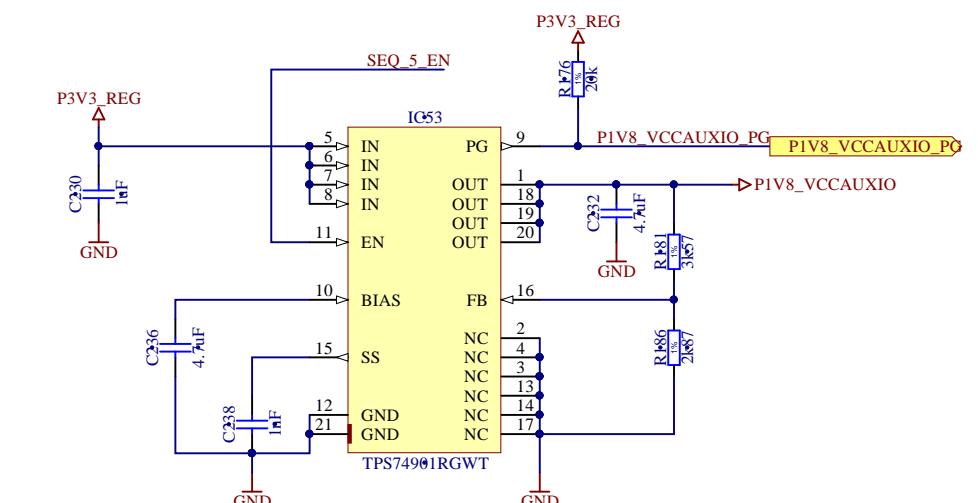
1.2V all (130mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area: 273 mW dissipation with a theta_{JA} of 120 °C/W.



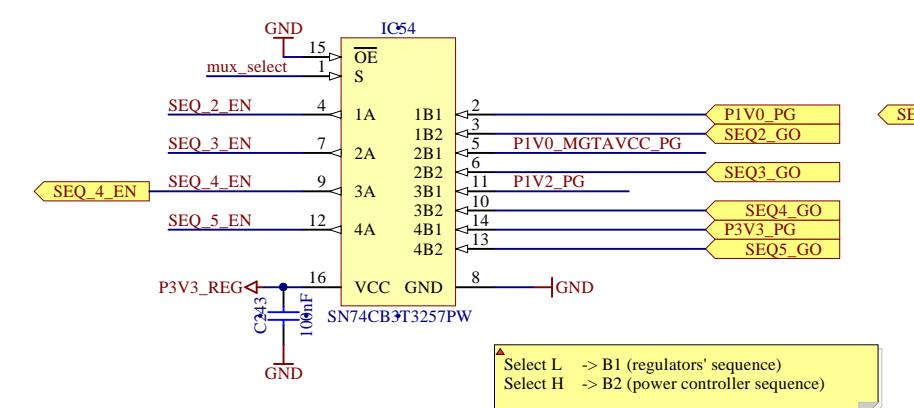
1.0V MGTAVCC (150mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 345 mW dissipation with a theta_{JA} of 120 °C/W.



1.8V VCCAUX IO (130mA linear)

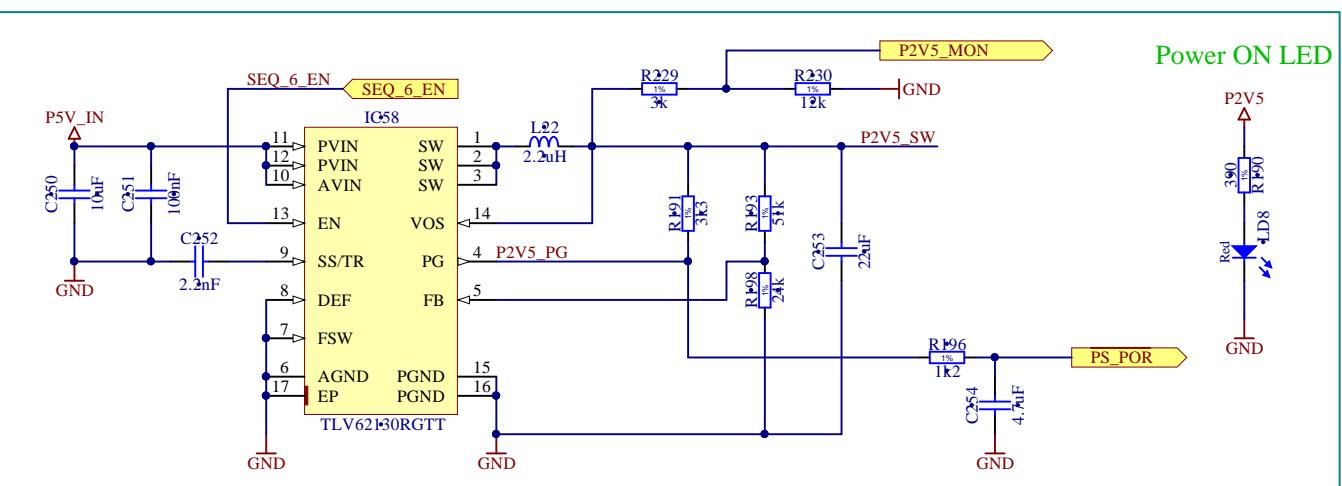
*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area: 273 mW dissipation with a theta JA of 120 °C/W.



The circuit diagram illustrates the connection of six sequence enable lines (SEQ_2_EN through SEQ_6_EN) to a 6-to-1 multiplexer (MUX). The MUX has a 2k resistor between its inputs and ground. The output of the MUX is connected to a switch (SW5), which then connects to a 2k resistor and finally to the P3V3_L pin.

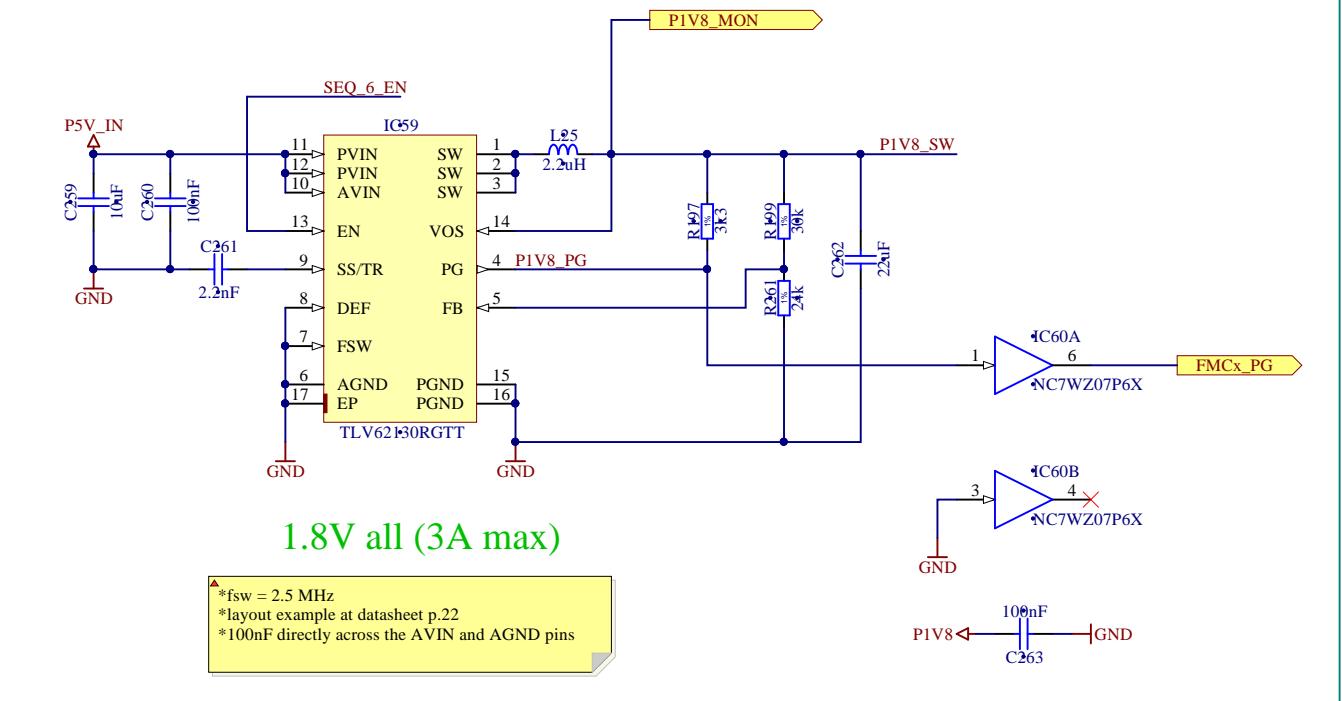
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Project/Equipment	Fast Interlocks Detection System (FIDS)	
Document		Designer P. Van Trappen
TE/ABT	<i>FIDS Carrier</i>	Drawn by PVT
	<i>Supplies 2</i>	14/12/2015
		Check by -
		Last Mod. -
		File FIDS_carrier_power-supplies-2.SchDoc
		Print Date 03/02/2016 15:22:38
		Sheet 14 of 18
European Organization for Nuclear Research CH-1211 Geneva 23 Switzerland		Size Rev A3 0.4
EDA-XXXXX-VX-X		



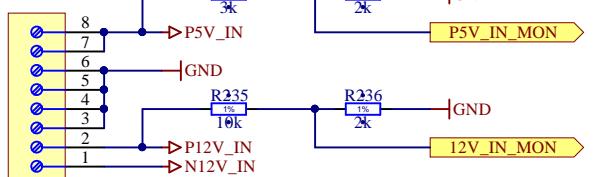
2.5V all (3A max)

- *fsw = 2.5 MHz
- *layout example at datasheet p.22
- *100nF directly across the AVIN and AGND pins



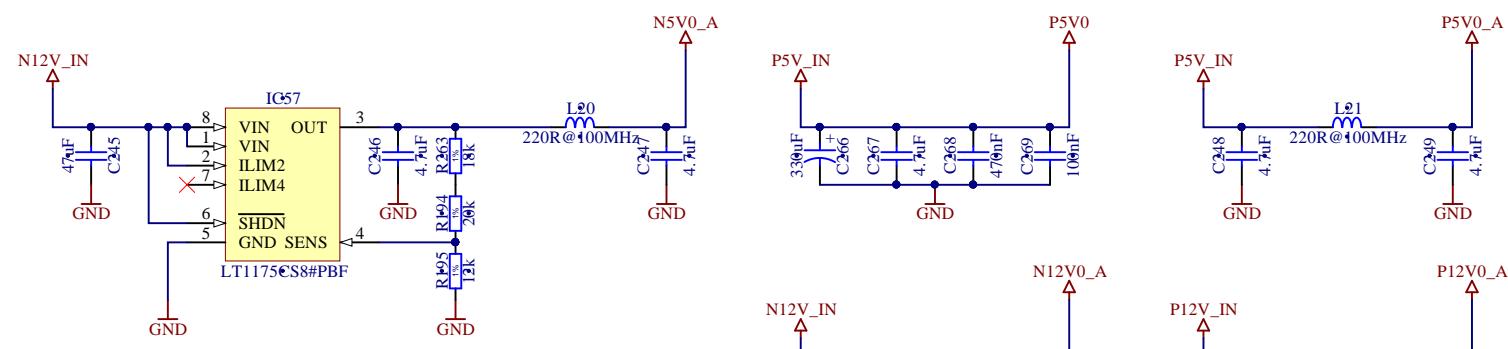
1.8V all (3A max)

- *fsw = 2.5 MHz
- *layout example at datasheet p.22
- *100nF directly across the AVIN and AGND pins



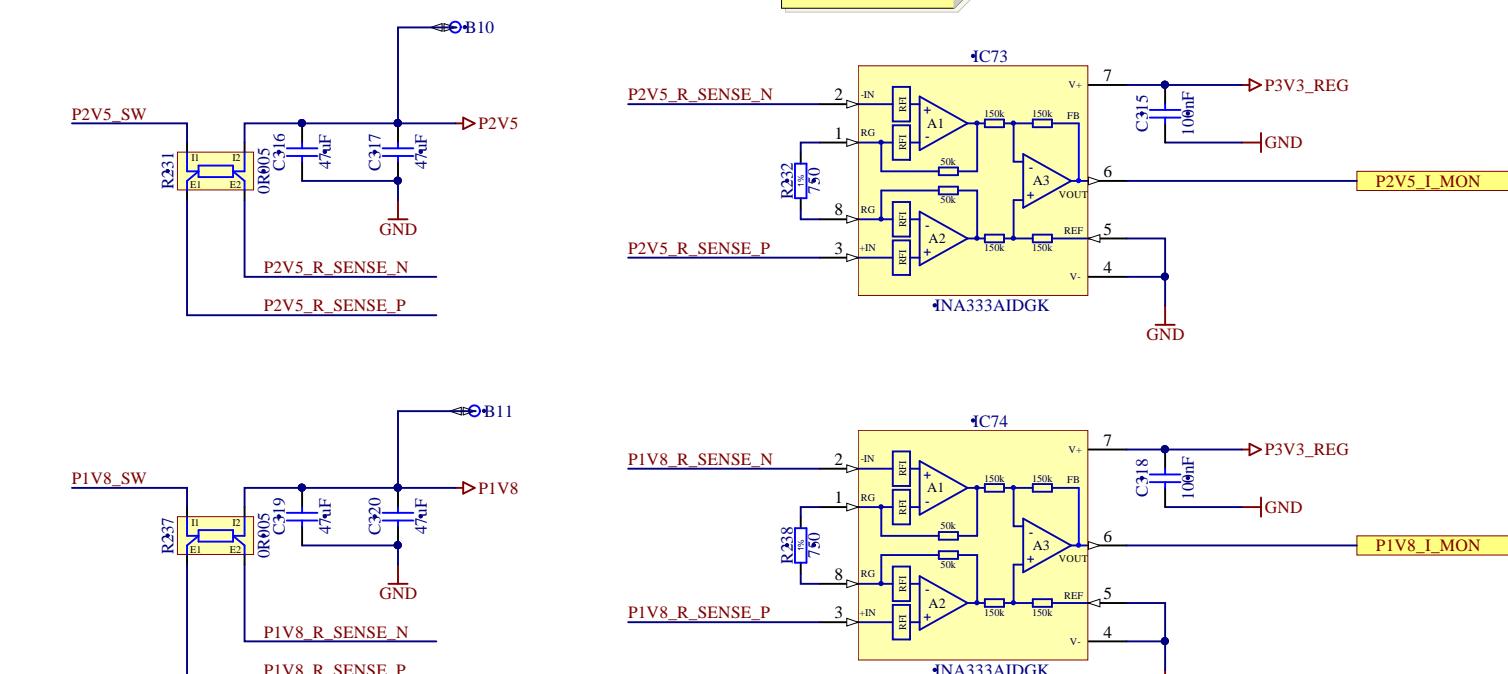
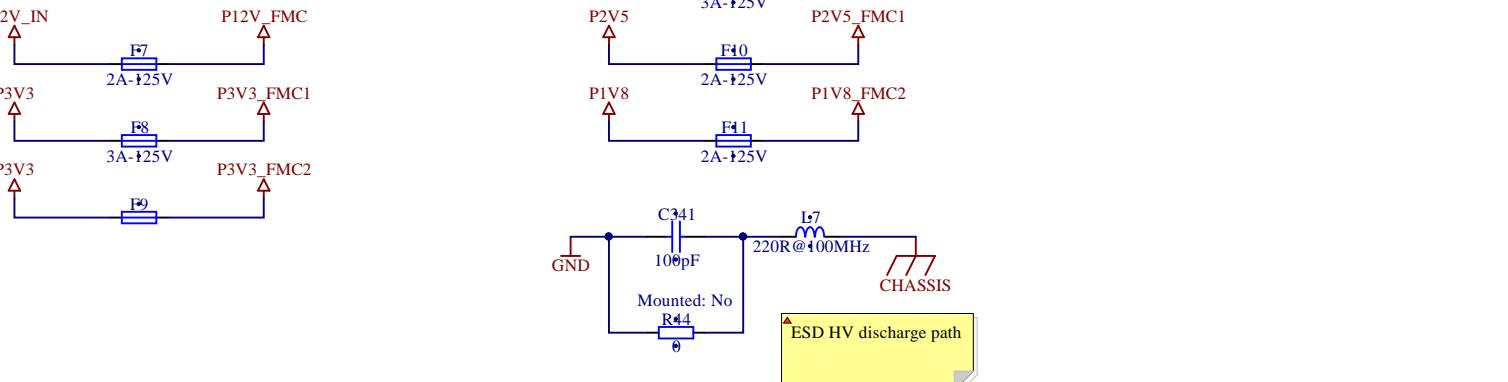
- ▲ A 80W switching power supply is needed:
 - * 43W 5V
 - * 25W 12V

Suggestion: Artesyn LPT102-M



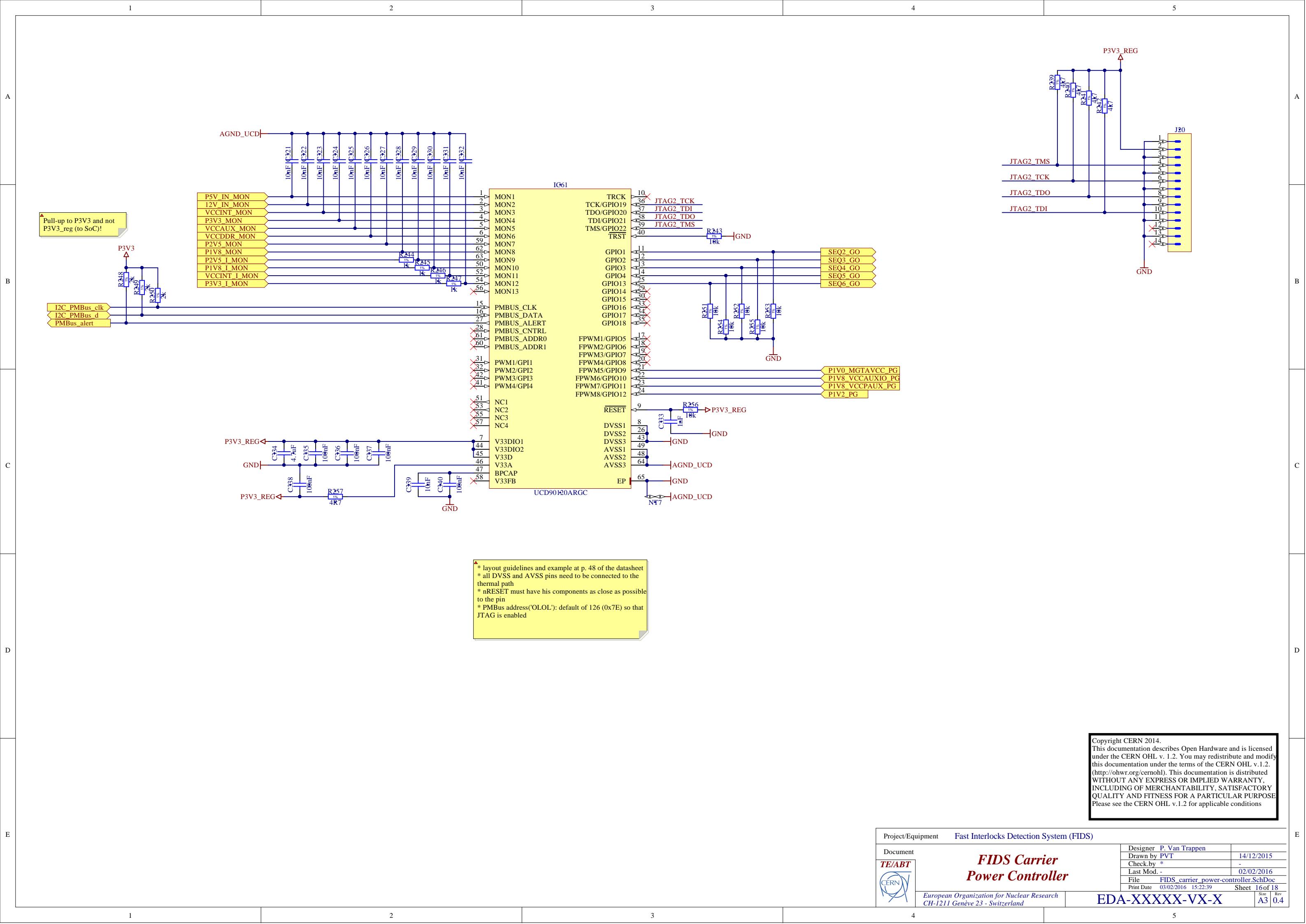
-5.0V all (100mA linear)

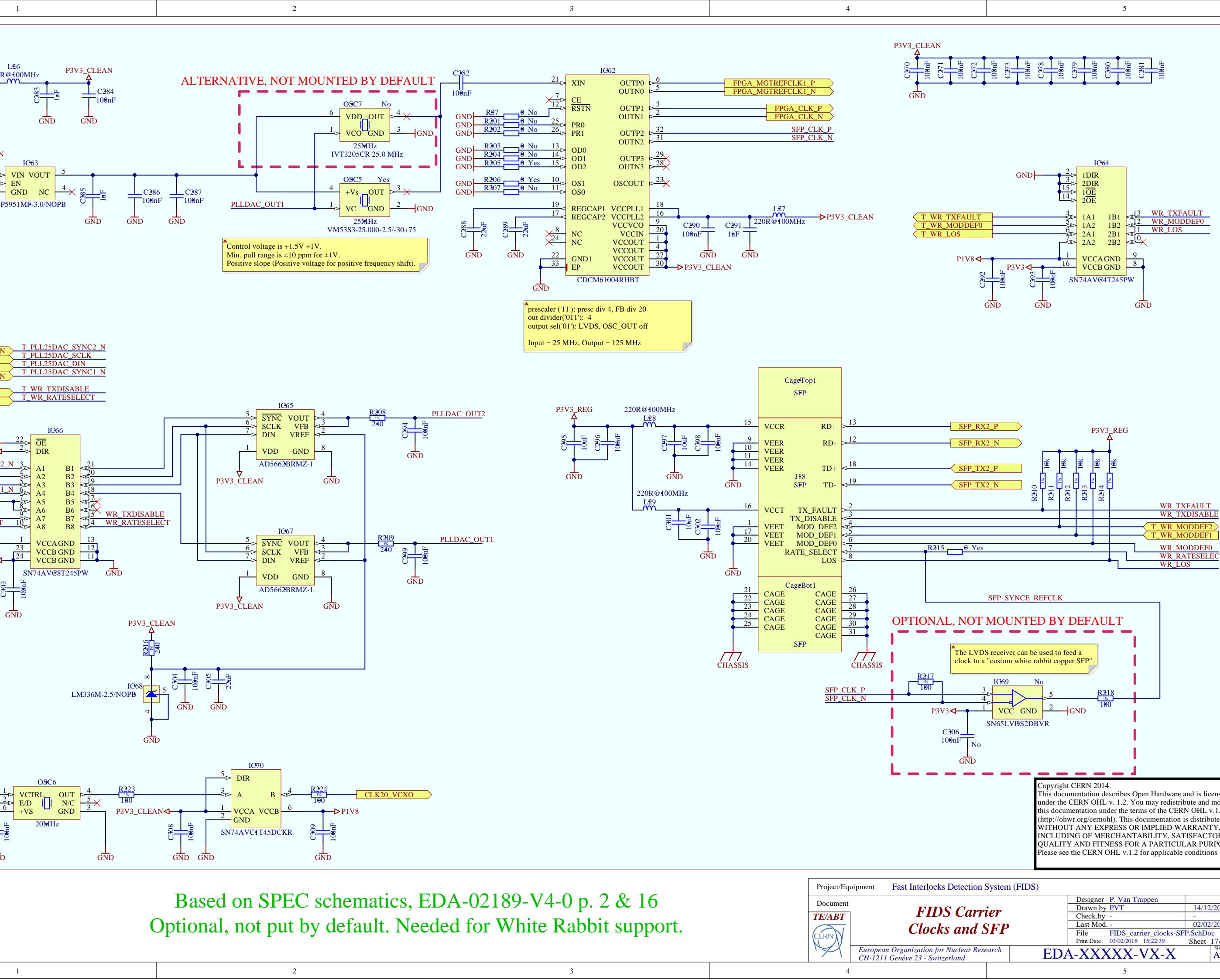
*pins 1 & 8 must be connected to a 20x20 mm amount of copper PCB area; 700 mW dissipation with a theta_JA of 60-100 °C/W.
*ILIM2 open -> max Iout=400mA.



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Project/Equipment	Fast Interlocks Detection System (FIDS)	
Document		Designer P. Van Trappen
TE/ABT	<i>FIDS Carrier</i>	Drawn by PVT
	<i>Supplies 3</i>	14/12/2015
		Check by *
		Last Mod. -
		02/02/2016
		File FIDS_carrier_power-supplies-3.SchDoc
		Print Date 03/02/2016 15:22:38
		Sheet 15 of 18
European Organization for Nuclear Research CH-1211 Geneva 23, Switzerland		Size Rev A3 0.4
EDA-XXXXX-VX-X		





Based on SPEC schematics, EDA-02189-V4-0 p. 2 & 16
Optional, not put by default. Needed for White Rabbit support.

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	Designer P. Van Trappen	Drawn by PVT	14/12/2015
TE/ABT	Check-by -	-	-
CERN	Last Mod. -	-	02/02/2016
	File FIDS_carrier_clocks-SFP.SchDoc	Print Date 03/02/2016 15:22:39	Sheet 17 of 18
	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		Size A3 Rev 0.4
			EDA-XXXXX-VX-X

