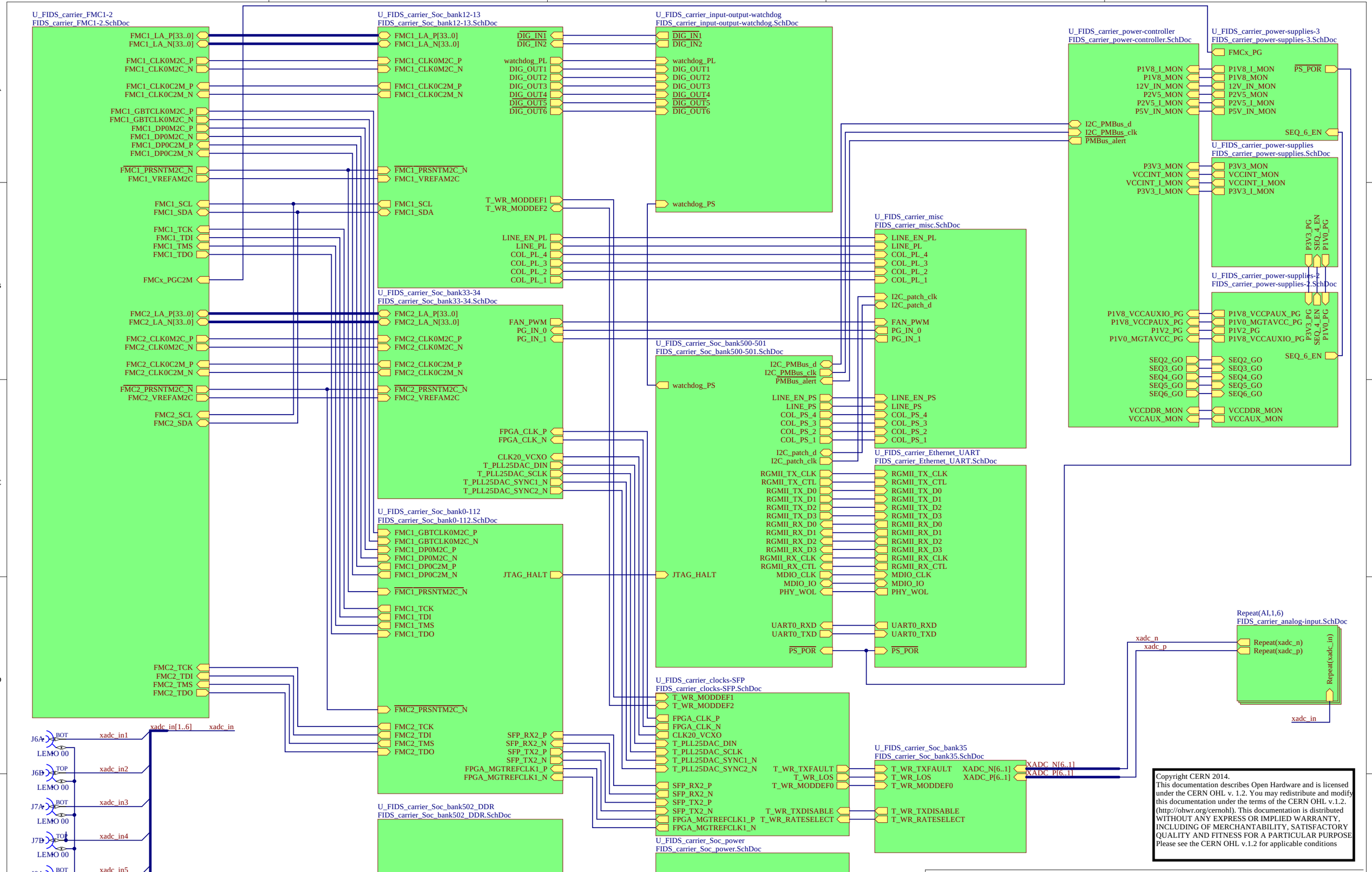
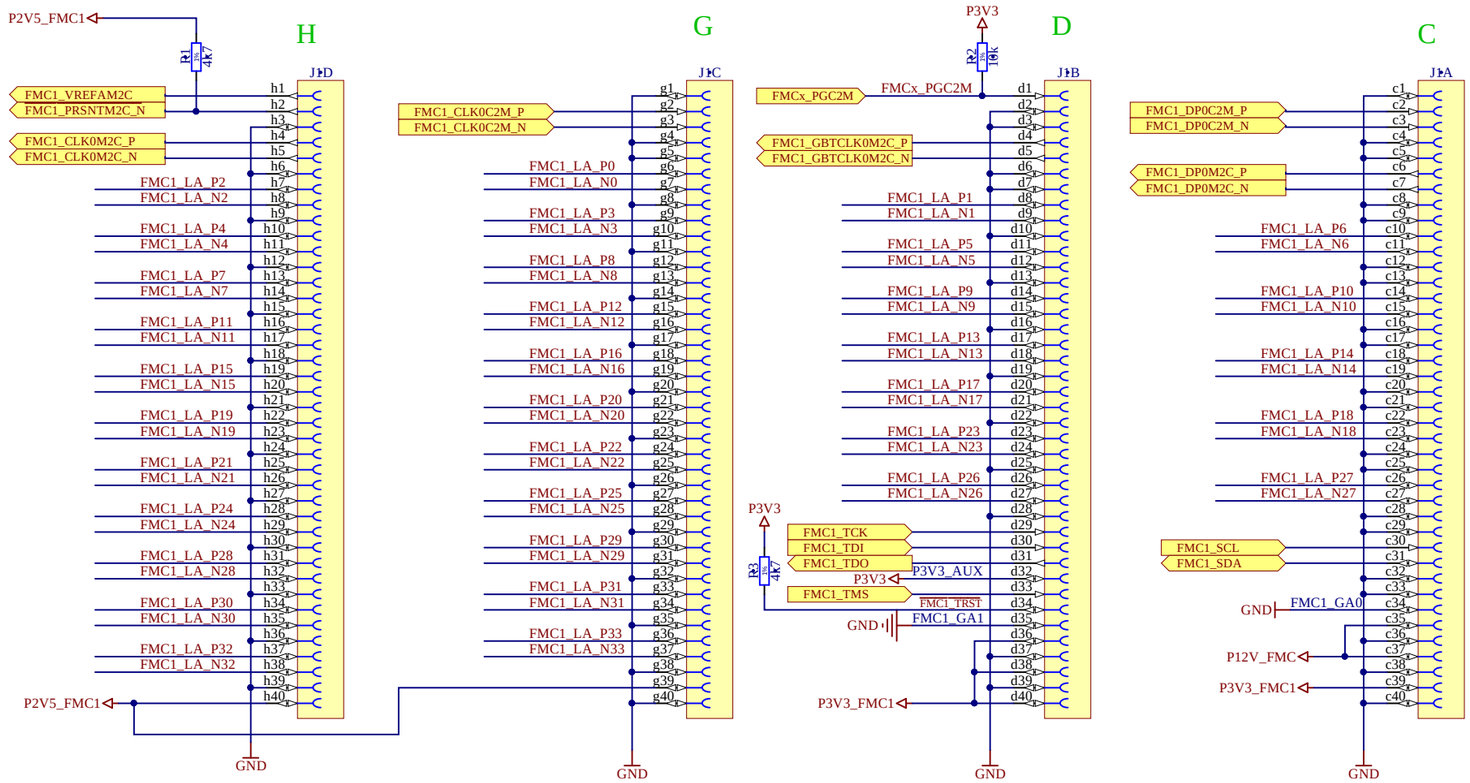


Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Top pages overview**	Designer	P. Van Trappen
TE/ABT		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 03/02/2016
		File	FIDS_carrier_top.SchDoc
		Print Date	03/02/2016 15:22:35 Sheet 1 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4

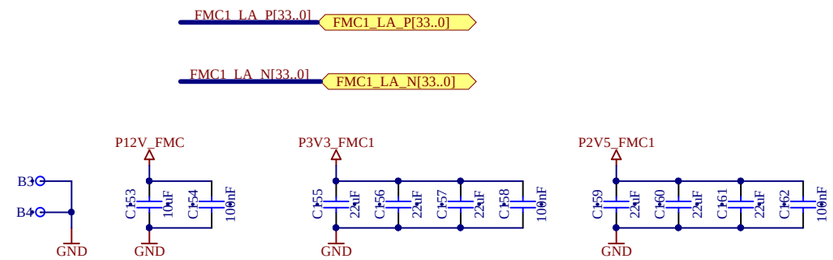


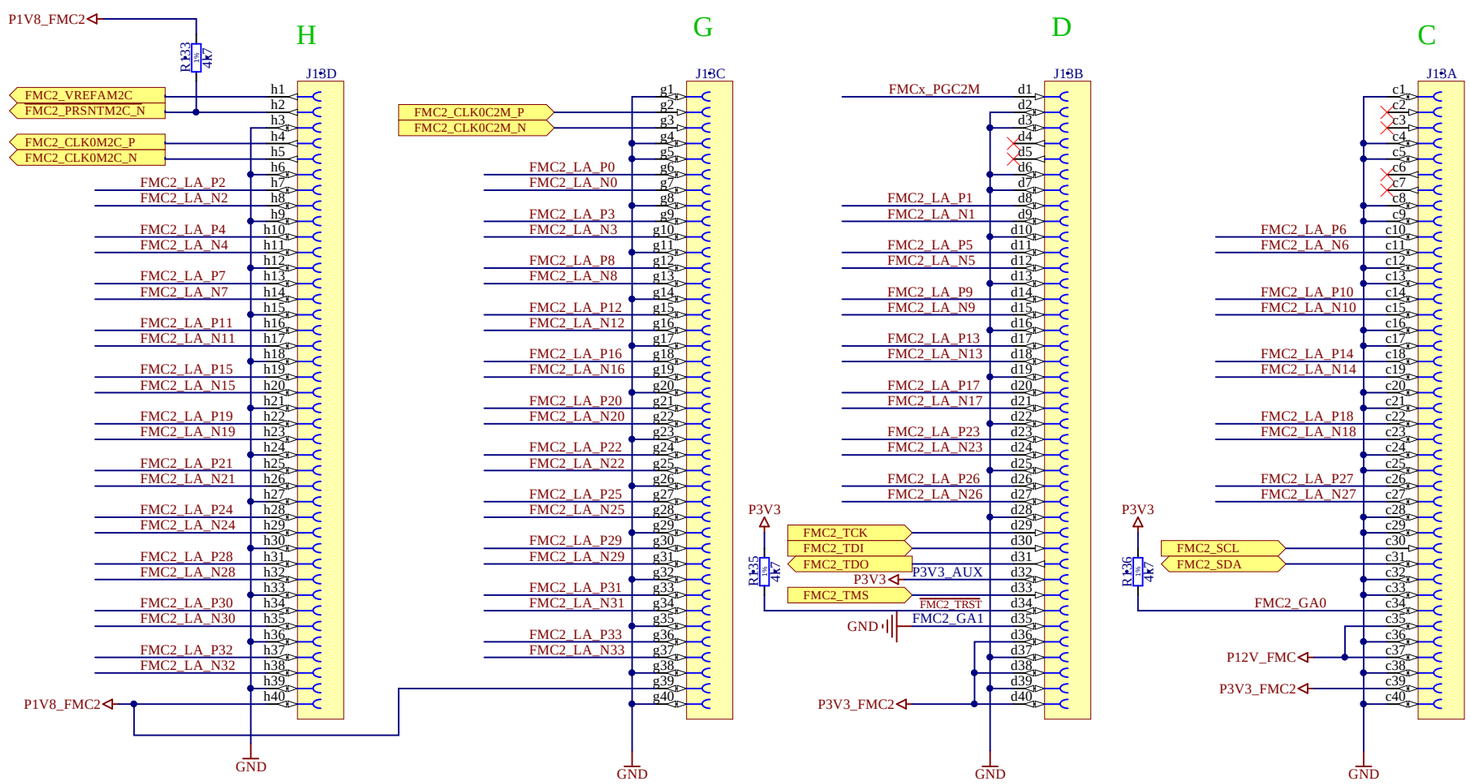
ANSI/VITA 57.1:
For all differential pairs:
Recommendation 5.3: When signals are routed differentially each pair should provide a differential impedance of 100Ω +/- 10%

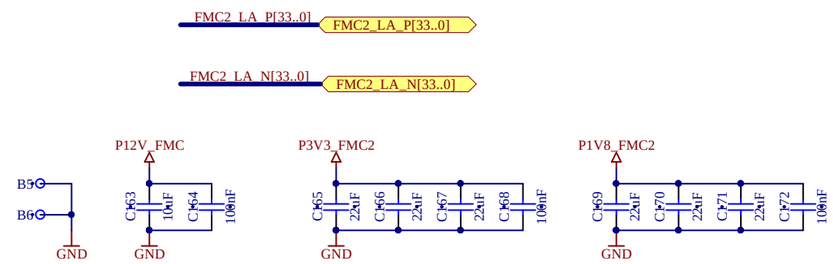
For FMCx_CLK0M2C and FMCx_CLK0C2M pairs:
Rule 5.22: Clock traces shall provide a differential impedance of 100Ω +/-10%
Rule 5.23: The differential length mismatch on each differential clock pair shall be a maximium 11ps.

For the FMCx_DP0 pairs:
Rule 5.43: The differential length mismatch on each differential data pair shall 1ps.

For the FMCx_GBTCLK0M2C pairs:
Rule 5.48: Clock traces shall provide a differential impedance of 100Ω +/-10%
Rule 5.49: The differential length mismatch on each differential clock pair shall 11ps.

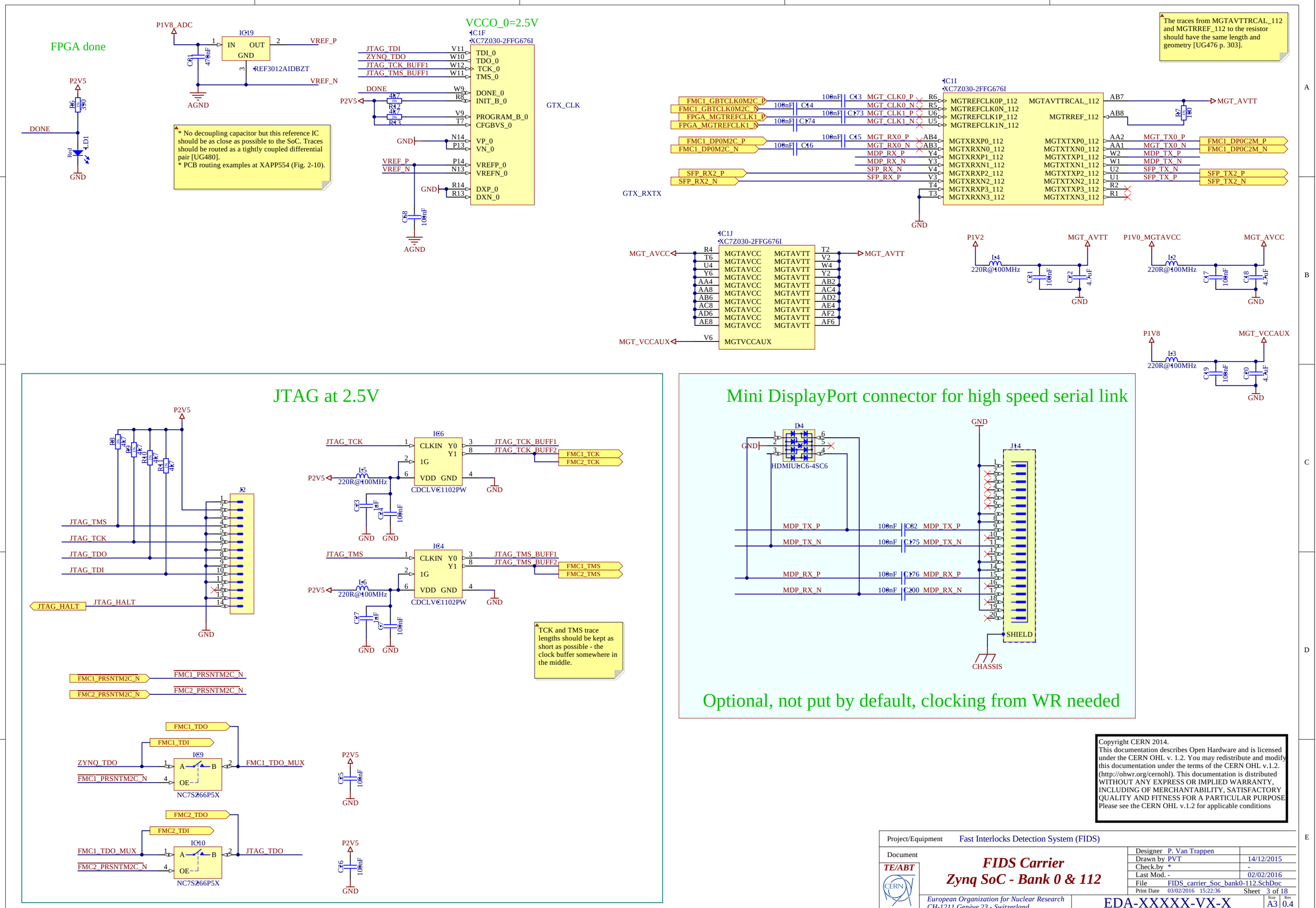






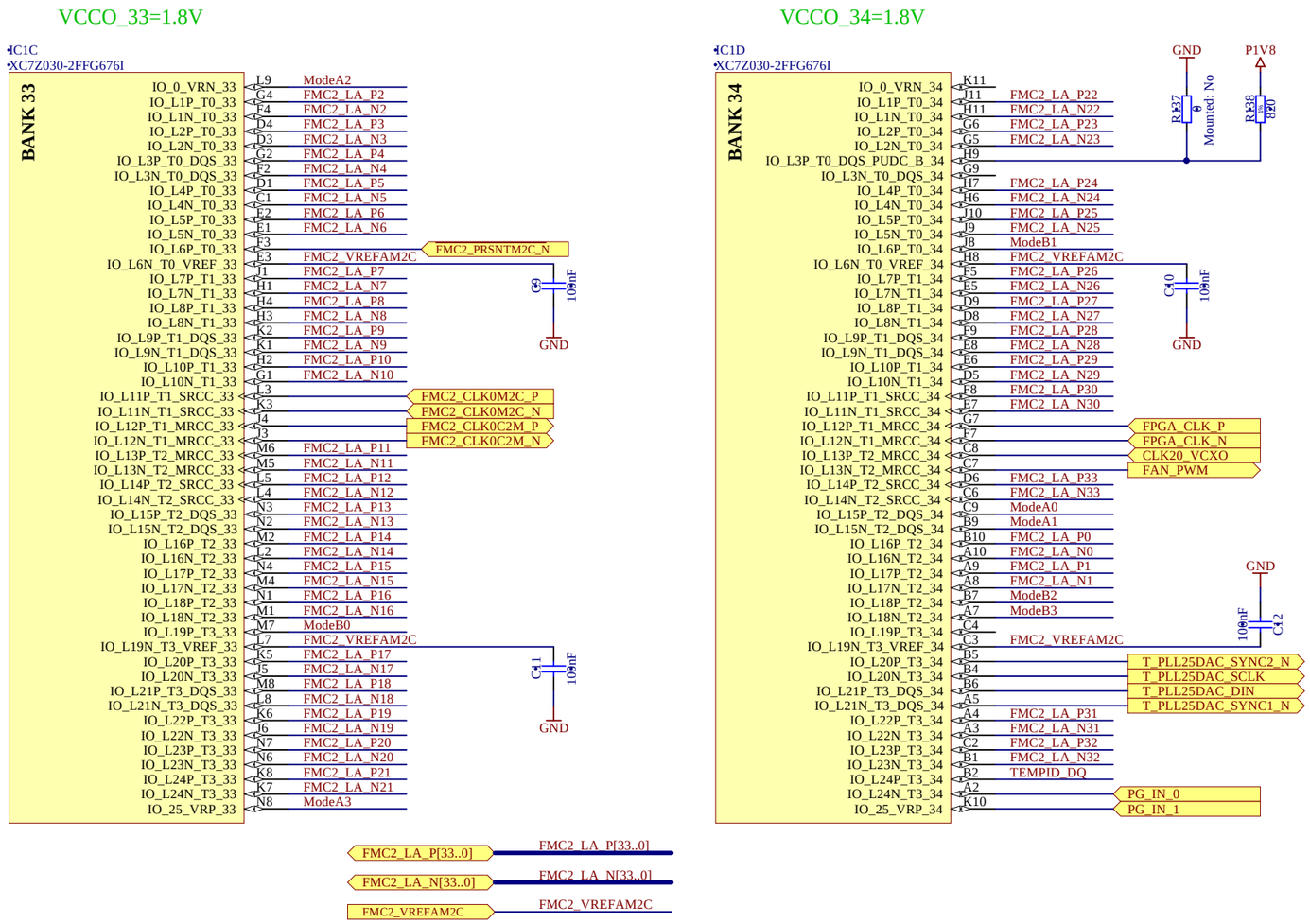
Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

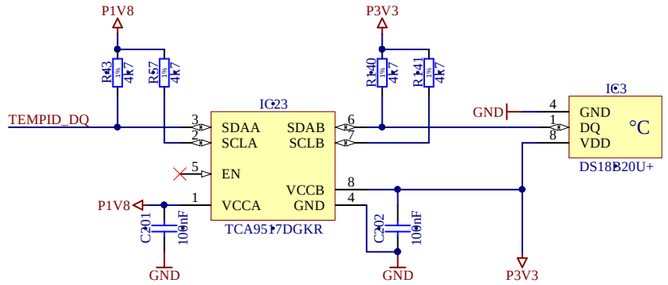
Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier** **FMC Connectors 1 & 2**	Designer P. Van Trappen	
TE/ABT		Drawn by PVT	14/12/2015
		Check.by *	-
		Last Mod. -	02/02/2016
		File FIDS_carrier_FMC1-2.SchDoc	
		Print Date 03/02/2016 15:22:35	Sheet 2 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4



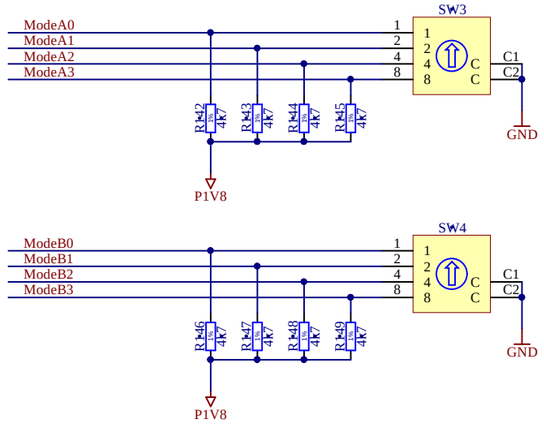
Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier** **Zynq SoC - Bank 0 & 112**	Designer P. Van Trappen	
TE/ABT		Drawn by PVT	14/12/2015
		Check.by *	-
		Last Mod. -	02/02/2016
		File FIDS_carrier_Soc_bank0-112.SchDoc	
		Print Date 03/02/2016 15:22:36	Sheet 3 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4





Unique ID and temperature



Generator mode selection

Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier** **Zynq SoC - Bank 33 & 34**	Designer	P. Van Trappen
TE/ABT		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_Soc_bank33-34.SchDoc
		Print Date	03/02/2016 15:22:36 Sheet 4 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4

No XADC pin swapping allowed! Input numbering doesn't follow package numbering but the order is imporant for full sampling rate support (i.e. simultaneous sampling mode).

VCCO_35=1.8V

C1E
XC7Z030-2FFG676I

BANK 35

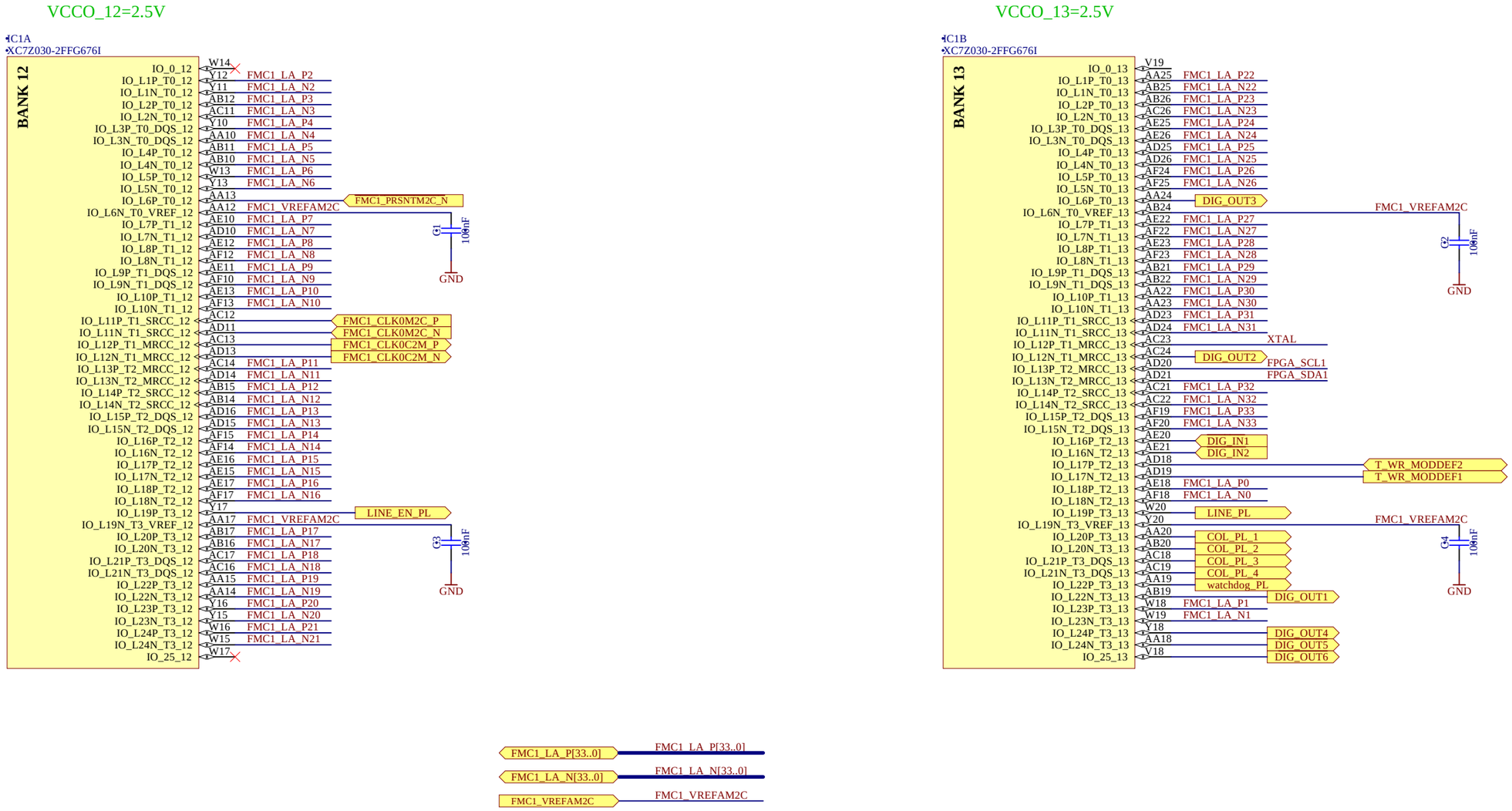
IO_0_VRN_35	H16	
IO_L1P_T0_AD0P_35	E12	XADC_P1
IO_L1N_T0_AD0N_35	E12	XADC_N1
IO_L2P_T0_AD8P_35	E10	XADC_P4
IO_L2N_T0_AD8N_35	D10	XADC_N4
IO_L3P_T0_DQS_AD1P_35	G10	XADC_P2
IO_L3N_T0_DQS_AD1N_35	F10	XADC_N2
IO_L4P_T0_35	E11	
IO_L4N_T0_35	D11	
IO_L5P_T0_AD9P_35	G12	XADC_P5
IO_L5N_T0_AD9N_35	G11	XADC_N5
IO_L6P_T0_35	F13	
IO_L6N_T0_VREF_35	E13	
IO_L7P_T1_AD2P_35	H13	XADC_P3
IO_L7N_T1_AD2N_35	H12	XADC_N3
IO_L8P_T1_AD10P_35	K13	XADC_P6
IO_L8N_T1_AD10N_35	J13	XADC_N6
IO_L9P_T1_DQS_AD3P_35	K15	T_WR_TXFAULT
IO_L9N_T1_DQS_AD3N_35	J15	T_WR_MODDEF0
IO_L10P_T1_AD11P_35	G16	T_WR_LOS
IO_L10N_T1_AD11N_35	G15	T_WR_TXDISABLE
IO_L11P_T1_SRCC_35	G14	T_WR_RATESELECT
IO_L11N_T1_SRCC_35	F14	
IO_L12P_T1_MRCC_35	J14	
IO_L12N_T1_MRCC_35	H14	
IO_L13P_T2_MRCC_35	D15	
IO_L13N_T2_MRCC_35	D14	
IO_L14P_T2_AD4P_SRCC_35	F15	
IO_L14N_T2_AD4N_SRCC_35	E15	
IO_L15P_T2_DQS_AD12P_35	C17	
IO_L15N_T2_DQS_AD12N_35	C16	
IO_L16P_T2_35	E16	
IO_L16N_T2_35	D16	
IO_L17P_T2_AD5P_35	B16	
IO_L17N_T2_AD5N_35	B15	
IO_L18P_T2_AD13P_35	B17	
IO_L18N_T2_AD13N_35	A17	
IO_L19P_T3_35	D13	
IO_L19N_T3_VREF_35	C13	
IO_L20P_T3_AD6P_35	C14	
IO_L20N_T3_AD6N_35	B14	
IO_L21P_T3_DQS_AD14P_35	A15	
IO_L21N_T3_DQS_AD14N_35	A14	
IO_L22P_T3_AD7P_35	C12	
IO_L22N_T3_AD7N_35	B12	
IO_L23P_T3_35	C11	
IO_L23N_T3_35	B11	
IO_L24P_T3_AD15P_35	A13	
IO_L24N_T3_AD15N_35	A12	
IO_25_VRP_35	K12	

XADC_P[6..1] — XADC_P[6..1]

XADC_N[6..1] — XADC_N[6..1]

Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

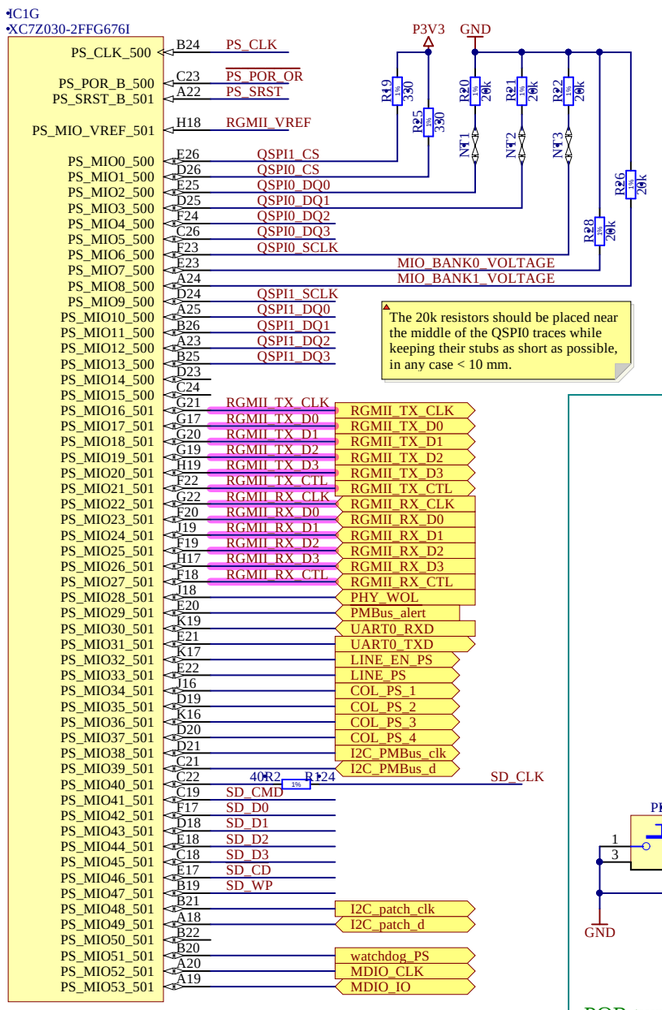
Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Zynq SoC - Bank 35**	Designer	P. Van Trappen
		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_Soc_bank35.SchDoc
		Print Date	03/02/2016 15:22:36 Sheet 5 of 18
TE/ABT	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev 0.4



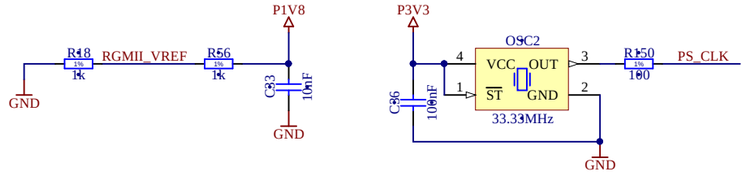
Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

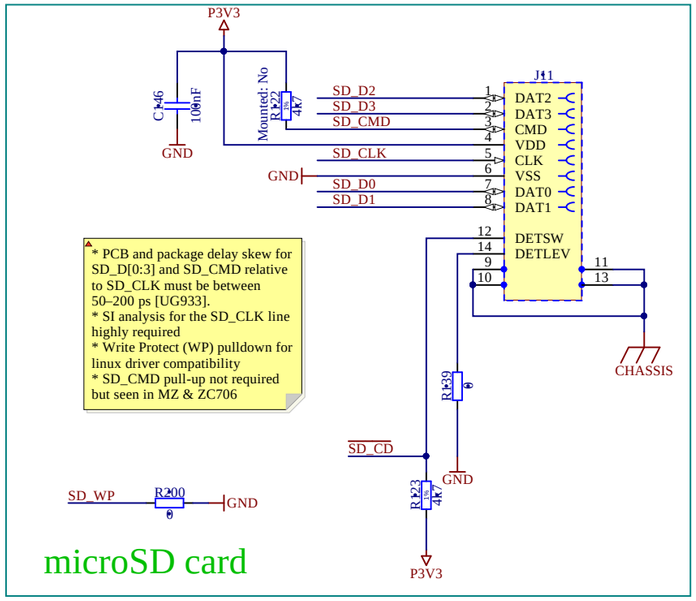
Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier** **Zynq SoC - Bank 12 & 13**	Designer P. Van Trappen	
TE/ABT		Drawn by PVT	14/12/2015
		Check.by *	-
		Last Mod. -	03/02/2016
		File FIDS_carrier_Soc_bank12-13.SchDoc	
		Print Date 03/02/2016 15:22:36	Sheet 6 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4

VCCO_500=3.3V
VCCO_501=3.3V



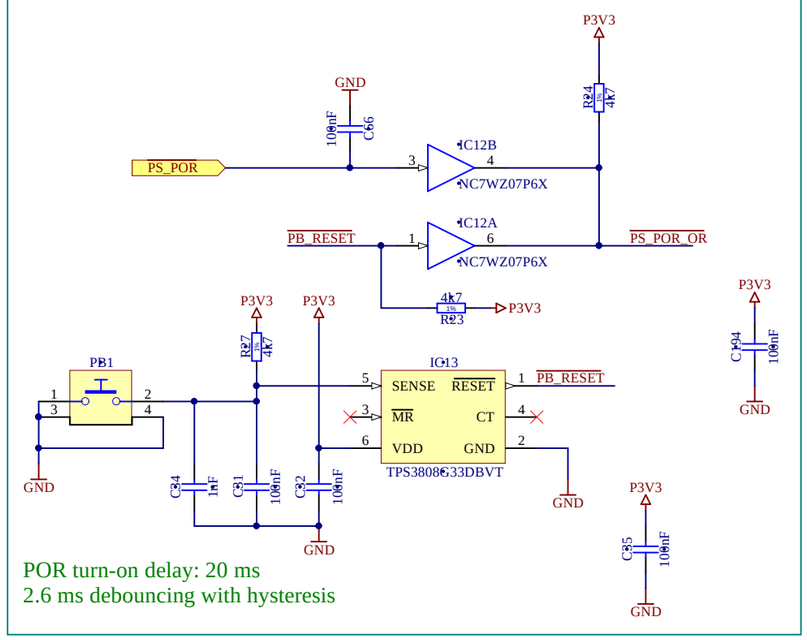
The 20k resistors should be placed near the middle of the QSPI0 traces while keeping their stubs as short as possible, in any case < 10 mm.





* PCB and package delay skew for SD_D[0:3] and SD_CMD relative to SD_CLK must be between 50–200 ps [UG933].
* SI analysis for the SD_CLK line highly required
* Write Protect (WP) pulldown for linux driver compatibility
* SD_CMD pull-up not required but seen in MZ & ZC706

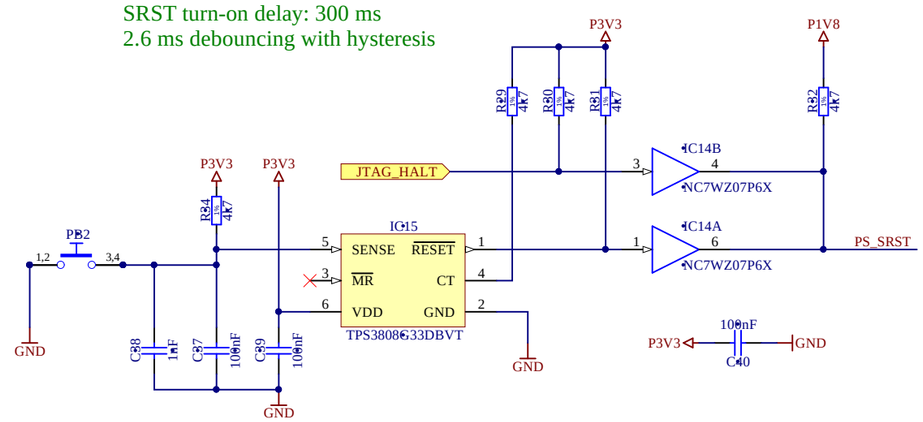
SoC POR (PB and PG VCCO_0)



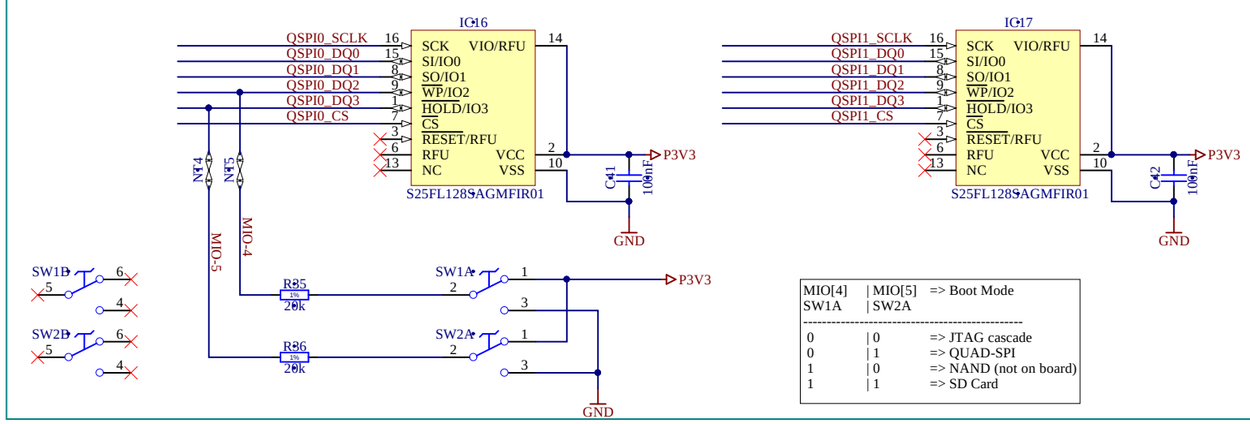
POR turn-on delay: 20 ms
2.6 ms debouncing with hysteresis

SoC SRST (PB and JTAG)

SRST turn-on delay: 300 ms
2.6 ms debouncing with hysteresis



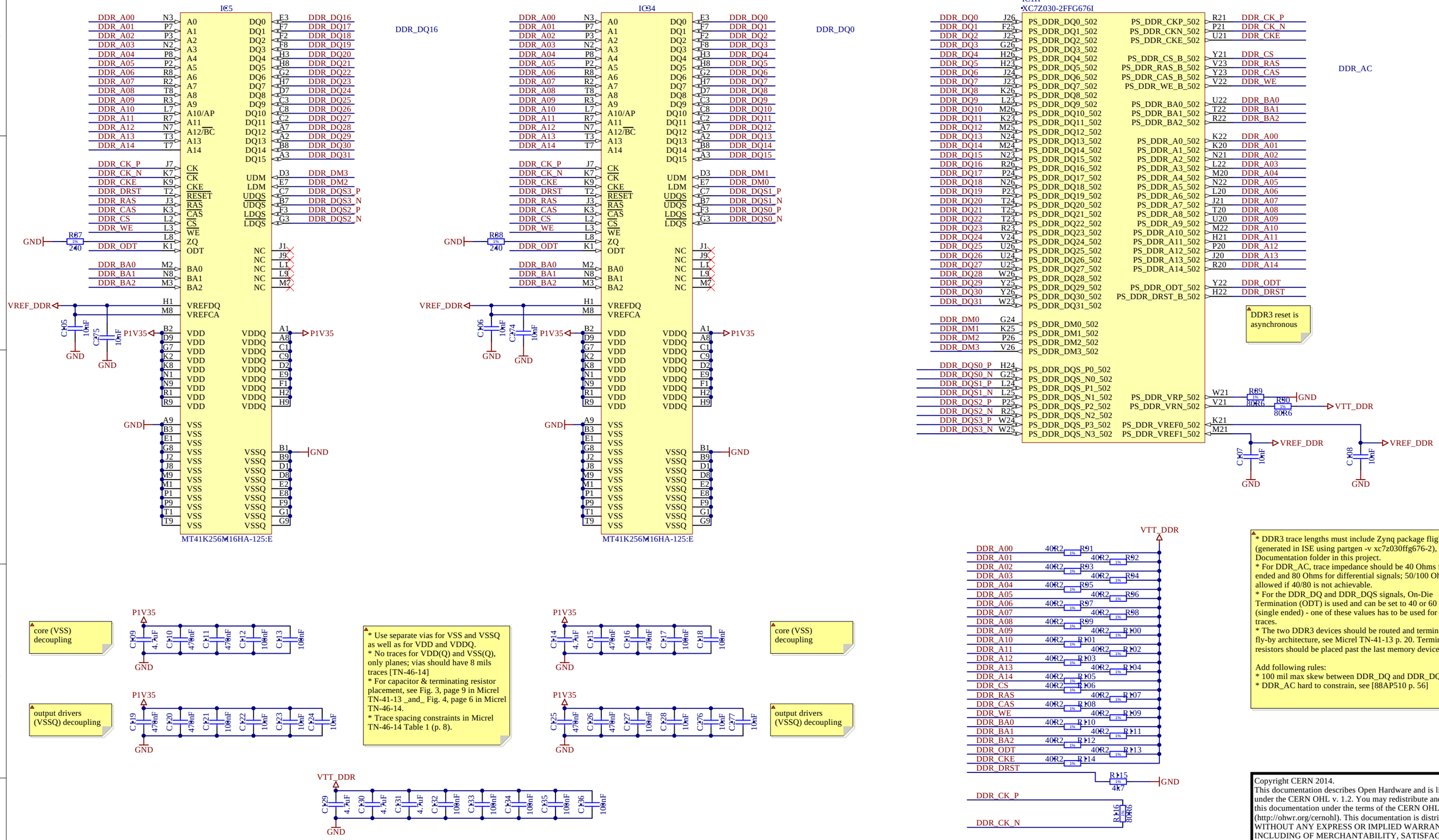
QSPI at 3.3V



MIO[4]	MIO[5]	=> Boot Mode
SW1A	SW2A	
0	0	=> JTAG cascade
0	1	=> QUAD-SPI
1	0	=> NAND (not on board)
1	1	=> SD Card

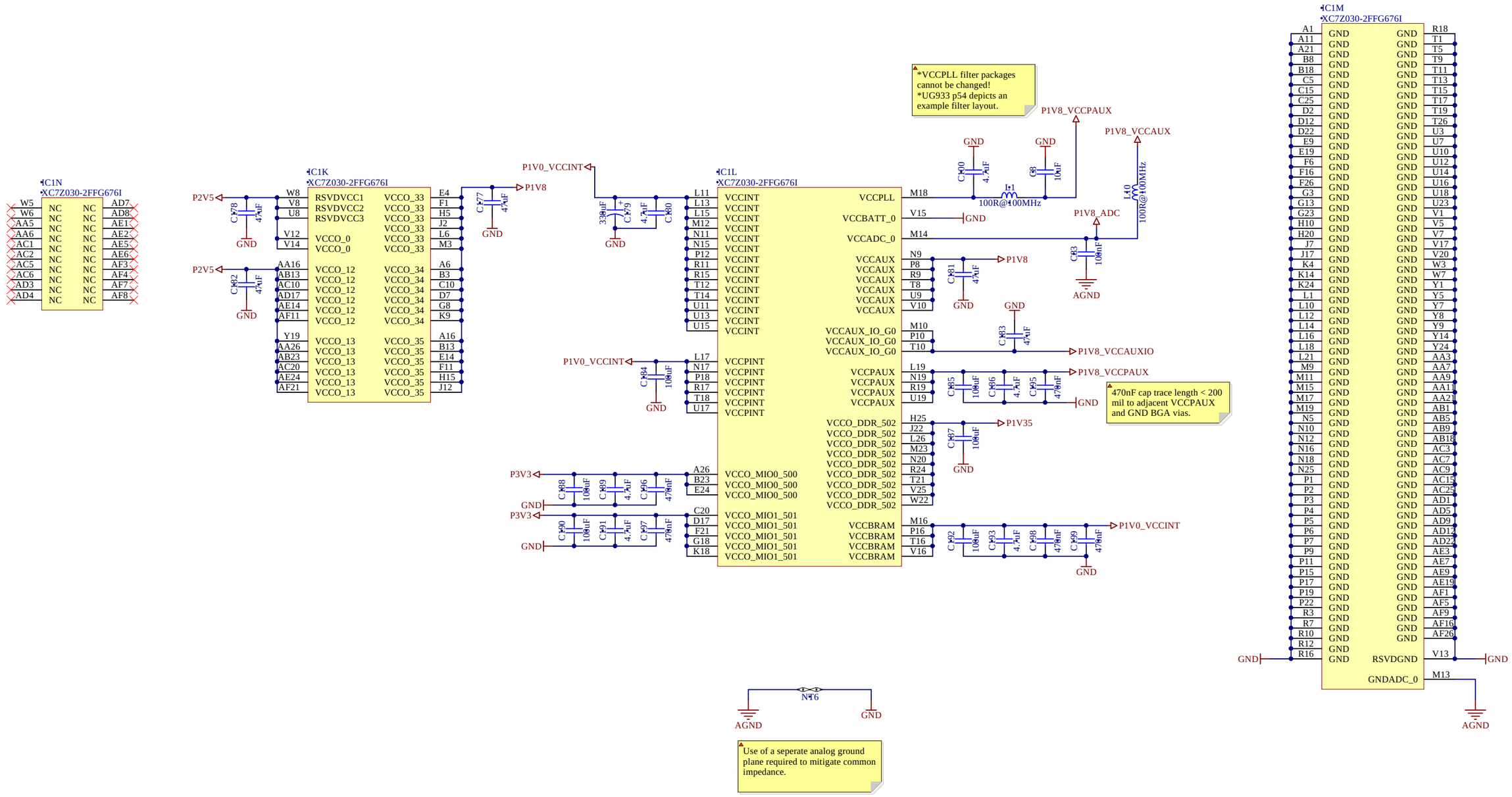
Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Zynq SoC - Bank 500 & 501**	Designer	P. Van Trappen
TE/ABT		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_Soc_bank500-501.SchDoc
		Print Date	03/02/2016 15:22:36 Sheet 7 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	Size A3 Rev 0.4



Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Zynq SoC - Bank 502 (DDR3L)**	Designer	P. Van Trappen
TE/ABT		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_Soc_bank502_DDR.SchDoc
		Print Date	03/02/2016 15:22:37 Sheet 8 of 18
	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev 0.4



Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Zynq SoC - Power**	Designer P. Van Trappen	
TE/ABT		Drawn by PVT	14/12/2015
		Check.by *	-
		Last Mod. -	02/02/2016
		File FIDS_carrier_Soc_power.SchDoc	
		Print Date 03/02/2016 15:22:37	Sheet 9 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4

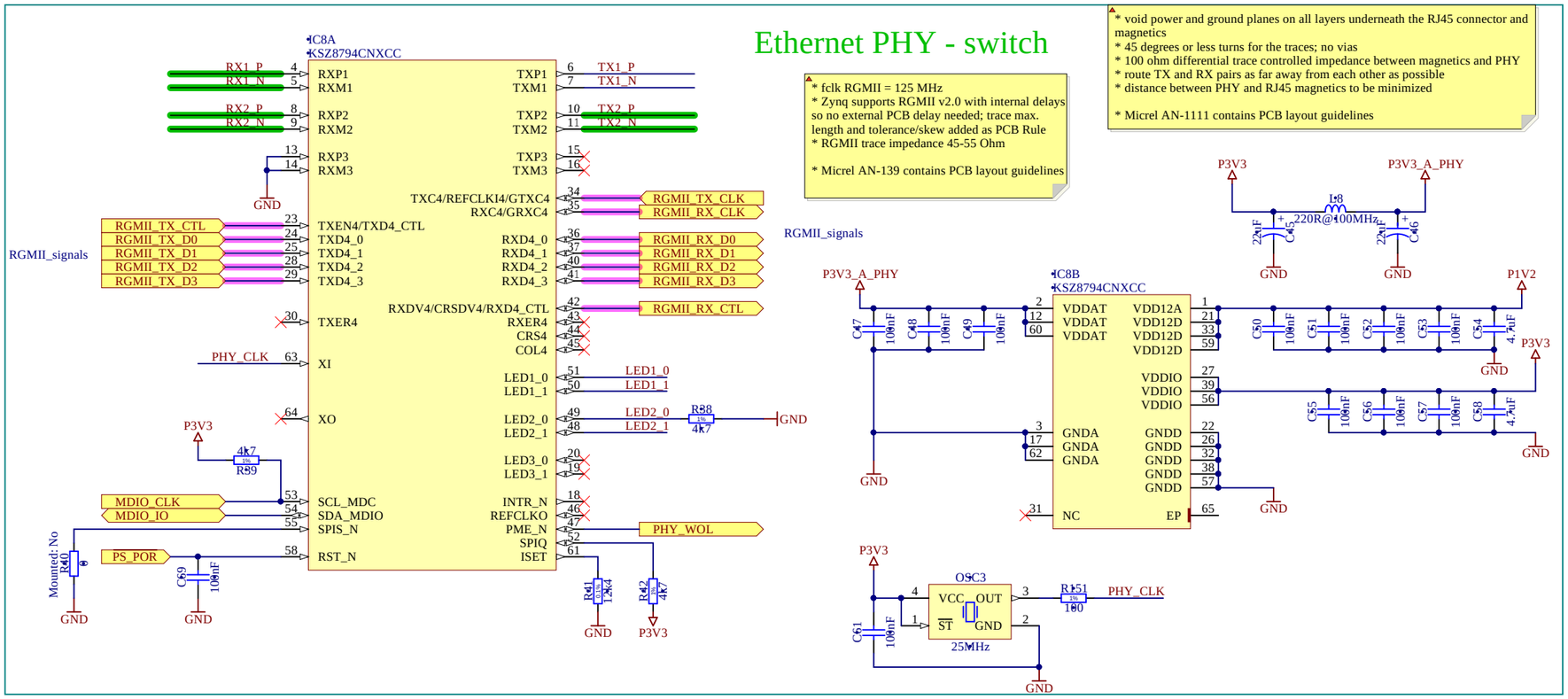
Ethernet PHY - switch

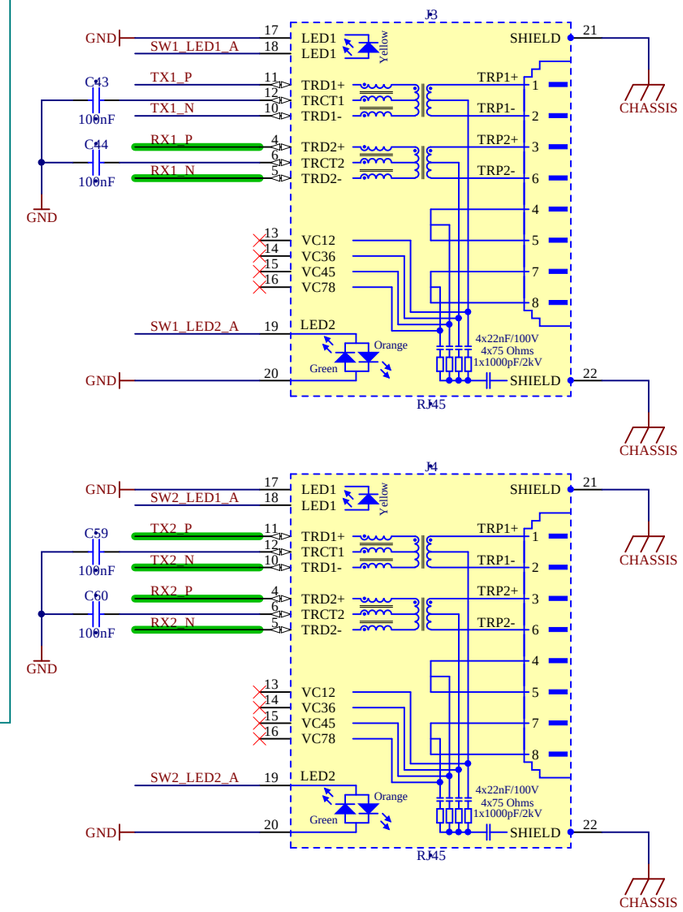
* void power and ground planes on all layers underneath the RJ45 connector and magnetics
* 45 degrees or less turns for the traces; no vias
* 100 ohm differential trace controlled impedance between magnetics and PHY
* route TX and RX pairs as far away from each other as possible
* distance between PHY and RJ45 magnetics to be minimized

* Micrel AN-1111 contains PCB layout guidelines

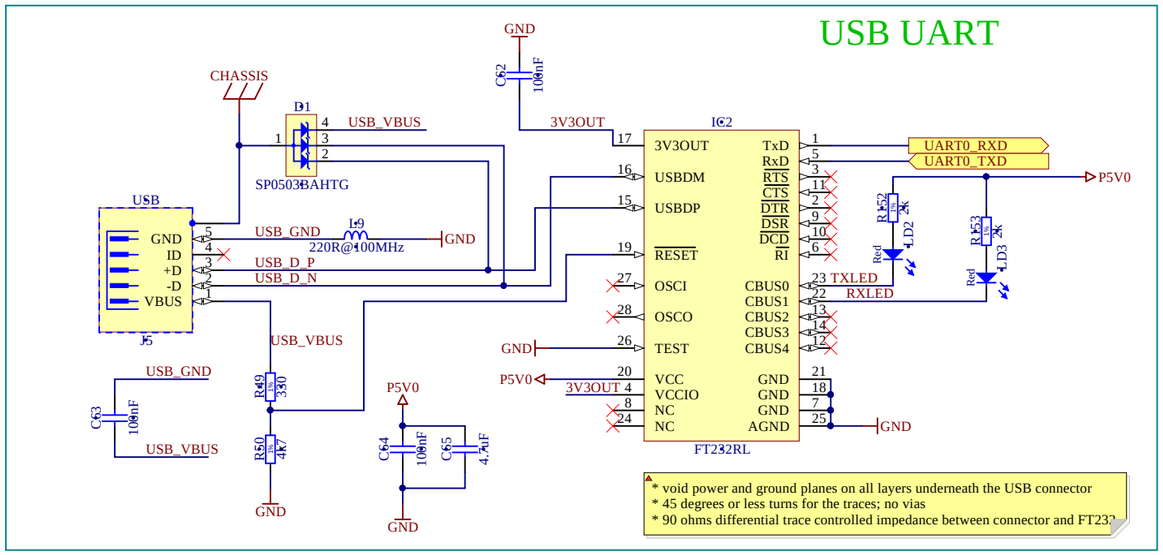
* fclk RGMII = 125 MHz
* Zynq supports RGMII v2.0 with internal delays so no external PCB delay needed; trace max. length and tolerance/skew added as PCB Rule
* RGMII trace impedance 45-55 Ohm

* Micrel AN-139 contains PCB layout guidelines





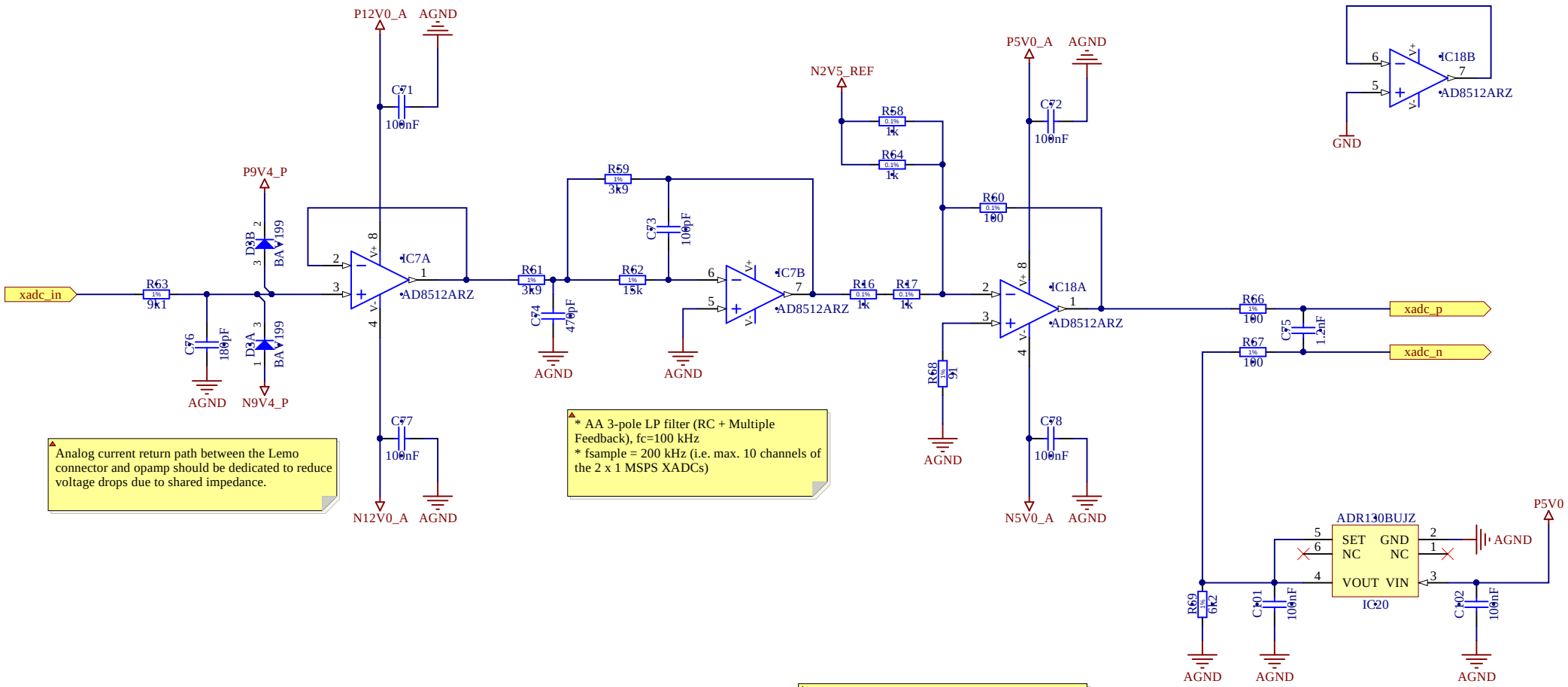
USB UART



* void power and ground planes on all layers underneath the USB connector
* 45 degrees or less turns for the traces; no vias
* 90 ohms differential trace controlled impedance between connector and FT232

Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	FIDS Carrier Ethernet, UART	Designer	P. Van Trappen
		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_Ethernet_UART.SchDoc
TE/ABT	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	Print Date	03/02/2016 15:22:37 Sheet 10 of 18
	EDA-XXXXX-VX-X	Size A3	Rev 0.4



Analog current return path between the Lemo connector and opamp should be dedicated to reduce voltage drops due to shared impedance.

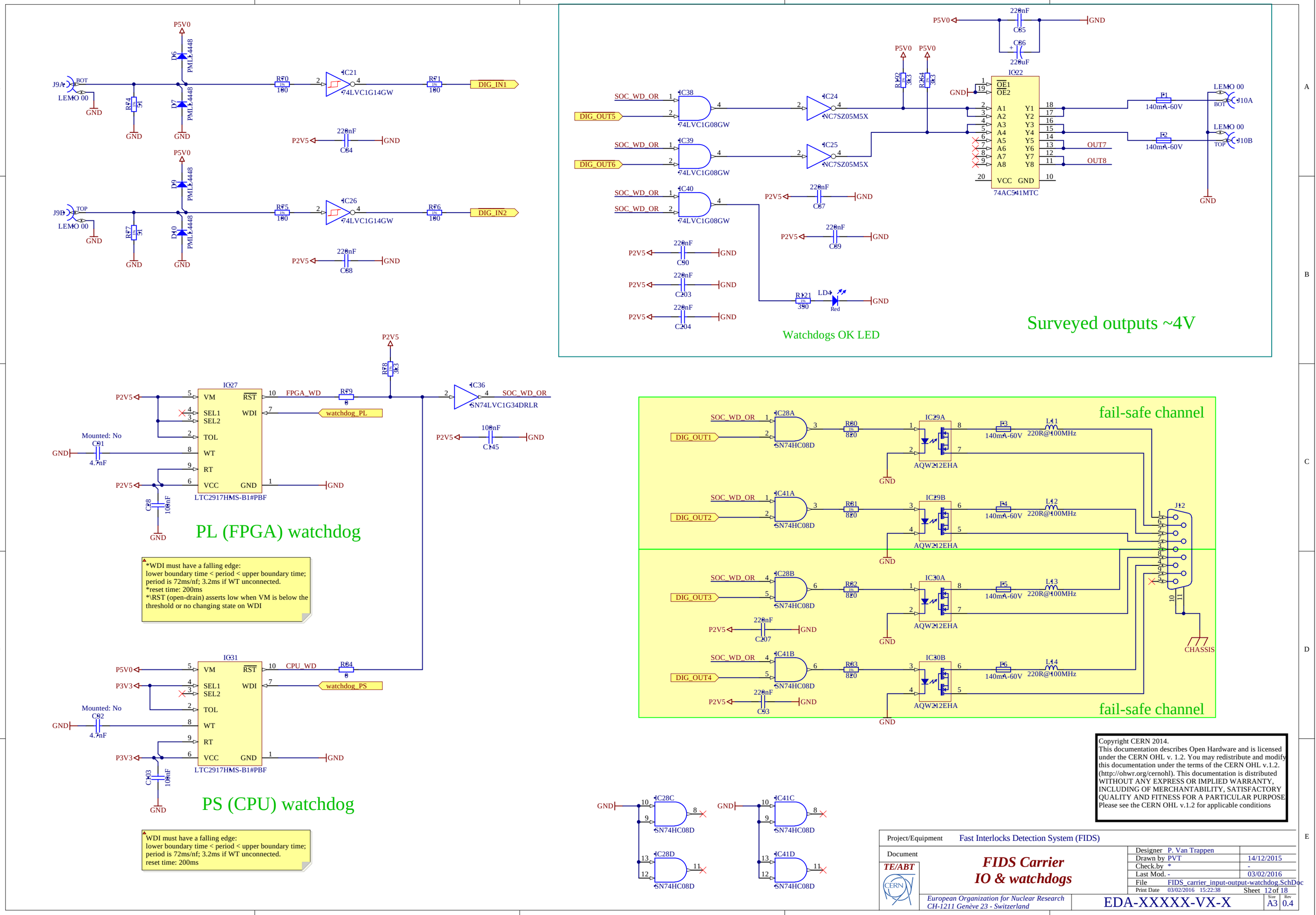
* AA 3-pole LP filter (RC + Multiple Feedback), fc=100 kHz
* fsample = 200 kHz (i.e. max. 10 channels of the 2 x 1 MSPS XADCs)

Summing opamp: 1/20 input plus 0.5V offset addition to treat bipolar input signals.

AAF RC components to be placed as close as possible to SoC package! See xapp554 p. 5

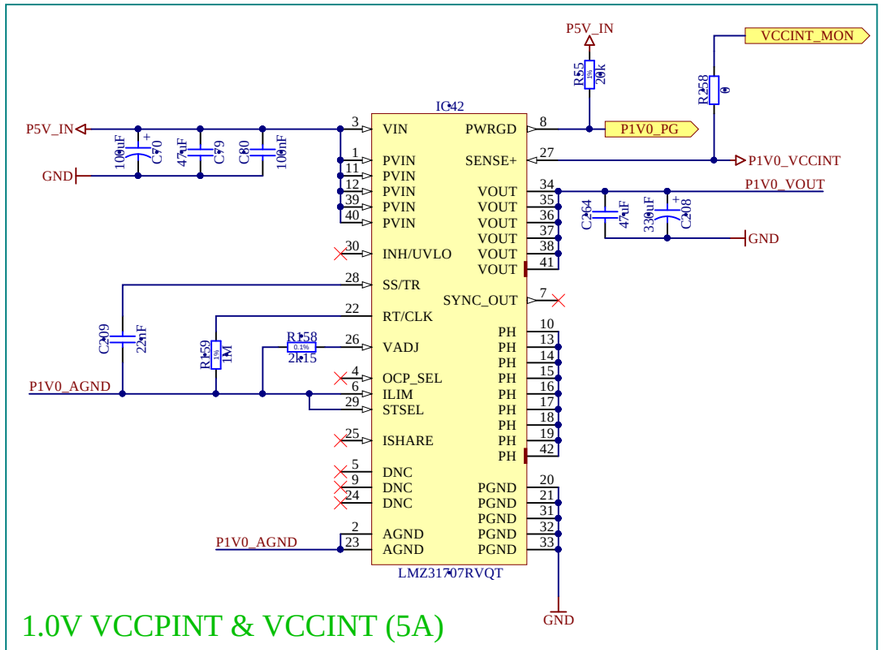
Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Analog input**	Designer	P. Van Trappen
TE/ABT		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_analog-input.SchDoc
		Print Date	03/02/2016 15:22:38 Sheet 11 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A4	Rev 0.4



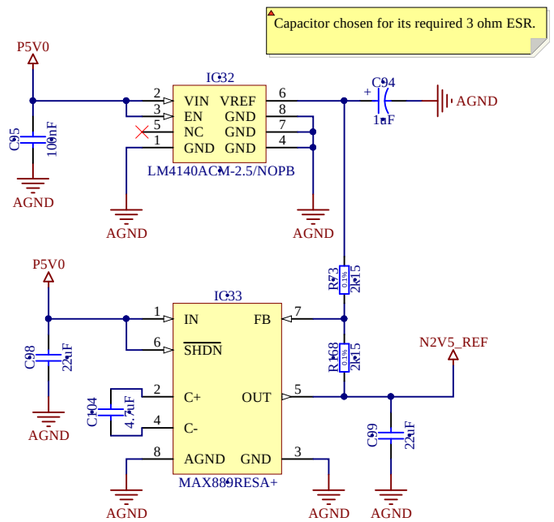
Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier IO & watchdogs**	Designer	P. Van Trappen
TE/ABT		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 03/02/2016
		File	FIDS_carrier_input-output-watchdog.SchDoc
		Print Date	03/02/2016 15:22:38 Sheet 12 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4

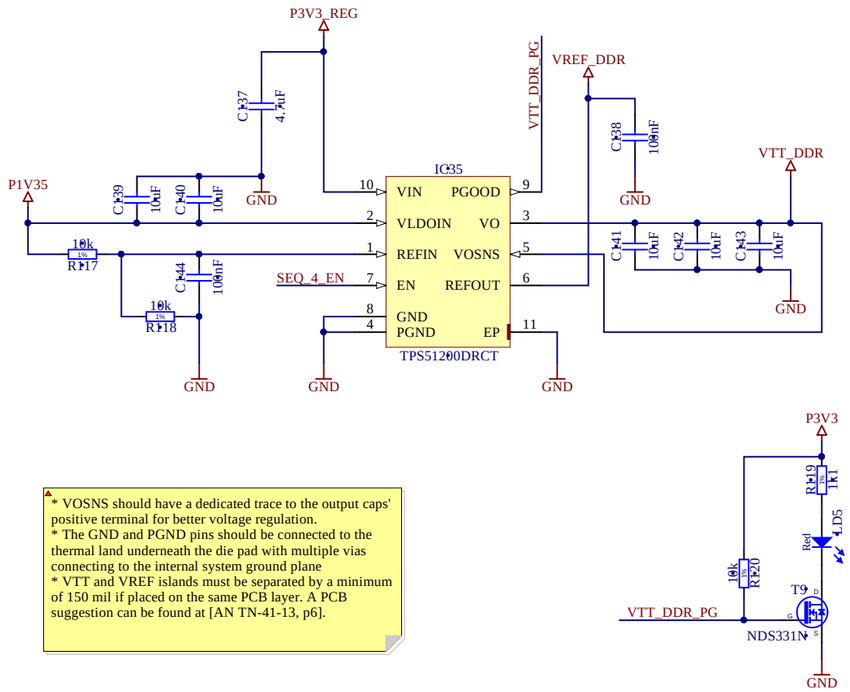


1.0V VCCPINT & VCCINT (5A)

*AGND should have a dedicated plane;
*datasheet p. 25 has an example layout
*PH pins must be connected to one another using a small copper island under the device;
*100nF directly across the PVIN and PGND pins
*Sense+ to be connected close to the load (VCCINT)
*RSET must be between pin 26 and 23 directly
*fsw = 250 kHz

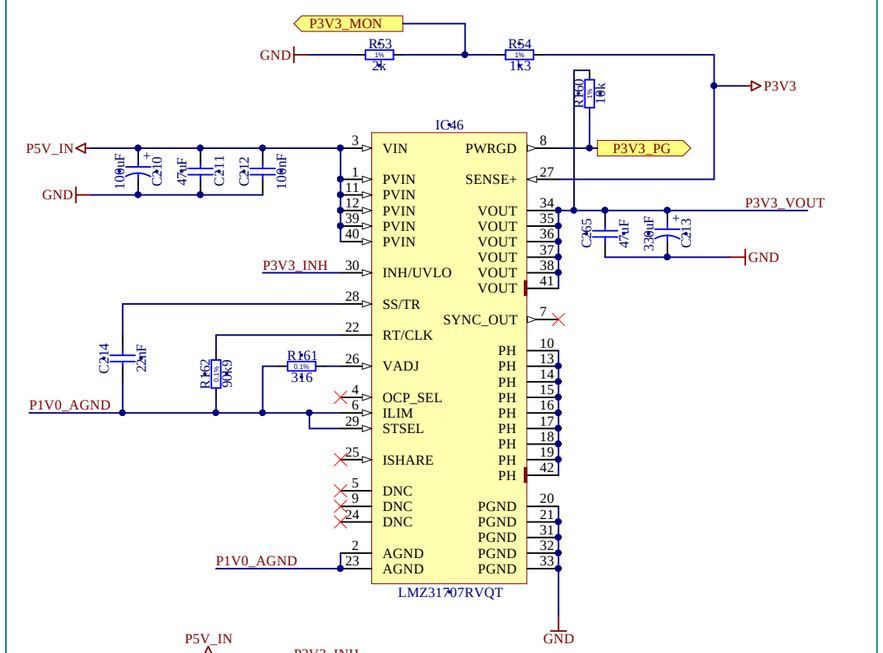


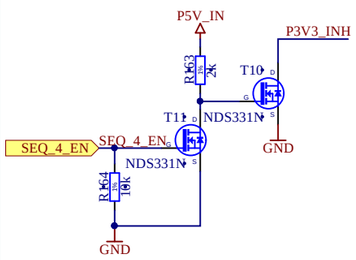
ADC -2.5V reference



* VOSNS should have a dedicated trace to the output caps' positive terminal for better voltage regulation.
* The GND and PGND pins should be connected to the thermal land underneath the die pad with multiple vias connecting to the internal system ground plane
* VTT and VREF islands must be separated by a minimum of 150 mil if placed on the same PCB layer. A PCB suggestion can be found at [AN TN-41-13, p6].

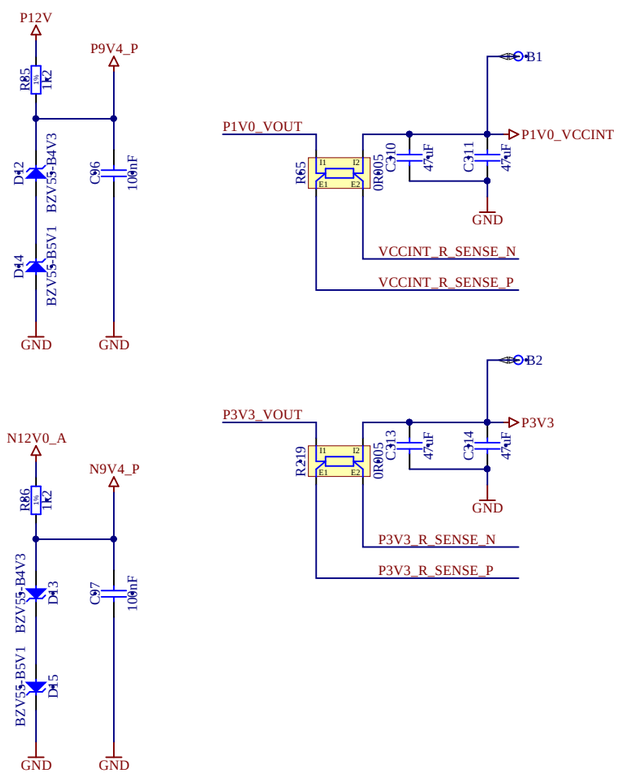
DDR3 - 0V675 VTT and VREF (210mA linear)

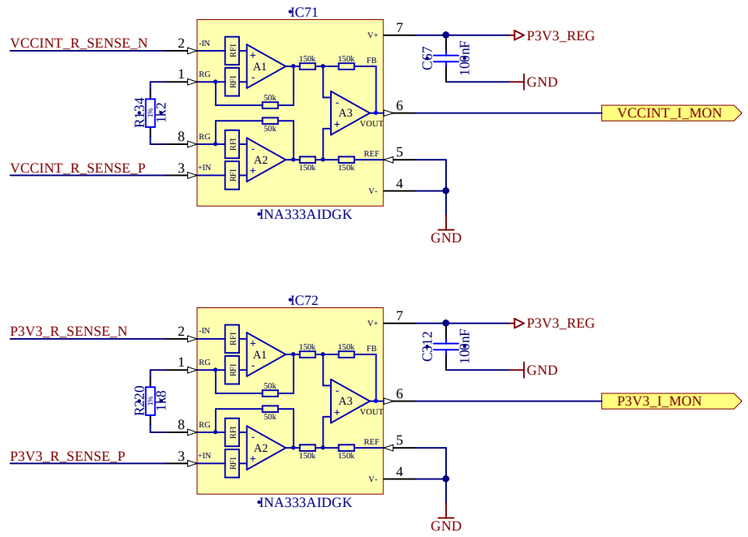




3.3V VCCO & FMCs (7A)

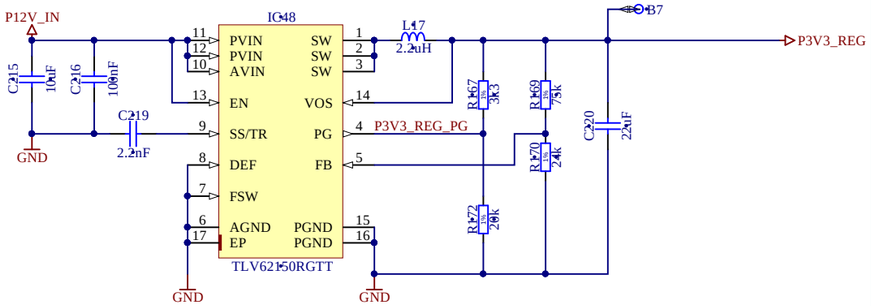
*AGND should have a dedicated plane;
*datasheet p. 25 has an example layout
*PH pins must be connected to one another using a small copper island under the device;
*100nF directly across the PVIN and PGND pins
*Sense+ to be connected close to the load (VCCINT)
*RSET must be between pin 26 and 23 directly
*fsw = 750 kHz





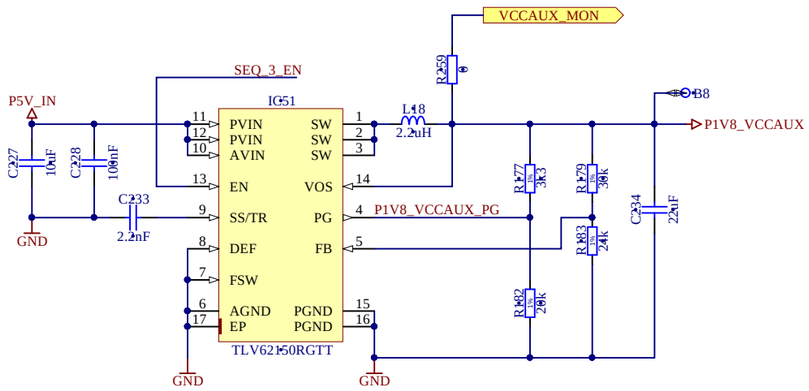
Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Supplies 1**	Designer	P. Van Trappen
		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_power-supplies.SchDoc
		Print Date	03/02/2016 15:22:38 Sheet 13 of 18
TE/ABT	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev 0.4



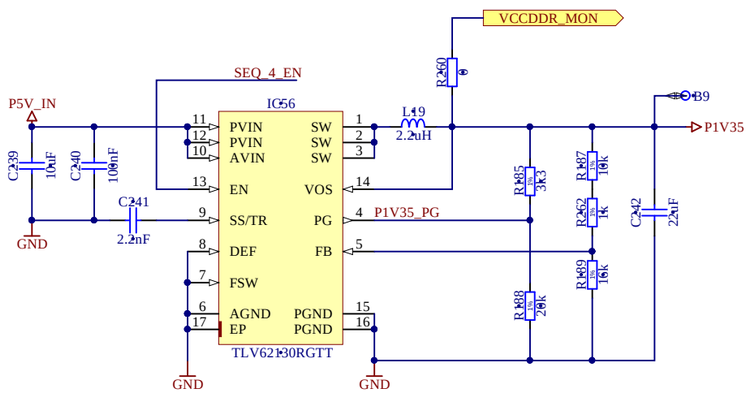
3.3V VREG (1A)

*fsw = 2.5 MHz
*layout example at datasheet p.21
*100nF directly across the AVIN and AGND pins



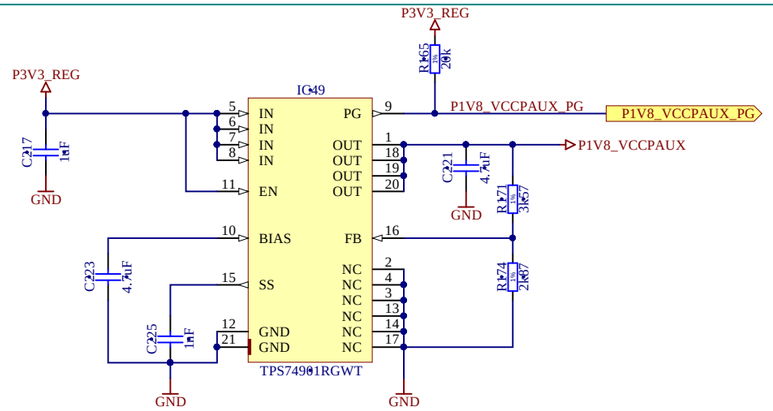
1.8V VCCAUX (800mA)

*fsw = 2.5 MHz
*layout example at datasheet p.21
*100nF directly across the AVIN and AGND pins



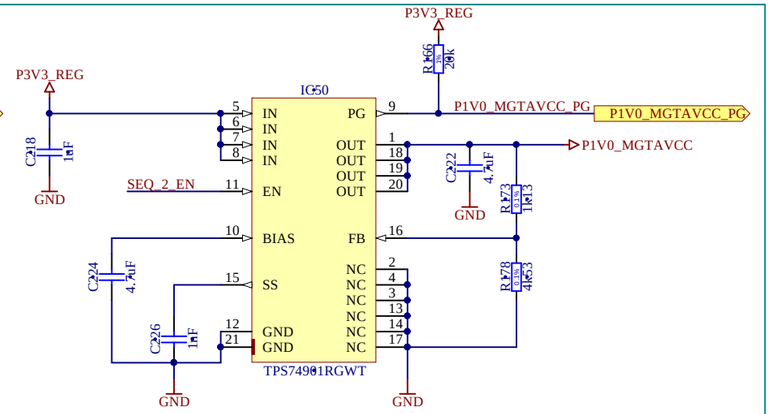
1.35V VCCDDR (1.1A)

*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins



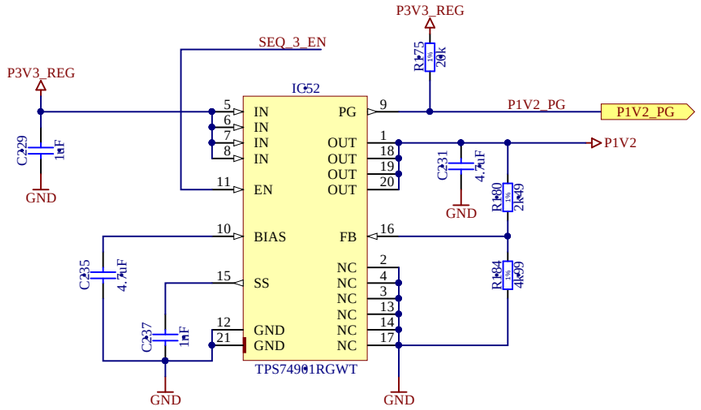
1.8V VCCPAUX (120mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; only 180 mW dissipation with a theta_JA of 120 °C/W.



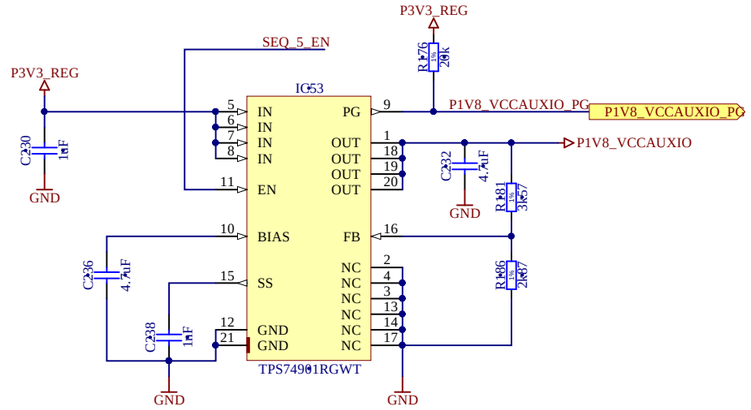
1.0V MGTAVCC (150mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 345 mW dissipation with a theta_JA of 120 °C/W.



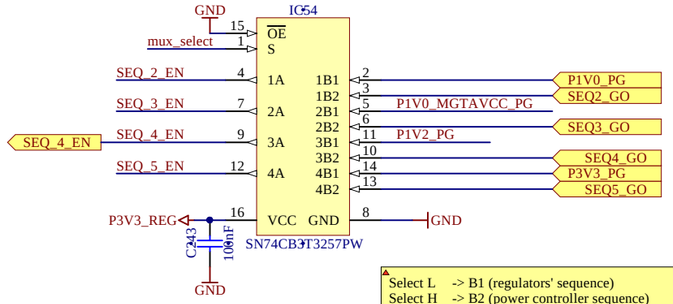
1.2V all (130mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a theta_JA of 120 °C/W.

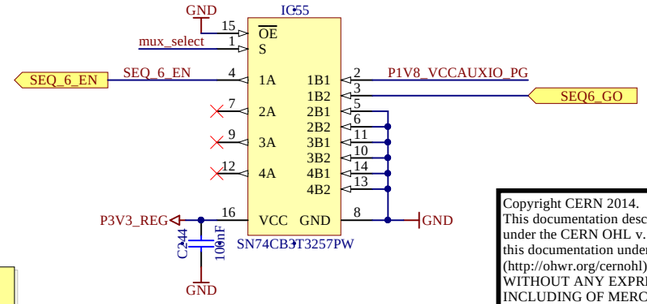


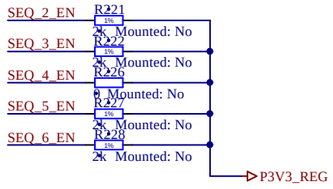
1.8V VCCAUX_IO (130mA linear)

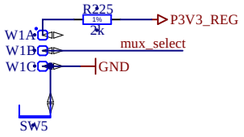
*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a theta_JA of 120 °C/W.



Select L -> B1 (regulators' sequence)
Select H -> B2 (power controller sequence)

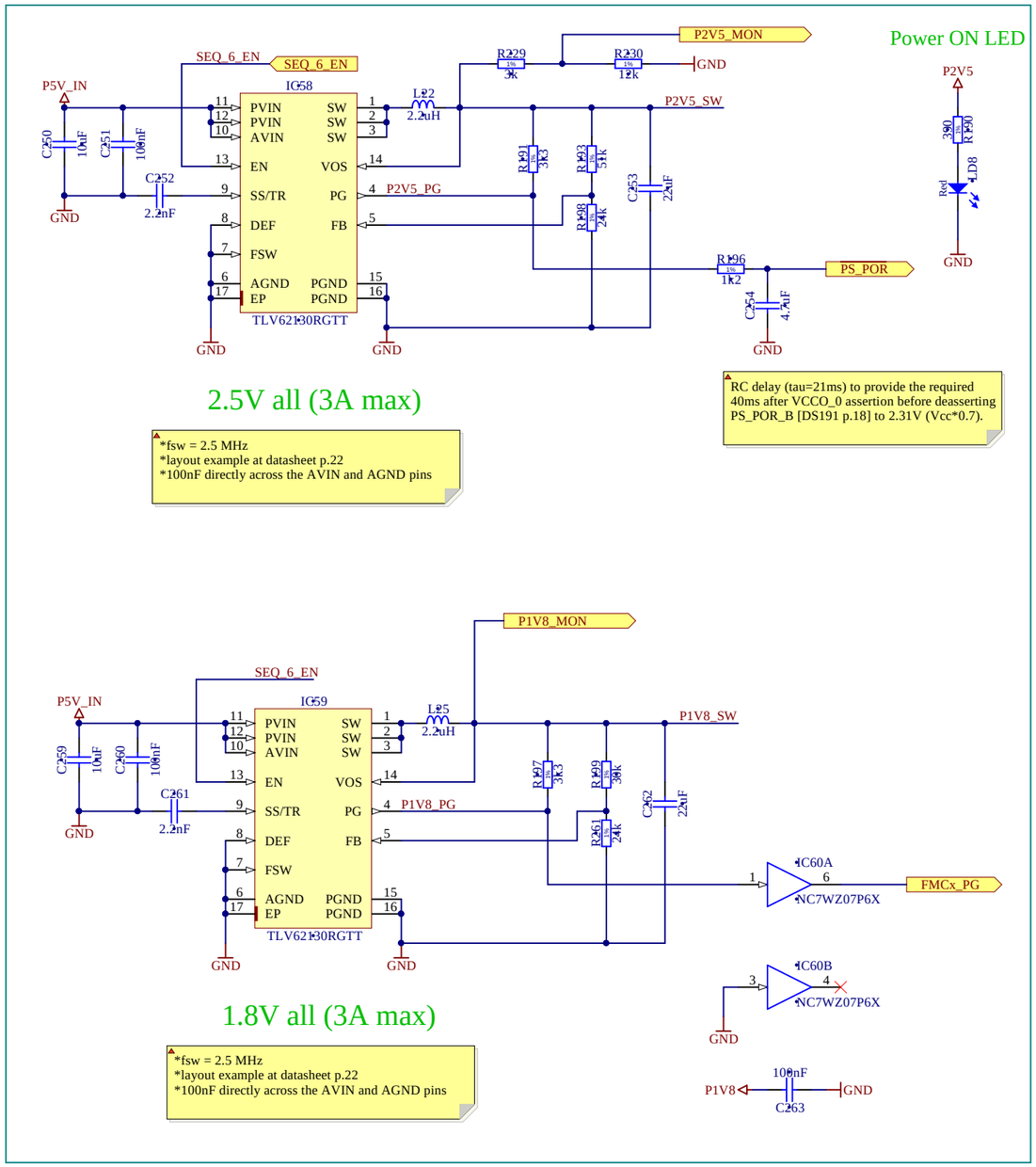


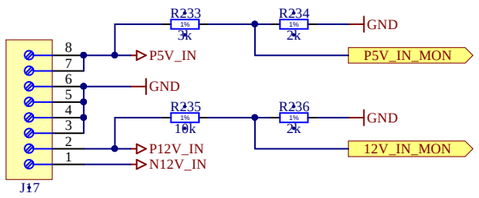




Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

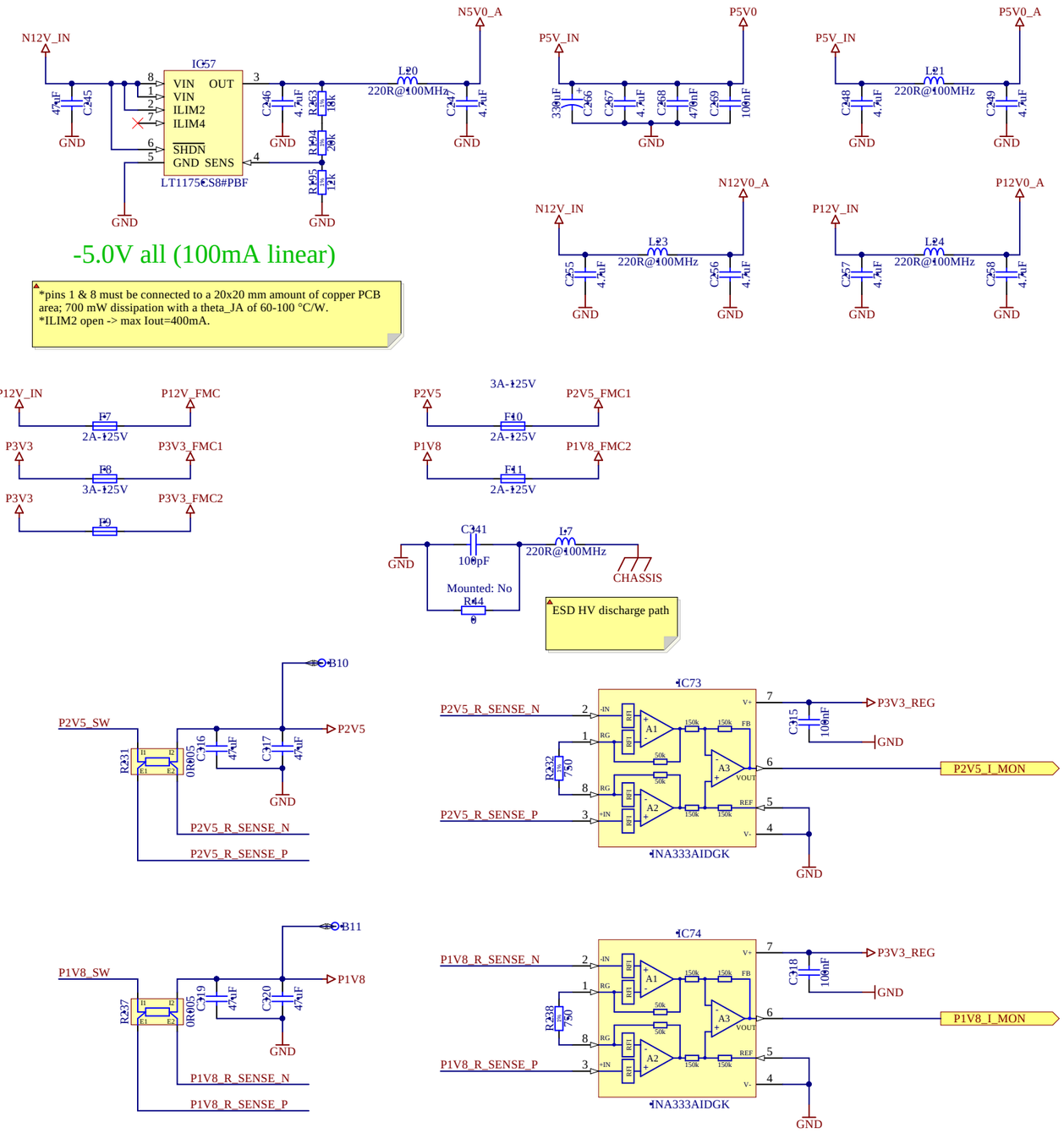
Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Supplies 2**	Designer	P. Van Trappen
TE/ABT		Drawn by	PVT 14/12/2015
		Check.by	- -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_power-supplies-2.SchDoc
		Print Date	03/02/2016 15:22:38 Sheet 14 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4





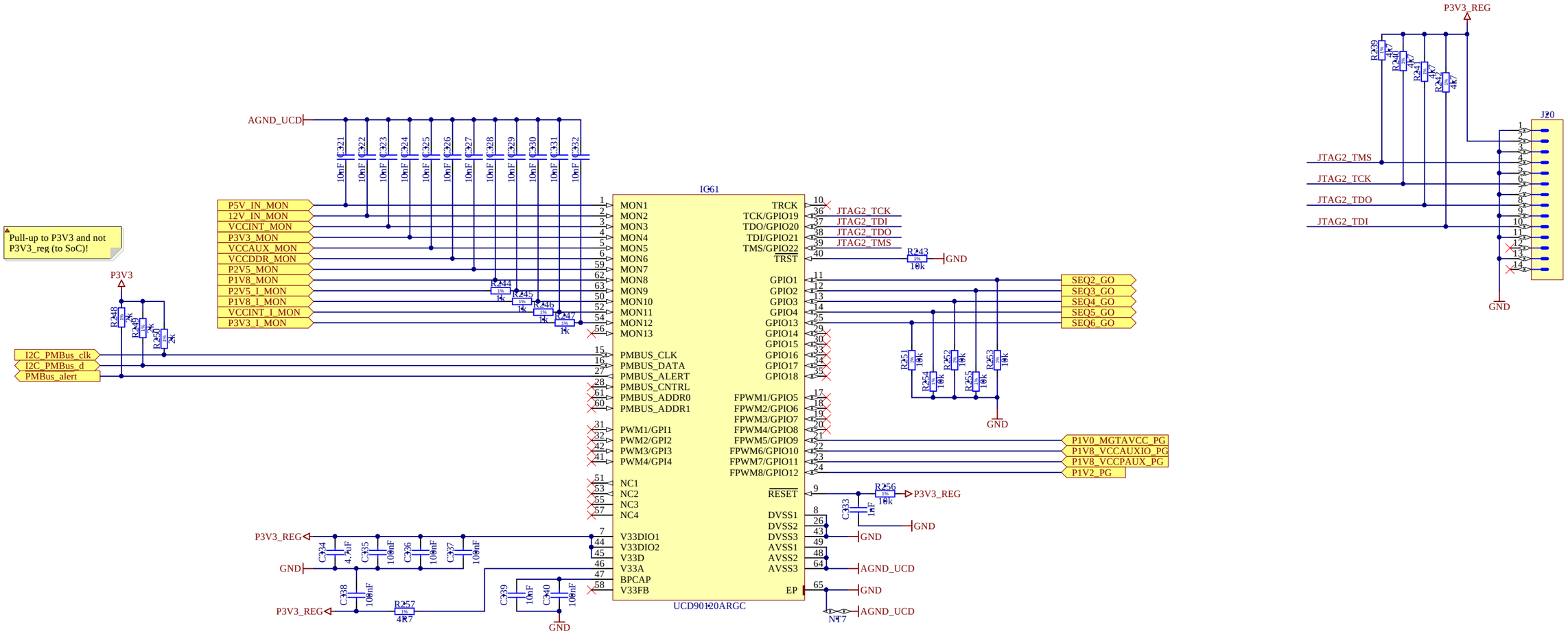
A 80W switching power supply is needed:
* 43W 5V
* 25W 12V
* 2W -12V

Suggestion: Artesyn LPT102-M



Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	FIDS Carrier Supplies 3	Designer	P. Van Trappen
		Drawn by	PVT 14/12/2015
		Check.by	* -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_power-supplies-3.SchDoc
		Print Date	03/02/2016 15:22:38 Sheet 15 of 18
TE/ABT	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev 0.4

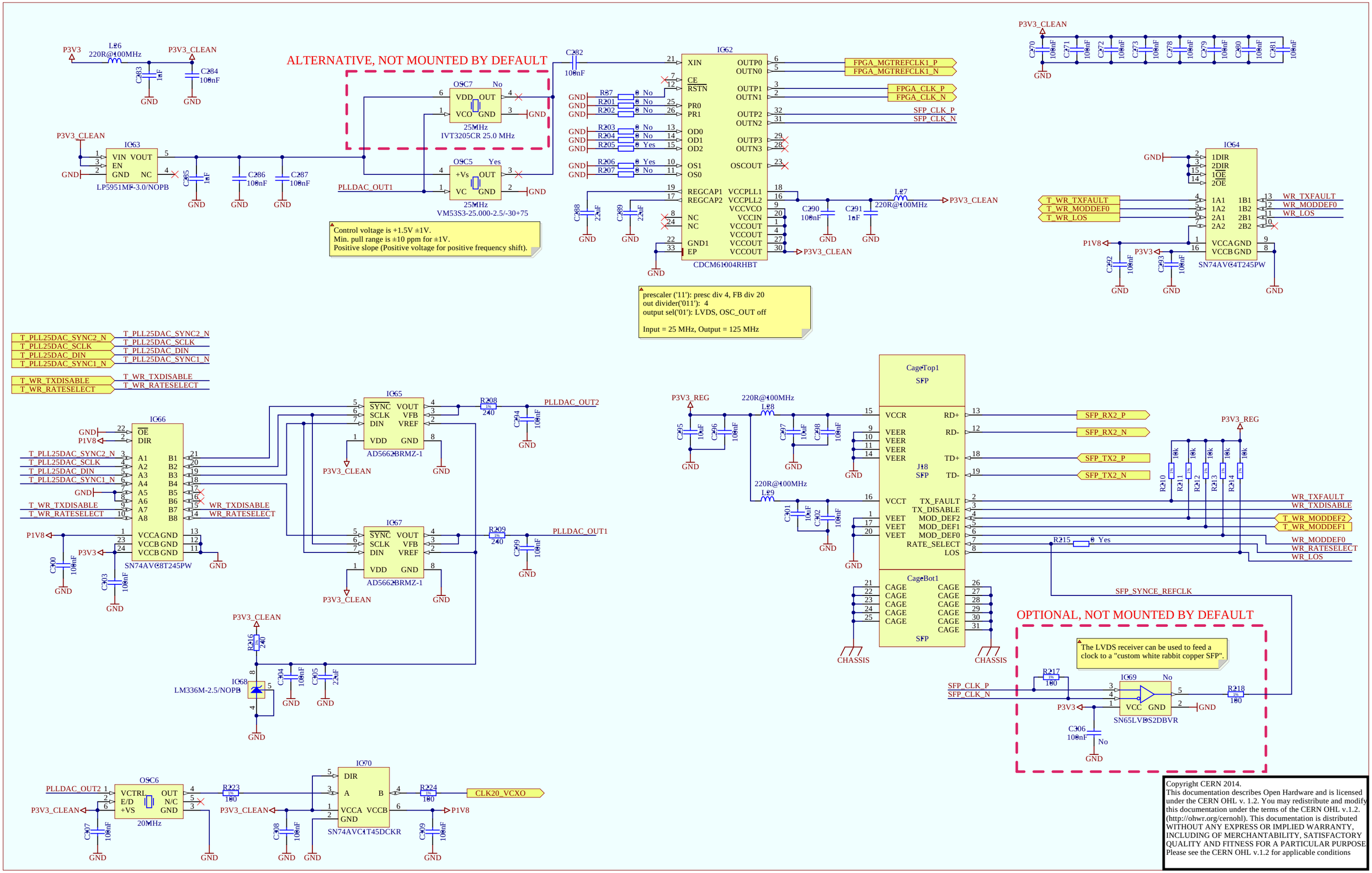


Pull-up to P3V3 and not P3V3_reg (to SoC)!

* layout guidelines and example at p. 48 of the datasheet
* all DVSS and AVSS pins need to be connected to the thermal path
* nRESET must have his components as close as possible to the pin
* PMBus address('OLOL'): default of 126 (0x7E) so that JTAG is enabled

Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

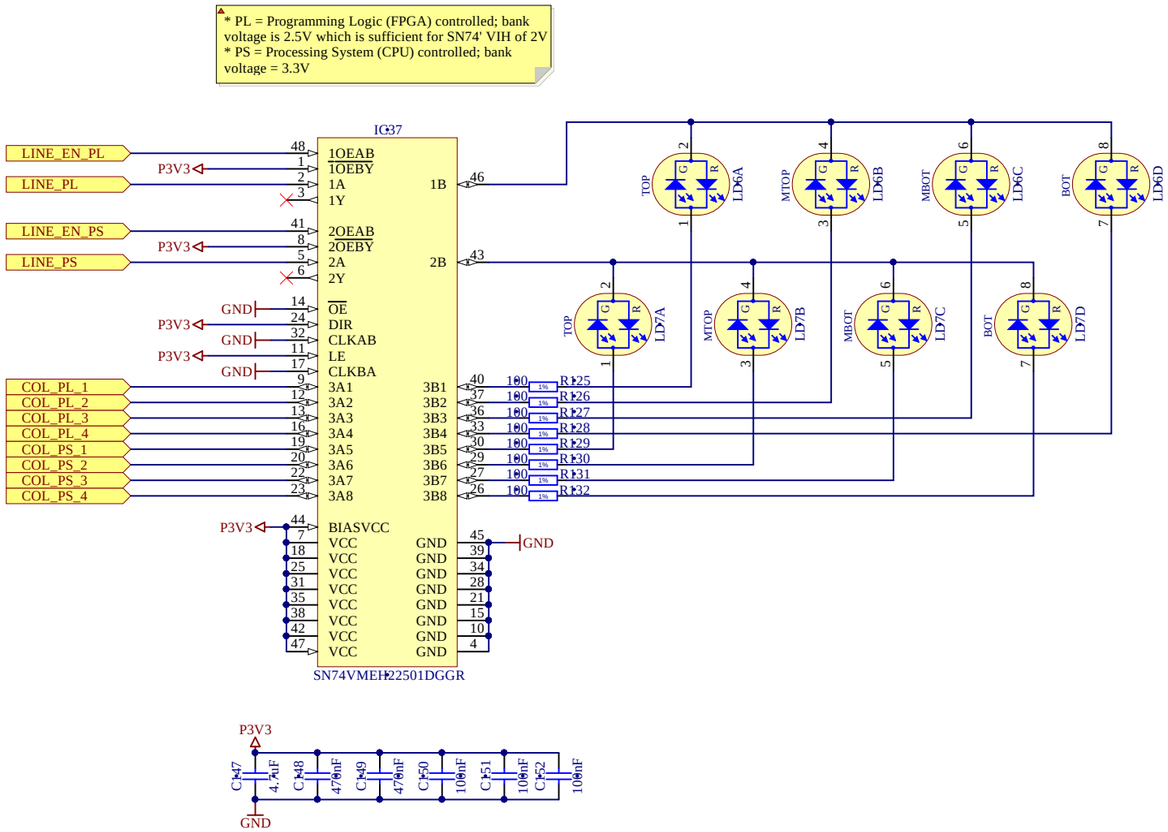
Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Power Controller**	Designer P. Van Trappen	
TE/ABT		Drawn by PVT	14/12/2015
		Check.by *	-
		Last Mod. -	02/02/2016
		File FIDS_carrier_power-controller.SchDoc	
		Print Date 03/02/2016 15:22:39	Sheet 16 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4

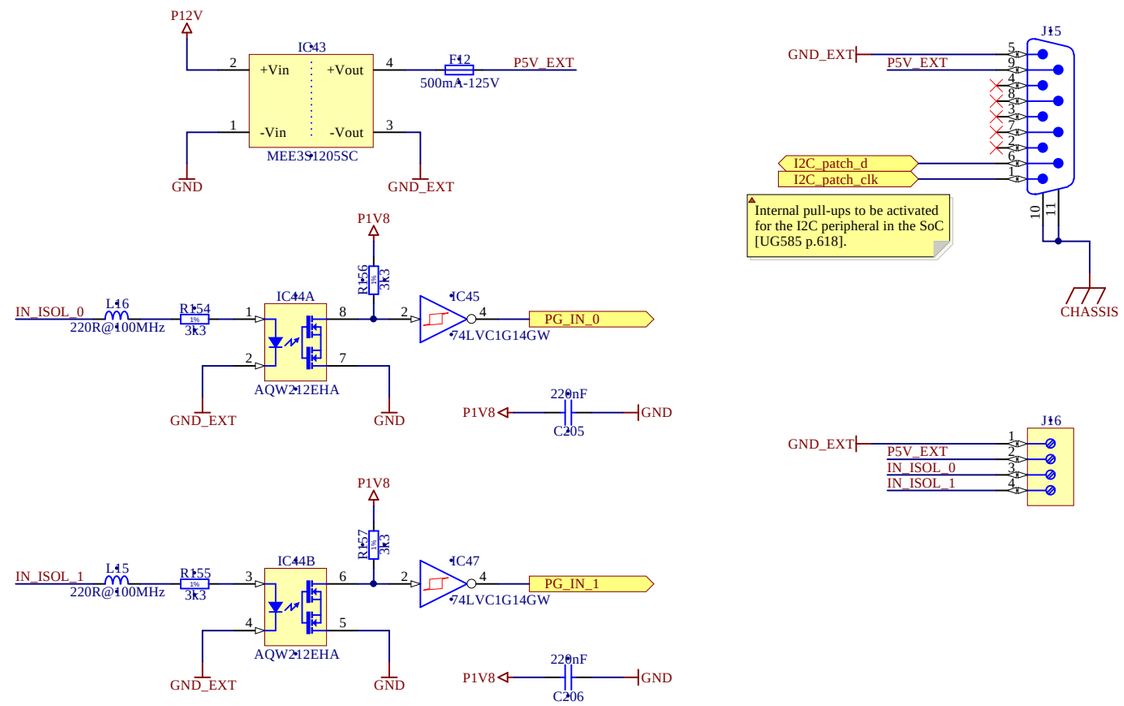


Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

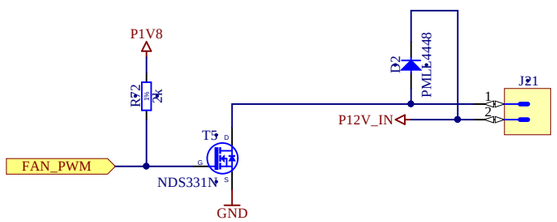
Based on SPEC schematics, EDA-02189-V4-0 p. 2 & 16
Optional, not put by default. Needed for White Rabbit support.

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	**FIDS Carrier Clocks and SFP**	Designer	P. Van Trappen
		Drawn by	PVT 14/12/2015
		Check.by	- -
		Last Mod.	- 02/02/2016
		File	FIDS_carrier_clocks-SFP.SchDoc
		Print Date	03/02/2016 15:22:39 Sheet 17 of 18
TE/ABT	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev 0.4





Isolated external PG contacts and I2C bus



PCB mounting holes, screws & heatsink

changelog

v0.3:
- pages reordered
- IC55 note removed (sheet 14)
- IC22 SN74BCT25244 replaced by 74AC541MTC to have a Voh of 4V (sheet 12)
- CERN OHL v1.2 added (all sheets)

v0.4:
- IC35 (TPS51200) EN connected to SEQ_4_EN (sheet 13)
- IC24 & IC25 now open-drain buffers (NC7SZ05M5X) to ensure Vih and asserted outputs on power loss (sheet 12)
- IC49 & IC53 needed a 3.3V pull-up resistor for the PG signal (sheet 14)
- additional PG singals added to UCD90120 (sheet 16)
- SoC BGA heatsink added (sheet 18)

Copyright CERN 2014.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

Project/Equipment	Fast Interlocks Detection System (FIDS)		
Document	FIDS Carrier Misc	Designer P. Van Trappen	
TE/ABT		Drawn by PVT	14/12/2015
		Check.by *	-
		Last Mod. -	03/02/2016
		File FIDS_carrier_misc.SchDoc	
		Print Date 03/02/2016 15:22:39	Sheet 18 of 18
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 0.4