Modular, low-cost, standards-compliant, reliable, high-performance, open hardware platform for custom electronics & industrial controls
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The DI/OT Team
The DI/OT Platform
Outline

1. The Kit
2. Use Cases
3. Interfaces with CO Services & Projects
4. Status & Plans
Controls Infrastructure

Client Presentation

Server Business

Hardware Front-End

Courtesy of R. Gorbonosov
Controls Infrastructure

Hardware

TCP/IP  VME  Industrial PC  MTCA.4  PLC

CABLE/FIBERS  WorldFIP  CABLE/FIBERS  PROFIBUS/PROFINET

Courtesy of R. Gorbonosov
Controls Infrastructure

- Industrial OR Custom Controls
- Radiation-tolerant OR not
- Technical Network OR Fieldbus
# Hardware Tier Architectures

1. Newly supported tier
   - Extension of CO services
   - For rad-exposed apps

2. DI/OT as a FEC
   - New CO services
   - For low-cost, low-latency apps
Modular DI/OT Platform

System Board
Backplane
PSU
Peripheral Boards
Front Panel
Internal Architecture

Platform:
- VME
- PICMG
- MTCA.4
- DI/OT

Controller:
- MEN A25
- PICMG
- MCH
- System Board

Carrier:
- SVEC
- SPEC
- AFC
- FMC-Carrier

Shared Mezz:
## DI/OT HW Modules

<table>
<thead>
<tr>
<th></th>
<th>Non-Rad-tol</th>
<th>Rad-tol</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Backplane</strong></td>
<td><img src="image1" alt="Backplane Non-Rad-tol" /></td>
<td><img src="image2" alt="Backplane Rad-tol" /></td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td><img src="image3" alt="Power Supply Non-Rad-tol" /></td>
<td><img src="image4" alt="Power Supply Rad-tol" /></td>
</tr>
<tr>
<td><strong>System Board</strong></td>
<td><img src="image5" alt="System Board Non-Rad-tol" /></td>
<td><img src="image6" alt="System Board Rad-tol" /></td>
</tr>
<tr>
<td><strong>Communication</strong></td>
<td>White Rabbit</td>
<td><img src="image7" alt="Communication Rad-tol" /></td>
</tr>
<tr>
<td></td>
<td>PROFINET</td>
<td>WorldFIP</td>
</tr>
<tr>
<td><strong>Peripheral FMC-Carrier</strong></td>
<td><img src="image8" alt="Peripheral FMC-Carrier Non-Rad-tol" /></td>
<td><img src="image9" alt="Peripheral FMC-Carrier Rad-tol" /></td>
</tr>
<tr>
<td></td>
<td><img src="image10" alt="Peripheral FMC-Carrier Rad-tol" /></td>
<td><img src="image9" alt="Peripheral FMC-Carrier Rad-tol" /></td>
</tr>
</tbody>
</table>
Backplane

- CPCI-S industrial standard
- 9 slots, fully passive
- Star of lanes from System to Peripherals
- RTM
PSU

- Off-the-shelf

Switched-mode AC/DC 100W
- Compact & Efficient
- Monitoring & Diagnostics
  - Power rails
  - Temperature sensors

Work of L. Patnaik & TE-EPC
System Board

**Communication:**
- GbE – TN/WhiteRabbit Fieldbus FMC

**Processing:**
- Zynq Ultrascale+ SoC
  - ARM Cortex A53 – Linux
  - ARM Coretex R5 – Bare metal/RTOS
  - FPGA

- Rad-tol Fieldbus FMC
- Rad-tol Smartfusion2
  - FPGA
  - Hydra SoC Architecture

Work of C. Gentsos
Rad-tol System Board
Hydra SoC Architecture

- Triplicated RISC-V
  - 50MHz
  - Watchdog
- ECC RAM in the FPGA
  - 96 kB code
  - 64 kB data
- Interfaces
  - SPI
  - UART
  - Ethernet MAC with DMA

M. Rizzi
Proof of Concept – WIC

- FEC
- SPEC+WorldFIP Master
- WorldFIP Fieldbus
- GbE TN
- TCP/IP
- System Board+WorldFIP Slave
- Peripheral IO
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#1: DI/OT controlled by Front-End
LHC Powering Interlock Controller (TE-MPE)

BE-CO Front-end
- MasterFIP

SCADA – WinCC OA

System Board running customized gateware

Beam Interlock System
- QPS
- Power Converters
- UPS Fault
- Emergency Stop Button

PIC Beam Dump Function

Courtesy of Alain Antoine (TE-MPE-MI)
LHC Powering Interlock Controller (TE-MPE)

System Board running customized gateware

Beam Interlock System
QPS
Power Converters
UPS Fault
Emergency Stop Button

Technical Network
WorldFIP

Translator WorldFIP / Profinet

SCADA – WinCC OA

Courtesy of Alain Antoine (TE-MPE-MI)
• Coupling-Loss Induced Quench
• Innovative quench protection method for HL-LHC inner triplet magnets
• DI/OT crates controlling CLIQ racks
• WorldFIP communication
• CLIQ-specific Peripheral Board and Rear Transition Modules
Full Remote Alignment System (EN-SMM)

Micrometric remote alignment of LSS* in IP1 and IP5 for HL-LHC

Survey:

- Readout of precise positioning sensors
- 4x more systems than currently
- DI/OT crates in radiation communicating over WorldFIP

*LSS = Long Straight Section

Courtesy of K.Kucel, M.Sosin (EN-SMM-HPA)
Full Remote Alignment System (EN-SMM)

Micrometric remote alignment of magnets in IP1 and IP5 for HL-LHC

Sambuca:

- DI/OT as part of generic motor control framework
- DI/OT crates controlled from PXIe
- DI/OT crates synchronized with White Rabbit

Courtesy of A. Masi, P. Peronnard (EN-SMM)
#2: DI/OT as Front-End

Hardware

System Board with SoC

FESA

radiation-free
Fast Interlocks proof of concept

- When ~1us reaction times are required
- When PLCs are not fast enough
DI/OT fast interlocks: application

- As simple as possible
- Timing is fully predictable

```c
#include <stdint.h>
#include "plc_urv_regs.h"

#define SLOT pins_5

//
#define OEN ((1 << 6) | (1 << 7) | (1 << 8) | (1 << 9) | (0 << 11))

void init (void)
{
    volatile struct plc_urv_regs *regs =
        (volatile struct plc_urv_regs *)0x00000;
    regs->relays.SLOT = OEN;
}

void main (void)
{
    volatile struct plc_urv_regs *regs =
        (volatile struct plc_urv_regs *)0x00000;
    while (1) {
        unsigned v = regs->loops.SLOT;
        v = !!(v & 0x27);
        regs->relays.SLOT = (v << 4) | OEN;
    }
}
```
# build fip_urv tool
$ make

# build Fast Interlocks application
$ make PROG=plc_dio

# load Fast Interlocks binary over WorldFIP
$ fip_urv load plc_dio.elf

# start CPU
$ fip_urv plc on
DI/OT as successor of FASEC (TE-ABT)

- Generic pizza-box hardware platform
- ... for fast interlock protection system
- Customized by 2 FMC slots
- Based on SoC (Zynq-7)
- Running embedded Linux and connected to TN

Courtesy of Pieter Van Trappen (TE-ABT)
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FEC Linux Standardisation

- Embedded Linux for DI/OT SoC

SoC project (under discussion)

- DI/OT as SoC test platform
- Software build environment
- CO software services for SoC

CCS

- Auto discovery of crate config
- ... and crate instances

DI/OT & CO Services

COSMOS

- Monitoring and diagnostics
- Collected by System Board
- Exposed over fieldbus / TN

Hardware Installation Team

- Crate and diagnostics specification
- Stock management
- Documentation and training
- Support deployments in equipment groups
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Timeline

- **Q4 2018**: First proof of concept available for lab developments
- **Q2 2020**: Crate and backplane designed
- **Q4 2020**: Non-rad-tol System Board ready
- **Q1 2021**: Powerlink FMC prototype, Profinet FMC prototype
- **Q1 2021**: Rad-tol System Board prototype
- **Q1 2021**: Non-rad-tol FMC carrier prototype
- **Q3 2021**: RaToPUS ready
- **2022**: Series production/procurement starts
- **2025**: HL-LHC deployments
• Modular platform for custom electronics
• Radiation-exposed and radiation-free areas
• Customised by Peripheral Boards and FPGA firmware
• Interfacing with custom electronics and industrial controls
• Controlled from Front-End or becoming Front-End

• Collaboration between CERN groups, industry and Quantum Computing community

https://ohwr.org/project/diot/wikis