As per CERN-OHL-W v2 section 4, should You produce hardware based on the Specifications in this software, You shall:

- **Satisfactory Quality and Fitness for a Particular Purpose**: The hardware produced shall be of satisfactory quality and fit for the particular purpose intended by CERN.

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According to the specification, all 8-bits of DQ, such as DM, DQS, DQS_N, and DQ signals, are aligned for proper signaling and timing.

Reference: EEA-PS

Class Name: DDR4-PS_BYTE1

Parameter: ClassName: DDR4-PS_BYTE7
As per CERN-OHL-W v2 section 4, should You produce hardware based on this document, You must maintain the Source Location visible on the hardware address plane must be enabled in ROCCON register two. 

Source location: https://www.ohwr.org/project/diot-sb-zu


Crate power cycle timer

This circuit does not support LVDS_25 output nor internal termination (DS25 v1.15 p21). It supports LVDS input without constraints about power supply rails.
To maintain the source location visible on the document, you must maintain the source location visible on the document.
Use DQS_BIAS = TRUE option for the AC-biased clock input IO

The assignment identical to an ACB with an exception of PAR and RST_N signals:
PAR is tied to ground, RST_N is connected instead to the FPGA.

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Source location: https://www.ohwr.org/project/diot-sb-zu

DI/OT System Board

FPGA Bank 63

Project/Equipment: DI/OT System Board

EDA-xxxx

24/02/2022 13:48:30

F. P. Kulik, G. Daniluk

Check.by

G. Kasprowicz

Drawn by

witakowski

Last Mod.

24/02/2022
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For more information and modifications, refer to the source location: https://www.ohwr.org/project/diot-sb-zu

Clock Capable

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Recommended capacitors given in UG583 p26 and checklist xtp427

Also, limit the DC resistance of each trace to less than 0.5 Ω.

Connect to MGTAVTT and to a 100 μF DC blocking capacitor between the power source and MGTAVTT.

Limit the DC resistance of each trace to less than 0.5 Ω.

Recommended capacitors given in UG583 p26 and checklist xtp427.
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Connector has MGT routed as in HPC:

- FMC_MGT.DP_M2C_N[7..0]
- FMC_MGT.GBTCLK_M2C_P[1..0]
Rx/Tx lines are swapped on the backplane

ETH_A - ETH_B; ETH_C - ETH_D lines are swapped on the backplane

P4 connector

P5 connector

P6 connector
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CH-1211 Geneve 23 – Switzerland

Then MGT_0V9, MGT_1V8, MGT_1V2

C431 is recommended to be NP0. But 220nF, 25V X7R is good enough.

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Note: 2V5 rail supplies only DDR Vpp so 300mA is enough.