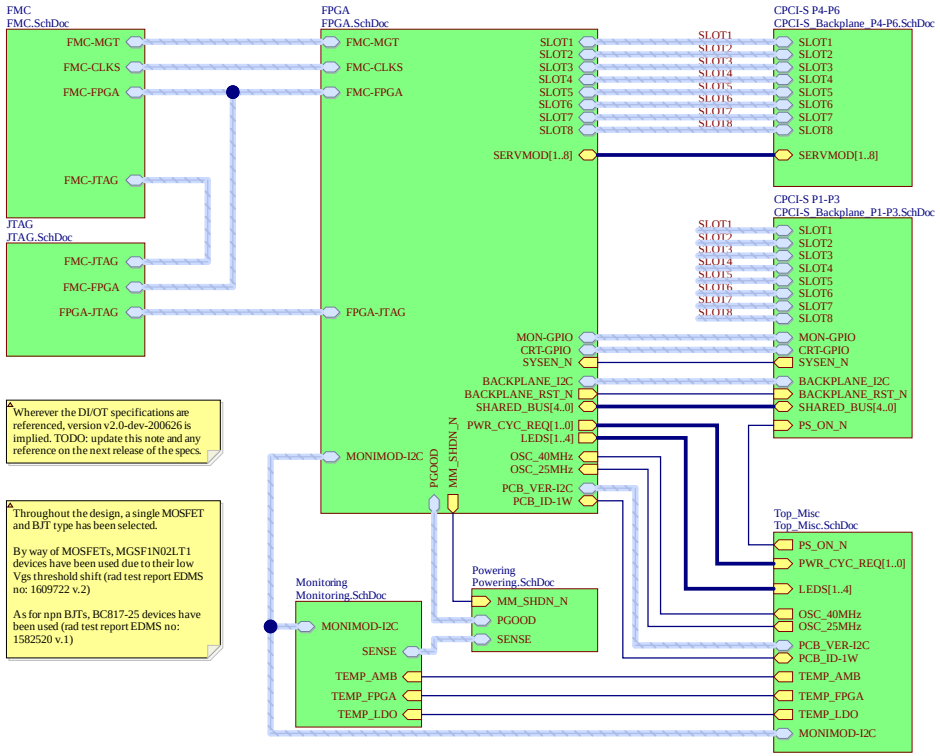
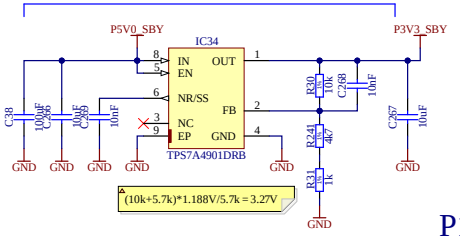


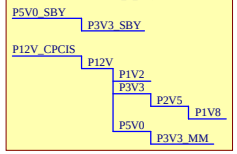
Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board Top Level**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/2/2021
		File DIOT-sb-igl_top.SchDoc	
		Print Date 5/10/2021 2:42:27 PM	Sheet 1 of 17
BE/CO	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3 / Rev *

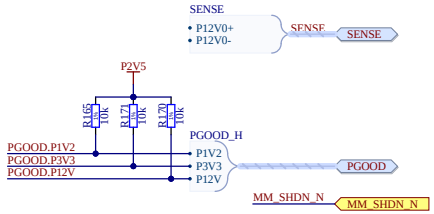
Always-on P3V3 power



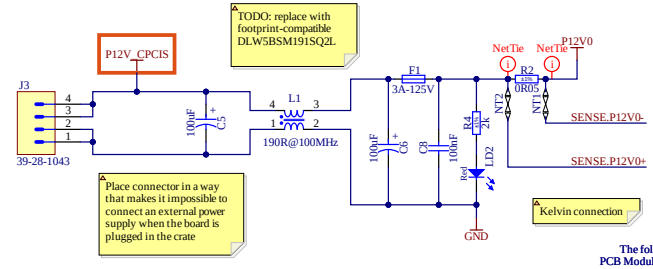
P12V is only enabled after P3V3_SBY is up because of PS_ON_N (see Top_Misc)

Power supply tree

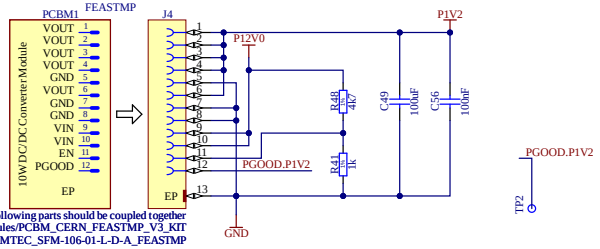




12V0 power cleanup

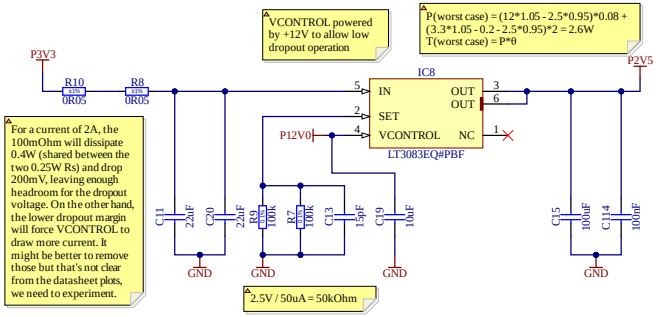


P1V2 power

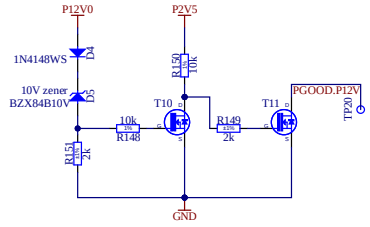


The following parts should be coupled together
PCB Modules/PCBM_CERN_FEASTMP_V3_KIT
SAMTEC/SAMTEC_SFM-106-01-L-D-A_FEASTMP

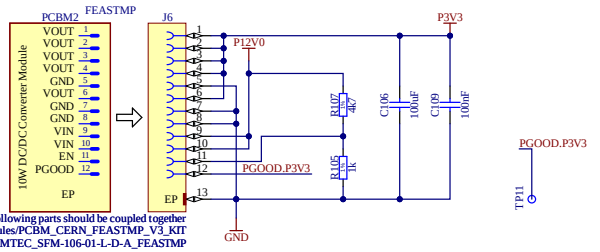
P2V5 power



12V brownout detection

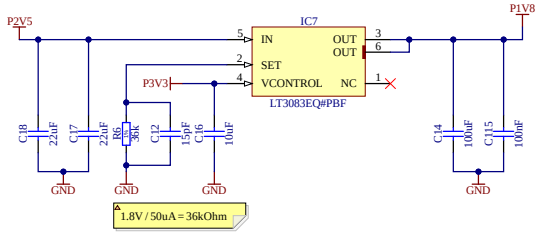


P3V3 power

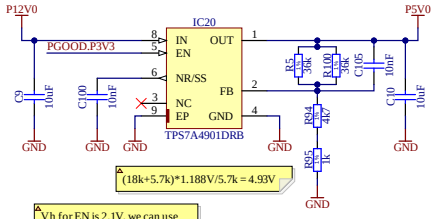


The following parts should be coupled together
PCB Modules/PCBM_CERN_FEASTMP_V3_KIT
SAMTEC/SAMTEC_SFM-106-01-L-D-A_FEASTMP

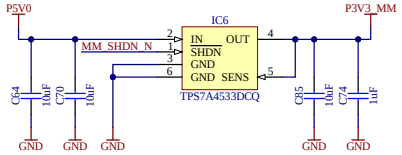
P1V8 power



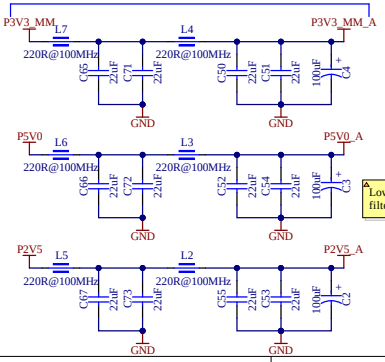
P5V0 power



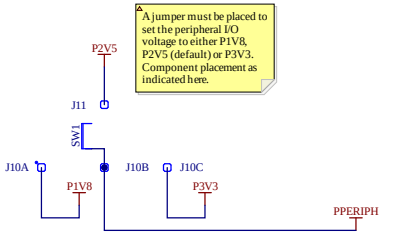
MoniMod P3V3 power



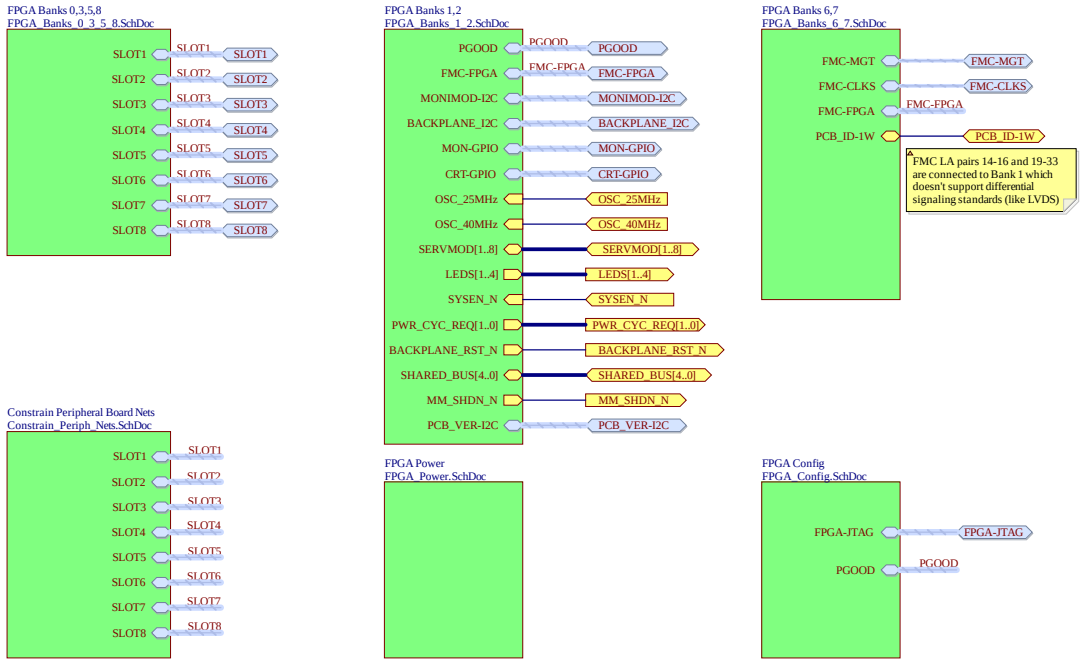
Analog power filtering



Peripheral voltage selection



Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board Power**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/21020
		Last Mod. C. Gentsos	4/14/2021
		File Powering.SchDoc	
		Print Date 5/10/2021 2:42:27 PM	Sheet 2 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3 Rev *



Project/Equipment	DI/OT		
Document	*DI/OT Rad-tol System Board FPGA Top*	Designer C. Gentsos	
BE/CO		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/23020
		Last Mod. C. Gentsos	4/2/2021
		File FPGA.SchDoc	
		Print Date 5/10/2021 2:42:27 PM	Sheet 3 of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3	Rev *

IC31M
M2GL090T-FGG676I

VSS, VSSNVM, GND

IC31L
M2GL090T-FGG676I

PPERIPH, P2V5, P3V3, P1V2, VREF1, VDDI0, VDDI1, VDDI2, VDDI3, VDDI4, VDDI5, VDDI6, VDDI7, VDDI8, VDD, VPP, VPPNVM

IC31K
M2GL090T-FGG676I

P2V5_PLL1_VDDA	J18	CCC_NE0_NE1_HPMS_MDDR_PLL_VDDA
P2V5_PLL1_VSSA	K17	CCC_NE0_NE1_HPMS_MDDR_PLL_VSSA
P2V5_PLL2_VDDA	K11	CCC_NW0_NW1_PLL_VDDA
P2V5_PLL2_VSSA	L11	CCC_NW0_NW1_PLL_VSSA
P2V5_PLL3_VDDA	U8	CCC_SW0_SW1_PLL_VDDA
P2V5_PLL3_VSSA	T9	CCC_SW0_SW1_PLL_VSSA

PLL power, 2.5V or 3.3V? 2.5V will be smoother due to the LDO so better jitter but is any of the two better for radiation?

VPPNVM must be shorted to VPP

25 VDD pins: 13x 10n, 12x 100n, 1x 100u, 3x 220u, 1x 330u

Some recent advice (URL below) indicates that if one MLCC is used per pin it's best to use the highest value of a given package size (here 0402). Microsemi still recommends using two different values (100n and 10n). Also, looking at the impedance-freq curves from a few same-package capacitors of different values, doesn't fully support that the inductance is the same for a given package. Still, we might want to consider this advice when we run an SIwave PI simulation after we have some layout.

7 VPP pins: 4x 10n, 3x 100n, 1x 10u

3 VREF1 pins: 2x 10n, 1x 100n, 1x 10u

1 VPPNVM pin: 1x 10n, 1x 10u

1 VDDI6 pin: 1x 100n, 1x 10u

12 VDDI1 pins: 6x 10n, 6x 100n, 1x 10u

1 VDDI4 pin: 1x 100n, 1x 10u

13 VDDI3 pins: 6x 10n, 7x 100n, 1x 10u

4 VDDI0 pins: 2x 10n, 2x 100n, 1x 10u

10 VDDI5 pins: 5x 10n, 5x 100n, 1x 10u

3 VDDI2 pins: 1x 10n, 2x 100n, 1x 10u

10 VDDI8 pins: 5x 10n, 5x 100n, 1x 10u

4 VDDI7 pins: 2x 10n, 2x 100n, 1x 10u

PLL RC filters

P2V5 — R200 (1R) — P2V5_PLL1_VDDA; 22uF C30; 100nF C167; P2V5_PLL1_VSSA

P2V5 — R218 (1R) — P2V5_PLL2_VDDA; 22uF C31; 100nF C171; P2V5_PLL2_VSSA

P2V5 — R221 (1R) — P2V5_PLL3_VDDA; 22uF C32; 100nF C200; P2V5_PLL3_VSSA

Place the 0402 100nF caps close to the FPGA pins

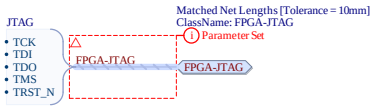
Project/Equipment	DI/OT
Document	DI/OT Rad-tol System Board FPGA Power
Designer	C. Gentsos
Drawn by	C. Gentsos 28/08/2020
Check.by	B. Recordon 20/11/2020
Last Mod.	C. Gentsos 4/20/2021
File	FPGA_Power.SchDoc
Print Date	5/10/2021 2:42:27 PM
Sheet	4 of 17
Size	A3
Rev	*

BE/CO

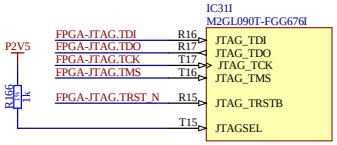
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

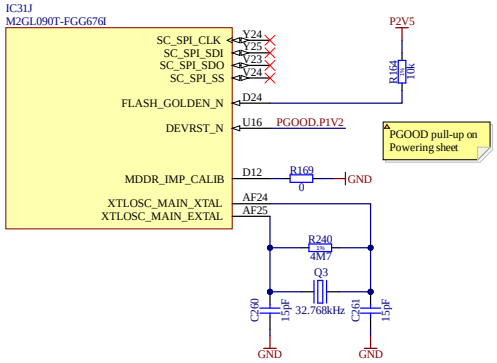
EDA-04326-V1-0

Parts powered by 2.5V



The JTAG and configuration pins are referred to as Bank 4





PGOOD pull-up on Powering sheet

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA Configuration and reset	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/20/2021
		File FPGA_Config.SchDoc	
		Print Date 5/10/2021 2:42:27 PM	Sheet 5 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3 Rev *

Banks powered by PPERIPH

Caution on pin-swapping: the S0_P pins are connected to Global I/O pins to be able to drive FPGA clocks and can't be swapped with other peripheral I/Os. Boards 1-3 can drive global buffers directly or use CCC blocks; Boards 4-6 can drive global buffers directly or through VCCC crossbars; and Boards 7-8 can only reach global buffers through CCC blocks.

IC31A
M2GL090T-FGG676I

BANK 0

MSIO111NB0	J12	SLOT3.LVDS_3_N (-1)
MSIO111PB0	J11	SLOT3.LVDS_3_P
MSIO112NB0	A9	SLOT7.LVDS_12_N
MSIO112PB0	A8	SLOT7.LVDS_12_P
MSIO113NB0	D11	SLOT5.LVDS_3_N
MSIO113PB0	C10	SLOT5.LVDS_3_P
MSIO114NB0	B8	SLOT8.LDVS_13_N
MSIO114PB0	A7	SLOT8.LVDS_13_P
MSIO115NB0	H10	SLOT7.LVDS_3_N
MSIO115PB0	H9	SLOT7.LVDS_3_P
MSIO116NB0	C8	SLOT4.LVDS_1_N
MSIO116PB0	D8	SLOT4.LVDS_1_P
MSIO117NB0	E10	SLOT2.LVDS_1_N
MSIO117PB0	E9	SLOT2.LVDS_1_P
MSIO118NB0	B7	SLOT2.LVDS_4_N
MSIO118PB0	B6	SLOT2.LVDS_4_P
MSIO119NB0	F9	SLOT3.LVDS_15_N
MSIO119PB0	E8	SLOT3.LVDS_15_P
MSIO120NB0	A5	SLOT8.LVDS_12_N (-10)
MSIO120PB0	A4	SLOT8.LVDS_12_P
MSIO121NB0	F7	SLOT3.LVDS_16_N
MSIO121PB0	F8	SLOT3.LVDS_16_P
MSIO122NB0	B5	SLOT4.LVDS_4_N
MSIO122PB0	C6	SLOT4.LVDS_4_P
MSIO123NB0	E5	SLOT8.LVDS_4_N
MSIO123PB0	C4	SLOT8.LVDS_4_P
MSIO124NB0	D7	SLOT7.LVDS_1_N
MSIO124PB0	D6	SLOT7.LVDS_1_P
MSIO125NB0	F6	SLOT3.LVDS_5_N
MSIO125PB0	F7	SLOT3.LVDS_5_P

IC31D
M2GL090T-FGG676I

BANK 3

MSIO00NB3	W22	SLOT5.LVDS_14_N
MSIO00PB3	W21	SLOT5.LVDS_14_P
MSIO01NB3	AA23	SLOT4.LVDS_14_N (-7)
MSIO01PB3	Y22	SLOT4.LVDS_14_P
MSIO02NB3	AC25	SLOT6.LVDS_15_N (-1)
MSIO02PB3	AC24	SLOT6.LVDS_15_P
MSIO03NB3	Y21	SLOT5.LVDS_13_N
MSIO03PB3	Y20	SLOT5.LVDS_13_P
MSIO04NB3	AC26	SLOT8.LVDS_5_N
MSIO04PB3	AD26	SLOT8.LVDS_5_P
MSIO05NB3	U21	SLOT2.LVDS_10_N
MSIO05PB3	U20	SLOT2.LVDS_10_P
MSIO06NB3	W24	SLOT7.LVDS_8_N
MSIO06PB3	W23	SLOT7.LVDS_8_P
MSIO07NB3	AA25	SLOT7.LVDS_15_N
MSIO07PB3	AA24	SLOT7.LVDS_15_P
MSIO08NB3	AB26	SLOT8.LVDS_9_N
MSIO08PB3	AB25	SLOT8.LVDS_9_P
MSIO11NB3/CCC_NE1_CLKI0	T22	SLOT8.LVDS_0_N
MSIO11PB3/CCC_NE0_CLKI0	U22	SLOT8.LVDS_0_P CC
MSIO12NB3/SPI_0_SDI	W26	SLOT3.LVDS_17_N
MSIO12PB3/SPI_0_CLK	Y26	SLOT3.LVDS_17_P
MSIO13NB3/SPI_0_SS0	T23	SLOT8.LVDS_16_N
MSIO13PB3/SPI_0_SDO	U23	SLOT8.LVDS_16_P
MSIO14NB3	V26	SLOT7.LVDS_17_N (-10)
MSIO14PB3	V25	SLOT7.LVDS_17_P
MSIO15NB3	T20	SLOT4.LVDS_3_N
MSIO15PB3	T19	SLOT4.LVDS_3_P
MSIO16NB3	U26	SLOT1.LVDS_13_N
MSIO16PB3	U25	SLOT1.LVDS_13_P
MSIO17NB3	T18	SLOT7.LVDS_14_N
MSIO17PB3	U18	SLOT7.LVDS_14_P
MSIO18NB3	T25	SLOT8.LVDS_15_N
MSIO18PB3	T24	SLOT8.LVDS_15_P
MSIO19NB3	R21	SLOT6.LVDS_14_N
MSIO19PB3	R22	SLOT6.LVDS_14_P
MSIO20NB3/GB13/VCCC_SE1_CLKI	R25	SLOT6.LVDS_0_N
MSIO20PB3/GB9/VCCC_SE0_CLKI	R24	SLOT6.LVDS_0_P CC
MSIO21NB3	R19	SLOT1.LVDS_11_N
MSIO21PB3	R20	SLOT1.LVDS_11_P
MSIO22NB3	P26	SLOT2.LVDS_13_N (-7)
MSIO22PB3	R26	SLOT2.LVDS_13_P
MSIO23NB3	P19	SLOT6.LVDS_3_N (-1)
MSIO23PB3	P18	SLOT6.LVDS_3_P
MSIO24NB3	P24	SLOT8.LVDS_7_N
MSIO24PB3	P23	SLOT8.LVDS_7_P
MSIO25NB3	P22	SLOT2.LVDS_12_N
MSIO25PB3	P21	SLOT2.LVDS_12_P
MSIO26NB3	N25	SLOT3.LVDS_11_N
MSIO26PB3	N26	SLOT3.LVDS_11_P
MSIO27NB3	P16	SLOT3.LVDS_13_N
MSIO27PB3	P17	SLOT3.LVDS_13_P
MSIO28NB3	N23	SLOT1.LVDS_17_N
MSIO28PB3	N24	SLOT1.LVDS_17_P
MSIO29NB3	N19	SLOT3.LVDS_2_N
MSIO29PB3	N18	SLOT3.LVDS_2_P
MSIO30NB3	M25	SLOT4.LVDS_13_N
MSIO30PB3	M26	SLOT4.LVDS_13_P
MSIO32NB3	M23	SLOT5.LVDS_17_N
MSIO32PB3	M22	SLOT5.LVDS_17_P
MSIO33NB3	N20	SLOT4.LVDS_11_N (-10)
MSIO33PB3	N21	SLOT4.LVDS_11_P
MSIO34NB3	L24	SLOT2.LVDS_2_N
MSIO34PB3	L25	SLOT2.LVDS_2_P
MSIO35NB3	M18	SLOT6.LVDS_2_N
MSIO35PB3	M17	SLOT6.LVDS_2_P
MSIO36NB3	L26	SLOT5.LVDS_11_N
MSIO36PB3	K26	SLOT5.LVDS_11_P
MSIO37NB3	M20	SLOT7.LVDS_2_N
MSIO37PB3	M21	SLOT7.LVDS_2_P
MSIO38NB3	K24	SLOT3.LVDS_12_N
MSIO38PB3	K25	SLOT3.LVDS_12_P
MSIO39NB3	K19	SLOT5.LVDS_2_N
MSIO39PB3	K20	SLOT5.LVDS_2_P
MSIO40NB3	H25	SLOT6.LVDS_11_N (-7)
MSIO40PB3	H26	SLOT6.LVDS_11_P
MSIO41NB3	L19	SLOT4.LVDS_12_N (-1)
MSIO41PB3	L20	SLOT4.LVDS_12_P
MSIO42NB3	G25	SLOT7.LVDS_11_N
MSIO42PB3	G26	SLOT7.LVDS_11_P
MSIO43NB3	L18	SLOT3.LVDS_14_N
MSIO43PB3	L17	SLOT3.LVDS_14_P
MSIO44NB3	L22	SLOT2.LVDS_14_N
MSIO44PB3	L23	SLOT2.LVDS_14_P
MSIO45NB3	J23	SLOT1.LVDS_12_N
MSIO45PB3	J24	SLOT1.LVDS_12_P
MSIO46NB3	K21	SLOT5.LVDS_12_N
MSIO46PB3	K22	SLOT5.LVDS_12_P
MSIO47NB3	J23	SLOT1.LVDS_14_N
MSIO47PB3	H24	SLOT1.LVDS_14_P
MSIO48NB3	H19	SLOT6.LVDS_12_N
MSIO48PB3	J19	SLOT6.LVDS_12_P
MSIO49NB3	J21	SLOT8.LVDS_11_N
MSIO49PB3	J22	SLOT8.LVDS_11_P
MSIO50NB3	H20	SLOT7.LVDS_13_N (-10)
MSIO50PB3	H21	SLOT7.LVDS_13_P

IC31E
M2GL090T-FGG676I

BANK 5

MSIO195NB5	W13	SLOT8.LVDS_14_N
MSIO195PB5	W12	SLOT8.LVDS_14_P
MSIO196NB5/CCC_SW0_CLKI2	AC11	SLOT4.LVDS_16_N
MSIO196PB5	AB11	SLOT4.LVDS_16_P
MSIO197NB5/PROBE_B	AD12	SLOT1.LVDS_1_N
MSIO197PB5/PROBE_A	AE12	SLOT1.LVDS_1_P
MSIO198NB5	Y12	SLOT8.LVDS_17_N
MSIO198PB5	AA12	SLOT8.LVDS_17_P
MSIO199NB5	AF13	SLOT1.LVDS_15_N
MSIO199PB5	AF12	SLOT1.LVDS_15_P
MSIO201NB5/GB7/CCC_SW1_CLKI2	AB13	SLOT3.LVDS_0_N
MSIO201PB5/GB3/CCC_SW0_CLKI3	AB12	SLOT3.LVDS_0_P CC
MSIO202NB5	AE14	SLOT1.LVDS_5_N
MSIO202PB5	AF14	SLOT1.LVDS_5_P
MSIO203NB5	V14	SLOT6.LVDS_17_N (-7)
MSIO203PB5	V13	SLOT6.LVDS_17_P
MSIO204NB5	AD14	SLOT3.LVDS_8_N (-1)
MSIO204PB5	AD13	SLOT3.LVDS_8_P
MSIO205NB5	AC14	SLOT1.LVDS_4_N
MSIO205PB5	AC13	SLOT1.LVDS_4_P
MSIO206NB5	AF17	SLOT1.LVDS_9_N
MSIO206PB5	AF18	SLOT1.LVDS_9_P
MSIO207NB5	AA14	SLOT1.LVDS_7_N
MSIO207PB5	AA13	SLOT1.LVDS_7_P
MSIO208NB5	AE15	SLOT7.LVDS_0_N
MSIO208PB5/CCC_SW1_CLKI3	AF15	SLOT7.LVDS_0_P CC
MSIO209NB5/VCCC_SE0_CLKI	Y14	SLOT2.LVDS_17_N
MSIO209PB5/VCCC_SE0_CLKI	W14	SLOT2.LVDS_17_P
MSIO210NB5	AE17	SLOT5.LVDS_0_N
MSIO210PB5/GB11/VCCC_SE0_CLKI	AE16	SLOT5.LVDS_0_P CC
MSIO211NB5	Y17	SLOT8.LVDS_6_N
MSIO211PB5	AA17	SLOT8.LVDS_6_P
MSIO212NB5	AD17	SLOT4.LVDS_0_N
MSIO212PB5/GB15/VCCC_SE1_CLKI	AD16	SLOT4.LVDS_0_P CC
MSIO213NB5	AB15	SLOT2.LVDS_6_N
MSIO213PB5/VCCC_SE1_CLKI	AC15	SLOT2.LVDS_6_P
MSIO214NB5	Y15	SLOT6.LVDS_7_N
MSIO214PB5	AA15	SLOT6.LVDS_7_P
MSIO215NB5	AB16	SLOT2.LVDS_7_N
MSIO215PB5	AC16	SLOT2.LVDS_7_P
MSIO216NB5	AB17	SLOT7.LVDS_9_N (-10)
MSIO216PB5	AB18	SLOT7.LVDS_9_P
MSIO217NB5	V16	SLOT8.LVDS_8_N
MSIO217PB5	V15	SLOT8.LVDS_8_P
MSIO218NB5	AF20	SLOT1.LVDS_3_N
MSIO218PB5	AF19	SLOT1.LVDS_3_P
MSIO221NB5	W17	SLOT1.LVDS_16_N
MSIO221PB5	W18	SLOT1.LVDS_16_P
MSIO222NB5	AE20	SLOT2.LVDS_5_N
MSIO222PB5	AE19	SLOT2.LVDS_5_P
MSIO223NB5	W16	SLOT8.LVDS_10_N
MSIO223PB5	Y16	SLOT8.LVDS_10_P
MSIO224NB5	AD19	SLOT4.LVDS_8_N
MSIO224PB5	AD18	SLOT4.LVDS_8_P
MSIO225NB5	AE21	SLOT5.LVDS_16_N (-7)
MSIO225PB5	AF22	SLOT5.LVDS_16_P
MSIO226NB5	Y19	SLOT2.LVDS_15_N (-1)
MSIO226PB5	W19	SLOT2.LVDS_15_P
MSIO227NB5	AE22	SLOT1.LVDS_2_N
MSIO227PB5	AF23	SLOT1.LVDS_2_P
MSIO228NB5	Y20	SLOT2.LVDS_9_N
MSIO228PB5	Y21	SLOT2.LVDS_9_P
MSIO229NB5	AC19	SLOT2.LVDS_8_N
MSIO229PB5	AC18	SLOT2.LVDS_8_P
MSIO230NB5	V18	SLOT6.LVDS_13_N
MSIO230PB5	V19	SLOT6.LVDS_13_P
MSIO231NB5	AA19	SLOT1.LVDS_8_N
MSIO231PB5	AA18	SLOT1.LVDS_8_P
MSIO232NB5	AD23	SLOT7.LVDS_7_N
MSIO232PB5	AD22	SLOT7.LVDS_7_P
MSIO233NB5	AC20	SLOT4.LVDS_17_N
MSIO233PB5	AD21	SLOT4.LVDS_17_P
MSIO234NB5	AD24	SLOT5.LVDS_7_N
MSIO234PB5	AE24	SLOT5.LVDS_7_P
MSIO235NB5	AB21	SLOT1.LVDS_6_N (-10)
MSIO235PB5	AC21	SLOT1.LVDS_6_P
MSIO236NB5	AB23	SLOT2.LVDS_11_N
MSIO236PB5	AC23	SLOT2.LVDS_11_P
MSIO237NB5	AB22	SLOT2.LVDS_16_N
MSIO237PB5	AA22	SLOT2.LVDS_16_P
MSIO238NB5	AA20	SLOT1.LVDS_10_N
MSIO238PB5	AB20	SLOT1.LVDS_10_P

IC31G
M2GL090T-FGG676I

BANK 8

MSIO126NB8	G7	SLOT6.LVDS_1_N
MSIO126PB8	G8	SLOT6.LVDS_1_P
MSIO127NB8	H6	SLOT4.LVDS_15_N
MSIO127PB8	H5	SLOT4.LVDS_15_P
MSIO128NB8	J7	SLOT8.LVDS_1_N
MSIO128PB8	J6	SLOT8.LVDS_1_P
MSIO129NB8	G6	SLOT3.LVDS_4_N (-7)
MSIO129PB8	G5	SLOT3.LVDS_4_P
MSIO131NB8	J5	SLOT3.LVDS_6_N (-1)
MSIO131PB8	J4	SLOT3.LVDS_6_P
MSIO132NB8	E5	SLOT3.LVDS_7_N
MSIO132PB8	E4	SLOT3.LVDS_7_P
MSIO133NB8	D4	SLOT4.LVDS_6_N
MSIO133PB8	D3	SLOT4.LVDS_6_P
MSIO134NB8	F3	SLOT3.LVDS_10_N
MSIO134PB8	F4	SLOT3.LVDS_10_P
MSIO135NB8	H4	SLOT5.LVDS_6_N
MSIO135PB8	H3	SLOT5.LVDS_6_P
MSIO136NB8	G3	SLOT4.LVDS_10_N
MSIO136PB8	F3	SLOT4.LVDS_10_P
MSIO137NB8	J3	SLOT5.LVDS_1_N
MSIO137PB8	J2	SLOT5.LVDS_1_P
MSIO138NB8	A3	SLOT3.LVDS_9_N
MSIO138PB8	A2	SLOT3.LVDS_9_P
MSIO139NB8	C9	SLOT8.LVDS_3_N
MSIO139PB8	C10	SLOT8.LVDS_3_P
MSIO140NB8	B2	SLOT5.LVDS_15_N (-1)
MSIO140PB8	B1	SLOT5.LVDS_15_P
MSIO142NB8	F9	SLOT3.LVDS_1_N
MSIO142PB8	F10	SLOT3.LVDS_1_P
MSIO143NB8	E9	SLOT6.LVDS_16_N
MSIO143PB8	D9	SLOT6.LVDS_16_P
MSIO145NB8	G7	SLOT4.LVDS_7_N
MSIO145PB8	G6	SLOT4.LVDS_7_P
MSIO146NB8	E6	SLOT6.LVDS_4_N
MSIO146PB8	F8	SLOT6.LVDS_4_P
MSIO147NB8	F7	SLOT5.LVDS_4_N
MSIO147PB8	M8	SLOT5.LVDS_4_P
MSIO148NB8	D2	SLOT4.LVDS_9_N
MSIO148PB8	E1	SLOT4.LVDS_9_P
MSIO149NB8	E2	SLOT7.LVDS_10_N (-7)
MSIO149PB8	E1	SLOT7.LVDS_10_P
MSIO150NB8	F2	SLOT6.LVDS_8_N (-1)
MSIO150PB8	F1	SLOT6.LVDS_8_P
MSIO151NB8	L5	SLOT5.LVDS_5_N
MSIO151PB8	M5	SLOT5.LVDS_5_P
MSIO152NB8	L4	SLOT5.LVDS_10_N
MSIO152PB8	K4	SLOT5.LVDS_10_P
MSIO153NB8	M6	SLOT2.LVDS_3_N
MSIO153PB8	M7	SLOT2.LVDS_3_P
MSIO154NB8	K2	SLOT7.LVDS_16_N
MSIO154PB8	L1	SLOT7.LVDS_16_P
MSIO156NB8	P4	SLOT1.LVDS_0_N
MSIO156PB8/GB6/CCC_NW1_CLKI1	N4	SLOT1.LVDS_0_P CC
MSIO157NB8	N5	SLOT2.LVDS_0_N
MSIO157PB8/GB2/CCC_NW0_CLKI1	N6	SLOT2.LVDS_0_P CC
MSIO158NB8	M3	SLOT5.LVDS_8_N
MSIO158PB8/CCC_NW1_CLKI0	N3	SLOT5.LVDS_8_P
MSIO159NB8	N8	SLOT4.LVDS_2_N
MSIO159PB8/CCC_NW0_CLKI0	N9	SLOT4.LVDS_2_P
MSIO160NB8	P3	SLOT4.LVDS_5_N
MSIO160PB8	R2	SLOT4.LVDS_5_P
MSIO161NB8	P2	SLOT5.LVDS_9_N
MSIO161PB8	M2	SLOT5.LVDS_9_P
MSIO163NB8	M10	SLOT8.LVDS_2_N (-10)
MSIO163PB8	N10	SLOT8.LVDS_2_P
MSIO165NB8	P6	SLOT7.LVDS_4_N
MSIO165PB8	P7	SLOT7.LVDS_4_P
MSIO166NB8	T2	SLOT6.LVDS_9_N
MSIO166PB8	T1	SLOT6.LVDS_9_P
MSIO167NB8	R1	SLOT7.LVDS_5_N
MSIO167PB8	P1	SLOT7.LVDS_5_P
MSIO168NB8	R3	SLOT6.LVDS_6_N
MSIO168PB8	R4	SLOT6.LVDS_6_P
MSIO170NB8	M1	SLOT6.LVDS_5_N
MSIO170PB8	N1	SLOT6.LVDS_5_P
MSIO172NB8	T2	SLOT6.LVDS_10_N
MSIO172PB8	R2	SLOT6.LVDS_10_P
MSIO173NB8	P1	SLOT7.LVDS_6_N (-7)
MSIO173PB8	R1	SLOT7.LVDS_6_P

PERIPH_CONN

- LVDS_0_P
- LVDS_0_N
- LVDS_1_P
- LVDS_1_N
- LVDS_2_P
- LVDS_2_N
- LVDS_3_P
- LVDS_3_N
- LVDS_4_P
- LVDS_4_N
- LVDS_5_P
- LVDS_5_N
- LVDS_6_P
- LVDS_6_N
- LVDS_7_P
- LVDS_7_N
- LVDS_8_P
- LVDS_8_N
- LVDS_9_P
- LVDS_9_N
- LVDS_10_P
- LVDS_10_N
- LVDS_11_P
- LVDS_11_N
- LVDS_12_P
- LVDS_12_N
- LVDS_13_P
- LVDS_13_N
- LVDS_14_P
- LVDS_14_N
- LVDS_15_P
- LVDS_15_N
- LVDS_16_P
- LVDS_16_N
- LVDS_17_P
- LVDS_17_N

Intra-diff pair rule. Inter-diff pair rules can be found on a dedicated sheet.

Matched Net Lengths [Tolerance = 2mm]
DifferentialPairClassName: PERIPH_DP

SLOT1	SLOT1
SLOT2	SLOT2
SLOT3	SLOT3
SLOT4	SLOT4
SLOT5	SLOT5
SLOT6	SLOT6
SLOT7	SLOT7
SLOT8	SLOT8

Project/Equipment: DI/OT

Document: **DI/OT Rad-tol System Board**
FPGA I/O Banks B0, B3

BE/CO

Designer	C. Gentsos	
Drawn by	C. Gentsos	28/08/2020
Check.by	B. Recordon	24/11/2020
Last Mod.	C. Gentsos	4/20/2021
File	FPGA_Banks_0_3_5_8.SchDoc	
Print Date	5/10/2021 2:42:27 PM	Sheet 6 of 17

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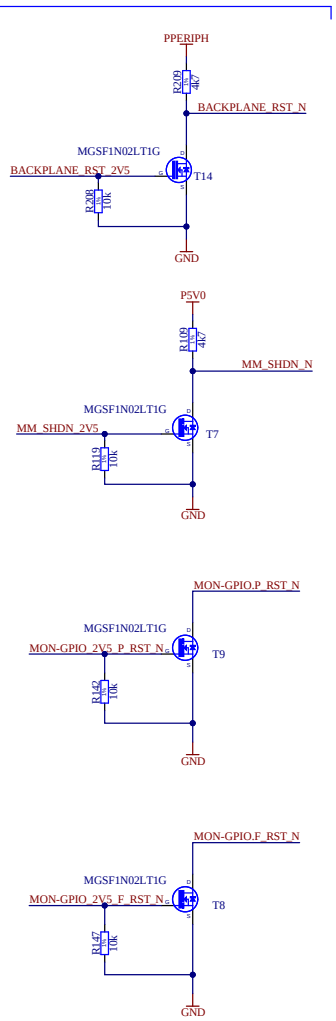
EDA-04326-V1-0 | Size A3 | Rev *

Bank 1 powered by 2.5V, Bank 2 by 3.3V

Level translators



IC31B
M2GL090T-FGG676I

BANK 1

DDRIO62NB1/MDDR_ADDR15	C23	SERVMOD_FPGA6
DDRIO62PB1/MDDR_ADDR14	D22	SHARED_BUS_DIR1
DDRIO63NB1/MDDR_ADDR13	B23	FMC-FPGA.LA.D_N3
DDRIO63PB1/MDDR_ADDR12	A23	FMC-FPGA.LA.D_P3
DDRIO64NB1/MDDR_ADDR11	E21	SHARED_BUS_DIR3
DDRIO64PB1/MDDR_ADDR10	D21	SHARED_BUS_DIR4
DDRIO65NB1/MDDR_ADDR9	E20	SHARED_BUS_FPGA3
DDRIO65PB1/MDDR_ADDR8	E20	SHARED_BUS_FPGA1
DDRIO66NB1/MDDR_ADDR7	B22	FMC-FPGA.LA.D_N8
DDRIO66PB1/MDDR_ODT	A22	FMC-FPGA.LA.D_P8
DDRIO67NB1/MDDR_ADDR6	H18	SHARED_BUS_DIR0
DDRIO67PB1/MDDR_ADDR5	G18	SHARED_BUS_FPGA4
DDRIO68NB1/MDDR_ADDR4	C21	SHARED_BUS_FPGA2
DDRIO68PB1/MDDR_ADDR3	B21	SHARED_BUS_DIR2
DDRIO69NB1/MDDR_ADDR2	E19	LEDS1
DDRIO69PB1/MDDR_ADDR1	F19	LEDS2
DDRIO70NB1/MDDR_ADDR0	F18	LEDS4
DDRIO70PB1/MDDR_BA2	G17	LEDS3
DDRIO71NB1/MDDR_BA1	B20	FMC-FPGA.LA.D_N9
DDRIO71PB1/MDDR_BA0	A20	FMC-FPGA.LA.D_P9
DDRIO72NB1/MDDR_CLK_N	C20	FMC-FPGA.LA.D_N23
DDRIO72PB1/MDDR_CLK	C19	FMC-FPGA.LA.D_P23
DDRIO73NB1/MDDR_CAS_N	D19	MON-GPIO_2V5_P_RST_N
DDRIO73PB1/MDDR_RESET_N	D18	MON-GPIO_2V5_F_RST_N
DDRIO74NB1/MDDR_CS_N	F17	FMC-FPGA.PRSNT
DDRIO74PB1/MDDR_CKE	E17	PWR_CYC_REQ1
DDRIO75NB1/MDDR_WE_N	H16	MONIMOD-I2C_2V5.SCL
DDRIO75PB1/MDDR_RAS_N	H16	MONIMOD-I2C_2V5.SDA
DDRIO76NB1/MDDR_DQ15	A19	FMC-FPGA.LA.D_N18
DDRIO76PB1/CCC_NE1_CLKI3/MDDR_DQ14	A18	FMC-FPGA.LA.D_P18
DDRIO77NB1/MDDR_DQ13	B18	FMC-FPGA.LA.D_N17
DDRIO77PB1/MDDR_DQ12/GB12/CCC_NE1_CLKI2	C18	FMC-FPGA.LA.D_P17
DDRIO78NB1/MDDR_DM_RDQS1	H15	BACKPLANE_RST_2V5
DDRIO78PB1/MDDR_TMATCH_0_IN	G16	PWR_CYC_REQ0
DDRIO79NB1/MDDR_DQS1_N	A17	FMC-FPGA.LA.D_N20
DDRIO79PB1/MDDR_DQS1/GB8/CCC_NE0_CLKI3	B17	FMC-FPGA.LA.D_P20
DDRIO80NB1/MDDR_DQ11	D17	SERVMOD_FPGA8
DDRIO80PB1/MDDR_DQ10/CCC_NE0_CLKI2	E16	SERVMOD_FPGA7
DDRIO81NB1/MDDR_DQ9	D16	SERVMOD_DIR
DDRIO81PB1/MDDR_DQ8	C16	MM_SHDN_2V5
DDRIO82NB1/MDDR_TMATCH_0_OUT	G15	SERVMOD_FPGA1
DDRIO82PB1/MDDR_DQ7	E15	SERVMOD_FPGA2
DDRIO83NB1/MDDR_DQ6	B16	SERVMOD_FPGA3
DDRIO83PB1/MDDR_DQ5	A15	SERVMOD_FPGA4
DDRIO84NB1/MDDR_DQ4	B15	SERVMOD_FPGA5
DDRIO84PB1/MDDR_DM_RDQS0	A14	SHARED_BUS_FPGA0
DDRIO85NB1/MDDR_DQS0_N	C15	FMC-FPGA.LA.D_N19
DDRIO85PB1/MDDR_DQS0	C14	FMC-FPGA.LA.D_P19
DDRIO86NB1/MDDR_DQ3	E14	FMC-FPGA.LA.D_N25
DDRIO86PB1/MDDR_DQ2	D14	FMC-FPGA.LA.D_P25
DDRIO87NB1/MDDR_DQ1	E15	FMC-FPGA.LA.D_N30
DDRIO87PB1/MDDR_DQ0	E14	FMC-FPGA.LA.D_P30
DDRIO88NB1	A13	FMC-FPGA.LA.D_N27
DDRIO88PB1/CCC_NW1_CLKI3	B13	FMC-FPGA.LA.D_P27
DDRIO89NB1/MDDR_DQ_ECC0	D13	FMC-FPGA.LA.D_N21
DDRIO89PB1/MDDR_DQ_ECC1	C13	FMC-FPGA.LA.D_P21
DDRIO90NB1/MDDR_DM_RDQS_ECC	E13	FMC-FPGA.LA.D_N28
DDRIO90PB1/MDDR_TMATCH_ECC_IN	G13	FMC-FPGA.LA.D_P28
DDRIO91NB1/MDDR_DQS_ECC_N	A12	FMC-FPGA.LA.D_N22
DDRIO91PB1/MDDR_DQS_ECC	B12	FMC-FPGA.LA.D_P22
DDRIO92NB1/GB4/CCC_NW1_CLKI2	E12	FMC-FPGA.LA.D_N24
DDRIO92PB1/GB0/CCC_NW0_CLKI3	H13	FMC-FPGA.LA.D_N31
DDRIO93NB1/CCC_NW0_CLKI2	H14	FMC-FPGA.LA.D_P31
DDRIO93PB1/MDDR_TMATCH_ECC_OUT	B11	FMC-FPGA.LA.D_N26
DDRIO94NB1	C11	FMC-FPGA.LA.D_P26
DDRIO94PB1	E11	FMC-FPGA.LA.D_N29
DDRIO95NB1	D11	FMC-FPGA.LA.D_P29
DDRIO95PB1	A10	PCB_VER-I2C_2V5.SCL
DDRIO96NB1	B10	PCB_VER-I2C_2V5.SDA
DDRIO96PB1	G12	USER_FLASH.SS_N
DDRIO97NB1	G11	USER_FLASH.MISO
DDRIO97PB1	G9	USER_FLASH.MOSI
DDRIO98NB1	E10	USER_FLASH.SCLK
DDRIO98PB1	C10	PGOOD.P12V
DDRIO99NB1	C9	PGOOD.P3V3
DDRIO99PB1		

IC31C
M2GL090T-FGG676I

BANK 2

MSIO51NB2	F25	CRT-GPIO.PWRBTN_N
MSIO51PB2	E26	CRT-GPIO.PRST_N
MSIO52NB2	E26	
MSIO52PB2/CCC_NE0_CLKI1	D26	OSC_25MHz
MSIO53NB2	B25	
MSIO53PB2/CCC_NE1_CLKI1	B26	OSC_40MHz
MSIO54NB2	E24	FMC-FPGA.I2C.SCL
MSIO54PB2/GB10/VCCCC_SE0_CLKI	E25	FMC-FPGA.I2C.SDA
MSIO55NB2	F23	MON-GPIO.F_IO0
MSIO55PB2/GB14/VCCCC_SE1_CLKI	E24	MON-GPIO.P_IO2
MSIO56NB2	E22	MON-GPIO.P_IO1
MSIO56PB2	G23	MON-GPIO.P_PRES1
MSIO57NB2	A24	MON-GPIO.P_IO0
MSIO57PB2	A25	MON-GPIO.I2C.SCL
MSIO58NB2	C24	MON-GPIO.I2C.SDA
MSIO58PB2	C25	MON-GPIO.F_IO1
MSI59NB2	D23	SYSEN_N
MSIO60NB2	F22	MON-GPIO.P_PRES0
MSIO60PB2	E22	MON-GPIO.PWR_FAIL_N
MSIO61NB2	G20	BACKPLANE_I2C.SCL
MSIO61PB2	G21	BACKPLANE_I2C.SDA

R187 10k
GND

MON-GPIO.F_IO1 — 2k — R123 — 2k — R140 — P3V3
MON-GPIO.P_IO1
MON-GPIO.P_IO2 — 2k — R139

FMC-FPGA.I2C.SCL — 2k — R199 — 2k — R186 — P3V3
FMC-FPGA.I2C.SDA

MON-GPIO.PWR_FAIL_N — 2k — R28 — P3V3
MON-GPIO.P_PRES0 — 2k — R247 — 2k — R243
MON-GPIO.P_PRES1

MON-GPIO.I2C.SCL — 2k — R150 — 2k — R121 — P3V3
MON-GPIO.I2C.SDA

BACKPLANE_I2C.SCL — 2k — R211 — 2k — R212 — P3V3
BACKPLANE_I2C.SDA

CRT-GPIO.PWRBTN_N — 2k — R188 — 2k — R190 — P3V3 — Mounted: No
CRT-GPIO.PRST_N

This could or could not be used as an I2C bus

Matched Net Lengths [Tolerance = 25mm]
ClassName: MoniMod-I2C-2V5
Parameter Set

MONIMOD-I2C_2V5.SCL — MoniMod_I2C_Translation_SCL Translate_OD_3V3_to_2V5.SchDoc — OD_2V5 / OD_3V3 — MONIMOD-I2C.SCL
MONIMOD-I2C_2V5.SDA — MoniMod_I2C_Translation_SDA Translate_OD_3V3_to_2V5.SchDoc — OD_2V5 / OD_3V3 — MONIMOD-I2C.SDA

Matched Net Lengths [Tolerance = 25mm]
ClassName: PcbVer-I2C-2V5
Parameter Set

PCB_VER-I2C_2V5.SCL — PCB_VER_I2C_Translation_SCL Translate_OD_3V3_to_2V5.SchDoc — OD_2V5 / OD_3V3 — PCB_VER-I2C.SCL
PCB_VER-I2C_2V5.SDA — PCB_VER_I2C_Translation_SDA Translate_OD_3V3_to_2V5.SchDoc — OD_2V5 / OD_3V3 — PCB_VER-I2C.SDA

P2V5
R106 4k7
Voltage_trans Translate_2V5_to_PPERIPH.SchDoc

SERVMOD_DIR
SERVMOD_FPGA[1..8] — SERVMOD_DIR / SERVMOD_FPGA[1..8] — SERVMOD[1..8] — SERVMOD[1..8]
SHARED_BUS_DIR[4..0]
SHARED_BUS_FPGA[4..0] — SHARED_BUS_DIR[4..0] / SHARED_BUS_FPGA[4..0] — SHARED_BUS[4..0] — SHARED_BUS[4..0]

FMC-SIGS
PRSNT
FMC-FPGA — FMC-FPGA
I2C — SCL / SDA — Parameter Set: Matched Net Lengths [Tolerance = 50mm], ClassName: FMC-I2C
LA — FMC-LA — D_N[33..0] / D_P[33..0] — Matched Net Lengths [Tolerance = 2mm], Matched Net Lengths [Tolerance = 20mm], DifferentialPairClassName: FMC_DP

MONIMOD-I2C — MONIMOD-I2C — Parameter Set: Matched Net Lengths [Tolerance = 25mm], ClassName: MoniMod-I2C-3V3
BACKPLANE_I2C — BACKPLANE_I2C — Parameter Set: Matched Net Lengths [Tolerance = 50mm], ClassName: Backplane-I2C

OSC_25MHz — OSC_25MHz
OSC_40MHz — OSC_40MHz
SYSEN_N — SYSEN_N
LEDS[1..4] — LEDS[1..4]
SERVMOD[1..8] — SERVMOD[1..8]
PWR_CYC_REQ[1..0] — PWR_CYC_REQ[1..0]
SHARED_BUS[4..0] — SHARED_BUS[4..0]
BACKPLANE_RST_N — BACKPLANE_RST_N
MM_SHDN_N — MM_SHDN_N

PGOOD_H
• P1V2
• P3V3
• P12V
PGOOD — PGOOD

I2C — SCL / SDA — Parameter Set: Matched Net Lengths [Tolerance = 50mm], ClassName: Mon-I2C
MON-GPIO — I2C — P_RST_N / P_IO0 / P_IO1 / P_IO2 / F_RST_N / F_IO0 / F_IO1 / PWR_FAIL_N / P_PRES0 / P_PRES1 — MON-GPIO
Parameter Set: Matched Net Lengths [Tolerance = 50mm], ClassName: Mon-P_SWD
Parameter Set: Matched Net Lengths [Tolerance = 50mm], ClassName: Mon-F_SWD
50mm = 3.5% UI @100MHz (stripline, FR-4)
CRT-GPIO — PRST_N / PWRBTN_N — CRT-GPIO
Parameter Set: Matched Net Lengths [Tolerance = 50mm], ClassName: FrontPanel-PossiblyI2C
Parameter Set: Matched Net Lengths [Tolerance = 25mm], ClassName: PcbVer-I2C-3V3 — PCB_VER-I2C

SPI Flash

SPI
• SS_N
• SCLK
• MOSI
• MISO
USER_FLASH — Parameter Set: Matched Net Lengths [Tolerance = 20mm], ClassName: User_Flash

IC27
USER_FLASH.SS_N — CS
USER_FLASH.SCLK — SCK
USER_FLASH.MOSI — SI
USER_FLASH.MISO — SO
P2V5 — WP / HOLD — VCC / GND
C116 100nF
GND
AT25DN512C-SSHF-B

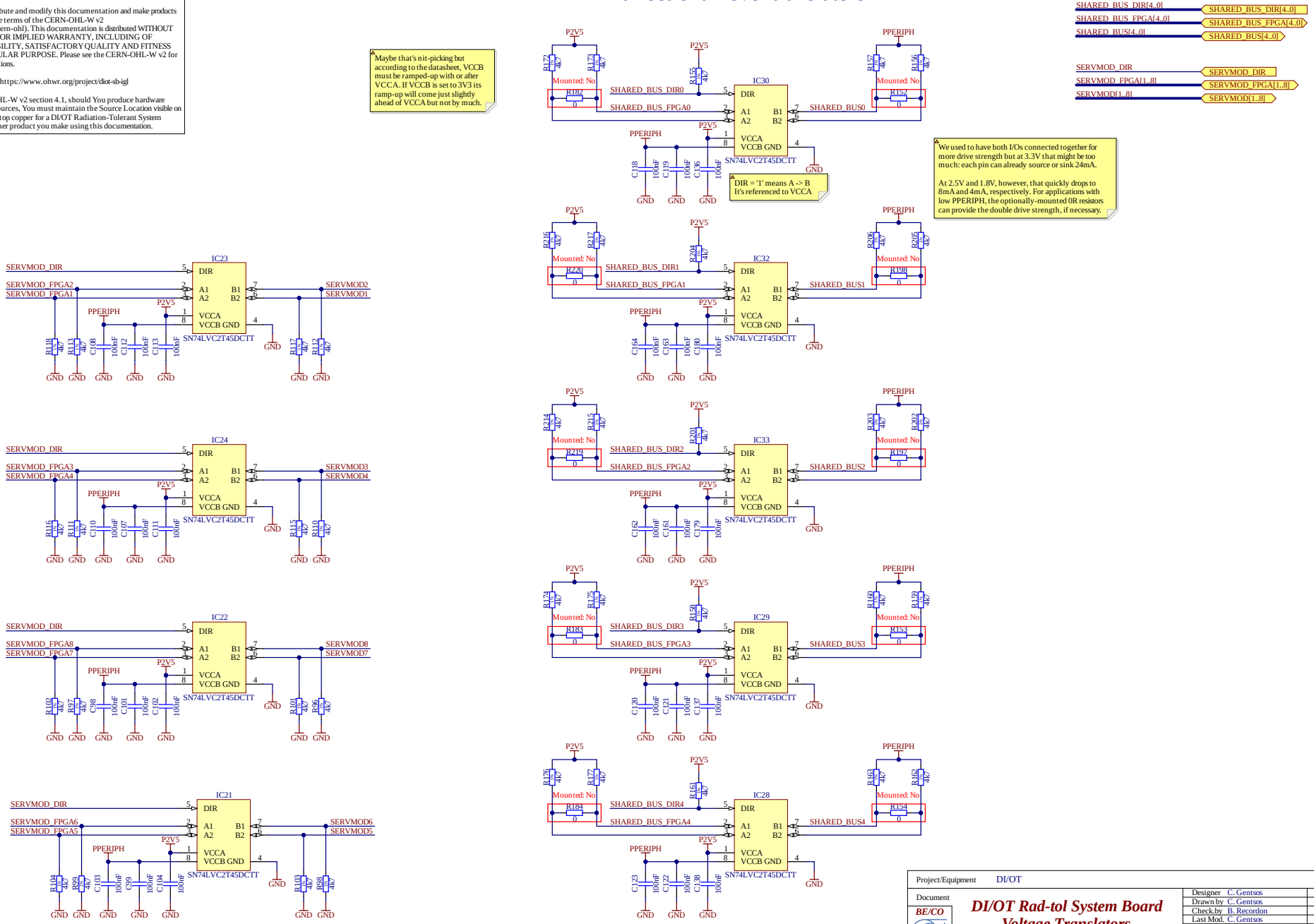
Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA I/O Banks B1, B2	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	5/1/2021
		File FPGA_Banks_1_2.SchDoc	
		Print Date 5/10/2021 2:42:28 PM	Sheet 7 of 17
European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3	Rev *

Bi-directional level translators

Maybe that's nit-picking but according to the datasheet, VCCB must be ramped-up with or after VCCA. If VCCB is set to 3V3 its ramp-up will come just slightly ahead of VCCA but not by much.

We used to have both I/Os connected together for more drive strength but at 3.3V that might be too much: each pin can already source or sink 24mA.

At 2.5V and 1.8V, however, that quickly drops to 8mA and 4mA, respectively. For applications with low PPERIPH, the optionally-mounted 0R resistors can provide the double drive strength, if necessary.



Project/Equipment	DI/OT
Document	DI/OT Rad-tol System Board Voltage Translators
Designer	C. Gentsos
Drawn by	C. Gentsos 16/09/2020
Check.by	B. Recordon 24/11/2020
Last Mod.	C. Gentsos 4/21/2021
File	Translate_2V5_to_PPERIPH.SchDoc
Print Date	5/10/2021 2:42:28 PM
Sheet	8 of 17
Size	A3
Rev	*

BE/CO

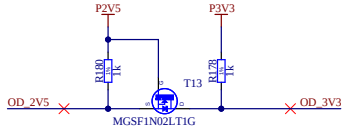
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-04326-V1-0

Level translators for open-drain interfaces as described in AN10441

OD_2V5 — OD_2V5

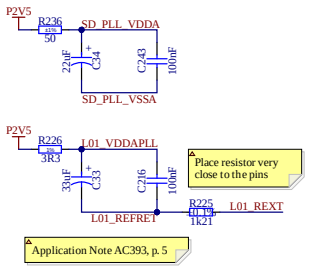
OD_3V3 — OD_3V3

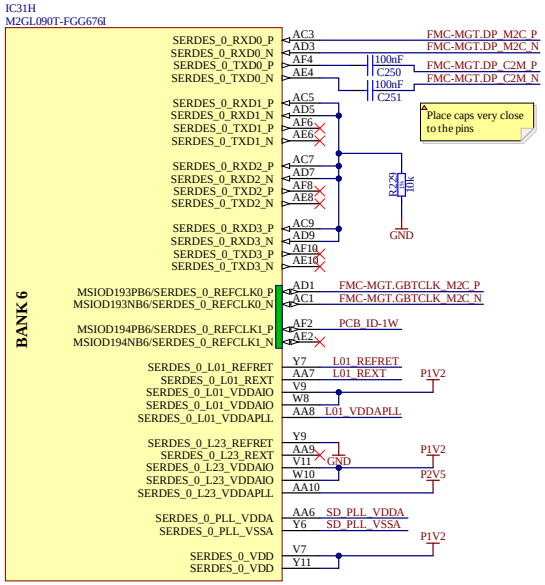


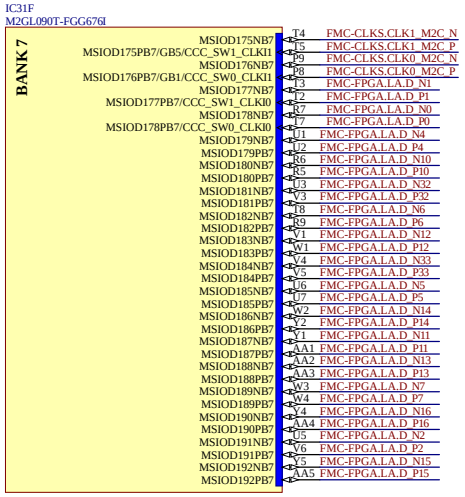
Project/Equipment	DI/OT	
Document	DI/OT Rad-tol System Board Open-drain Voltage Translators	
Designer	C. Gentsos	
Drawn by	C. Gentsos	06/10/2020
Check.by	B. Recordon	24/11/2020
Last Mod.	C. Gentsos	4/2/2021
File	Translate_OD_3V3_to_2V5.SchDoc	
Print Date	5/10/2021 2:42:28 PM	Sheet 9 of 17
European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3, Rev *

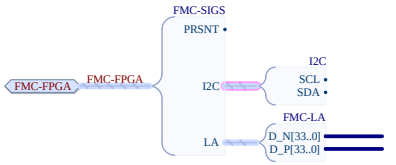
Banks powered by 2.5V

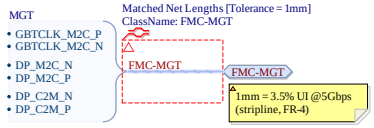
SerDes PLL RC filters

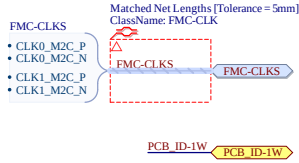








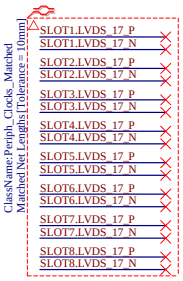


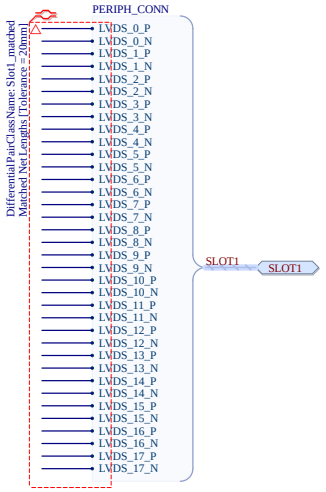


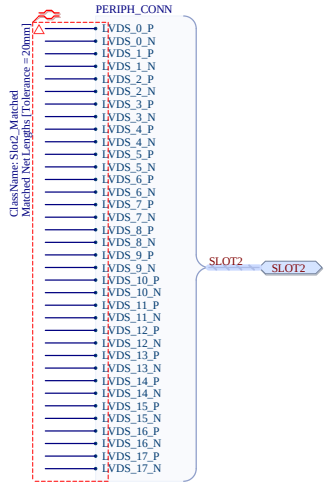
Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA I/O Banks B6, B7	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/20/2021
		File FPGA_Banks_6_7.SchDoc	
		Print Date 5/10/2021 2:42:28 PM	Sheet 10 of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3	Rev *

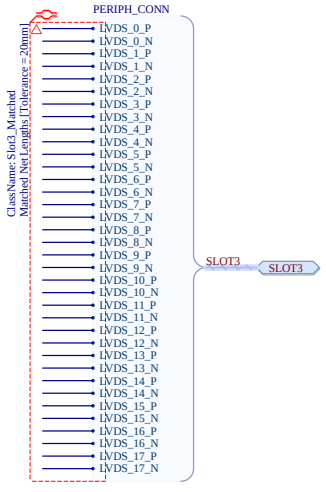
The diff. pairs that go to each peripheral board are length-matched, excluding the clock-capable pair

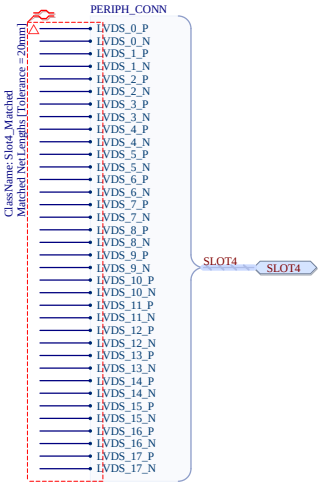
The clock-capable pairs are length-matched between the different peripheral boards, instead

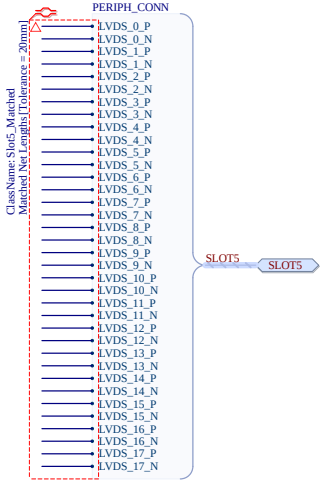


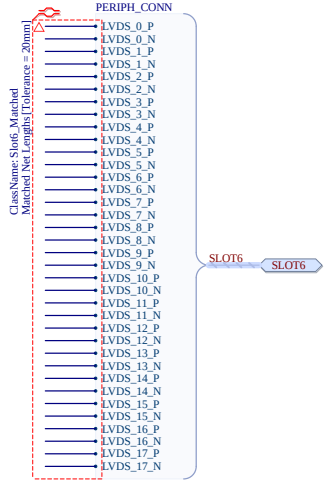


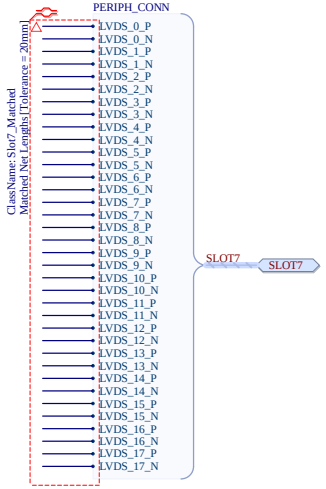


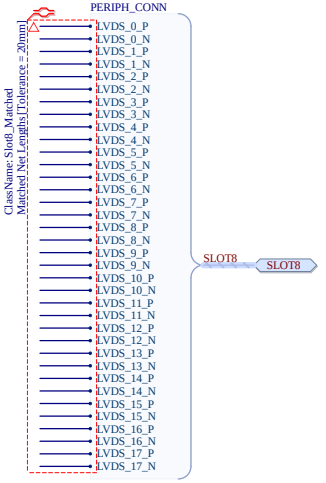




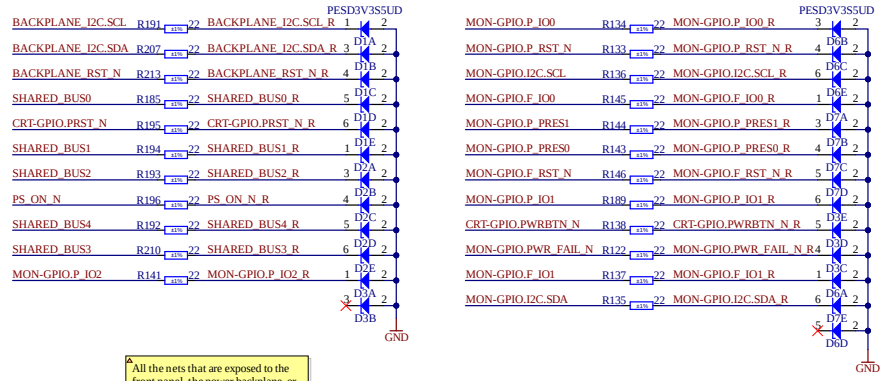


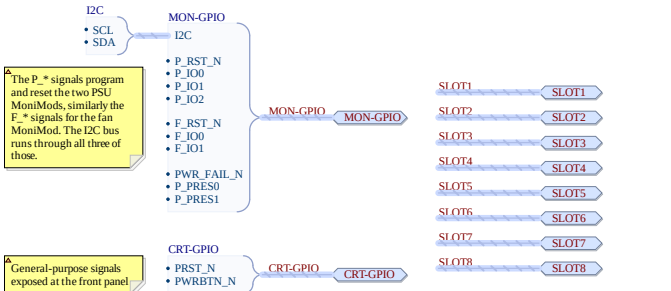






Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board Constrain Periph. Board Signals**	Designer C. Gentsos	
		Drawn by C. Gentsos	09/10/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/21/2021
		File Constrain_Periph_Nets.SchDoc	
		Print Date 5/10/2021 2:42:28 PM	Sheet 11 of 17
BE/CO	*European Organization for Nuclear Research* *CH-1211 Genève 23 - Switzerland*	EDA-04326-V1-0	Size A3 Rev *

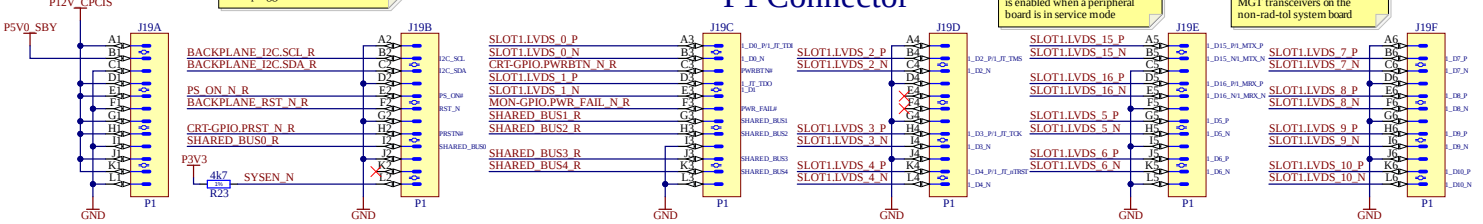




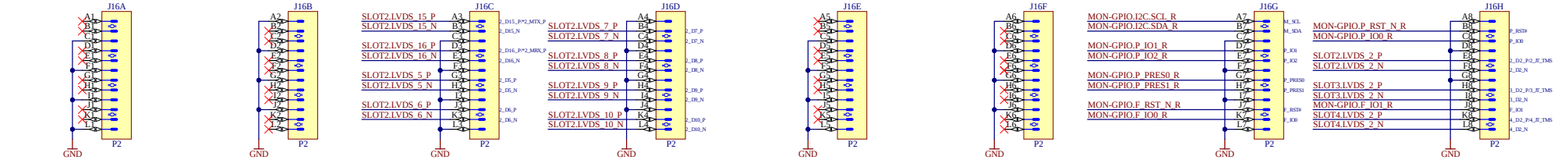
All the nets that are exposed to the front panel, the power backplane, or that run through all the peripheral boards, are protected

Backplane grounds L2 at the system slot, leaves it open at the peripheral slots. Sensing that we can tell where we're plugged in.

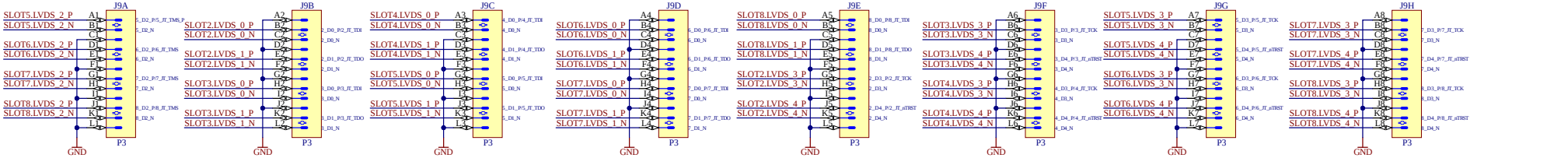
P1 Connector



P2 Connector



P3 Connector

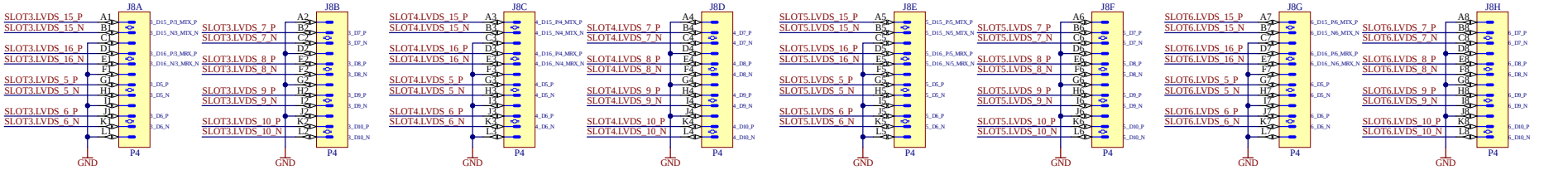


Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board CPCI-S Backplane (1/2)**	Designer C. Gentsos	
BE/CO		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/23/2021
		File CPCI-S_Backplane_P1-P3.SchDoc	
		Print Date 5/10/2021 2:42:28 PM	Sheet 12 of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3	Rev *

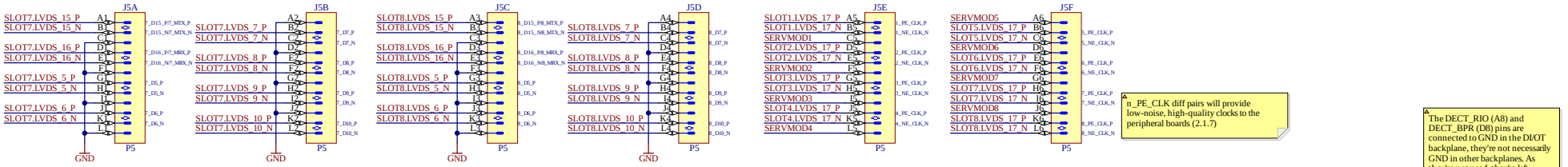
SLOT1 SLOT2 SLOT3 SLOT4 SLOT5 SLOT6 SLOT7 SLOT8

SERVMOD[1..8]

P4 Connector



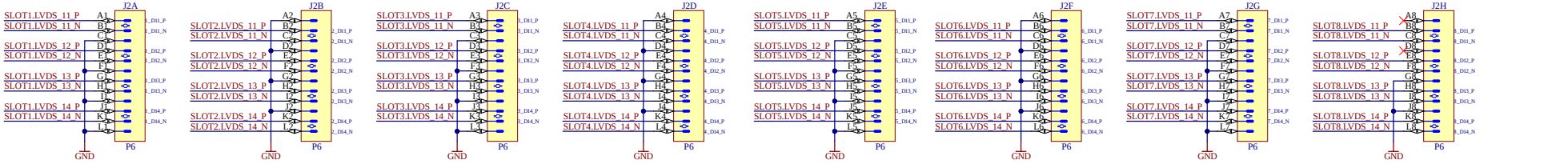
P5 Connector



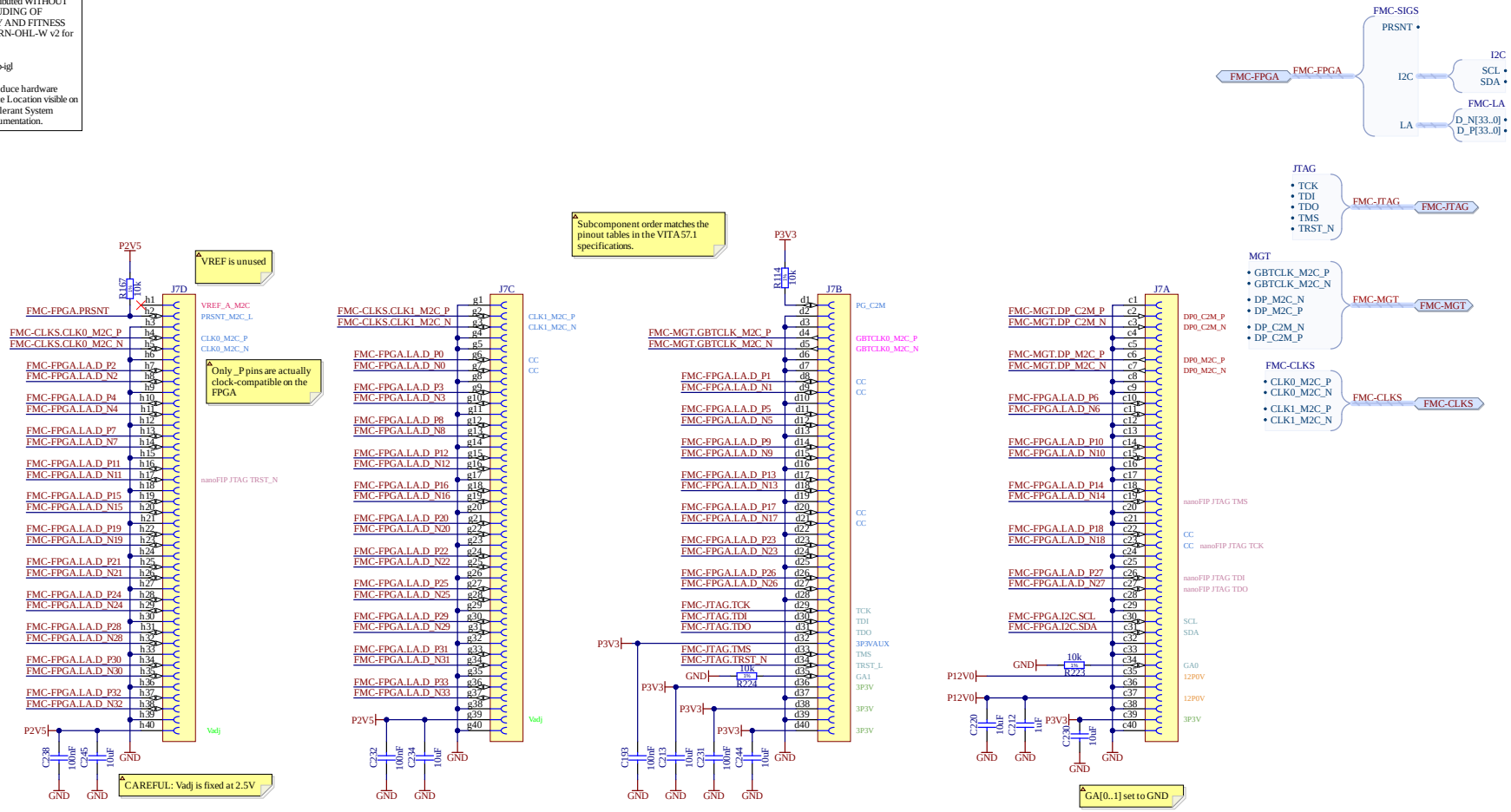
n_PE_CLK diff pairs will provide low-noise, high-quality clocks to the peripheral boards (2.1.7)

The DECT_RIO (A8) and DECT_BPR (D8) pins are connected to GND in the DI/OT backplane, they're not necessarily GND in other backplanes. As they're not used, they're left unconnected to improve compatibility.

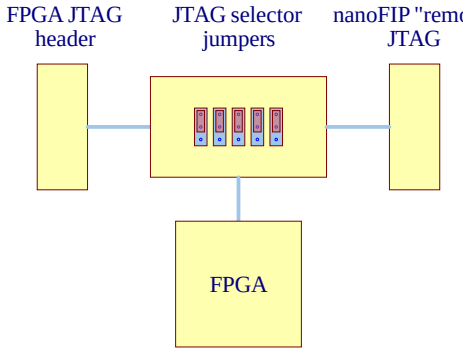
P6 Connector

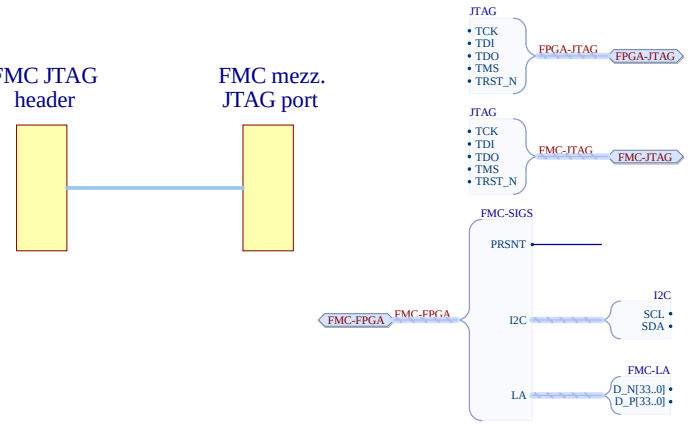


Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board CPCI-S Backplane (2/2)**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/2/2021
		File CPCI-S_Backplane_P4-P6.SchDoc	
		Print Date 5/10/2021 2:42:28 PM	Sheet 13 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3 Rev *

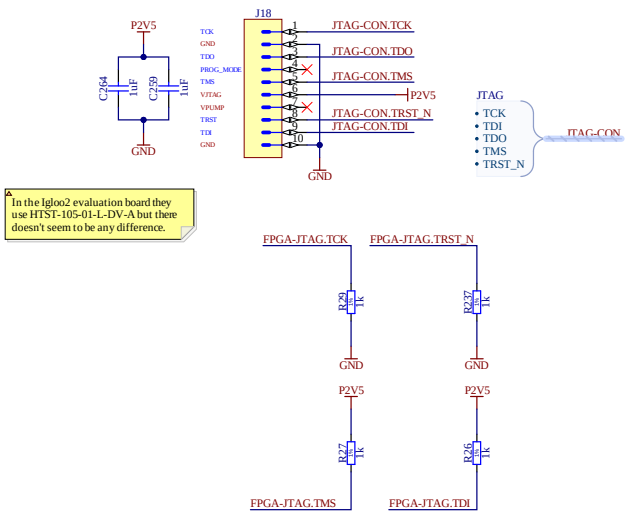


Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FMC	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/2/2021
		File FMC.SchDoc	
		Print Date 5/10/2021 2:42:29 PM	Sheet 14 of 17
BE/CO	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3, Rev *

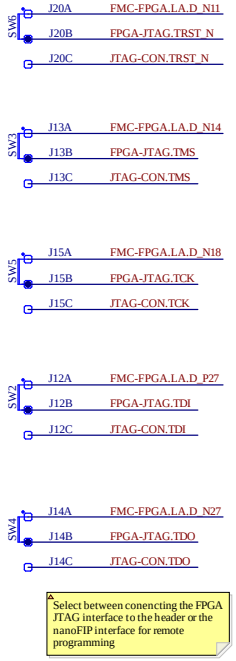




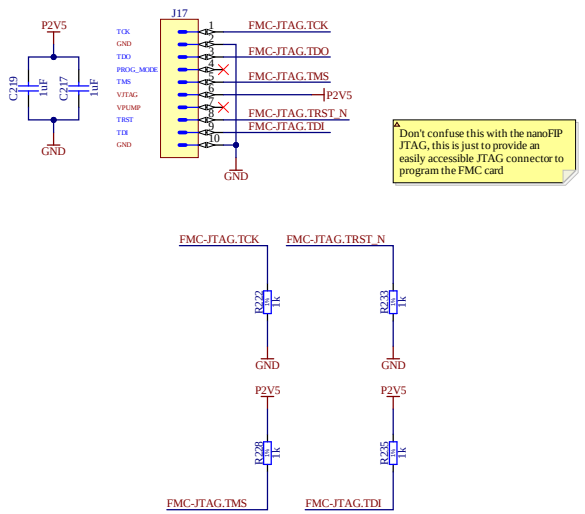
FPGA JTAG header



FPGA JTAG selector



FMC JTAG header



Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board JTAG Chains	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/2/2021
		File JTAG.SchDoc	
		Print Date 5/10/2021 2:42:29 PM	Sheet 15 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3 Rev *

SENSE
- P12V0+
- P12V0-

SENSE

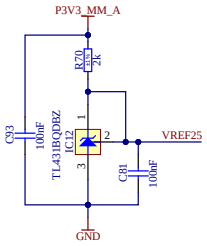
MONIMOD-I2C

TEMP_LDO

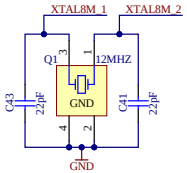
TEMP_FPGA

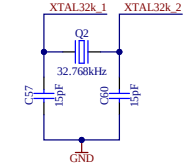
TEMP_AMB

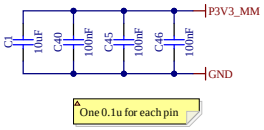
Voltage reference

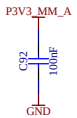


XTALs

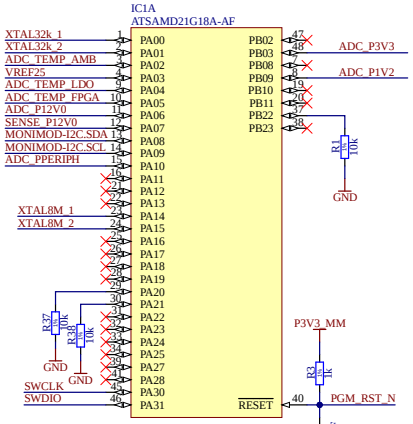


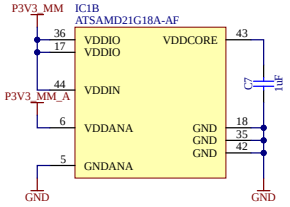


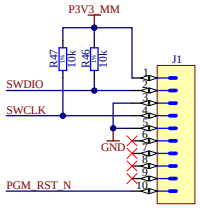




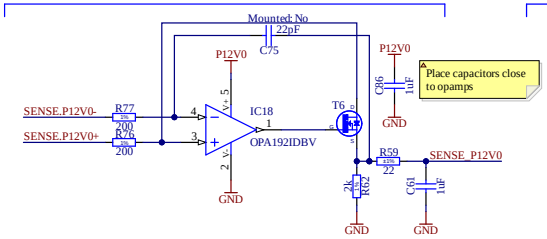
uC running MoniMod FW





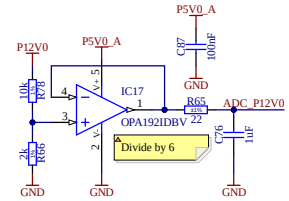


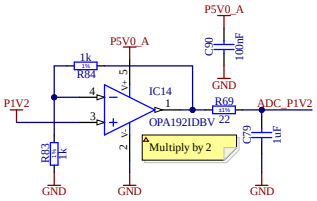
Current sense

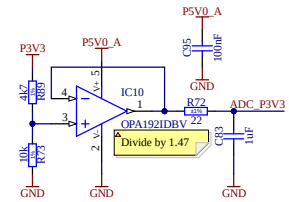


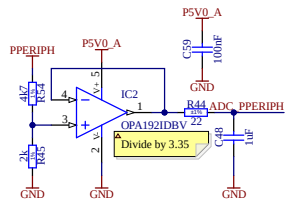
About P2V5 we only care when it's used as PPERIPH so its being omitted as a separate channel is fine

Voltage div. and buffers

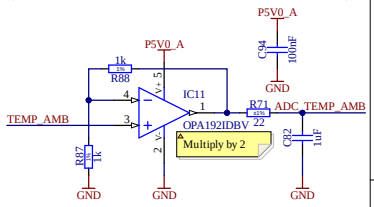


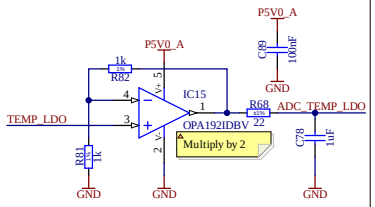


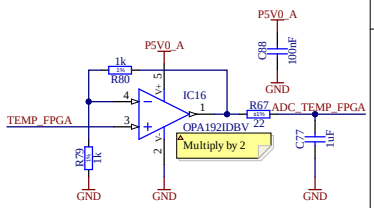




Temp. sensor amps

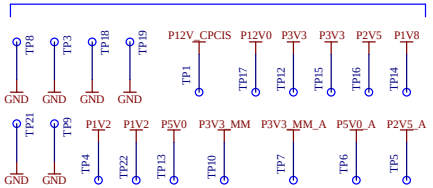




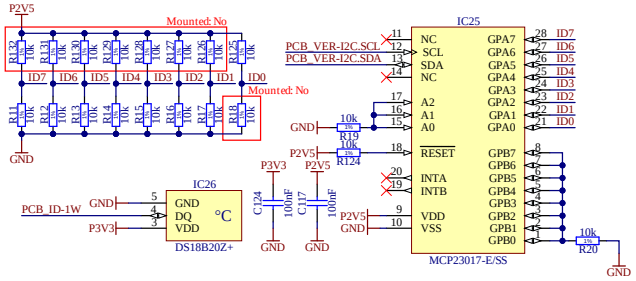


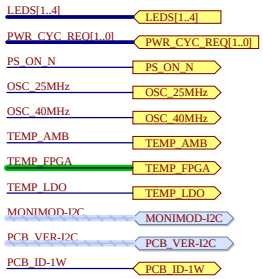
Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board Monitoring**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/14/2021
		File Monitoring.SchDoc	
		Print Date 5/10/2021 2:42:29 PM	Sheet 16of 17
BE/CO	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3 / Rev *

Power rail test points

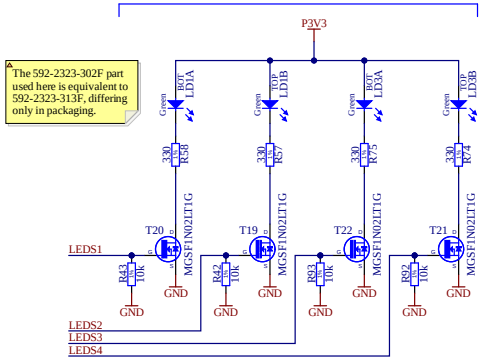


Board version encoding and ID

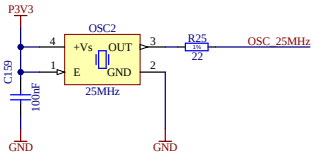




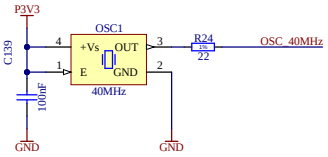
User LEDs



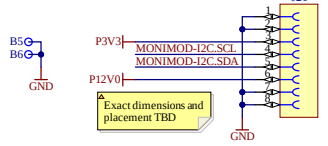
25MHz oscillator



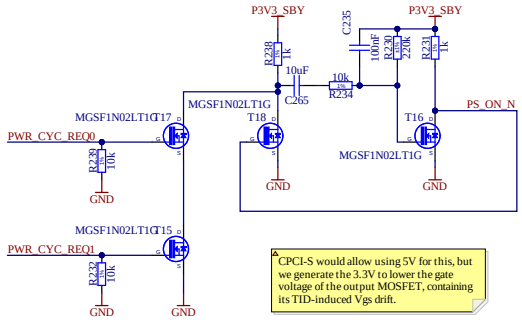
40MHz oscillator



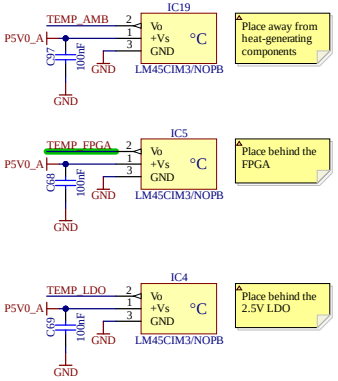
Expansion pin header



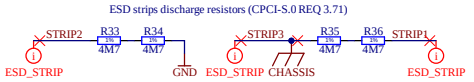
Power cycle pulse generator



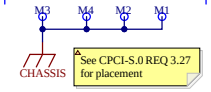
Temp sensors



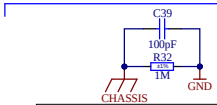
ESD Protection



Front panel mounting holes



Chassis-GND connection



Fiducials

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Miscellaneous	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by B. Recordon	24/11/2020
		Last Mod. C. Gentsos	4/2/2021
		File Top_Misc.SchDoc	
		Print Date 5/10/2021 2:42:29 PM	Sheet 17 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-04326-V1-0	Size A3 Rev *