

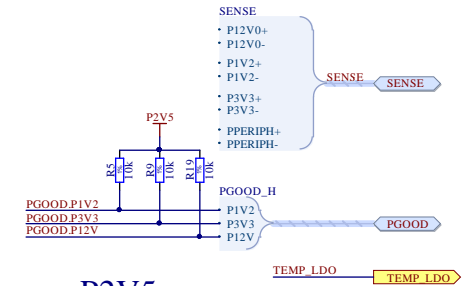
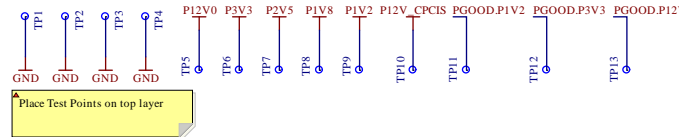
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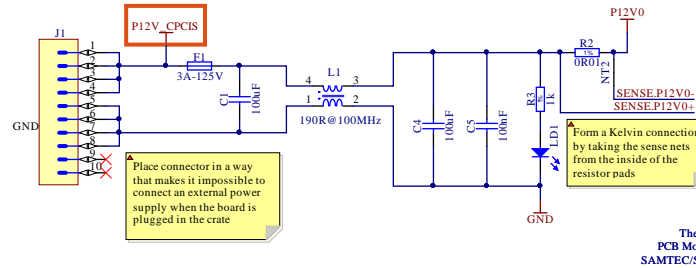
Source location: <https://www.hwr.org/project/diot-sb-ig1>

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Test points

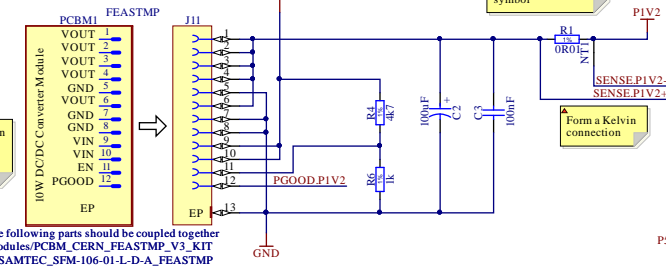


12V0 power cleanup

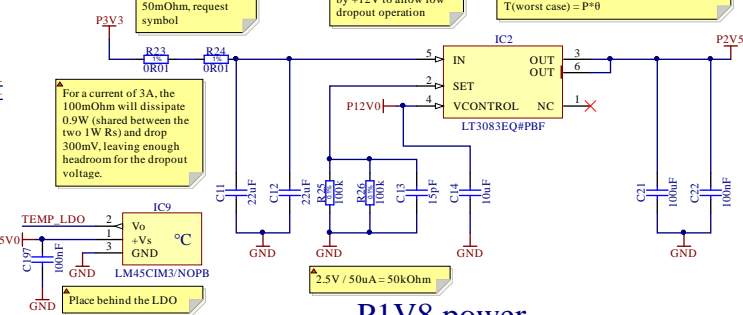


The following parts should be coupled together
PCB Modules/PCBM_CERN_FEASTMP_V3_KIT
SAMTEC/SAMTEC_SFMM-106-01-L-D-A_FEASTMP

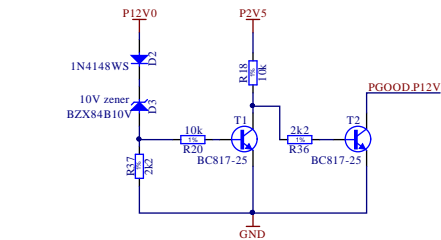
P1V2 power



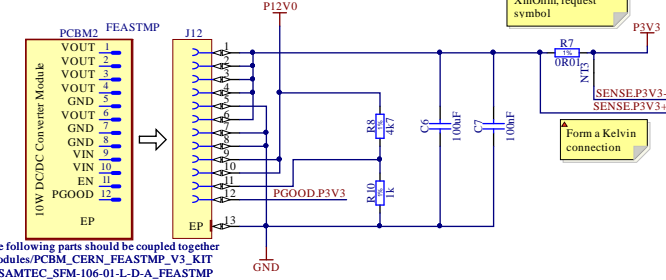
P2V5 power



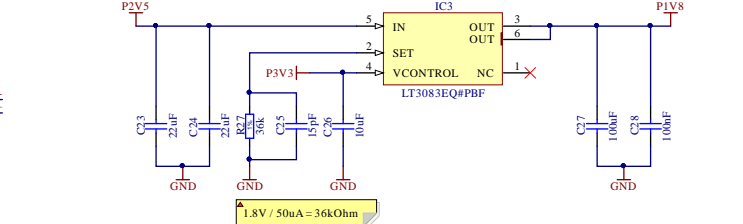
12V brownout detection



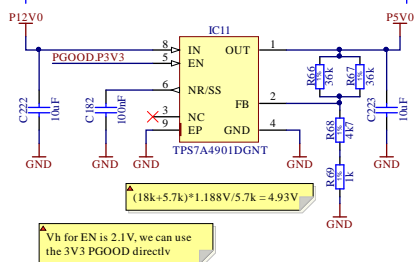
P3V3 power



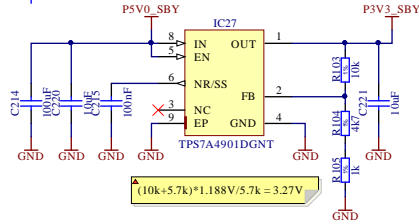
P1V8 power



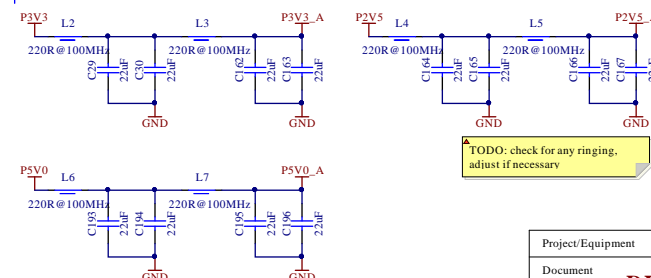
P5V0 power



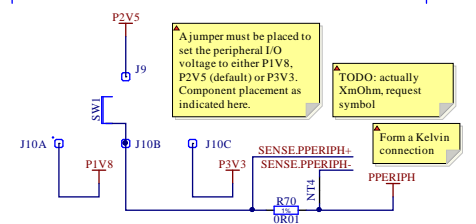
Always-on P3V3 power



Analog power filtering



Peripheral voltage selection

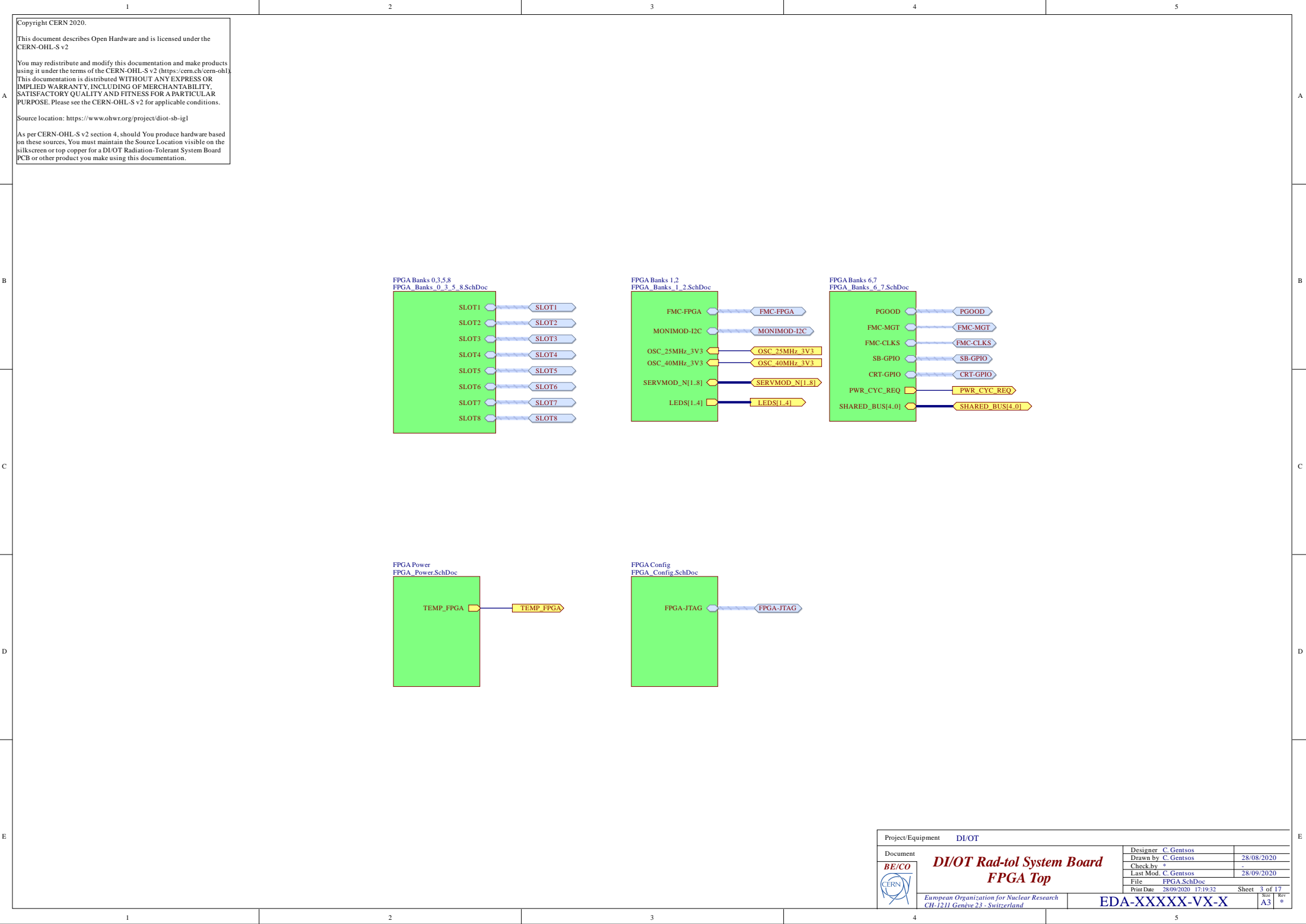


Project/Equipment	DIOT	Designer	C. Gentsos	28/08/2020
Document	BE/CO	Drawn by	C. Gentsos	28/08/2020
		Check by	*	28/09/2020
		Last Mod.	C. Gentsos	28/09/2020
		File	Powering_SchDoc	
		Print Date	28/09/2020 17:19:31	Sheet 2 of 17
				A3

**DIOT Rad-tol System Board
Power**

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EDA-XXXXX-VX-X



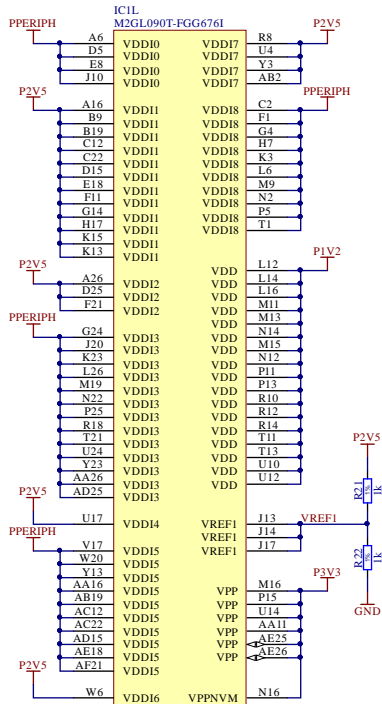
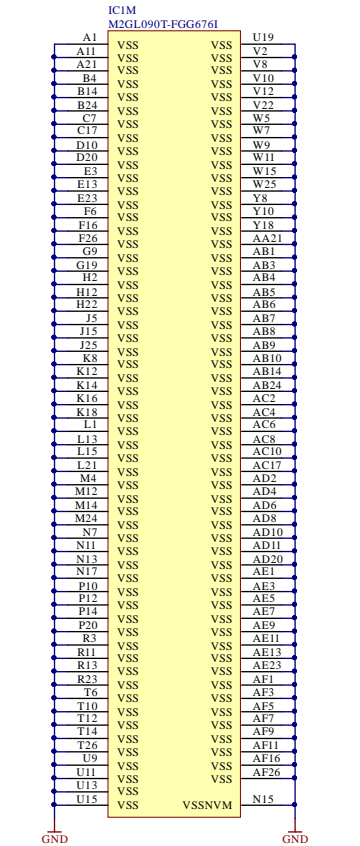
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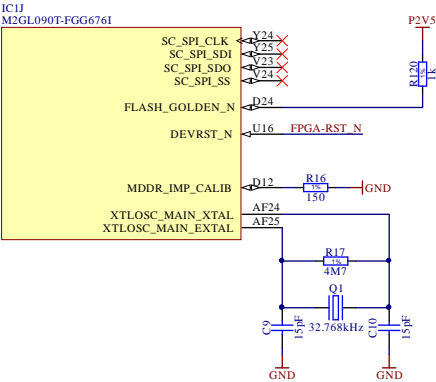
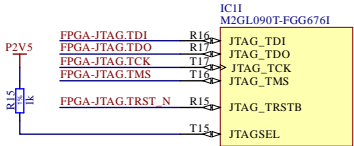
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Parts powered by 2.5V

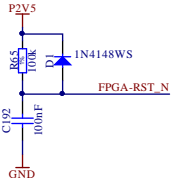


The JTAG and configuration pins are referred to as Bank 4



TODO: calibration not required so 0R may be acceptable, to be clarified.

This is to trigger a reprogram from the flash, assuming that



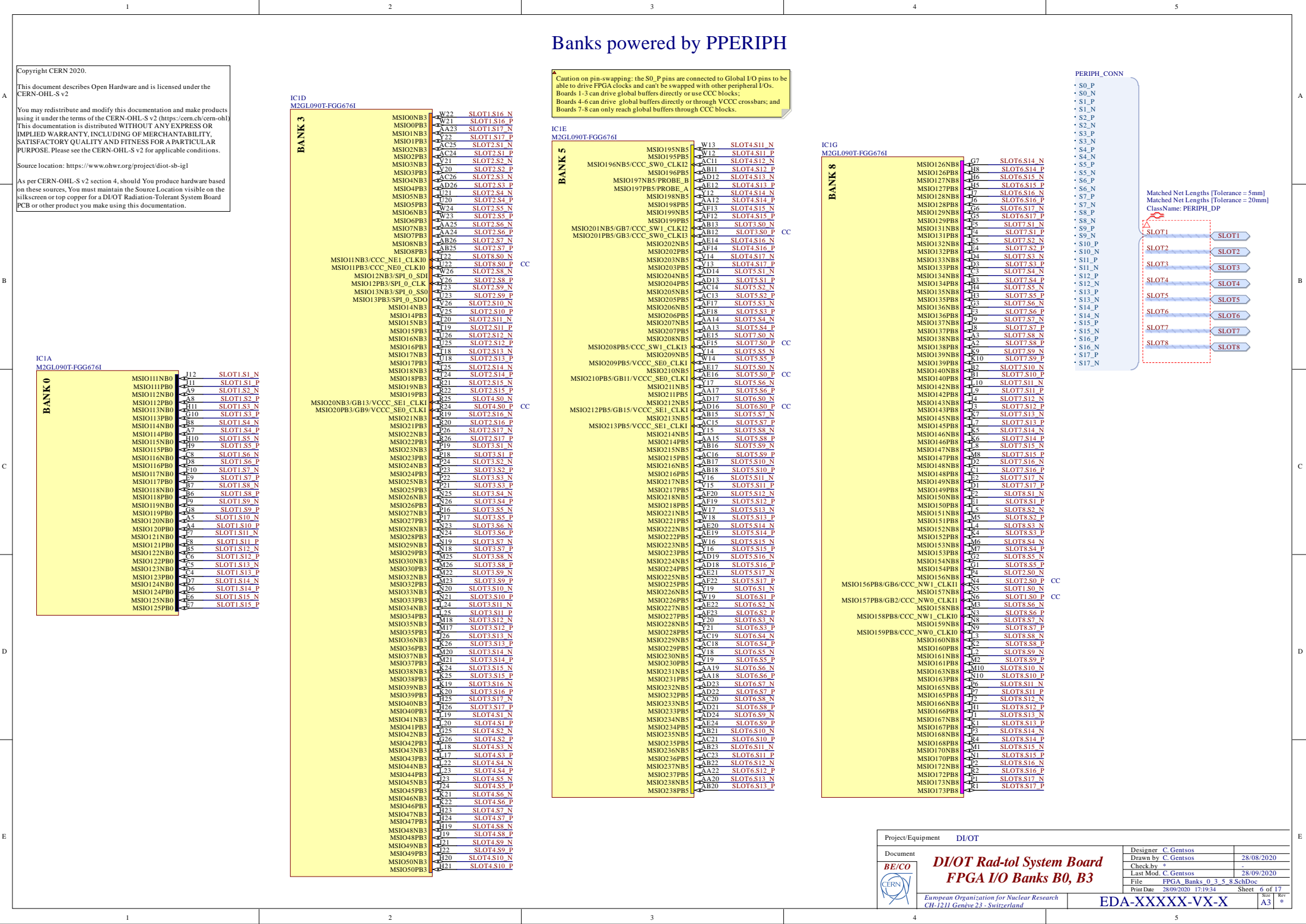
Project/Equipment		DI/OT	
Document		Designer C. Gentsos	
		Drawn by C. Gentsos	
		Check by *	
		Last Mod. C. Gentsos	
		File FPGA_Config.SchDoc	
		Print Date 28/09/2020 17:19:34	
		Sheet 5 of 17	
		Size A3	
		Rev *	

BE/CO

DI/OT Rad-tol System Board
FPGA Configuration

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-XXXXX-VX-X



Banks powered by 2.5V

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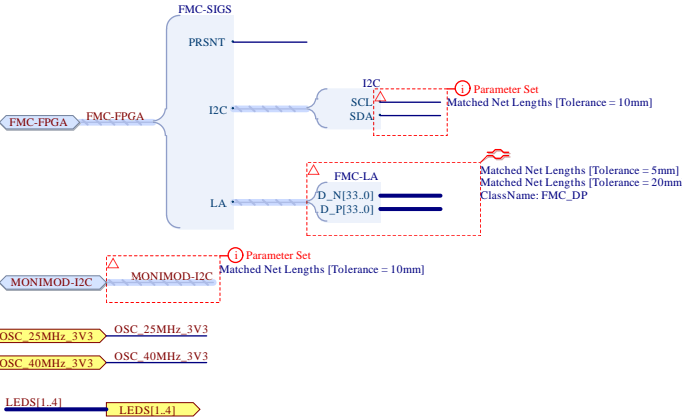
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Careful with pin swapping: the P nets of the differential pairs 0, 1, 17 and 18 are connected to clock-capable pins and can't be swapped with the other I/Os.

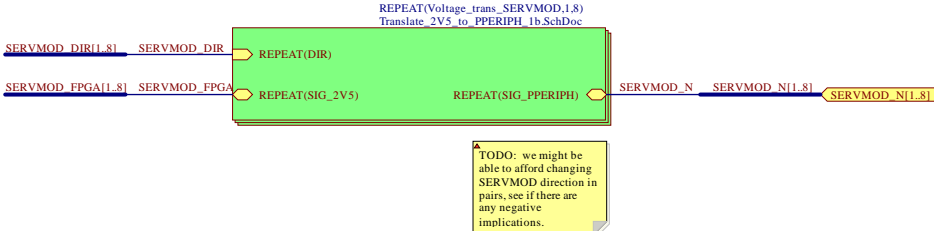
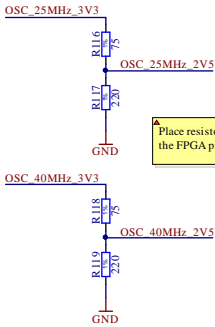
IC1B
M2GL090T-FGG6761

BANK 1		
DDRIO62NB1/MDDR_ADDR15	C23	FMC-FPGA.L.A.D_N14
DDRIO62PB1/MDDR_ADDR14	C22	FMC-FPGA.L.A.D_P14
DDRIO63NB1/MDDR_ADDR15	C23	FMC-FPGA.L.A.D_N15
DDRIO63PB1/MDDR_ADDR12	C23	FMC-FPGA.L.A.D_P15
DDRIO64NB1/MDDR_ADDR11	C21	FMC-FPGA.L.A.D_N2
DDRIO64PB1/MDDR_ADDR10	C20	FMC-FPGA.L.A.D_N3
DDRIO65NB1/MDDR_ADDR9	C20	FMC-FPGA.L.A.D_P3
DDRIO65PB1/MDDR_ADDR8	C22	FMC-FPGA.L.A.D_N4
DDRIO66NB1/MDDR_ADDR7	C22	FMC-FPGA.L.A.D_P4
DDRIO67NB1/MDDR_ADDR6	C18	FMC-FPGA.L.A.D_N5
DDRIO67PB1/MDDR_ADDR5	C18	FMC-FPGA.L.A.D_P5
DDRIO68NB1/MDDR_ADDR4	C21	FMC-FPGA.L.A.D_N6
DDRIO68PB1/MDDR_ADDR3	C21	FMC-FPGA.L.A.D_P6
DDRIO69NB1/MDDR_ADDR2	C19	FMC-FPGA.L.A.D_N7
DDRIO69PB1/MDDR_ADDR1	C19	FMC-FPGA.L.A.D_P7
DDRIO70NB1/MDDR_ADDR0	C18	FMC-FPGA.L.A.D_N8
DDRIO70PB1/MDDR_BA2	C17	FMC-FPGA.L.A.D_P8
DDRIO71NB1/MDDR_BA1	C20	FMC-FPGA.L.A.D_N9
DDRIO71PB1/MDDR_BA0	C20	FMC-FPGA.L.A.D_P9
DDRIO72NB1/MDDR_CLK_N	C20	FMC-FPGA.L.A.D_N10
DDRIO72PB1/MDDR_CLK_N	C19	FMC-FPGA.L.A.D_P10
DDRIO73NB1/MDDR_CAS_N	C19	FMC-FPGA.L.A.D_N11
DDRIO73PB1/MDDR_RESET_N	C18	FMC-FPGA.L.A.D_P11
DDRIO74NB1/MDDR_CS_N	C17	FMC-FPGA.L.A.D_N12
DDRIO74PB1/MDDR_CKE	C16	FMC-FPGA.L.A.D_P12
DDRIO75NB1/MDDR_WE_N	C16	FMC-FPGA.L.A.D_N13
DDRIO75PB1/MDDR_RAS_N	C16	FMC-FPGA.L.A.D_P13
DDRIO76NB1/MDDR_DQ15	C19	FMC-FPGA.L.A.D_N1
DDRIO76PB1/CCC_NE1_CLK13/MDDR_DQ14	C18	FMC-FPGA.L.A.D_P1
DDRIO77NB1/MDDR_DQ13	C18	FMC-FPGA.L.A.D_N12
DDRIO77PB1/MDDR_DQ12/GB12/CCC_NE1_CLK12	C15	FMC-FPGA.L.A.D_P0
DDRIO78NB1/MDDR_DM_RDQS1	C16	FMC-FPGA.L.A.D_N16
DDRIO78PB1/MDDR_TMATCH_0_IN	C17	FMC-FPGA.L.A.D_P16
DDRIO79NB1/MDDR_DQS1_N	C17	FMC-FPGA.L.A.D_N17
DDRIO79PB1/MDDR_DQS1/GB8/CCC_NE0_CLK13	C17	FMC-FPGA.L.A.D_P17
DDRIO80NB1/MDDR_DQ11	C16	FMC-FPGA.L.A.D_N18
DDRIO80PB1/MDDR_DQ10/CCC_NE0_CLK12	C16	FMC-FPGA.L.A.D_P18
DDRIO81NB1/MDDR_DQ9	C16	FMC-FPGA.L.A.D_N19
DDRIO81PB1/MDDR_DQ8	C15	FMC-FPGA.L.A.D_P19
DDRIO82NB1/MDDR_TMATCH_0_OUT	C15	FMC-FPGA.L.A.D_N20
DDRIO82PB1/MDDR_DQ7	C15	FMC-FPGA.L.A.D_P20
DDRIO83NB1/MDDR_DQ6	C16	FMC-FPGA.L.A.D_N21
DDRIO83PB1/MDDR_DQ5	C15	FMC-FPGA.L.A.D_P21
DDRIO84NB1/MDDR_DQ4	C15	FMC-FPGA.L.A.D_N22
DDRIO84PB1/MDDR_DM_RDQS0	C14	FMC-FPGA.L.A.D_P22
DDRIO85NB1/MDDR_DQS0_N	C15	FMC-FPGA.L.A.D_N23
DDRIO85PB1/MDDR_DQS0	C14	FMC-FPGA.L.A.D_P23
DDRIO86NB1/MDDR_DQ3	C14	FMC-FPGA.L.A.D_N24
DDRIO86PB1/MDDR_DQ2	C15	FMC-FPGA.L.A.D_P24
DDRIO87NB1/MDDR_DQ1	C15	FMC-FPGA.L.A.D_N25
DDRIO87PB1/MDDR_DQ0	C14	FMC-FPGA.L.A.D_P25
DDRIO88NB1	C13	FMC-FPGA.L.A.D_N26
DDRIO88PB1/CCC_NW1_CLK13	C13	FMC-FPGA.L.A.D_P26
DDRIO89NB1/MDDR_DQ_ECC0	C13	FMC-FPGA.L.A.D_N27
DDRIO89PB1/MDDR_DQ_ECC1	C13	FMC-FPGA.L.A.D_P27
DDRIO90NB1/MDDR_DM_RDQS_ECC	C13	FMC-FPGA.L.A.D_N28
DDRIO90PB1/MDDR_TMATCH_ECC_IN	C12	FMC-FPGA.L.A.D_P28
DDRIO91NB1/MDDR_DQS_ECC_N	C12	FMC-FPGA.L.A.D_N29
DDRIO91PB1/MDDR_DQS_ECC	C12	FMC-FPGA.L.A.D_P29
DDRIO92NB1/GB4/CCC_NW1_CLK12	C12	FMC-FPGA.L.A.D_N30
DDRIO92PB1/GB0/CCC_NW0_CLK13	C12	FMC-FPGA.L.A.D_P30
DDRIO93NB1/CCC_NW0_CLK12	C13	FMC-FPGA.L.A.D_N31
DDRIO93PB1/MDDR_TMATCH_ECC_OUT	C14	FMC-FPGA.L.A.D_P31
DDRIO94PB1	C11	FMC-FPGA.L.A.D_N32
DDRIO95NB1	C11	FMC-FPGA.L.A.D_P32
DDRIO95PB1	C11	FMC-FPGA.L.A.D_N33
DDRIO96NB1	C10	FMC-FPGA.L.A.D_P33
DDRIO96PB1	C10	FMC-FPGA.L.A.D_N34
DDRIO97NB1	C12	SERVMOD_DIR1
DDRIO97PB1	C11	SERVMOD_DIR2
DDRIO98NB1	C9	SERVMOD_DIR3
DDRIO98PB1	C10	SERVMOD_DIR4
DDRIO99NB1	C10	SERVMOD_DIR5
DDRIO99PB1	C9	SERVMOD_DIR6



IC1C
M2GL090T-FGG6761

BANK 2		
MSIO51NB2	F25	SERVMOD_DIR7
MSIO51PB2	F26	SERVMOD_DIR8
MSIO52NB2	F26	OSC_25MHz_2V5
MSIO52PB2/CCC_NE0_CLK11	F25	OSC_40MHz_2V5
MSIO53PB2/CCC_NE1_CLK11	F26	OSC_40MHz_2V5
MSIO54NB2	F24	LED51
MSIO54PB2/GB10/VCCC_SE0_CLK1	F25	LED52
MSIO55NB2	F24	LED53
MSIO55PB2/GB14/VCCC_SE1_CLK1	F24	LED54
MSIO56NB2	G23	SERVMOD_FPGA1
MSIO56PB2	G23	SERVMOD_FPGA2
MSIO57NB2	G24	SERVMOD_FPGA3
MSIO57PB2	G25	SERVMOD_FPGA4
MSIO58NB2	G24	SERVMOD_FPGA5
MSIO58PB2	G25	SERVMOD_FPGA6
MSIO59NB2	G23	FMC-FPGA.PRSNT
MSIO60NB2	F22	SERVMOD_FPGA7
MSIO60PB2	F22	SERVMOD_FPGA8
MSIO61NB2	G20	MONIMOD-I2C.SCL
MSIO61PB2	G21	MONIMOD-I2C.SDA



TOD0: we might be able to afford changing SERVMOD direction in pairs, see if there are any negative implications.

Project/Equipment		DI/OT	
Document		Designer C. Gentsos	
BE/CO		Drawn by C. Gentsos	
CERN		Check by *	
DI/OT Rad-tol System Board		Last Mod. C. Gentsos	
FPGA I/O Banks B1, B2		File FPGA_Banks_1_2.SchDoc	
European Organization for Nuclear Research		Print Date 28/09/2020 17:19:35	
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EDA-XXXXX-VX-X		A3	

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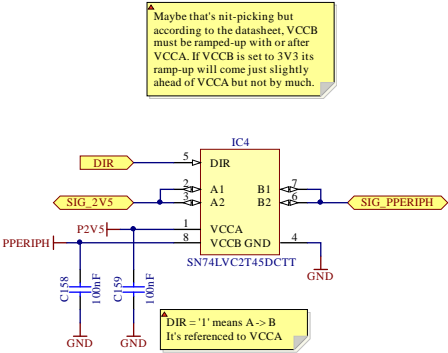
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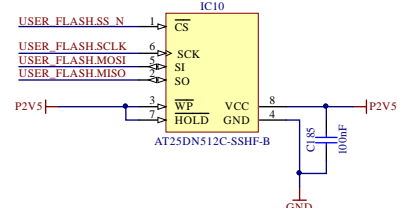
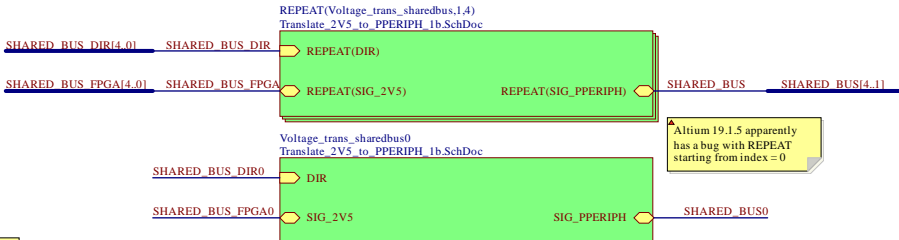
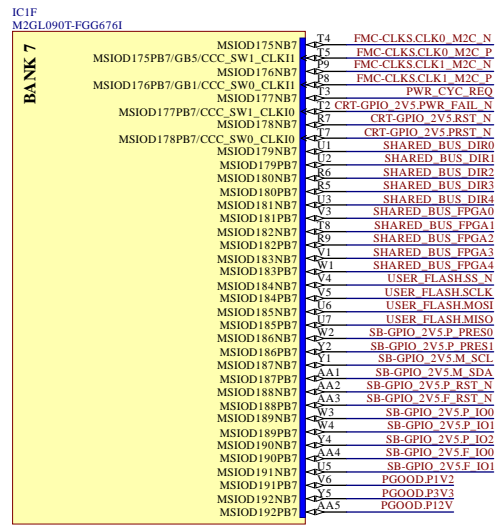
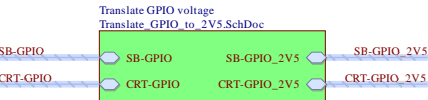
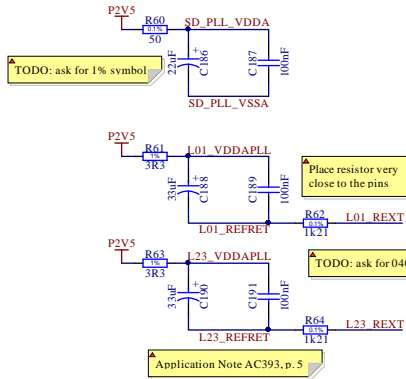
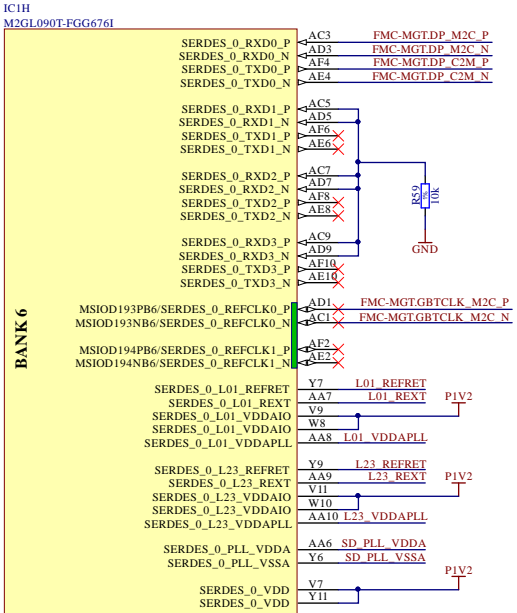
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Banks powered by 2.5V



Project/Equipment		DI/OT	
Document		Designer	C. Gentsos
		Drawn by	C. Gentsos
		Check by	*
		Last Mod.	C. Gentsos
		File	FPGA_Banks_6_7.SchDoc
		Print Date	28/09/2020 17:19:36
		Sheet	9 of 17
		Size	A3
		Rev	*

BE/CO

DI/OT Rad-tol System Board
FPGA I/O Banks B6, B7

European Organization for Nuclear Research
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EDA-XXXXX-VX-X

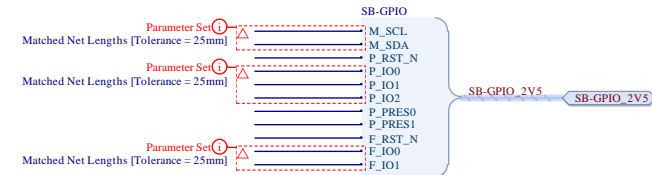
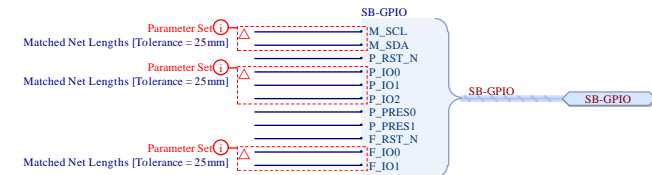
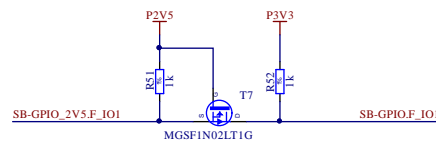
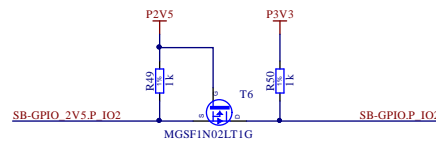
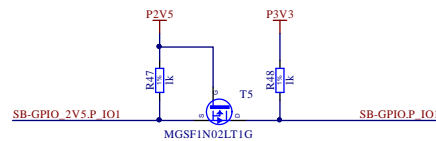
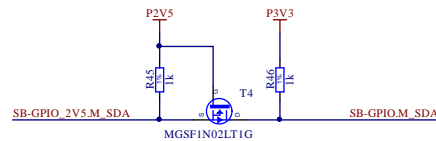
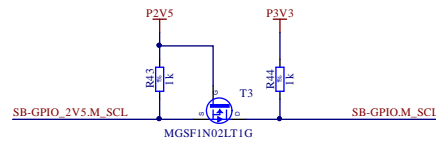
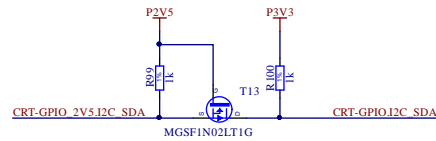
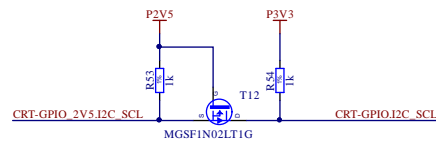
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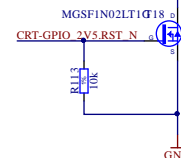
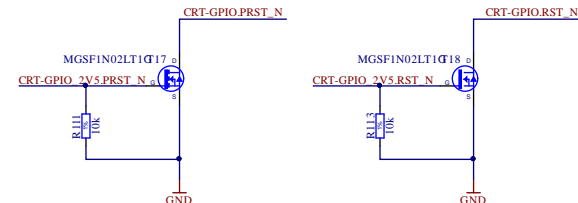
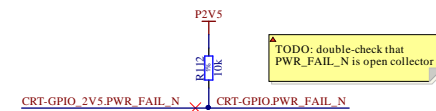
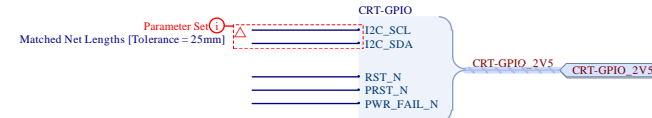
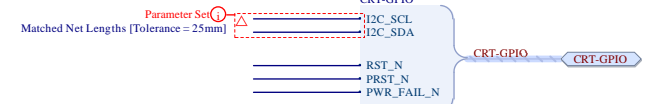
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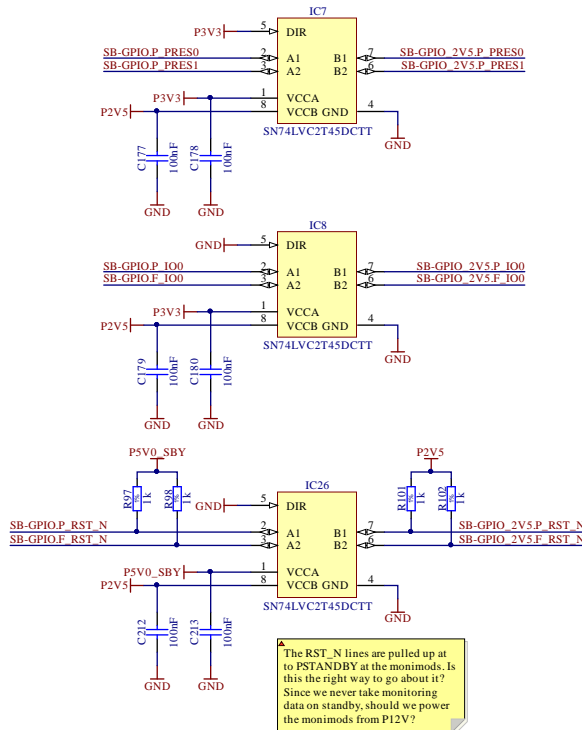
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50mm = 3.5% UI @ 100MHz
(stripline, FR-4)



TODO: monimod powered by standby voltage, add protection for when that's the only voltage on board



The RST_N lines are pulled up at to PSTANDBY at the monimods. Is this the right way to go about it? Since we never take monitoring data on standby, should we power the monimods from P12V?

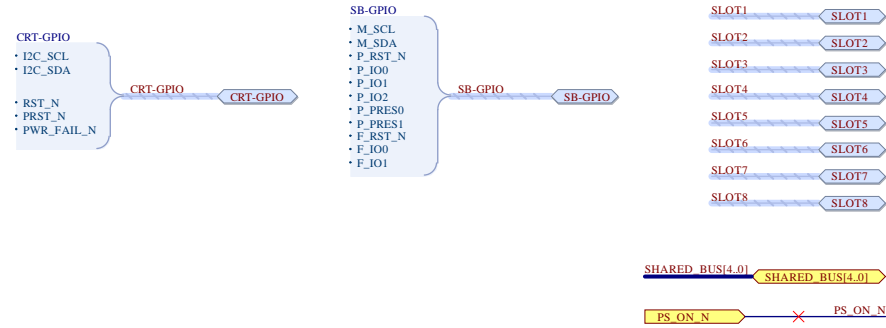
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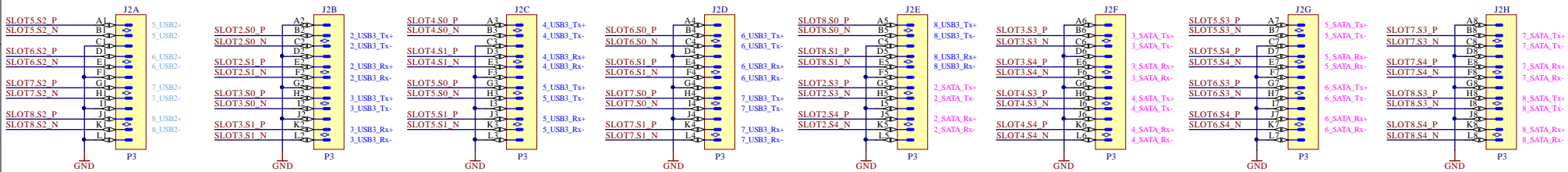
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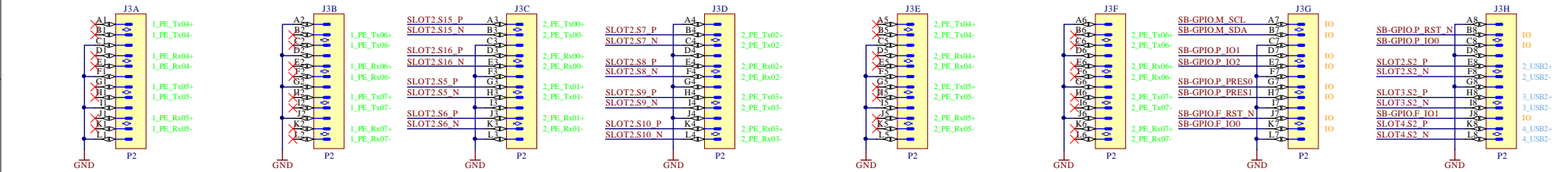
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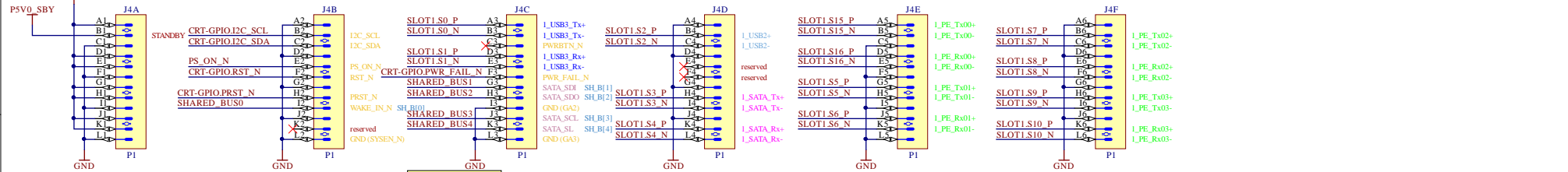
P3 Connector



P2 Connector



P1 Connector



TODO: how to handle PWRBTN?

n_PE_Tx00 and n_PE_Rx00 diff pairs can carry Multi-Gigabit signals (2.1.6). 100Ohm impedance, 5mm tolerance

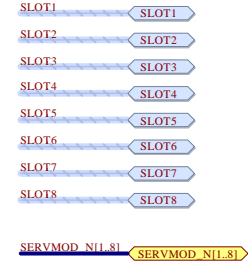
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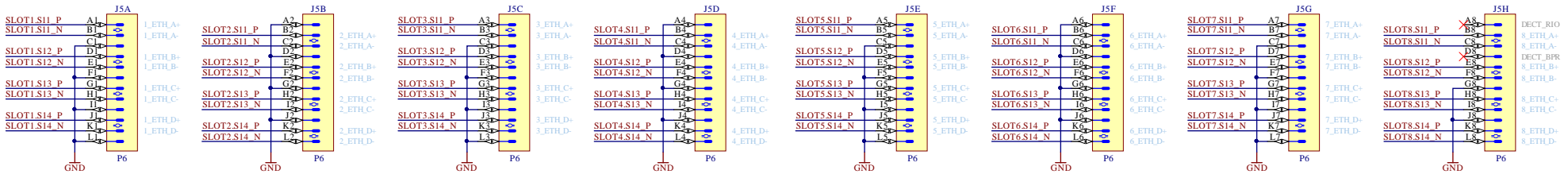
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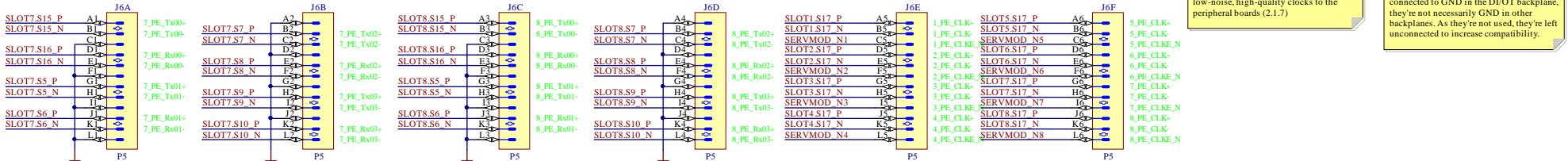
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P6 Connector



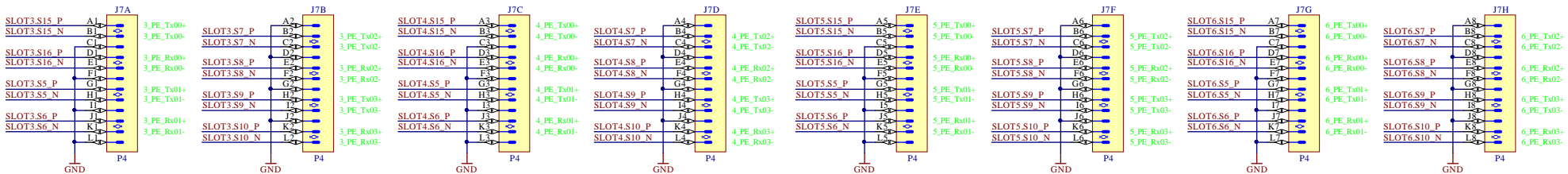
P5 Connector



1. PE_CLK diff pairs will provide low-noise, high-quality clocks to the peripheral boards (2.1.7)

The DECT_RIO and DECT_BPR pins are connected to GND in the DIOT backplane, they're not necessarily GND in other backplanes. As they're not used, they're left unconnected to increase compatibility.

P4 Connector



Project/Equipment		DIOT	
Document		Designer C. Gentsos	
BE/CO		Drawn by C. Gentsos	
CERN		Check by *	
		Last Mod. C. Gentsos	
		File CPCL-S Backplane_P4-P6_SchDoc	
		Print Date 28/09/2020 17:19:38	
		Sheet 12 of 17	
		A3	

DIOT Rad-tol System Board
CPCL-S Backplane (2/2)

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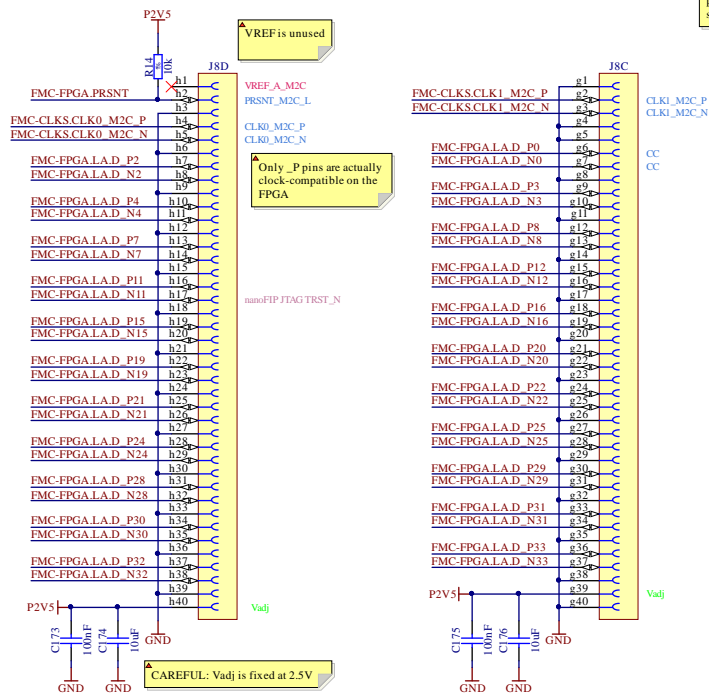
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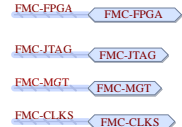
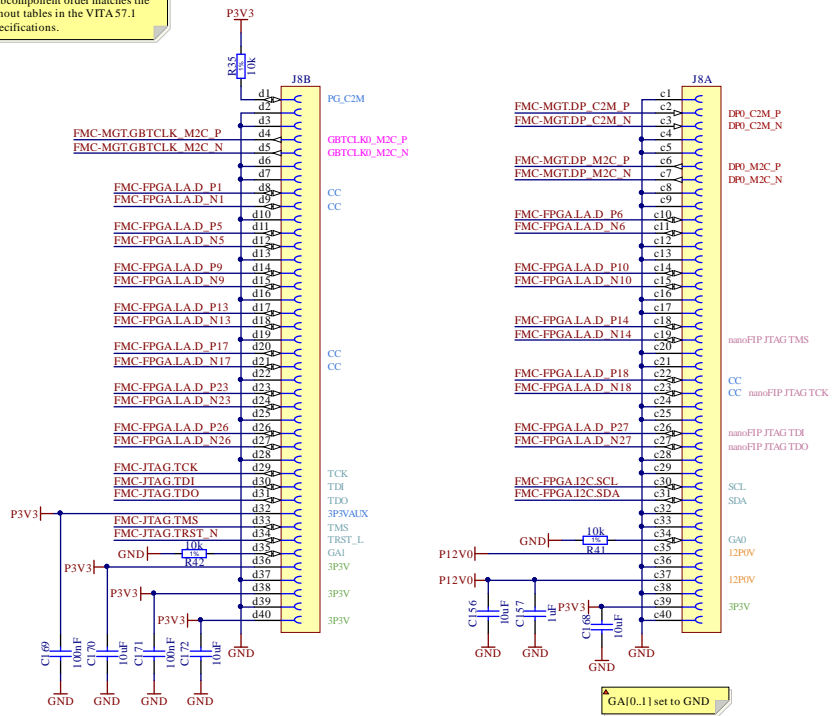
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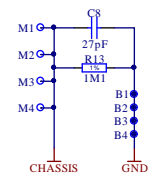
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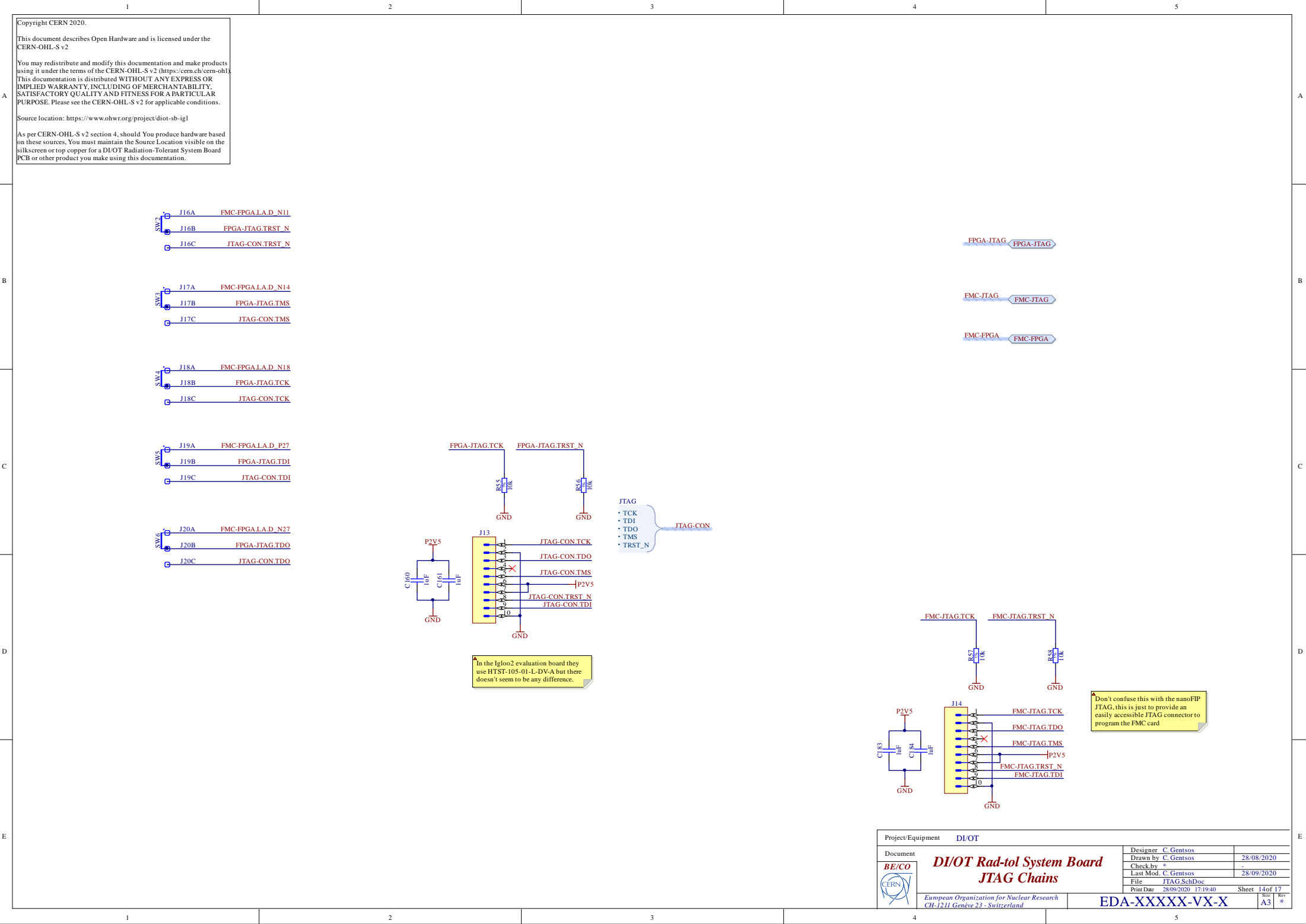
Subcomponent order matches the pinout tables in the VITA 57.1 specifications.



Front panel and FMC slot spacers



Project/Equipment		DI/OT	
Document		Designer C. Gentsos	
BE/CO		Drawn by C. Gentsos	
DI/OT Rad-tol System Board		28/08/2020	
FMC		Check by *	
Last Mod. C. Gentsos		28/09/2020	
File FMC_SchDoc		Print Date 28/09/2020 17:19:39	
European Organization for Nuclear Research		Sheet 13 of 17	
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EDA-XXXXX-VX-X		Rev *	



Project/Equipment

DI/OT

Document

BE/CO



DI/OT Rad-tol System Board

JTAG Chains

European Organization for Nuclear Research

CH-1211 Genève 23 - Switzerland

Designer

C. Gentsos

28/08/2020

Drawn by

C. Gentsos

28/08/2020

Check by

*

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C. Gentsos

28/09/2020

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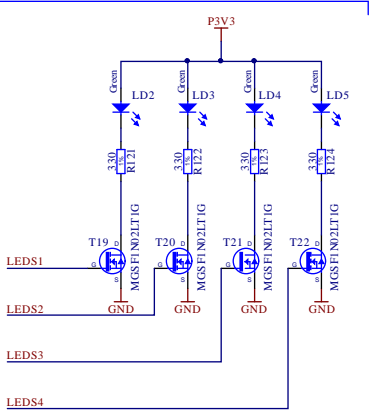
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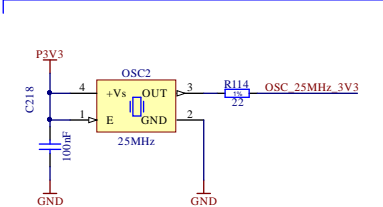
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User LEDs

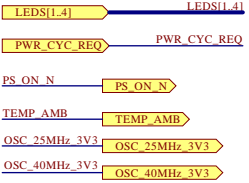
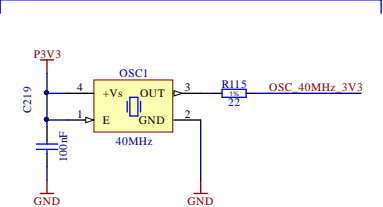


TODO: We have the pins, do we want to double the clocks in case someone likes redundancy?

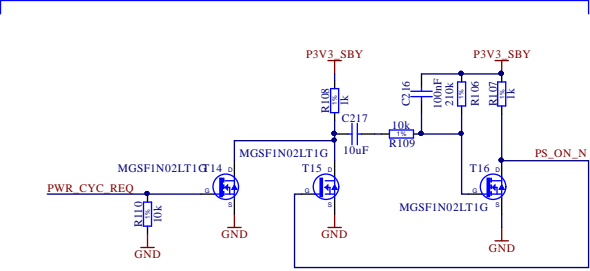
25MHz oscillator



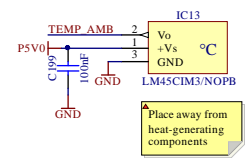
40MHz oscillator



Power cycle pulse generator

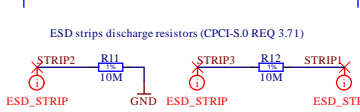


Ambient temp sensor



Place away from heat-generating components

ESD Protection



Project/Equipment		DI/OT	
Document		Designer	C. Gentsos
		Drawn by	C. Gentsos
		Check by	*
		Last Mod.	C. Gentsos
		File	Top_Misc.SchDoc
		Print Date	28/09/2020 17:19:41
		Sheet	17 of 17
		Size	A3
		Rev	*

DI/OT Rad-tol System Board
Miscellaneous

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