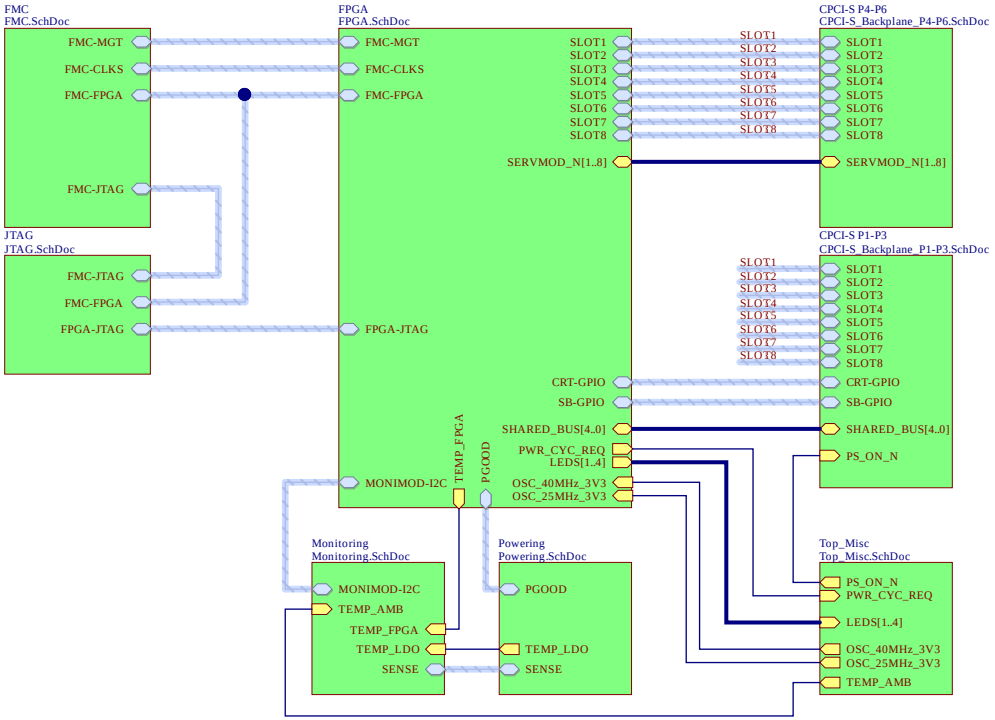

Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board Top Level**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	28/09/2020
		File DIOT-sb-igl_top.SchDoc	
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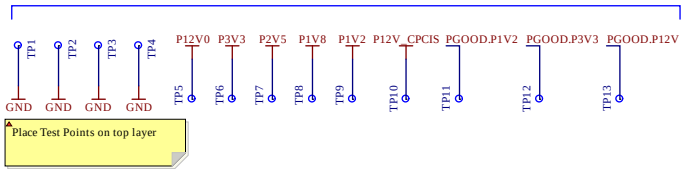
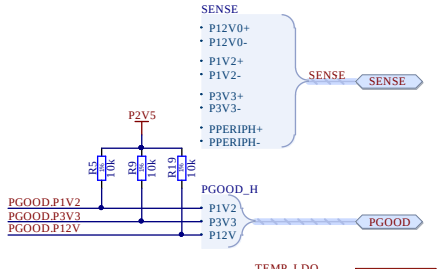
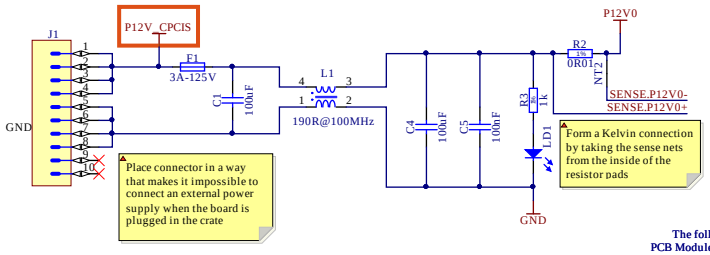
Test points

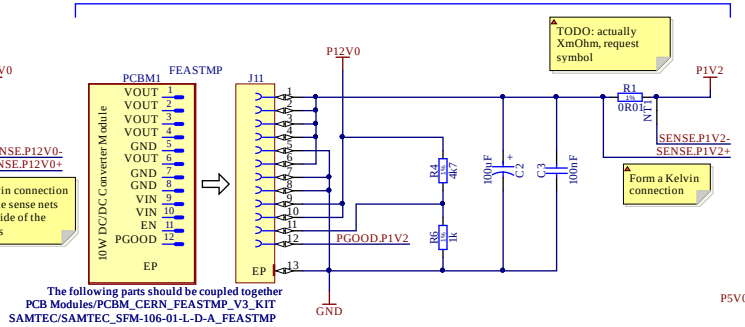




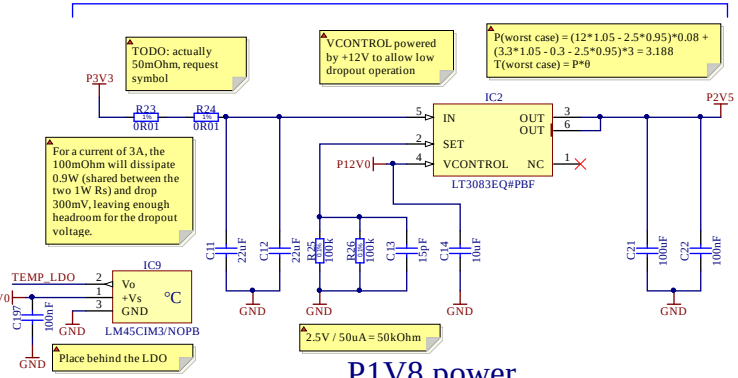
12V0 power cleanup



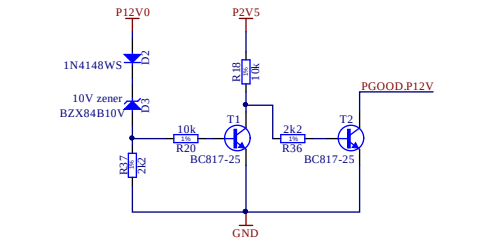
P1V2 power



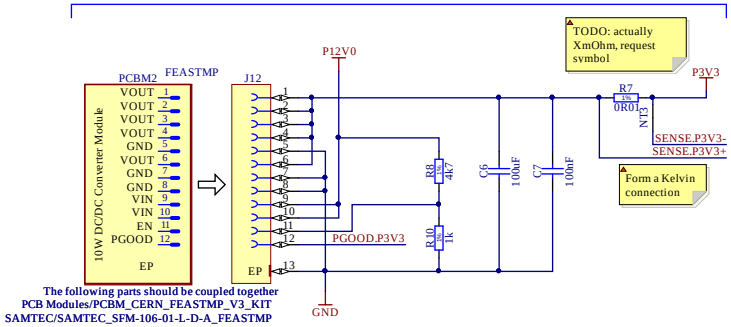
P2V5 power



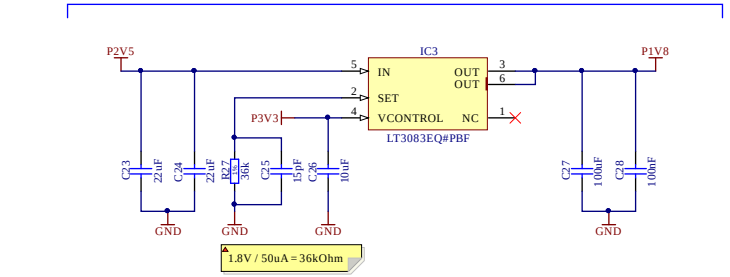
12V brownout detection



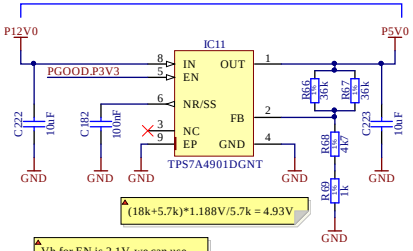
P3V3 power



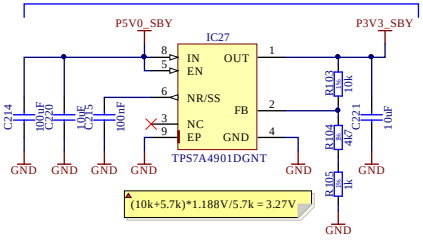
P1V8 power



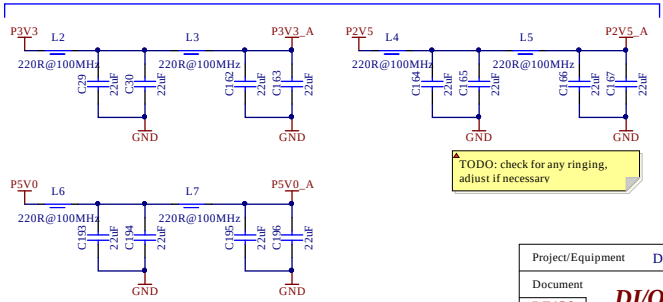
P5V0 power



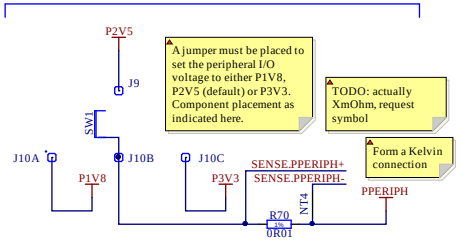
Always-on P3V3 power



Analog power filtering



Peripheral voltage selection



Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board Power**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
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		Last Mod. C. Gentsos	28/09/2020
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		Print Date 01/10/2020 12:00:25	Sheet 2 of 17
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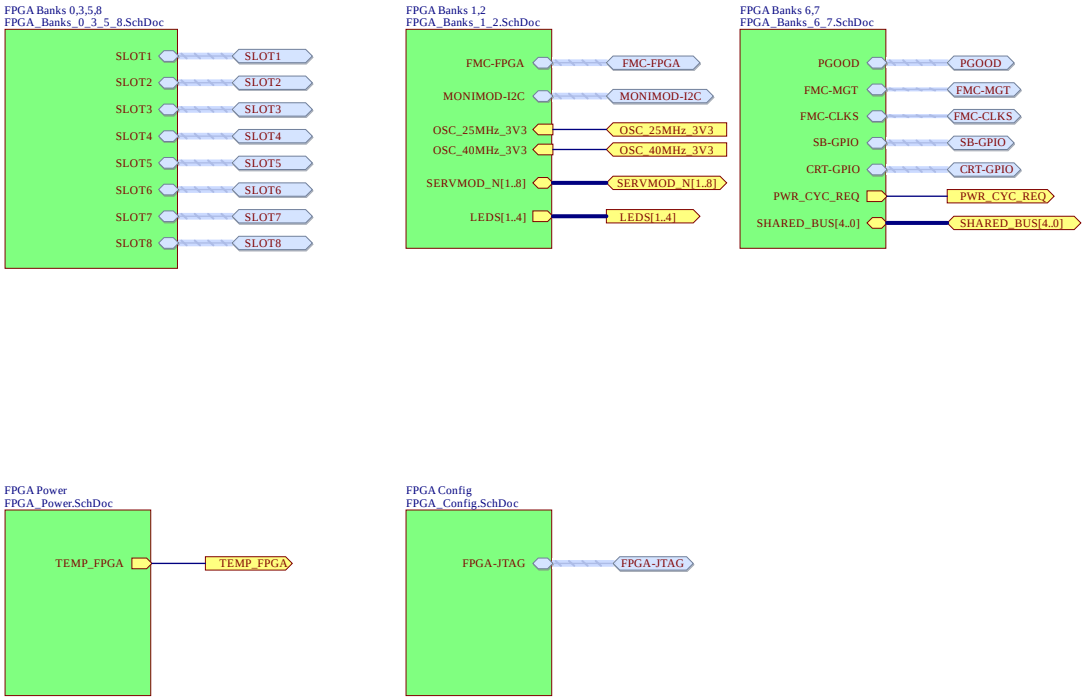

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA Top	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	28/09/2020
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IC1M
M2GL090T-FGG676I

IC1L
M2GL090T-FGG676I

IC1K
M2GL090T-FGG676I

IC12
LM45CIM3/NOPB

TEMP_FPGA

Place behind the FPGA

25 VDD pins: 13x 10n, 12x 100n, 1x 100u, 3x 220u, 1x 330u

Some recent advice (URL below) indicates that if one MLCC is used per pin it's best to use the highest value of a given package size (here 0402). Microsemi still recommends using two different values (100n and 10n). Should we switch to the more modern advice?

https://www.signalintegrityjournal.com/articles/1589-the-myth-of-three

7 VPP pins: 4x 10n, 3x 100n, 1x 10u

3 VREF1 pins: 2x 10n, 1x 100n, 1x 10u

1 VPPNVM pin: 1x 10n, 1x 10u

TODO: PLL power, 2.5V or 3.3V? 2.5V will be smoother due to the LDO so better jitter but which one is better for radiation?

1 VDDI6 pin: 1x 100n, 1x 10u

12 VDDI1 pins: 6x 10n, 6x 100n, 1x 10u

1 VDDI4 pin: 1x 100n, 1x 10u

13 VDDI3 pins: 6x 10n, 7x 100n, 1x 10u

4 VDDI0 pins: 2x 10n, 2x 100n, 1x 10u

10 VDDI5 pins: 5x 10n, 5x 100n, 1x 10u

3 VDDI2 pins: 1x 10n, 2x 100n, 1x 10u

10 VDDI8 pins: 5x 10n, 5x 100n, 1x 10u

4 VDDI7 pins: 2x 10n, 2x 100n, 1x 10u

VPPNVM must be shorted to VPP

Place the 0402 100nF caps close to the FPGA pins

Project/Equipment	DI/OT
Document	DI/OT Rad-tol System Board FPGA Power
Designer	C. Gentsos
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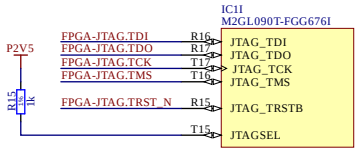
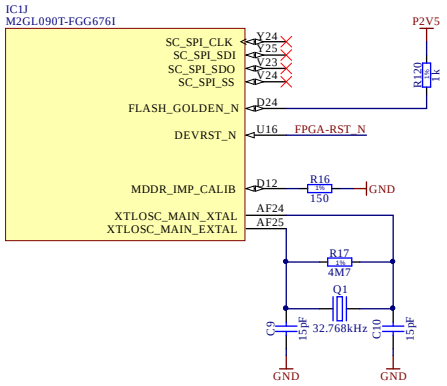
Parts powered by 2.5V

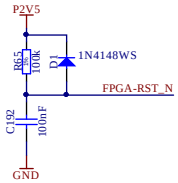
The JTAG and configuration pins are referred to as Bank 4





TODO: calibration not required so 0R may be acceptable, to be clarified.

This is to trigger a reprogram from the flash, assuming that



Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA Configuration	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
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		Last Mod. C. Gentsos	28/09/2020
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Banks powered by PPERIPH

Caution on pin-swapping: the S0_P pins are connected to Global I/O pins to be able to drive FPGA clocks and can't be swapped with other peripheral I/Os.
Boards 1-3 can drive global buffers directly or use CCC blocks;
Boards 4-6 can drive global buffers directly or through VCCC crossbars; and
Boards 7-8 can only reach global buffers through CCC blocks.

IC1A
M2GL090T-FGG676I

BANK 0

MSIO111NB0	J12	SLOT1.LVDS_1_N
MSIO111PB0	J11	SLOT1.LVDS_1_P
MSIO112NB0	A9	SLOT1.LVDS_2_N
MSIO112PB0	A8	SLOT1.LVDS_2_P
MSIO113NB0	H11	SLOT1.LVDS_3_N
MSIO113PB0	G10	SLOT1.LVDS_3_P
MSIO114NB0	B8	SLOT1.LVDS_4_N
MSIO114PB0	A7	SLOT1.LVDS_4_P
MSIO115NB0	H10	SLOT1.LVDS_5_N
MSIO115PB0	H9	SLOT1.LVDS_5_P
MSIO116NB0	C8	SLOT1.LVDS_6_N
MSIO116PB0	D8	SLOT1.LVDS_6_P
MSIO117NB0	E10	SLOT1.LVDS_7_N
MSIO117PB0	E9	SLOT1.LVDS_7_P
MSIO118NB0	B7	SLOT1.LVDS_8_N
MSIO118PB0	B6	SLOT1.LVDS_8_P
MSIO119NB0	F9	SLOT1.LVDS_9_N
MSIO119PB0	G8	SLOT1.LVDS_9_P
MSIO120NB0	A5	SLOT1.LVDS_10_N
MSIO120PB0	A4	SLOT1.LVDS_10_P
MSIO121NB0	F7	SLOT1.LVDS_11_N
MSIO121PB0	E8	SLOT1.LVDS_11_P
MSIO122NB0	B5	SLOT1.LVDS_12_N
MSIO122PB0	C6	SLOT1.LVDS_12_P
MSIO123NB0	E5	SLOT1.LVDS_13_N
MSIO123PB0	E4	SLOT1.LVDS_13_P
MSIO124NB0	D7	SLOT1.LVDS_14_N
MSIO124PB0	D6	SLOT1.LVDS_14_P
MSIO125NB0	E6	SLOT1.LVDS_15_N
MSIO125PB0	E7	SLOT1.LVDS_15_P

IC1D
M2GL090T-FGG676I

BANK 3

MSIO0NB3	W22	SLOT1.LVDS_16_N	
MSIO0PB3	W21	SLOT1.LVDS_16_P	
MSIO1NB3	AA23	SLOT1.LVDS_17_N	
MSIO1PB3	T22	SLOT1.LVDS_17_P	
MSIO2NB3	AC25	SLOT2.LVDS_1_N	
MSIO2PB3	AC24	SLOT2.LVDS_1_P	
MSIO3NB3	Y21	SLOT2.LVDS_2_N	
MSIO3PB3	Y20	SLOT2.LVDS_2_P	
MSIO4NB3	AC26	SLOT2.LVDS_3_N	
MSIO4PB3	AD26	SLOT2.LVDS_3_P	
MSIO5NB3	U21	SLOT2.LVDS_4_N	
MSIO5PB3	U20	SLOT2.LVDS_4_P	
MSIO6NB3	W24	SLOT2.LVDS_5_N	
MSIO6PB3	V23	SLOT2.LVDS_5_P	
MSIO7NB3	AA25	SLOT2.LVDS_6_N	
MSIO7PB3	AA24	SLOT2.LVDS_6_P	
MSIO8NB3	AB26	SLOT2.LVDS_7_N	
MSIO8PB3	AB25	SLOT2.LVDS_7_P	
MSIO11NB3/CCC_NE1_CLKI0	T22	SLOT8.LVDS_0_N	CC
MSIO11PB3/CCC_NE0_CLKI0	U22	SLOT8.LVDS_0_P	CC
MSIO12NB3/SPI_0_SDI	W26	SLOT2.LVDS_8_N	
MSIO12PB3/SPI_0_CLK	V26	SLOT2.LVDS_8_P	
MSIO13NB3/SPI_0_SS0	Y23	SLOT2.LVDS_9_N	
MSIO13PB3/SPI_0_SDO	T23	SLOT2.LVDS_9_P	
MSIO14NB3	V26	SLOT2.LVDS_10_N	
MSIO14PB3	V25	SLOT2.LVDS_10_P	
MSIO15NB3	T20	SLOT2.LVDS_11_N	
MSIO15PB3	T19	SLOT2.LVDS_11_P	
MSIO16NB3	U26	SLOT2.LVDS_12_N	
MSIO16PB3	U25	SLOT2.LVDS_12_P	
MSIO17NB3	T18	SLOT2.LVDS_13_N	
MSIO17PB3	U18	SLOT2.LVDS_13_P	
MSIO18NB3	T25	SLOT2.LVDS_14_N	
MSIO18PB3	T24	SLOT2.LVDS_14_P	
MSIO19NB3	R21	SLOT2.LVDS_15_N	
MSIO19PB3	R22	SLOT2.LVDS_15_P	
MSIO20NB3/GB13/VCCC_SE1_CLKI	R25	SLOT4.LVDS_0_N	
MSIO20PB3/GB9/VCCC_SE0_CLKI	R24	SLOT4.LVDS_0_P	CC
MSIO21NB3	R19	SLOT3.LVDS_1_N	
MSIO21PB3	R20	SLOT2.LVDS_16_P	
MSIO22NB3	P26	SLOT2.LVDS_17_N	
MSIO22PB3	R26	SLOT2.LVDS_17_P	
MSIO23NB3	P19	SLOT3.LVDS_1_N	
MSIO23PB3	P18	SLOT3.LVDS_1_P	
MSIO24NB3	P24	SLOT3.LVDS_2_N	
MSIO24PB3	P23	SLOT3.LVDS_2_P	
MSIO25NB3	P22	SLOT3.LVDS_3_N	
MSIO25PB3	P21	SLOT3.LVDS_3_P	
MSIO26NB3	N25	SLOT3.LVDS_4_N	
MSIO26PB3	N26	SLOT3.LVDS_4_P	
MSIO27NB3	P16	SLOT3.LVDS_5_N	
MSIO27PB3	P17	SLOT3.LVDS_5_P	
MSIO28NB3	N23	SLOT3.LVDS_6_N	
MSIO28PB3	N24	SLOT3.LVDS_6_P	
MSIO29NB3	N19	SLOT3.LVDS_7_N	
MSIO29PB3	N18	SLOT3.LVDS_7_P	
MSIO30NB3	M25	SLOT3.LVDS_8_N	
MSIO30PB3	M26	SLOT3.LVDS_8_P	
MSIO32NB3	M22	SLOT3.LVDS_9_N	
MSIO32PB3	M23	SLOT3.LVDS_9_P	
MSIO33NB3	Y20	SLOT6.LVDS_10_N	
MSIO33PB3	V21	SLOT6.LVDS_10_P	
MSIO34NB3	N24	SLOT3.LVDS_11_N	
MSIO34PB3	N25	SLOT3.LVDS_11_P	
MSIO35NB3	M18	SLOT3.LVDS_12_N	
MSIO35PB3	M17	SLOT3.LVDS_12_P	
MSIO36NB3	L26	SLOT3.LVDS_13_N	
MSIO36PB3	L26	SLOT3.LVDS_13_P	
MSIO37NB3	M20	SLOT3.LVDS_14_N	
MSIO37PB3	M21	SLOT3.LVDS_14_P	
MSIO38NB3	L24	SLOT3.LVDS_15_N	
MSIO38PB3	L25	SLOT3.LVDS_15_P	
MSIO39NB3	L19	SLOT3.LVDS_16_N	
MSIO39PB3	L20	SLOT3.LVDS_16_P	
MSIO40NB3	H25	SLOT3.LVDS_17_N	
MSIO40PB3	H26	SLOT3.LVDS_17_P	
MSIO41NB3	L19	SLOT4.LVDS_1_N	
MSIO41PB3	L20	SLOT4.LVDS_1_P	
MSIO42NB3	K25	SLOT4.LVDS_2_N	
MSIO42PB3	K26	SLOT4.LVDS_2_P	
MSIO43NB3	K18	SLOT4.LVDS_3_N	
MSIO43PB3	K17	SLOT4.LVDS_3_P	
MSIO44NB3	K22	SLOT4.LVDS_4_N	
MSIO44PB3	K23	SLOT4.LVDS_4_P	
MSIO45NB3	J23	SLOT4.LVDS_5_N	
MSIO45PB3	J24	SLOT4.LVDS_5_P	
MSIO46NB3	K21	SLOT4.LVDS_6_N	
MSIO46PB3	K22	SLOT4.LVDS_6_P	
MSIO47NB3	H23	SLOT4.LVDS_7_N	
MSIO47PB3	H24	SLOT4.LVDS_7_P	
MSIO48NB3	H19	SLOT4.LVDS_8_N	
MSIO48PB3	J19	SLOT4.LVDS_8_P	
MSIO49NB3	J21	SLOT4.LVDS_9_N	
MSIO49PB3	J22	SLOT4.LVDS_9_P	
MSIO50NB3	H20	SLOT4.LVDS_10_N	
MSIO50PB3	H21	SLOT4.LVDS_10_P	

IC1E
M2GL090T-FGG676I

BANK 5

MSIO195NB5	W13	SLOT4.LVDS_11_N	
MSIO195PB5	W12	SLOT4.LVDS_11_P	
MSIO196NB5/CCC_SW0_CLKI2	AC11	SLOT4.LVDS_12_N	
MSIO196PB5	AB11	SLOT4.LVDS_12_P	
MSIO197NB5/PROBE_B	AD12	SLOT4.LVDS_13_N	
MSIO197PB5/PROBE_A	AE12	SLOT4.LVDS_13_P	
MSIO198NB5	Y12	SLOT4.LVDS_14_N	
MSIO198PB5	AA12	SLOT4.LVDS_14_P	
MSIO199NB5	AF13	SLOT4.LVDS_15_N	
MSIO199PB5	AF12	SLOT4.LVDS_15_P	
MSIO201NB5/GB7/CCC_SW1_CLKI2	AB13	SLOT3.LVDS_0_N	
MSIO201PB5/GB3/CCC_SW0_CLKI3	AB12	SLOT3.LVDS_0_P	CC
MSIO202NB5	AE14	SLOT4.LVDS_16_N	
MSIO202PB5	AF14	SLOT4.LVDS_16_P	
MSIO203NB5	V14	SLOT4.LVDS_17_N	
MSIO203PB5	V13	SLOT4.LVDS_17_P	
MSIO204NB5	AD14	SLOT5.LVDS_1_N	
MSIO204PB5	AD13	SLOT5.LVDS_1_P	
MSIO205NB5	AC14	SLOT5.LVDS_2_N	
MSIO205PB5	AC13	SLOT5.LVDS_2_P	
MSIO206NB5	AF17	SLOT5.LVDS_3_N	
MSIO206PB5	AF18	SLOT5.LVDS_3_P	
MSIO207NB5	AA14	SLOT5.LVDS_4_N	
MSIO207PB5	AA13	SLOT5.LVDS_4_P	
MSIO208NB5	AE15	SLOT7.LVDS_0_N	
MSIO208PB5/CCC_SW1_CLKI3	AF15	SLOT7.LVDS_0_P	CC
MSIO209NB5	Y14	SLOT5.LVDS_5_N	
MSIO209PB5/VCCC_SE0_CLKI	W14	SLOT5.LVDS_5_P	
MSIO210NB5	AE17	SLOT5.LVDS_0_N	
MSIO210PB5/GB11/VCCC_SE0_CLKI	AE16	SLOT5.LVDS_0_P	CC
MSIO211NB5	Y17	SLOT5.LVDS_6_N	
MSIO211PB5	AA17	SLOT5.LVDS_6_P	
MSIO212NB5	AD17	SLOT6.LVDS_0_N	
MSIO212PB5/GB15/VCCC_SE1_CLKI	AD16	SLOT6.LVDS_0_P	CC
MSIO213NB5	AB15	SLOT5.LVDS_7_N	
MSIO213PB5/VCCC_SE1_CLKI	AC15	SLOT5.LVDS_7_P	
MSIO214NB5	Y15	SLOT5.LVDS_8_N	
MSIO214PB5	AA15	SLOT5.LVDS_8_P	
MSIO215NB5	AB16	SLOT5.LVDS_9_N	
MSIO215PB5	AC16	SLOT5.LVDS_9_P	
MSIO216NB5	AB17	SLOT5.LVDS_10_N	
MSIO216PB5	AB18	SLOT5.LVDS_10_P	
MSIO217NB5	V16	SLOT5.LVDS_11_N	
MSIO217PB5	V15	SLOT5.LVDS_11_P	
MSIO218NB5	AF20	SLOT5.LVDS_12_N	
MSIO218PB5	AF19	SLOT5.LVDS_12_P	
MSIO221NB5	W17	SLOT5.LVDS_13_N	
MSIO221PB5	W18	SLOT5.LVDS_13_P	
MSIO222NB5	AE20	SLOT5.LVDS_14_N	
MSIO222PB5	AE19	SLOT5.LVDS_14_P	
MSIO223NB5	W16	SLOT5.LVDS_15_N	
MSIO223PB5	Y16	SLOT5.LVDS_15_P	
MSIO224NB5	AD19	SLOT5.LVDS_16_N	
MSIO224PB5	AD18	SLOT5.LVDS_16_P	
MSIO225NB5	AE21	SLOT5.LVDS_17_N	
MSIO225PB5	AF22	SLOT5.LVDS_17_P	
MSIO226NB5	Y19	SLOT6.LVDS_1_N	
MSIO226PB5	W19	SLOT6.LVDS_1_P	
MSIO227NB5	AE22	SLOT6.LVDS_2_N	
MSIO227PB5	AF23	SLOT6.LVDS_2_P	
MSIO228NB5	Y20	SLOT6.LVDS_3_N	
MSIO228PB5	Y21	SLOT6.LVDS_3_P	
MSIO229NB5	AC19	SLOT6.LVDS_4_N	
MSIO229PB5	AC18	SLOT6.LVDS_4_P	
MSIO230NB5	V18	SLOT6.LVDS_5_N	
MSIO230PB5	V19	SLOT6.LVDS_5_P	
MSIO231NB5	AA19	SLOT6.LVDS_6_N	
MSIO231PB5	AA18	SLOT6.LVDS_6_P	
MSIO232NB5	AD23	SLOT6.LVDS_7_N	
MSIO232PB5	AD22	SLOT6.LVDS_7_P	
MSIO233NB5	AC20	SLOT6.LVDS_8_N	
MSIO233PB5	AD21	SLOT6.LVDS_8_P	
MSIO234NB5	AD24	SLOT6.LVDS_9_N	
MSIO234PB5	AE24	SLOT6.LVDS_9_P	
MSIO235NB5	AB21	SLOT6.LVDS_10_N	
MSIO235PB5	AC21	SLOT6.LVDS_10_P	
MSIO236NB5	AB23	SLOT6.LVDS_11_N	
MSIO236PB5	AC23	SLOT6.LVDS_11_P	
MSIO237NB5	AB22	SLOT6.LVDS_12_N	
MSIO237PB5	AA22	SLOT6.LVDS_12_P	
MSIO238NB5	AA20	SLOT6.LVDS_13_N	
MSIO238PB5	AB20	SLOT6.LVDS_13_P	

IC1G
M2GL090T-FGG676I

BANK 8

MSIO126NB8	G7	SLOT6.LVDS_14_N	
MSIO126PB8	H8	SLOT6.LVDS_14_P	
MSIO127NB8	H6	SLOT6.LVDS_15_N	
MSIO127PB8	H5	SLOT6.LVDS_15_P	
MSIO128NB8	J7	SLOT6.LVDS_16_N	
MSIO128PB8	J6	SLOT6.LVDS_16_P	
MSIO129NB8	G6	SLOT6.LVDS_17_N	
MSIO129PB8	G5	SLOT6.LVDS_17_P	
MSIO131NB8	L5	SLOT7.LVDS_1_N	
MSIO131PB8	L4	SLOT7.LVDS_1_P	
MSIO132NB8	L5	SLOT7.LVDS_2_N	
MSIO132PB8	L4	SLOT7.LVDS_2_P	
MSIO133NB8	D4	SLOT7.LVDS_3_N	
MSIO133PB8	D3	SLOT7.LVDS_3_P	
MSIO134NB8	C3	SLOT7.LVDS_4_N	
MSIO134PB8	B3	SLOT7.LVDS_4_P	
MSIO135NB8	H4	SLOT7.LVDS_5_N	
MSIO135PB8	H3	SLOT7.LVDS_5_P	
MSIO136NB8	E3	SLOT7.LVDS_6_N	
MSIO136PB8	F3	SLOT7.LVDS_6_P	
MSIO137NB8	J9	SLOT7.LVDS_7_N	
MSIO137PB8	J8	SLOT7.LVDS_7_P	
MSIO138NB8	A3	SLOT7.LVDS_8_N	
MSIO138PB8	A2	SLOT7.LVDS_8_P	
MSIO139NB8	K9	SLOT7.LVDS_9_N	
MSIO139PB8	K10	SLOT7.LVDS_9_P	
MSIO140NB8	B2	SLOT7.LVDS_10_N	
MSIO140PB8	B1	SLOT7.LVDS_10_P	
MSIO142NB8	L10	SLOT7.LVDS_11_N	
MSIO142PB8	L9	SLOT7.LVDS_11_P	
MSIO143NB8	J4	SLOT7.LVDS_12_N	
MSIO143PB8	J3	SLOT7.LVDS_12_P	
MSIO145NB8	K7	SLOT7.LVDS_13_N	
MSIO145PB8	L7	SLOT7.LVDS_13_P	
MSIO146NB8	K5	SLOT7.LVDS_14_N	
MSIO146PB8	K6	SLOT7.LVDS_14_P	
MSIO147NB8	L8	SLOT7.LVDS_15_N	
MSIO147PB8	M8	SLOT7.LVDS_15_P	
MSIO148NB8	D2	SLOT7.LVDS_16_N	
MSIO148PB8	E1	SLOT7.LVDS_16_P	
MSIO149NB8	E2	SLOT7.LVDS_17_N	
MSIO149PB8	D1	SLOT7.LVDS_17_P	
MSIO150NB8	F2	SLOT8.LVDS_1_N	
MSIO150PB8	F1	SLOT8.LVDS_1_P	
MSIO151NB8	L5	SLOT8.LVDS_2_N	
MSIO151PB8	M5	SLOT8.LVDS_2_P	
MSIO152NB8	L4	SLOT8.LVDS_3_N	
MSIO152PB8	K4	SLOT8.LVDS_3_P	
MSIO153NB8	M6	SLOT8.LVDS_4_N	
MSIO153PB8	M7	SLOT8.LVDS_4_P	
MSIO154NB8	G2	SLOT8.LVDS_5_N	
MSIO154PB8	G1	SLOT8.LVDS_5_P	
MSIO156NB8	P4	SLOT2.LVDS_0_N	
MSIO156PB8/GB6/CCC_NW1_CLKI1	N4	SLOT2.LVDS_0_P	CC
MSIO157NB8	N5	SLOT1.LVDS_0_N	
MSIO157PB8/GB2/CCC_NW0_CLKI1	N6	SLOT1.LVDS_0_P	CC
MSIO158NB8	M3	SLOT8.LVDS_6_N	
MSIO158PB8/CCC_NW1_CLKI0	N3	SLOT8.LVDS_6_P	
MSIO159NB8	N8	SLOT8.LVDS_7_N	
MSIO159PB8/CCC_NW0_CLKI0	N9	SLOT8.LVDS_7_P	
MSIO160NB8	L3	SLOT8.LVDS_8_N	
MSIO160PB8	L2	SLOT8.LVDS_8_P	
MSIO161NB8	F2	SLOT8.LVDS_9_N	
MSIO161PB8	M2	SLOT8.LVDS_9_P	
MSIO163NB8	M10	SLOT8.LVDS_10_N	
MSIO163PB8	N10	SLOT8.LVDS_10_P	
MSIO165NB8	P6	SLOT8.LVDS_11_N	
MSIO165PB8	P7	SLOT8.LVDS_11_P	
MSIO166NB8	J2	SLOT8.LVDS_12_N	
MSIO166PB8	J1	SLOT8.LVDS_12_P	
MSIO167NB8	F1	SLOT8.LVDS_13_N	
MSIO167PB8	G1	SLOT8.LVDS_13_P	
MSIO168NB8	P3	SLOT8.LVDS_14_N	
MSIO168PB8	P4	SLOT8.LVDS_14_P	
MSIO170NB8	M1	SLOT8.LVDS_15_N	
MSIO170PB8	N1	SLOT8.LVDS_15_P	
MSIO172NB8	P2	SLOT8.LVDS_16_N	
MSIO172PB8	R2	SLOT8.LVDS_16_P	
MSIO173NB8	P1	SLOT8.LVDS_17_N	
MSIO173PB8	R1	SLOT8.LVDS_17_P	

PERIPH_CONN

- LVDS_0_P
- LVDS_0_N
- LVDS_1_P
- LVDS_1_N
- LVDS_2_P
- LVDS_2_N
- LVDS_3_P
- LVDS_3_N
- LVDS_4_P
- LVDS_4_N
- LVDS_5_P
- LVDS_5_N
- LVDS_6_P
- LVDS_6_N
- LVDS_7_P
- LVDS_7_N
- LVDS_8_P
- LVDS_8_N
- LVDS_9_P
- LVDS_9_N
- LVDS_10_P
- LVDS_10_N
- LVDS_11_P
- LVDS_11_N
- LVDS_12_P
- LVDS_12_N
- LVDS_13_P
- LVDS_13_N
- LVDS_14_P
- LVDS_14_N
- LVDS_15_P
- LVDS_15_N
- LVDS_16_P
- LVDS_16_N
- LVDS_17_P
- LVDS_17_N

Matched Net Lengths [Tolerance = 5mm]
Matched Net Lengths [Tolerance = 20mm]
ClassName: PERIPH_DP

SLOT1	SLOT1
SLOT2	SLOT2
SLOT3	SLOT3
SLOT4	SLOT4
SLOT5	SLOT5
SLOT6	SLOT6
SLOT7	SLOT7
SLOT8	SLOT8

Project/Equipment: DI/OT

Document: **DI/OT Rad-tol System Board**
FPGA I/O Banks B0, B3

BE/CO

Designer	C. Gentsos	
Drawn by	C. Gentsos	28/08/2020
Check.by	*	-
Last Mod.	C. Gentsos	01/10/2020
File	FPGA_Banks_0_3_5_8.SchDoc	
Print Date	01/10/2020 12:00:28	Sheet 6 of 17

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-XXXXX-VX-X

Size A3 | Rev *

Banks powered by 2.5V

Careful with pin swapping: the P nets of the differential pairs 0, 1, 17 and 18 are connected to clock-capable pins and can't be swapped with the other I/Os.

IC1B
M2GL090T-FGG676I

BANK 1

DDRIO62NB1/MDDR_ADDR15	C23	FMC-FPGA.LA.D_N14
DDRIO62PB1/MDDR_ADDR14	D22	FMC-FPGA.LA.D_P14
DDRIO63NB1/MDDR_ADDR13	B23	FMC-FPGA.LA.D_N15
DDRIO63PB1/MDDR_ADDR12	A23	FMC-FPGA.LA.D_P15
DDRIO64NB1/MDDR_ADDR11	E21	FMC-FPGA.LA.D_N2
DDRIO64PB1/MDDR_ADDR10	D21	FMC-FPGA.LA.D_P2
DDRIO65NB1/MDDR_ADDR9	E20	FMC-FPGA.LA.D_N3
DDRIO65PB1/MDDR_ADDR8	D20	FMC-FPGA.LA.D_P3
DDRIO66NB1/MDDR_ADDR7	B22	FMC-FPGA.LA.D_N4
DDRIO66PB1/MDDR_ODT	A22	FMC-FPGA.LA.D_P4
DDRIO67NB1/MDDR_ADDR6	H18	FMC-FPGA.LA.D_N5
DDRIO67PB1/MDDR_ADDR5	G18	FMC-FPGA.LA.D_P5
DDRIO68NB1/MDDR_ADDR4	C21	FMC-FPGA.LA.D_N6
DDRIO68PB1/MDDR_ADDR3	B21	FMC-FPGA.LA.D_P6
DDRIO69NB1/MDDR_ADDR2	E19	FMC-FPGA.LA.D_N7
DDRIO69PB1/MDDR_ADDR1	F19	FMC-FPGA.LA.D_P7
DDRIO70NB1/MDDR_ADDR0	F18	FMC-FPGA.LA.D_N8
DDRIO70PB1/MDDR_BA2	E17	FMC-FPGA.LA.D_P8
DDRIO71NB1/MDDR_BA1	B20	FMC-FPGA.LA.D_N9
DDRIO71PB1/MDDR_BA0	A20	FMC-FPGA.LA.D_P9
DDRIO72NB1/MDDR_CLK_N	C20	FMC-FPGA.LA.D_N10
DDRIO72PB1/MDDR_CLK	C19	FMC-FPGA.LA.D_P10
DDRIO73NB1/MDDR_CAS_N	D19	FMC-FPGA.LA.D_N11
DDRIO73PB1/MDDR_RESET_N	D18	FMC-FPGA.LA.D_P11
DDRIO74NB1/MDDR_CS_N	F17	FMC-FPGA.LA.D_N12
DDRIO74PB1/MDDR_CKE	E17	FMC-FPGA.LA.D_P12
DDRIO75NB1/MDDR_WE_N	J16	FMC-FPGA.LA.D_N13
DDRIO75PB1/MDDR_RAS_N	H16	FMC-FPGA.LA.D_P13
DDRIO76NB1/MDDR_DQ15	G19	FMC-FPGA.LA.D_N1
DDRIO76PB1/CCC_NE1_CLKI3/MDDR_DQ14	F18	FMC-FPGA.LA.D_P1 CC
DDRIO77NB1/MDDR_DQ13	B18	FMC-FPGA.LA.D_N0
DDRIO77PB1/MDDR_DQ12/GB12/CCC_NE1_CLKI2	C18	FMC-FPGA.LA.D_P0 CC
DDRIO78NB1/MDDR_DM_RDQS1	H15	FMC-FPGA.LA.D_N16
DDRIO78PB1/MDDR_TMATCH_0_IN	G16	FMC-FPGA.LA.D_P16
DDRIO79NB1/MDDR_DQS1_N	A17	FMC-FPGA.LA.D_N17
DDRIO79PB1/MDDR_DQS1/GB8/CCC_NE0_CLKI3	B17	FMC-FPGA.LA.D_P17 CC
DDRIO80NB1/MDDR_DQ11	D17	FMC-FPGA.LA.D_N18
DDRIO80PB1/MDDR_DQ10/CCC_NE0_CLKI2	E16	FMC-FPGA.LA.D_P18 CC
DDRIO81NB1/MDDR_DQ9	D16	FMC-FPGA.LA.D_N19
DDRIO81PB1/MDDR_DQ8	C16	FMC-FPGA.LA.D_P19
DDRIO82NB1/MDDR_TMATCH_0_OUT	E15	FMC-FPGA.LA.D_N20
DDRIO82PB1/MDDR_DQ7	F15	FMC-FPGA.LA.D_P20
DDRIO83NB1/MDDR_DQ6	B16	FMC-FPGA.LA.D_N21
DDRIO83PB1/MDDR_DQ5	A15	FMC-FPGA.LA.D_P21
DDRIO84NB1/MDDR_DQ4	B15	FMC-FPGA.LA.D_N22
DDRIO84PB1/MDDR_DM_RDQS0	A14	FMC-FPGA.LA.D_P22
DDRIO85NB1/MDDR_DQS0_N	C15	FMC-FPGA.LA.D_N23
DDRIO85PB1/MDDR_DQS0	C14	FMC-FPGA.LA.D_P23
DDRIO86NB1/MDDR_DQ3	E14	FMC-FPGA.LA.D_N24
DDRIO86PB1/MDDR_DQ2	F14	FMC-FPGA.LA.D_P24
DDRIO87NB1/MDDR_DQ1	E15	FMC-FPGA.LA.D_N25
DDRIO87PB1/MDDR_DQ0	F14	FMC-FPGA.LA.D_P25
DDRIO88NB1	A13	FMC-FPGA.LA.D_N26
DDRIO88PB1/CCC_NW1_CLKI3	B13	FMC-FPGA.LA.D_P26
DDRIO89NB1/MDDR_DQ_ECC0	D13	FMC-FPGA.LA.D_N27
DDRIO89PB1/MDDR_DQ_ECC1	C13	FMC-FPGA.LA.D_P27
DDRIO90NB1/MDDR_DM_RDQS_ECC	E13	FMC-FPGA.LA.D_N28
DDRIO90PB1/MDDR_TMATCH_ECC_IN	G13	FMC-FPGA.LA.D_P28
DDRIO91NB1/MDDR_DQS_ECC_N	A12	FMC-FPGA.LA.D_N29
DDRIO91PB1/MDDR_DQS_ECC	B12	FMC-FPGA.LA.D_P29
DDRIO92NB1/GB4/CCC_NW1_CLKI2	F12	FMC-FPGA.LA.D_N30
DDRIO92PB1/GB0/CCC_NW0_CLKI3	G12	FMC-FPGA.LA.D_P30
DDRIO93NB1/CCC_NW0_CLKI2	H13	FMC-FPGA.LA.D_N31
DDRIO93PB1/MDDR_TMATCH_ECC_OUT	H14	FMC-FPGA.LA.D_P31
DDRIO94NB1	B11	FMC-FPGA.LA.D_N32
DDRIO94PB1	C11	FMC-FPGA.LA.D_P32
DDRIO95NB1	F11	FMC-FPGA.LA.D_N33
DDRIO95PB1	D11	FMC-FPGA.LA.D_P33
DDRIO96NB1	A10	FMC-FPGA.I2C.SCL
DDRIO96PB1	B10	FMC-FPGA.I2C.SDA
DDRIO97NB1	G12	SERVMOD_DIR1
DDRIO97PB1	F11	SERVMOD_DIR2
DDRIO98NB1	J9	SERVMOD_DIR3
DDRIO98PB1	E10	SERVMOD_DIR4
DDRIO99NB1	J10	SERVMOD_DIR5
DDRIO99PB1	G9	SERVMOD_DIR6

FMC-SIGS
PRSNT
I2C
SCL
SDA
LA
FMC-FPGA
FMC-FPGA
I2C
Parameter Set
Matched Net Lengths [Tolerance = 10mm]
FMC-LA
D_N[33..0]
D_P[33..0]
Matched Net Lengths [Tolerance = 5mm]
Matched Net Lengths [Tolerance = 20mm]
ClassName: FMC_DP
MONIMOD-I2C
MONIMOD-I2C
Parameter Set
Matched Net Lengths [Tolerance = 10mm]
OSC_25MHz_3V3
OSC_25MHz_3V3
OSC_40MHz_3V3
OSC_40MHz_3V3
LEDS[1..4]
LEDS[1..4]

IC1C
M2GL090T-FGG676I

BANK 2

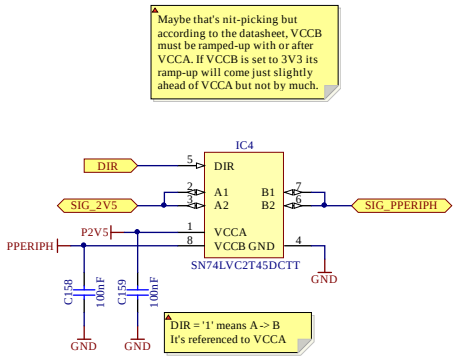
MSIO51NB2	F25	SERVMOD_DIR7
MSIO51PB2	E26	SERVMOD_DIR8
MSIO52NB2	C26	
MSIO52PB2/CCC_NE0_CLKI1	D26	OSC_25MHz_2V5
MSIO53NB2	B25	
MSIO53PB2/CCC_NE1_CLKI1	B26	OSC_40MHz_2V5
MSIO54NB2	E24	LEDS1
MSIO54PB2/GB10/VCCC_SE0_CLKI	E25	LEDS2
MSIO55NB2	F23	LEDS3
MSIO55PB2/GB14/VCCC_SE1_CLKI	F24	LEDS4
MSIO56NB2	G22	SERVMOD_FPGA1
MSIO56PB2	G23	SERVMOD_FPGA2
MSIO57NB2	A24	SERVMOD_FPGA3
MSIO57PB2	A25	SERVMOD_FPGA4
MSIO58NB2	C24	SERVMOD_FPGA5
MSIO58PB2	C25	SERVMOD_FPGA6
MSI59NB2	D23	FMC-FPGA.PRSNT
MSIO60NB2	E22	SERVMOD_FPGA7
MSIO60PB2	F22	SERVMOD_FPGA8
MSIO61NB2	G20	MONIMOD-I2C.SCL
MSIO61PB2	G21	MONIMOD-I2C.SDA

OSC_25MHz_3V3
R116 75
OSC_25MHz_2V5
R117 220
GND
OSC_40MHz_3V3
R118 75
OSC_40MHz_2V5
R119 220
GND
Place resistor dividers close to the FPGA pins

REPEAT(Voltage_trans_SERVMOD,1,8)
Translate_2V5_to_PPERIPH_1b.SchDoc
SERVMOD_DIR[1..8]
SERVMOD_DIR
REPEAT(DIR)
SERVMOD_FPGA[1..8]
SERVMOD_FPGA
REPEAT(SIG_2V5)
REPEAT(SIG_PPERIPH)
SERVMOD_N
SERVMOD_N[1..8]
SERVMOD_N[1..8]

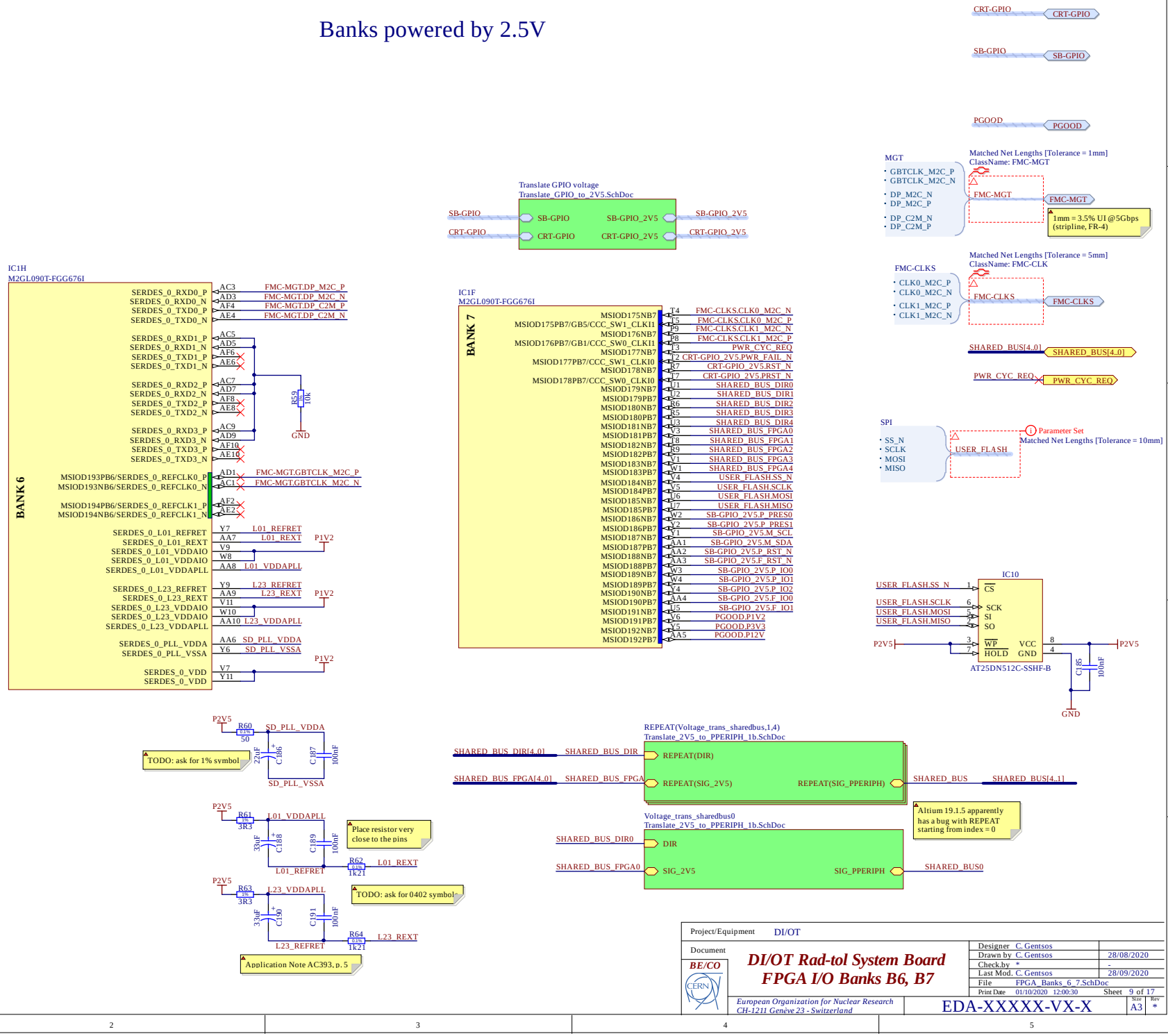
TODO: we might be able to afford changing SERVMOD direction in pairs, see if there are any negative implications.

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA I/O Banks B1, B2	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	28/09/2020
		File FPGA_Banks_1_2.SchDoc	
		Print Date 01/10/2020 12:00:29	Sheet 7 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

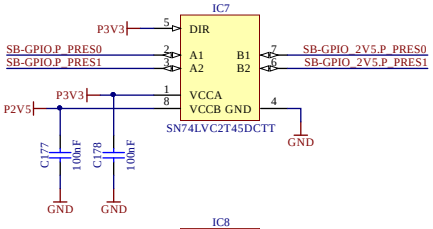


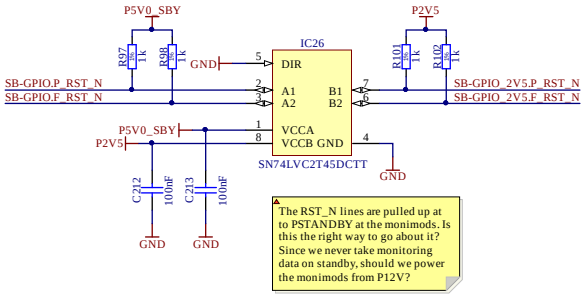
Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Voltage Translators	Designer C. Gentsos	
		Drawn by C. Gentsos	16/09/2020
		Check.by *	-
		Last Mod. C. Gentsos	01/10/2020
		File Translate_2V5_to_PPERIPH_1b.SchDoc	
		Print Date 01/10/2020 12:00:30	Sheet 8 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

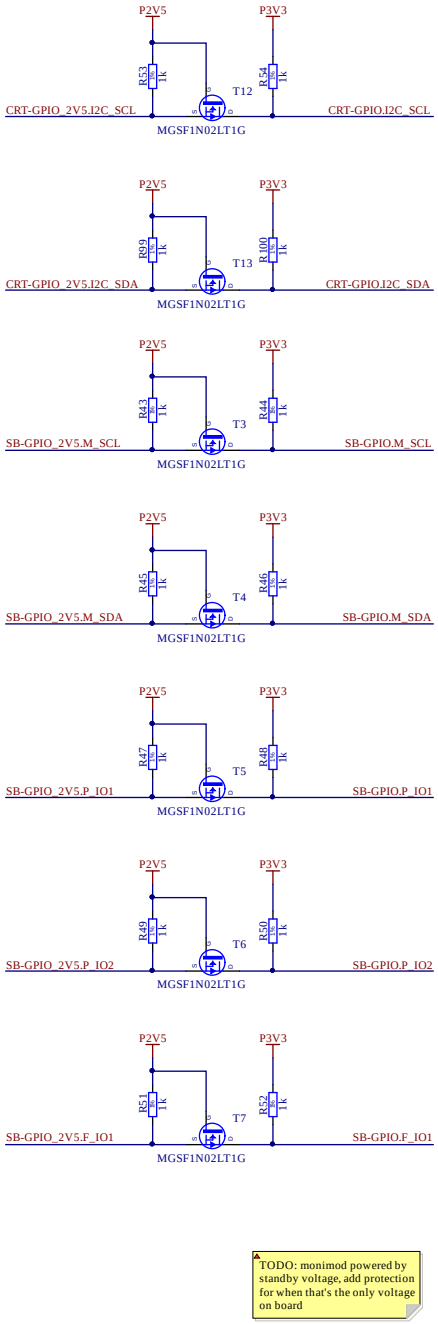
Banks powered by 2.5V

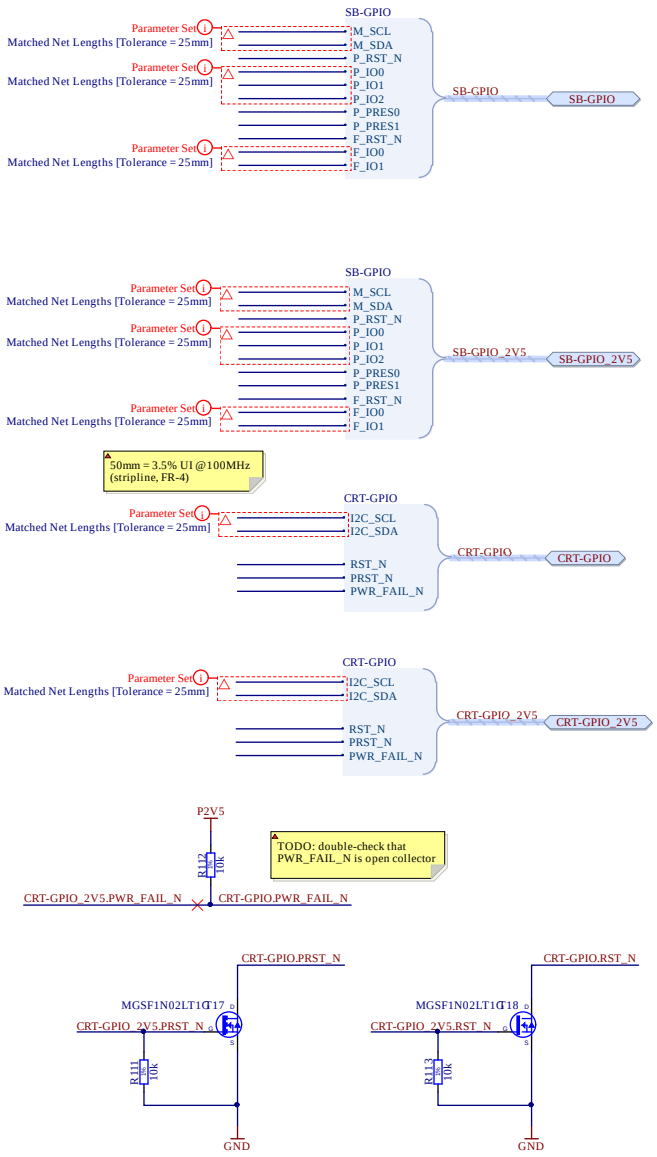


Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA I/O Banks B6, B7	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	28/09/2020
		File FPGA_Banks_6_7.SchDoc	
		Print Date 01/10/2020 12:00:30	Sheet 9 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

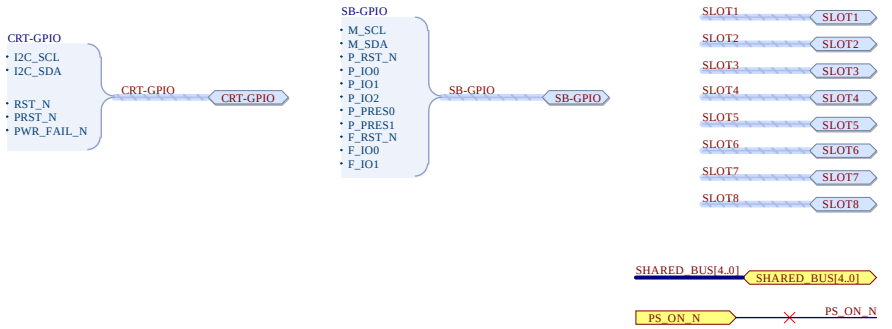




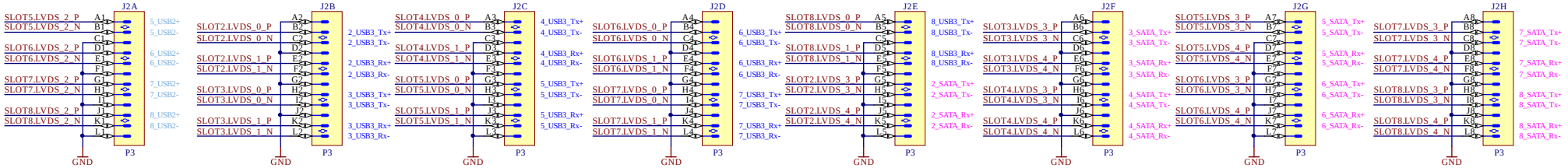




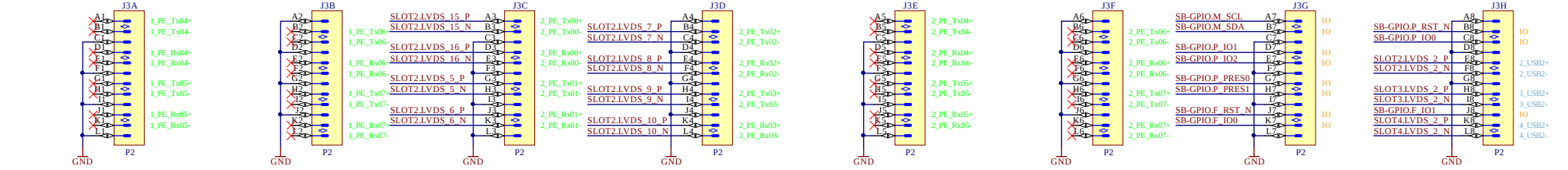
Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board GPIO Voltage Translators	Designer C. Gentsos	
		Drawn by C. Gentsos	23/09/2020
		Check.by *	-
		Last Mod. C. Gentsos	01/10/2020
		File Translate_GPIO_to_2V5.SchDoc	
		Print Date 01/10/2020 12:00:31	Sheet 10of 17
BE/CO CERN	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *



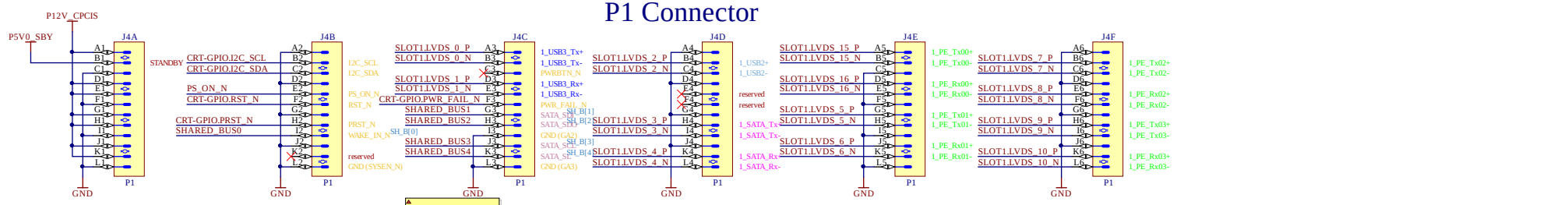
P3 Connector



P2 Connector



P1 Connector



TODO: how to handle PWRBTN?

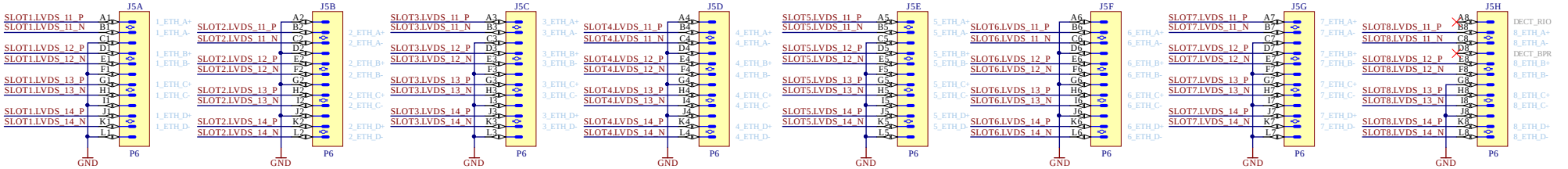
n_PE_Tx00 and n_PE_Rx00 diff pairs can carry Multi-Gigabit signals (2.1.6). 100Ohm impedance, 5mm tolerance

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board CPCI-S Backplane (1/2)	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	01/10/2020
		File CPCI-S_Backplane_P1-P3.SchDoc	
		Print Date 01/10/2020 12:00:32	Sheet 11 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

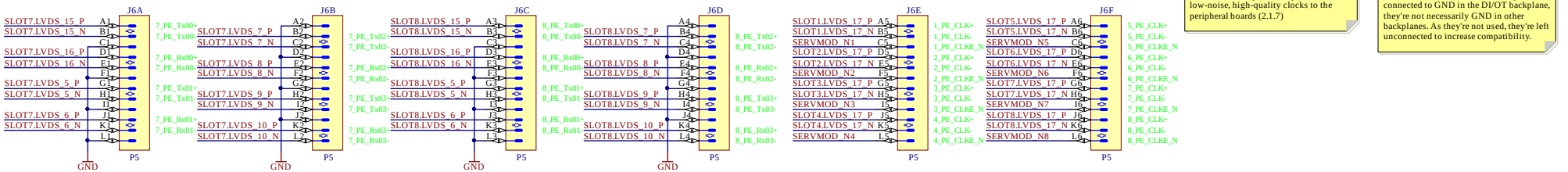
SLOT1 SLOT1
SLOT2 SLOT2
SLOT3 SLOT3
SLOT4 SLOT4
SLOT5 SLOT5
SLOT6 SLOT6
SLOT7 SLOT7
SLOT8 SLOT8

SERVMOD_N[1..8] SERVMOD_N[1..8]

P6 Connector



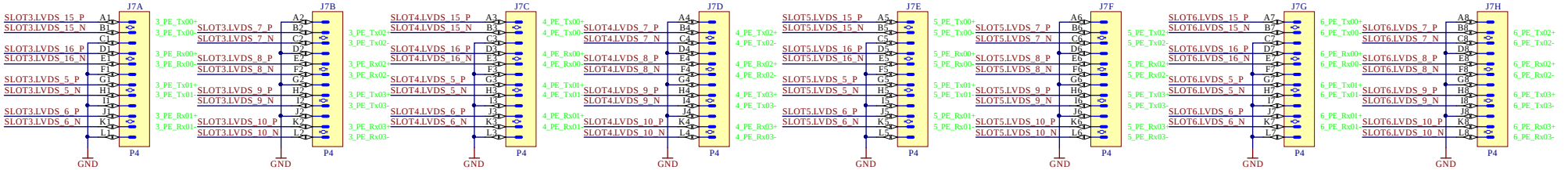
P5 Connector



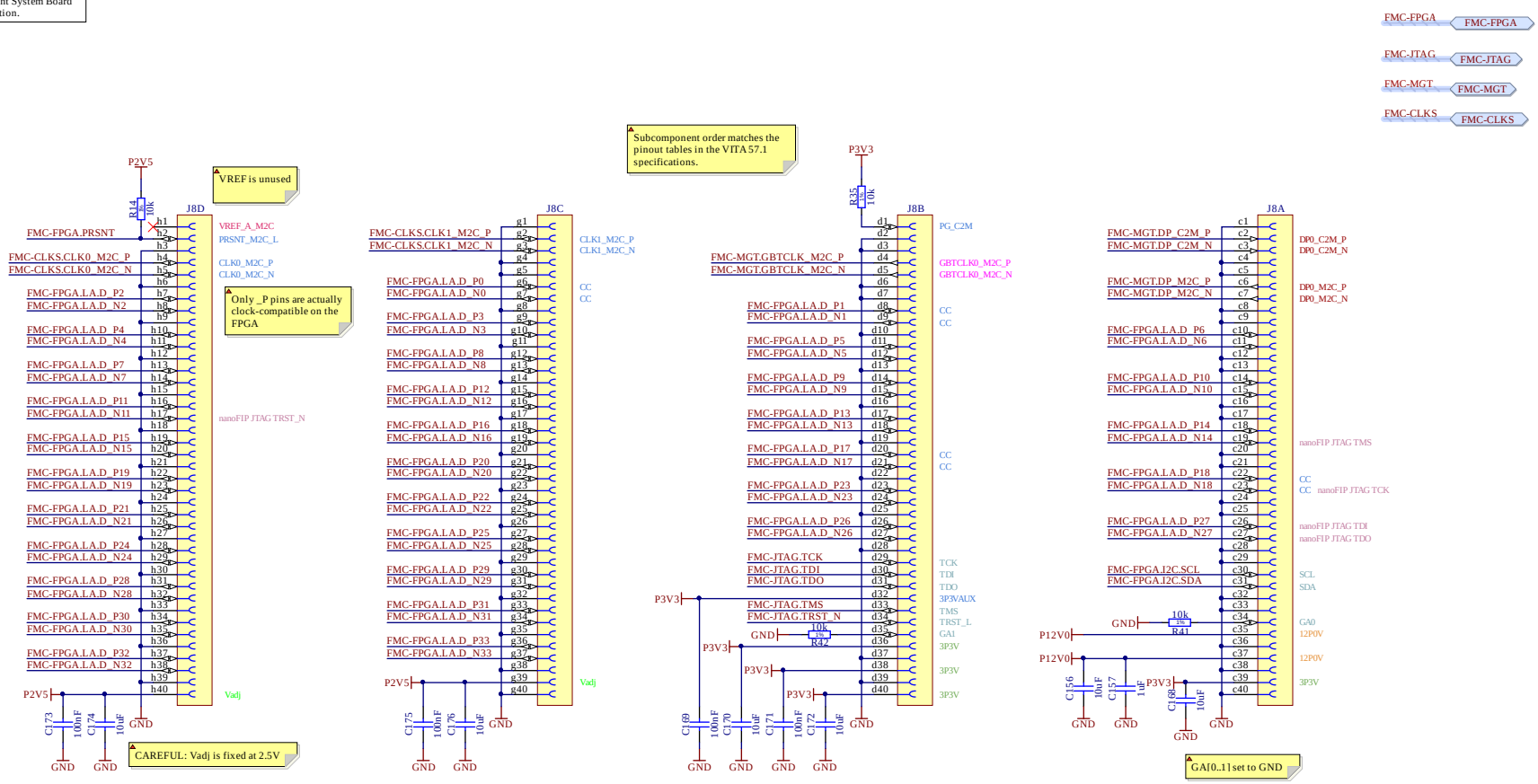
n_PE_CLK diff pairs will provide low-noise, high-quality clocks to the peripheral boards (2.1.7)

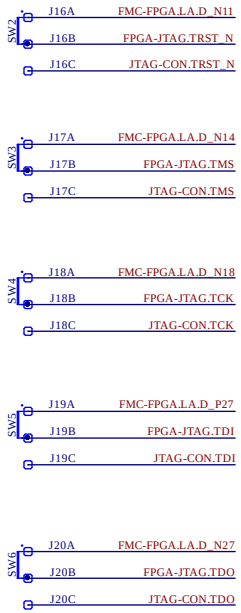
The DECT_RIO and DECT_BPR pins are connected to GND in the DI/OT backplane, they're not necessarily GND in other backplanes. As they're not used, they're left unconnected to increase compatibility.

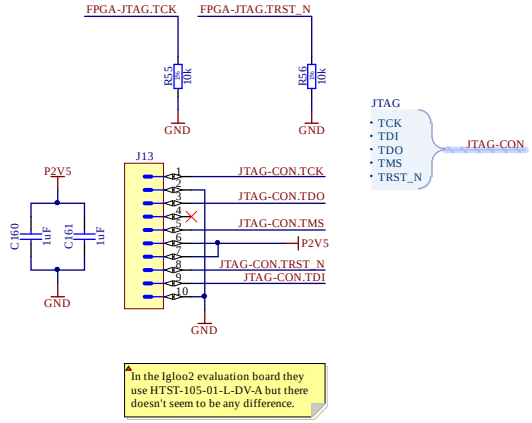
P4 Connector

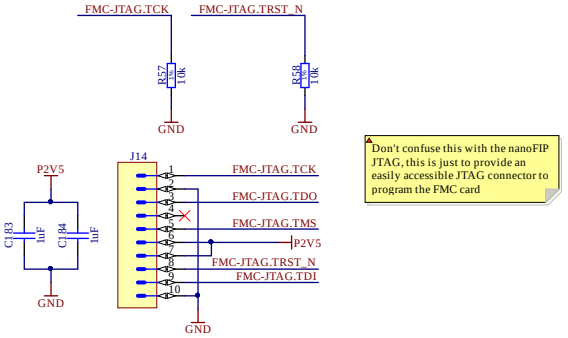


Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board CPCI-S Backplane (2/2)	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	01/10/2020
		File CPCI-S_Backplane_P4-P6.SchDoc	
		Print Date 01/10/2020 12:00:33	Sheet 12of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

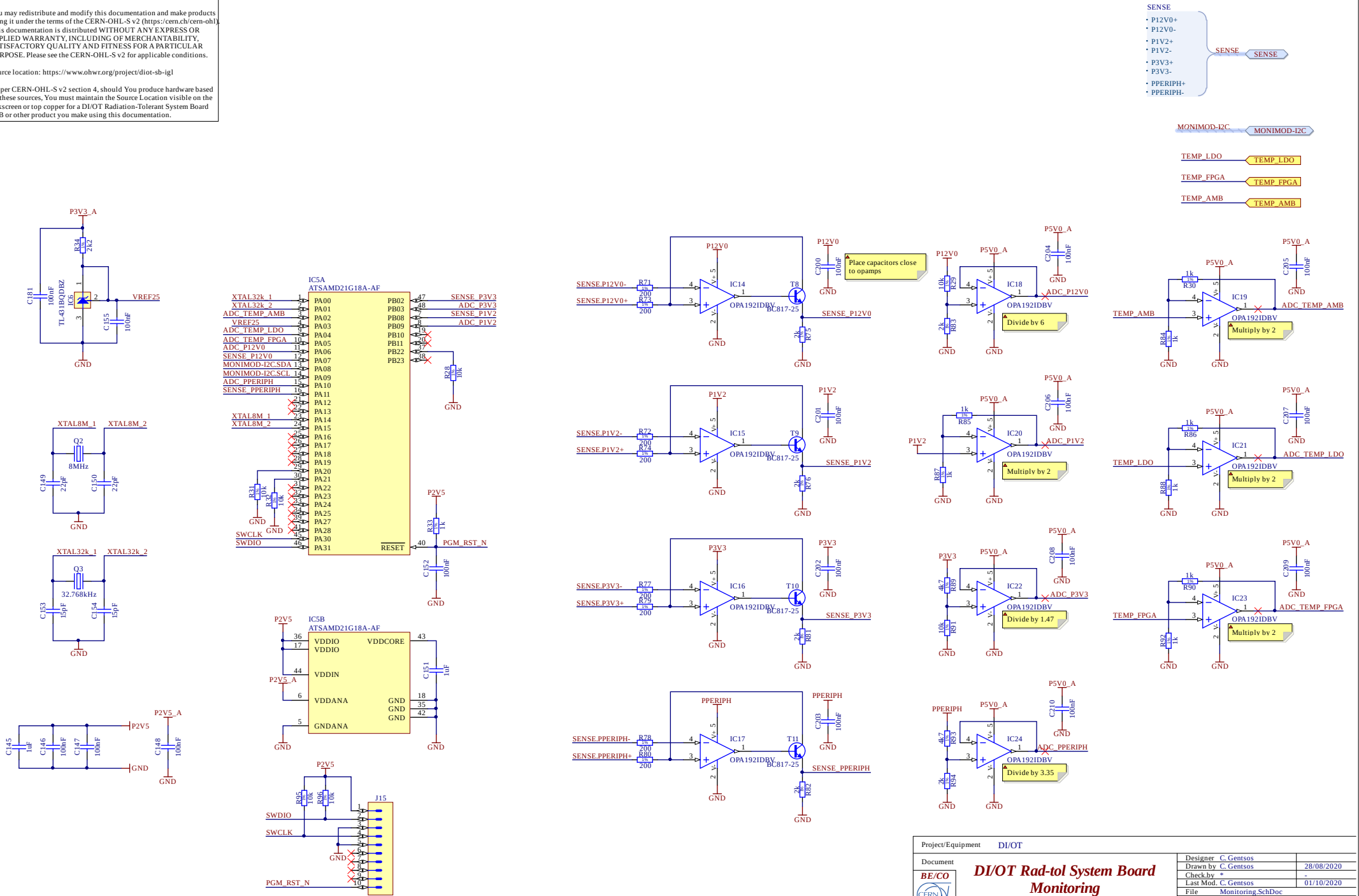








Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board JTAG Chains	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	28/09/2020
		File JTAG.SchDoc	
		Print Date 01/10/2020 12:00:35	Sheet 14of 17
BE/CO CERN	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *



Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Monitoring	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	01/10/2020
		File Monitoring.SchDoc	
		Print Date 01/10/2020 12:00:36	Sheet 16of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

LEDS[1..4] → LEDS[1..4]

PWR_CYC_REQ → PWR_CYC_REQ

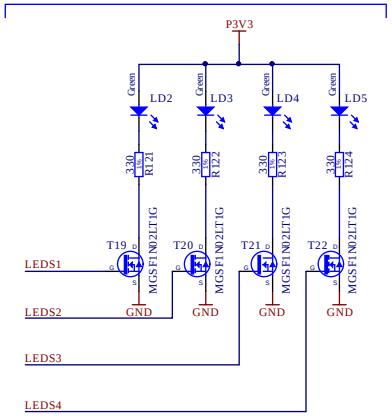
PS_ON_N → PS_ON_N

TEMP_AMB → TEMP_AMB

OSC_25MHz_3V3 → OSC_25MHz_3V3

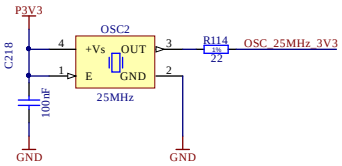
OSC_40MHz_3V3 → OSC_40MHz_3V3

User LEDs

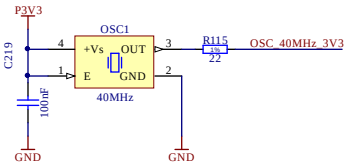


TODO: We have the pins, do we want to double the clocks in case someone likes redundancy?

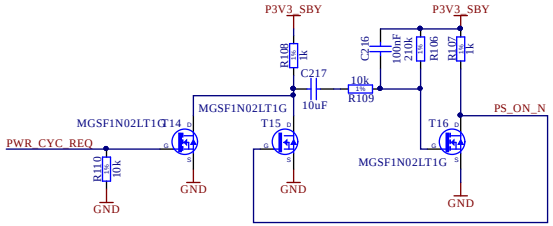
25MHz oscillator



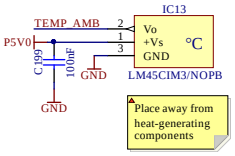
40MHz oscillator



Power cycle pulse generator



Ambient temp sensor



Place away from heat-generating components

ESD Protection

ESD strips discharge resistors (CPCI-S.0 REQ 3.71)

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Miscellaneous	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	28/09/2020
		File Top_Misc.SchDoc	
		Print Date 01/10/2020 12:00:37	Sheet 17of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *