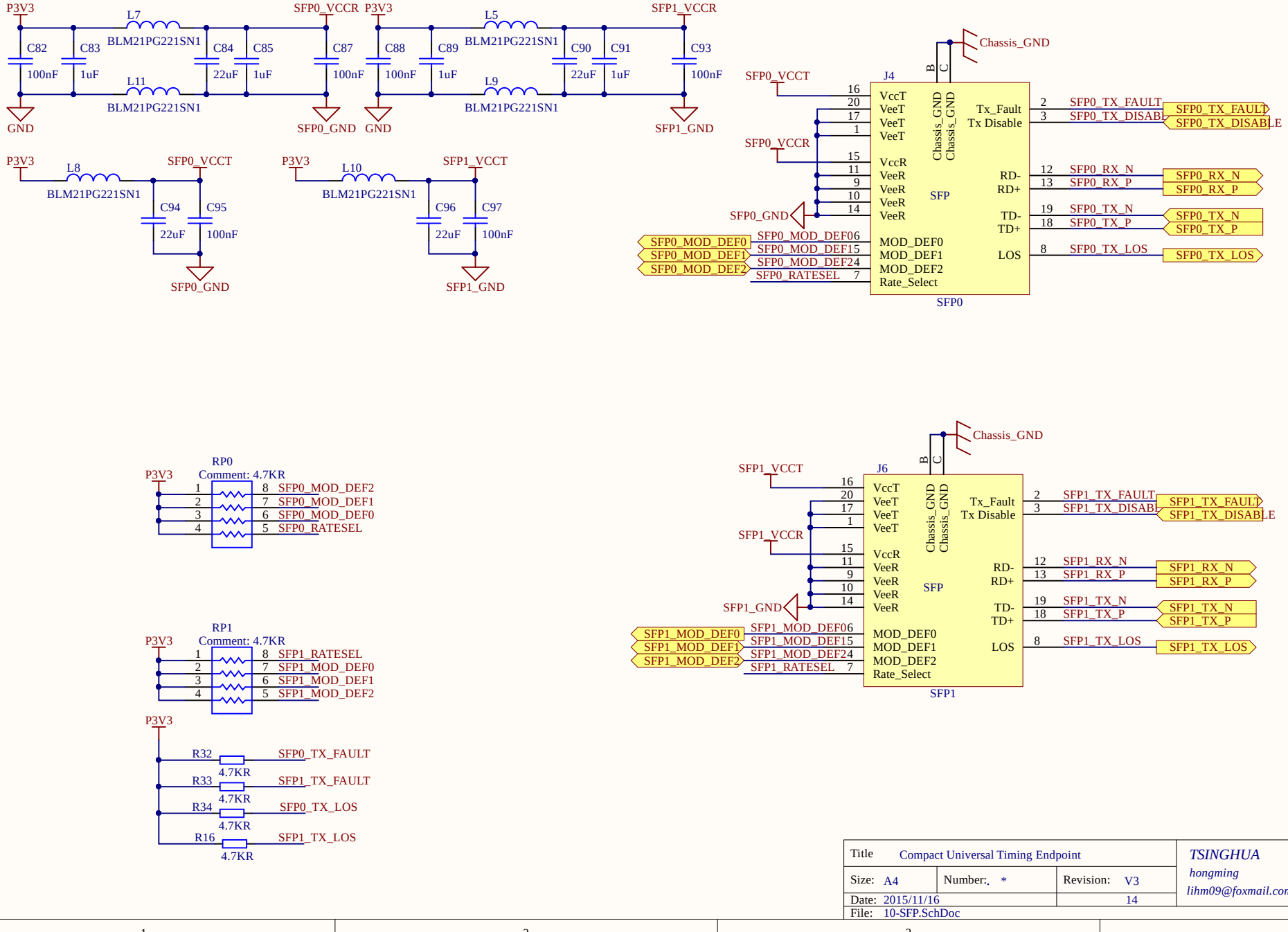
P3V3
L7
BLM21PG221SN1
C82
100nF
C83
1uF
C84
22uF
C85
1uF
C87
100nF
L11
BLM21PG221SN1
GND
SFP0_VCCR
SFP0_GND
P3V3
L5
BLM21PG221SN1
C88
100nF
C89
1uF
C90
22uF
C91
1uF
C93
100nF
L9
BLM21PG221SN1
GND
SFP1_VCCR
SFP1_GND
P3V3
L8
BLM21PG221SN1
C94
22uF
C95
100nF
SFP0_VCCT
SFP0_GND
P3V3
L10
BLM21PG221SN1
C96
22uF
C97
100nF
SFP1_VCCT
SFP1_GND
Chassis_GND
J4
SFP0_VCCT
SFP0_VCCR
SFP0_GND
SFP0_MOD_DEF0
SFP0_MOD_DEF1
SFP0_MOD_DEF2
VccT
VeeT
VeeT
VeeT
VccR
VeeR
VeeR
VeeR
VeeR
MOD_DEF0
MOD_DEF1
MOD_DEF2
Rate_Select
Chassis_GND
Chassis_GND
SFP
Tx_Fault
Tx Disable
RD-
RD+
TD-
TD+
LOS
SFP0_MOD_DEF06
SFP0_MOD_DEF15
SFP0_MOD_DEF24
SFP0_RATESEL
SFP0_TX_FAULT
SFP0_TX_DISABLE
SFP0_RX_N
SFP0_RX_P
SFP0_TX_N
SFP0_TX_P
SFP0_TX_LOS
SFP0
RP0
Comment: 4.7KR
P3V3
SFP0_MOD_DEF2
SFP0_MOD_DEF1
SFP0_MOD_DEF0
SFP0_RATESEL
RP1
Comment: 4.7KR
P3V3
SFP1_RATESEL
SFP1_MOD_DEF0
SFP1_MOD_DEF1
SFP1_MOD_DEF2
P3V3
R32
4.7KR
SFP0_TX_FAULT
R33
4.7KR
SFP1_TX_FAULT
R34
4.7KR
SFP0_TX_LOS
R16
4.7KR
SFP1_TX_LOS
Chassis_GND
J6
SFP1_VCCT
SFP1_VCCR
SFP1_GND
SFP1_MOD_DEF0
SFP1_MOD_DEF1
SFP1_MOD_DEF2
VccT
VeeT
VeeT
VeeT
VccR
VeeR
VeeR
VeeR
VeeR
MOD_DEF0
MOD_DEF1
MOD_DEF2
Rate_Select
Chassis_GND
Chassis_GND
SFP
Tx_Fault
Tx Disable
RD-
RD+
TD-
TD+
LOS
SFP1_MOD_DEF06
SFP1_MOD_DEF15
SFP1_MOD_DEF24
SFP1_RATESEL
SFP1_TX_FAULT
SFP1_TX_DISABLE
SFP1_RX_N
SFP1_RX_P
SFP1_TX_N
SFP1_TX_P
SFP1_TX_LOS
SFP1
Title
Compact Universal Timing Endpoint
Size: A4
Number: *
Revision: V3
Date: 2015/11/16
14
File: 10-SFP.SchDoc
TSINGHUA
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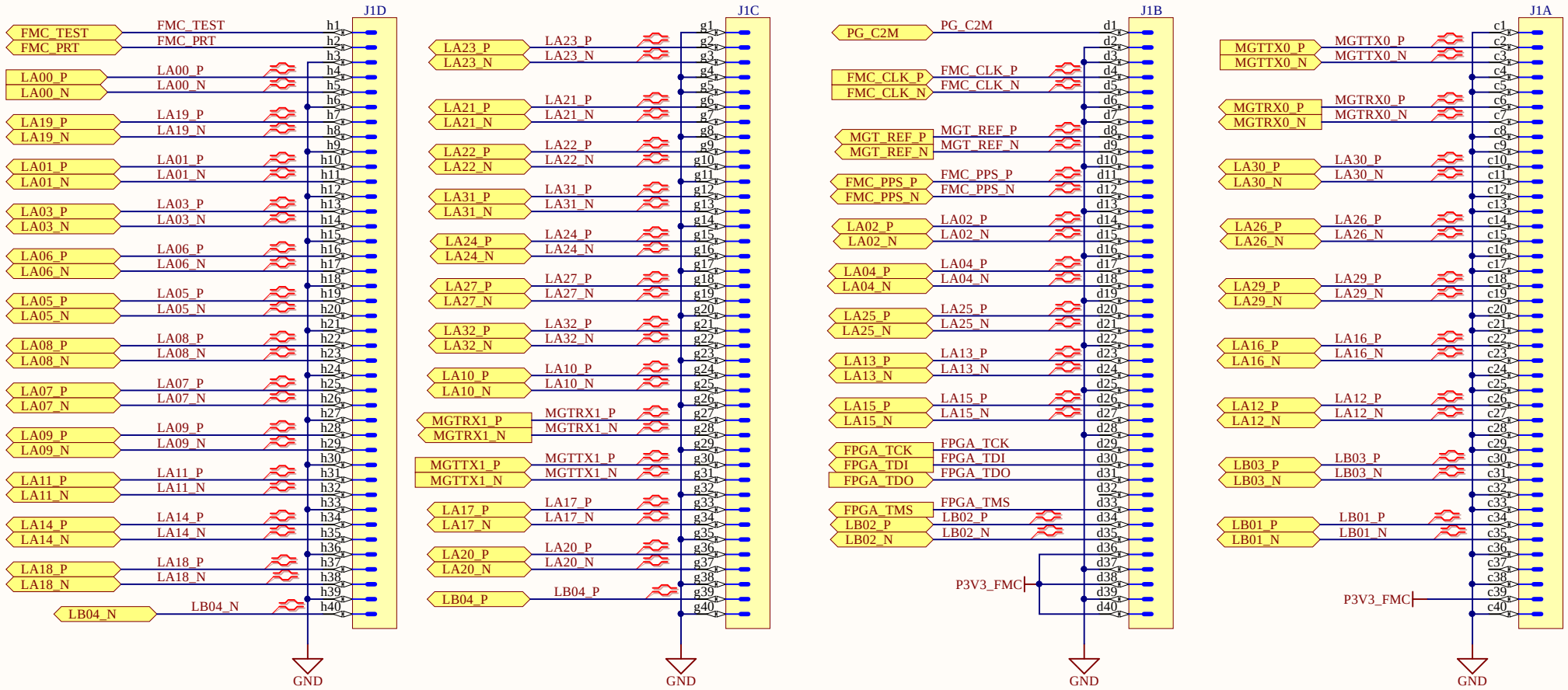
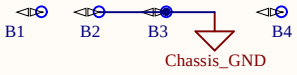


Rounting Differences among all FMC Differential Pairs are within 150 mil



Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 11-FMC_Connector.SchDoc			

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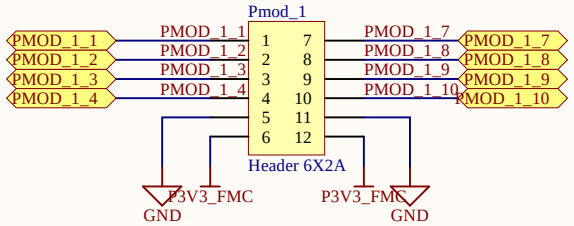

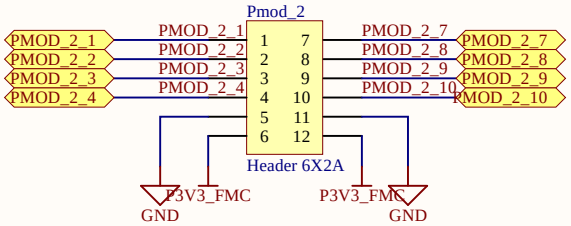

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 12-Pmod_Connector.SchDoc			

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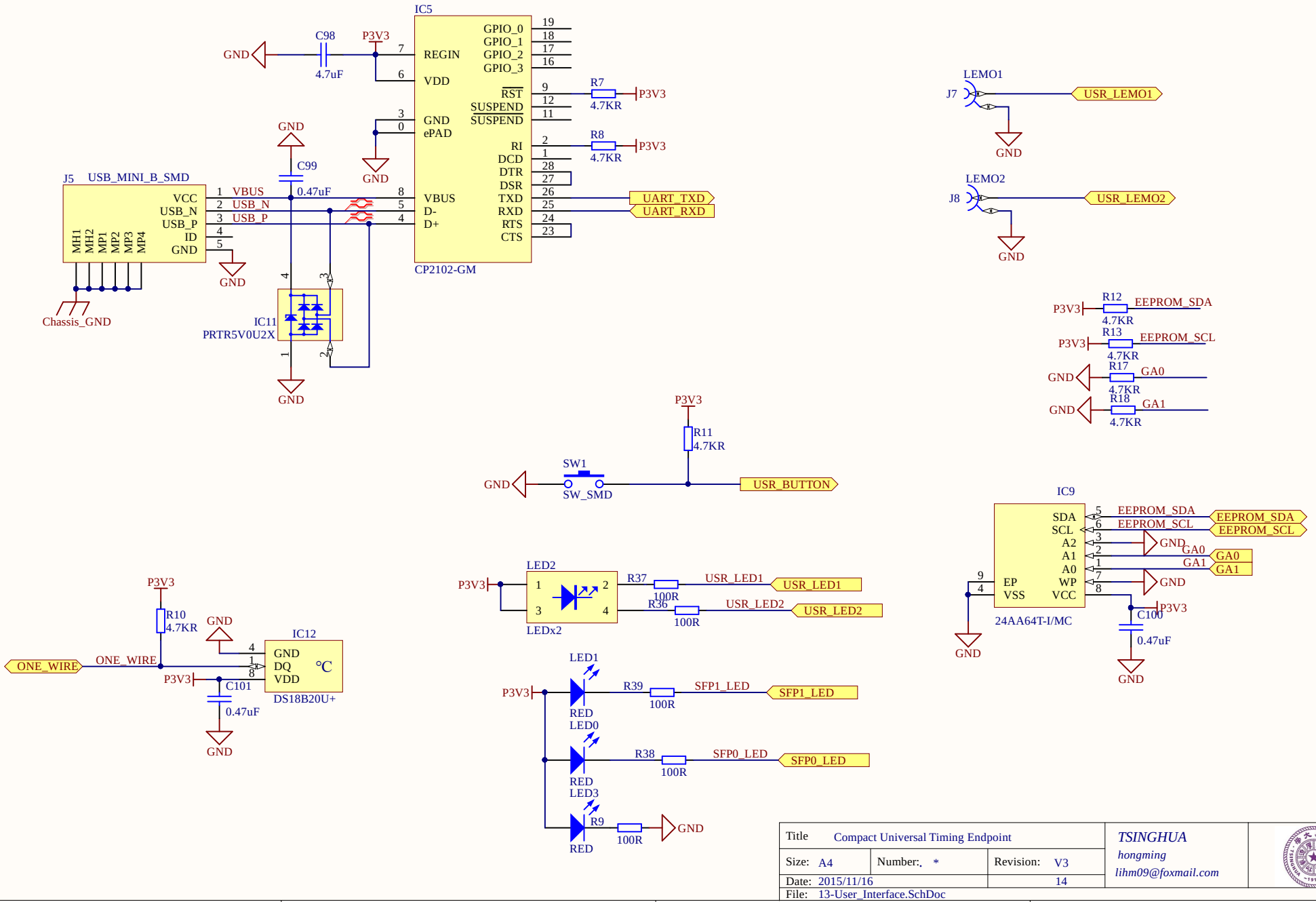

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 13-User_Interface.SchDoc			

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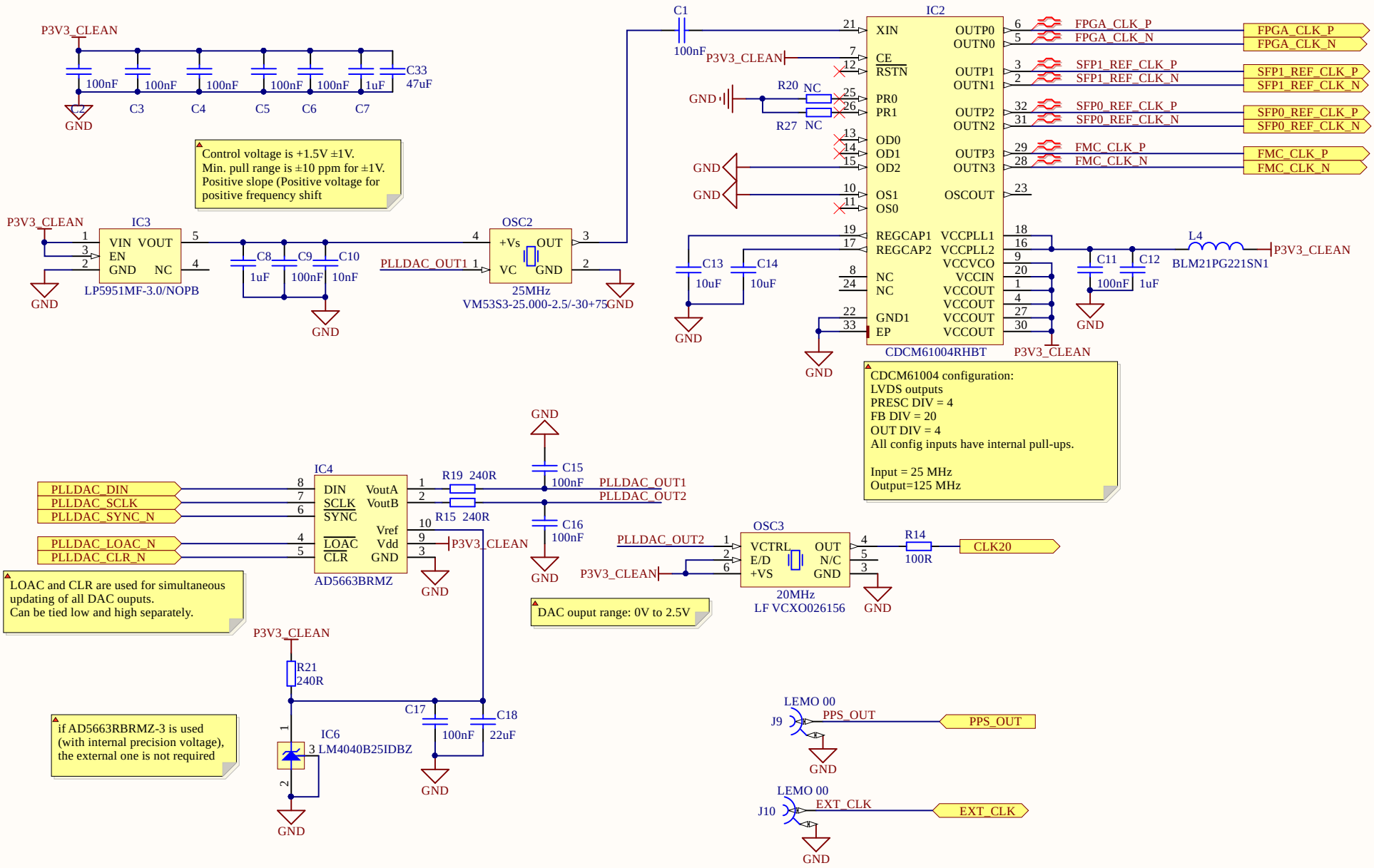

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 1-Clocks.SchDoc			

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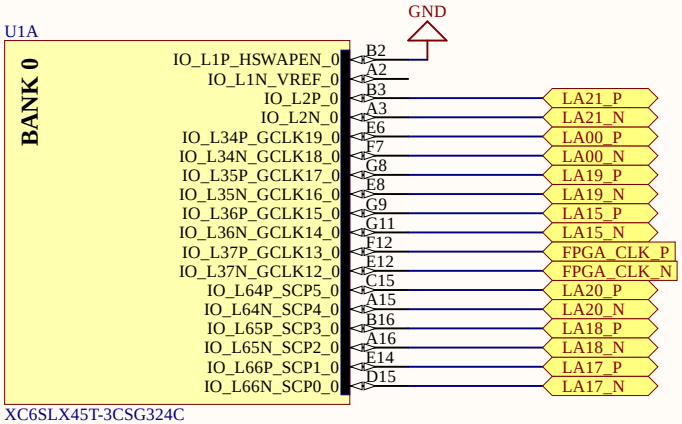
Bank 0 Supports differential output



Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 2-FPGA_bank0.SchDoc			

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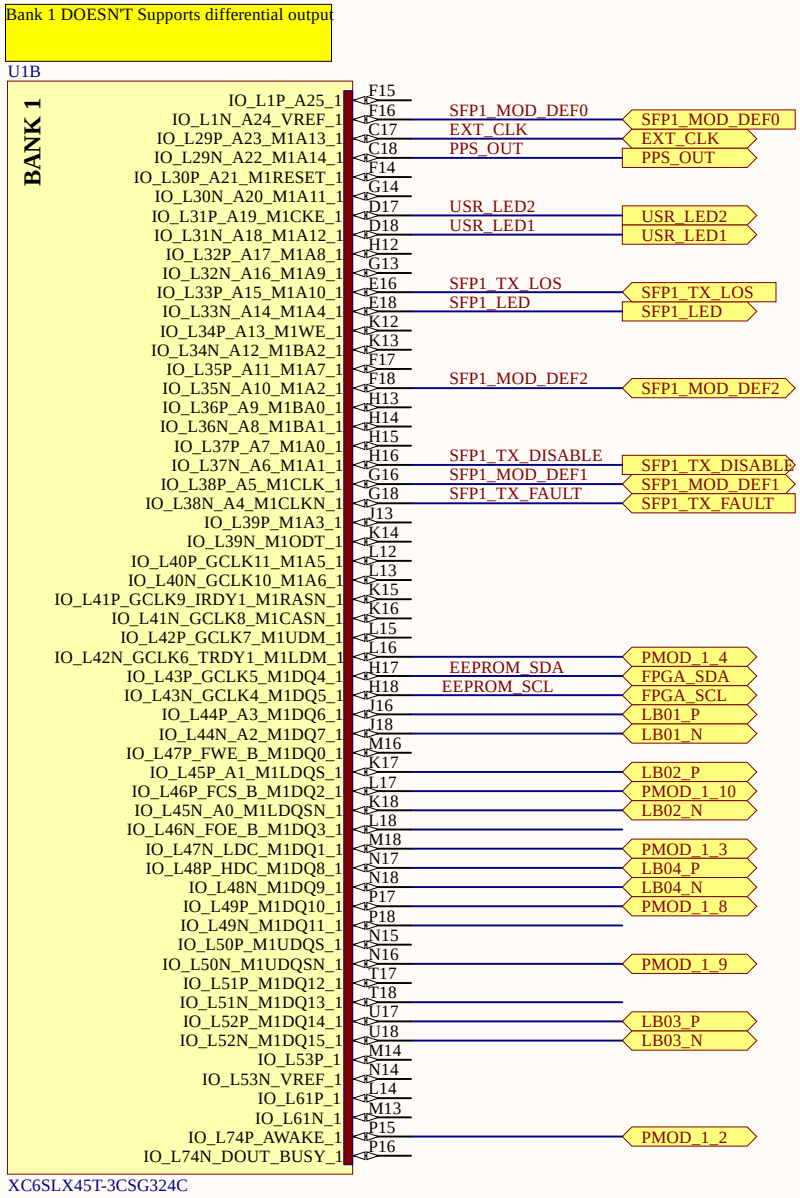

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 3-FPGA_bank1.SchDoc			

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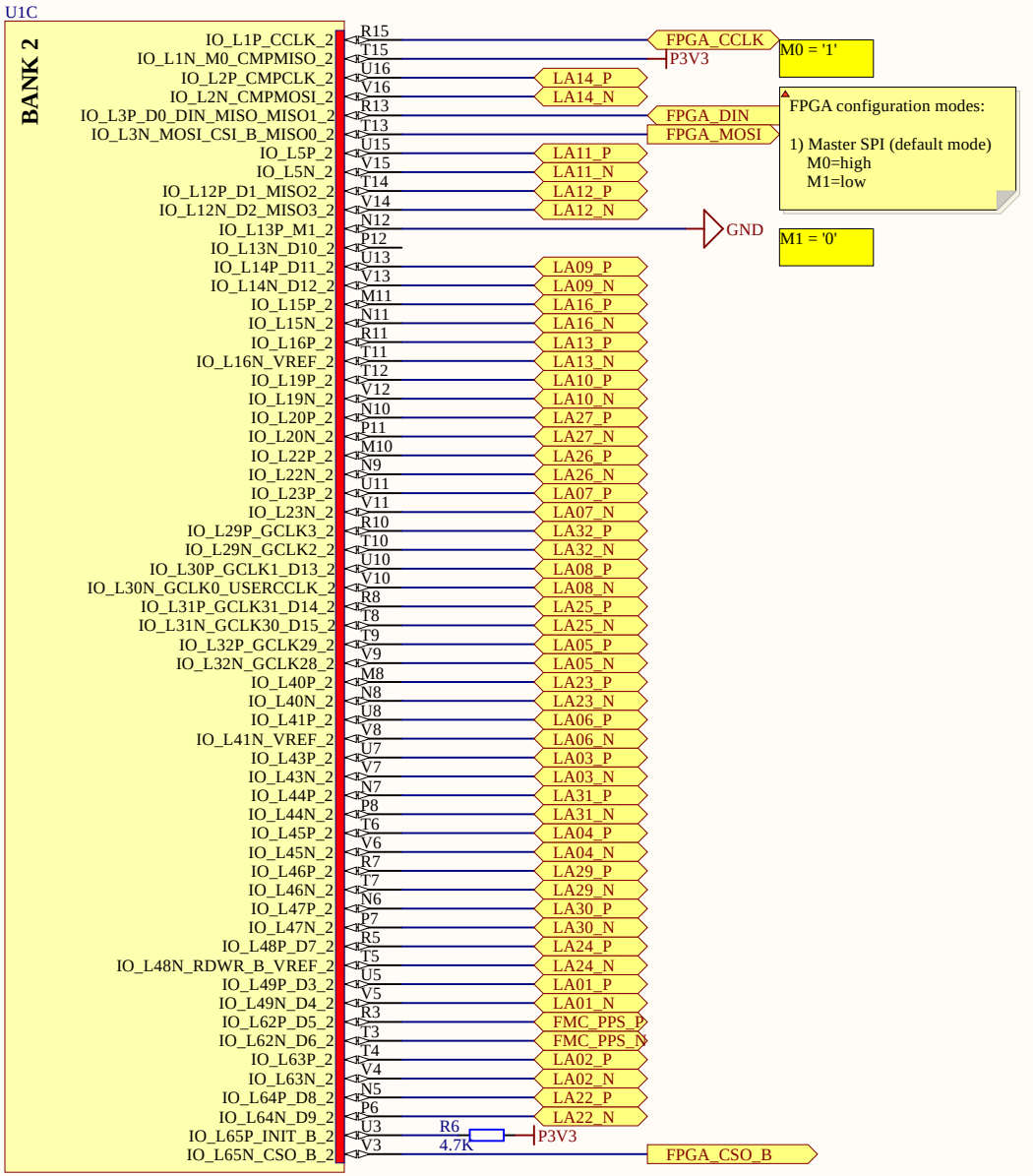

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 4-FPGA_bank2.SchDoc			

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Bank 3 DOESN'T Supports differential output

U1D

BANK 3

IO_L1P_3	N4	
IO_L1N_VREF_3	N3	
IO_L2P_3	P4	
IO_L2N_3	P3	PMOD_1_7
IO_L31P_3	L6	
IO_L31N_VREF_3	M5	
IO_L32P_M3DQ14_3	U2	FMC_PRT
IO_L32N_M3DQ15_3	U1	FMC_TEST
IO_L33P_M3DQ12_3	T2	PG_C2M
IO_L33N_M3DQ13_3	T1	PMOD_1_1
IO_L34P_M3UDQS_3	P2	PMOD_2_3
IO_L34N_M3UDQSN_3	P1	PMOD_2_10
IO_L35P_M3DQ10_3	N2	PMOD_2_4
IO_L35N_M3DQ11_3	N1	PMOD_2_2
IO_L36P_M3DQ8_3	M3	
IO_L36N_M3DQ9_3	M1	PMOD_2_8
IO_L37P_M3DQ0_3	L2	PMOD_2_9
IO_L37N_M3DQ1_3	L1	PMOD_2_7
IO_L38P_M3DQ2_3	K2	PMOD_2_1
IO_L38N_M3DQ3_3	K1	USR_LEMO1
IO_L39P_M3LDQS_3	L4	
IO_L39N_M3LDQSN_3	L3	
IO_L40P_M3DQ6_3	J3	USR_LEMO2
IO_L40N_M3DQ7_3	J1	ONE_WIRE
IO_L41P_GCLK27_M3DQ4_3	H2	UART_RX
IO_L41N_GCLK26_M3DQ5_3	H1	CLK20
IO_L42P_GCLK25_TRDY2_M3UDM_3	K4	
IO_L42N_GCLK24_M3LDM_3	K3	
IO_L43P_GCLK23_M3RASN_3	L5	
IO_L43N_GCLK22_IRDY2_M3CASN_3	K5	
IO_L44P_GCLK21_M3A5_3	H4	
IO_L44N_GCLK20_M3A6_3	H3	UART_TX
IO_L45P_M3A3_3	L7	
IO_L45N_M3ODT_3	K6	
IO_L46P_M3CLK_3	G3	USR_BUTTON
IO_L46N_M3CLKN_3	G1	CLR_N
IO_L47P_M3A0_3	J7	
IO_L47N_M3A1_3	J6	
IO_L48P_M3BA0_3	F2	SFP0_TX_DISABLE
IO_L48N_M3BA1_3	F1	LOAC_N
IO_L49P_M3A7_3	H6	
IO_L49N_M3A2_3	H5	
IO_L50P_M3WE_3	E3	SFP0_MOD_DEF1
IO_L50N_M3BA2_3	E1	PLLDAC_SYNC_N
IO_L51P_M3A10_3	F4	
IO_L51N_M3A4_3	F3	SFP0_TX_FAULT
IO_L52P_M3A8_3	D2	SFP0_MOD_DEF0
IO_L52N_M3A9_3	D1	PLLDAC_SCLK
IO_L53P_M3CKE_3	H7	
IO_L53N_M3A12_3	G6	
IO_L54P_M3RESET_3	E4	SFP0_MOD_DEF2
IO_L54N_M3A11_3	D3	SFP0_TX_LOS
IO_L55P_M3A13_3	F6	
IO_L55N_M3A14_3	F5	
IO_L83P_3	C2	SFP0_LED
IO_L83N_VREF_3	C1	DIN

XC6SLX45T-3CSG324C

PLLDAC_CLR_N
PLLDAC_LOAC_N
PLLDAC_SYNC_N
PLLDAC_SCLK
PLLDAC_DIN

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 5-FPGA_bank3.SchDoc			

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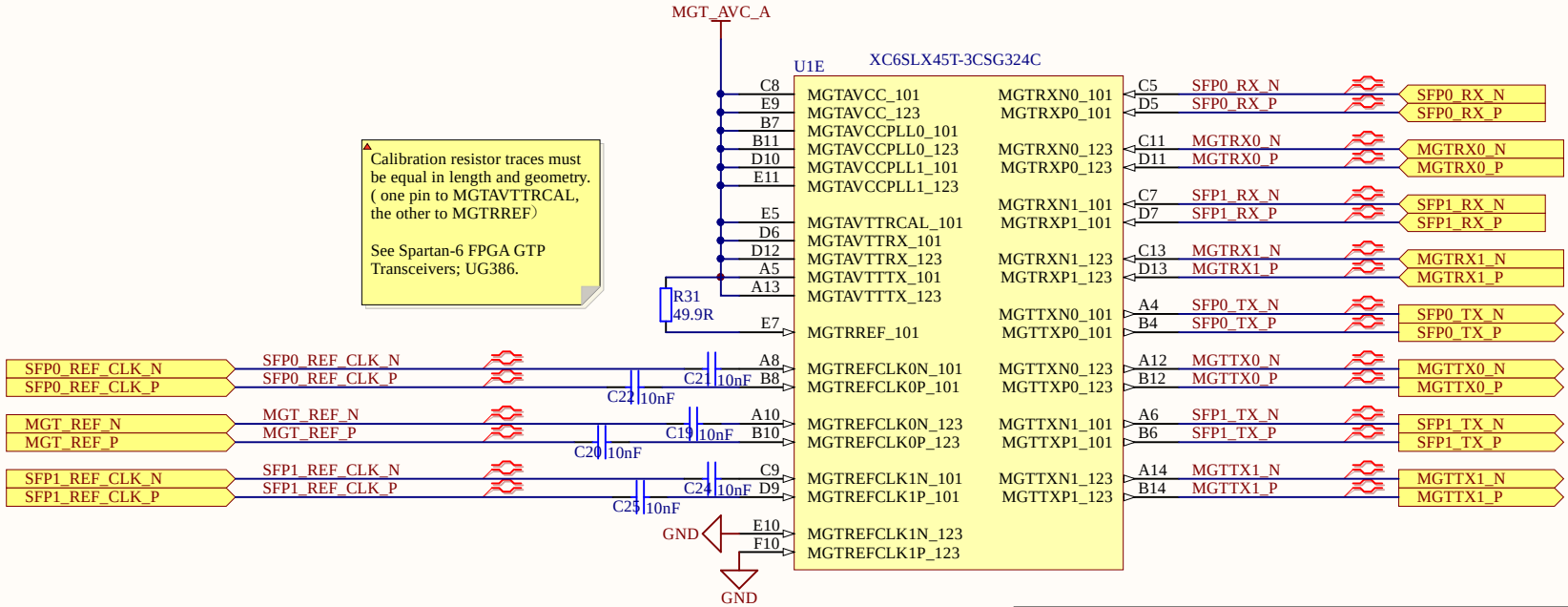

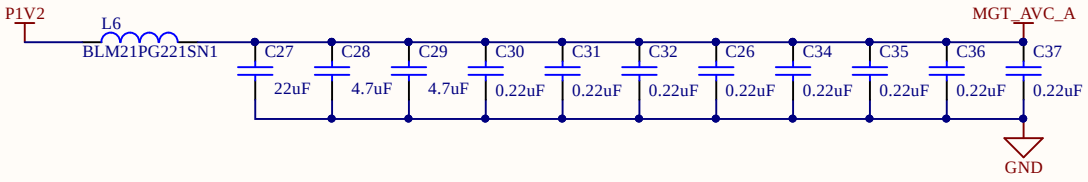

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 6-FPGA_GTP.SchDoc			

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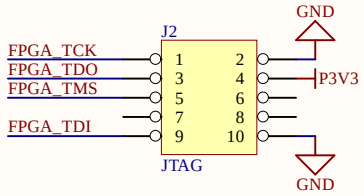
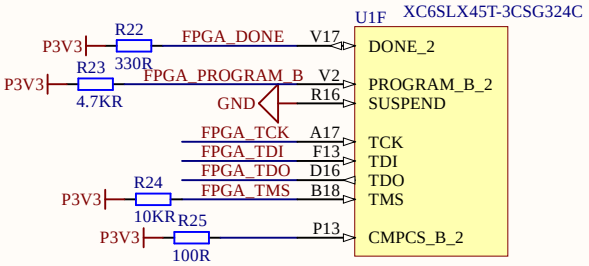
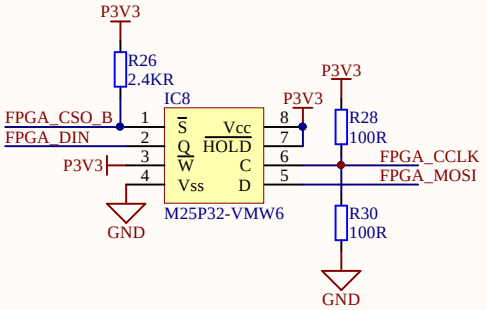
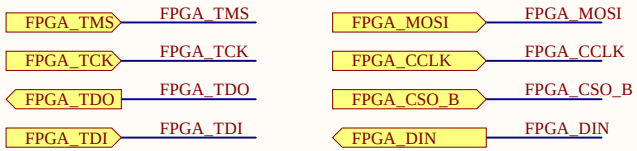


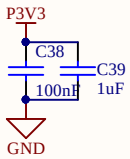




When CS_n is high, Q will stay high impedence



CCLK Termination. See Spartan6 FPGA Configuration User Guide P52



Title	Compact Universal Timing Endpoint		
Size: A4	Number:. *	Revision: V3	
Date: 2015/11/16		14	
File: 7-FPGA_Config.SchDoc			

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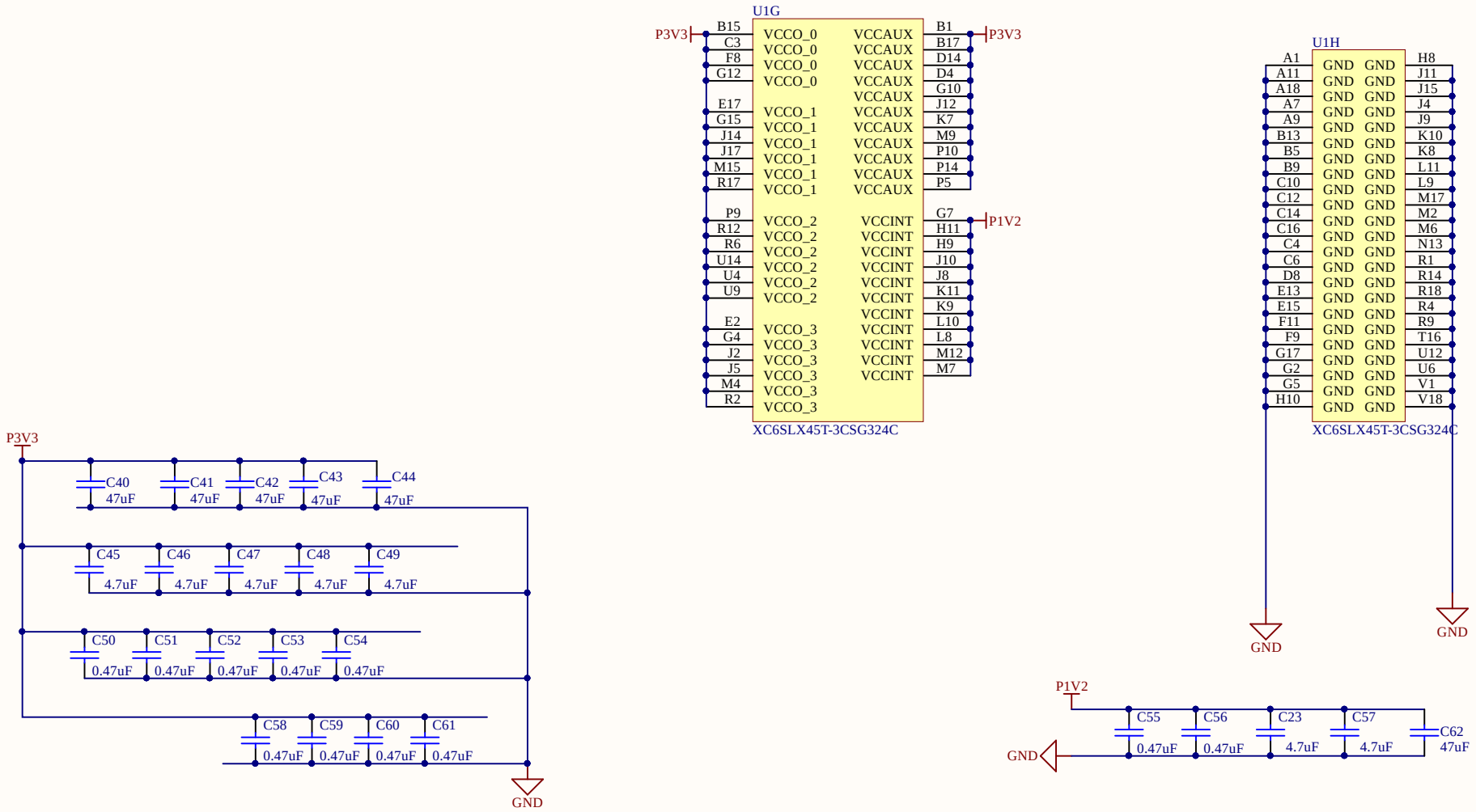

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 8-FPGA_Power.SchDoc			

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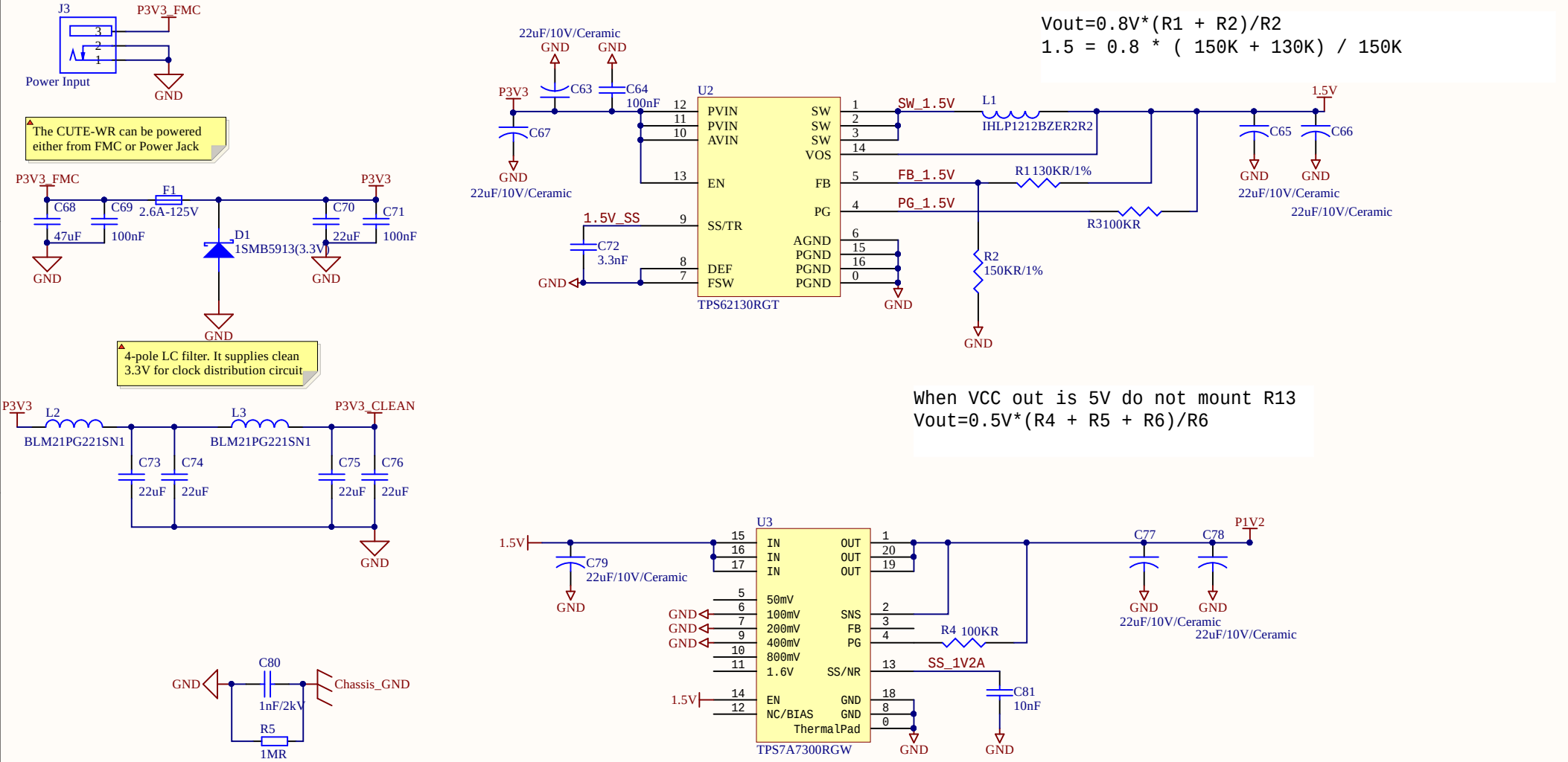

Title	Compact Universal Timing Endpoint		
Size: A4	Number: *	Revision: V3	
Date: 2015/11/16		14	
File: 9-Power.SchDoc			

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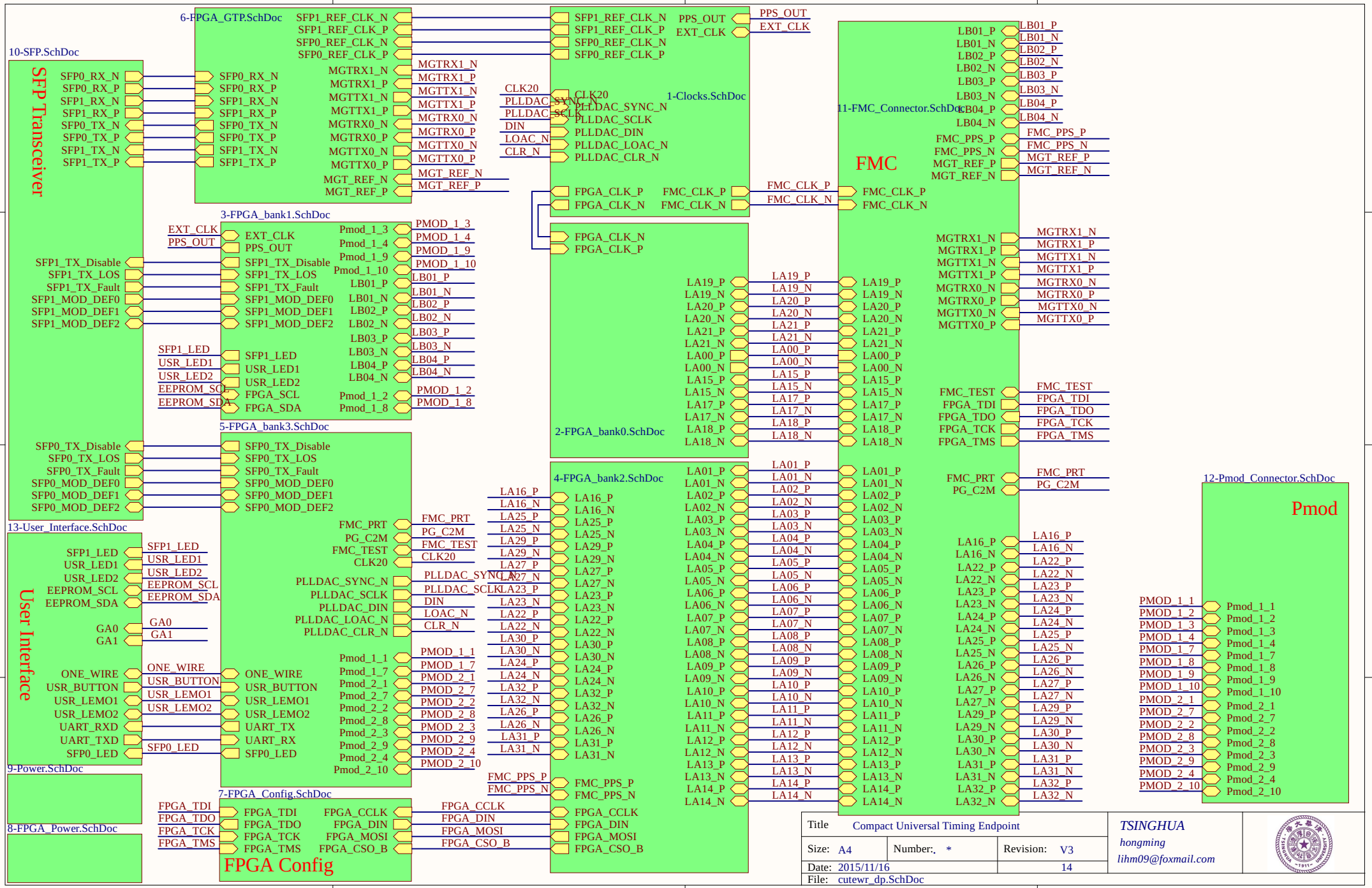
10-SFP.SchDoc
SFP Transceiver
SFP0_RX_N
SFP0_RX_P
SFP1_RX_N
SFP1_RX_P
SFP0_TX_N
SFP0_TX_P
SFP1_TX_N
SFP1_TX_P
6-FPGA_GTP.SchDoc
SFP1_REF_CLK_N
SFP1_REF_CLK_P
SFP0_REF_CLK_N
SFP0_REF_CLK_P
MGTRX1_N
MGTRX1_P
MGTTX1_N
MGTTX1_P
MGTRX0_N
MGTRX0_P
MGTTX0_N
MGTTX0_P
MGT_REF_N
MGT_REF_P
CLK20
PLLDAC_SYNC_N
PLLDAC_SCLK
DIN
LOAC_N
CLR_N
1-Clocks.SchDoc
PLLDAC_SYNC_N
PLLDAC_SCLK
PLLDAC_DIN
PLLDAC_LOAC_N
PLLDAC_CLR_N
FPGA_CLK_P
FPGA_CLK_N
FMC_CLK_P
FMC_CLK_N
PPS_OUT
EXT_CLK
11-FMC_Connector.SchDoc
FMC
LB01_P
LB01_N
LB02_P
LB02_N
LB03_P
LB03_N
LB04_P
LB04_N
FMC_PPS_P
FMC_PPS_N
MGT_REF_P
MGT_REF_N
3-FPGA_bank1.SchDoc
EXT_CLK
PPS_OUT
SFP1_TX_Disable
SFP1_TX_LOS
SFP1_TX_Fault
SFP1_MOD_DEF0
SFP1_MOD_DEF1
SFP1_MOD_DEF2
SFP1_LED
USR_LED1
USR_LED2
EEPROM_SCL
EEPROM_SDA
FPGA_SCL
FPGA_SDA
Pmod_1_3
Pmod_1_4
Pmod_1_9
Pmod_1_10
Pmod_1_2
Pmod_1_8
PMOD_1_3
PMOD_1_4
PMOD_1_9
PMOD_1_10
PMOD_1_2
PMOD_1_8
2-FPGA_bank0.SchDoc
LA19_P
LA19_N
LA20_P
LA20_N
LA21_P
LA21_N
LA00_P
LA00_N
LA15_P
LA15_N
LA17_P
LA17_N
LA18_P
LA18_N
5-FPGA_bank3.SchDoc
SFP0_TX_Disable
SFP0_TX_LOS
SFP0_TX_Fault
SFP0_MOD_DEF0
SFP0_MOD_DEF1
SFP0_MOD_DEF2
FMC_PRT
PG_C2M
FMC_TEST
CLK20
PLLDAC_SYNC_N
PLLDAC_SCLK
PLLDAC_DIN
PLLDAC_LOAC_N
PLLDAC_CLR_N
LOAC_N
CLR_N
Pmod_1_1
Pmod_1_7
Pmod_2_1
Pmod_2_7
Pmod_2_2
Pmod_2_8
Pmod_2_3
Pmod_2_9
Pmod_2_4
Pmod_2_10
PMOD_1_1
PMOD_1_7
PMOD_2_1
PMOD_2_7
PMOD_2_2
PMOD_2_8
PMOD_2_3
PMOD_2_9
PMOD_2_4
PMOD_2_10
4-FPGA_bank2.SchDoc
LA16_P
LA16_N
LA25_P
LA25_N
LA29_P
LA29_N
LA27_P
LA27_N
LA23_P
LA23_N
LA22_P
LA22_N
LA30_P
LA30_N
LA24_P
LA24_N
LA32_P
LA32_N
LA26_P
LA26_N
LA31_P
LA31_N
LA01_P
LA01_N
LA02_P
LA02_N
LA03_P
LA03_N
LA04_P
LA04_N
LA05_P
LA05_N
LA06_P
LA06_N
LA07_P
LA07_N
LA08_P
LA08_N
LA09_P
LA09_N
LA10_P
LA10_N
LA11_P
LA11_N
LA12_P
LA12_N
LA13_P
LA13_N
LA14_P
LA14_N
12-Pmod_Connector.SchDoc
Pmod
13-User_Interface.SchDoc
User Interface
SFP1_LED
USR_LED1
USR_LED2
EEPROM_SCL
EEPROM_SDA
GA0
GA1
ONE_WIRE
USR_BUTTON
USR_LEMO1
USR_LEMO2
UART_RXD
UART_TXD
SFP0_LED
UART_TX
UART_RX
9-Power.SchDoc
8-FPGA_Power.SchDoc
7-FPGA_Config.SchDoc
FPGA_TDI
FPGA_TDO
FPGA_TCK
FPGA_TMS
FPGA_CCLK
FPGA_DIN
FPGA_MOSI
FPGA_CSO_B
FPGA Config
Title Compact Universal Timing Endpoint
Size: A4
Number: *
Revision: V3
Date: 2015/11/16
File: cutewr_dp.SchDoc
14
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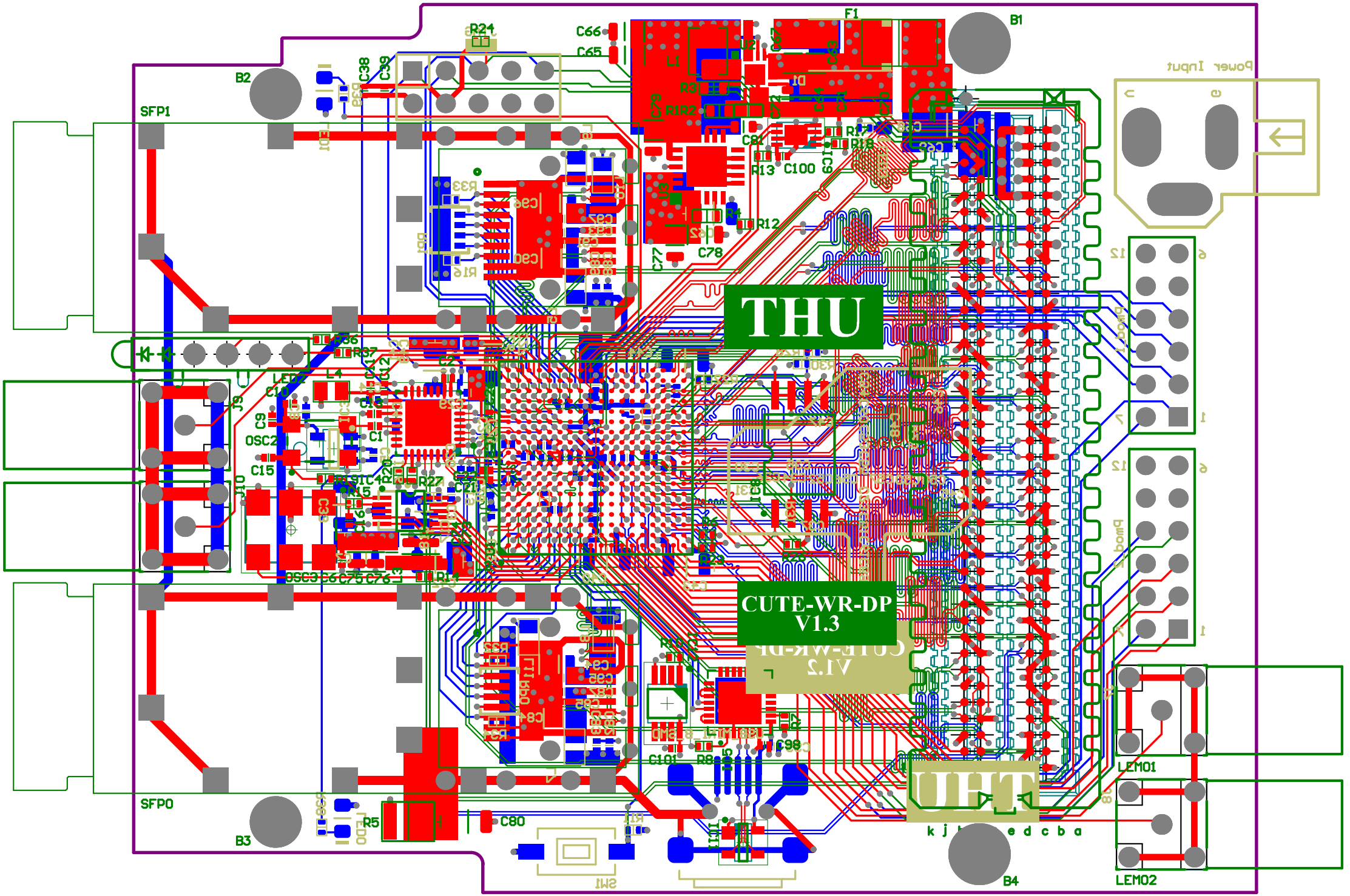
THU
CUTE-WR-DP
V1.3
SFP1
SFP0
B1
B2
B3
B4
LEM01
LEM02
OSC2
OSC3
Power Input
Pmod1
Pmod2