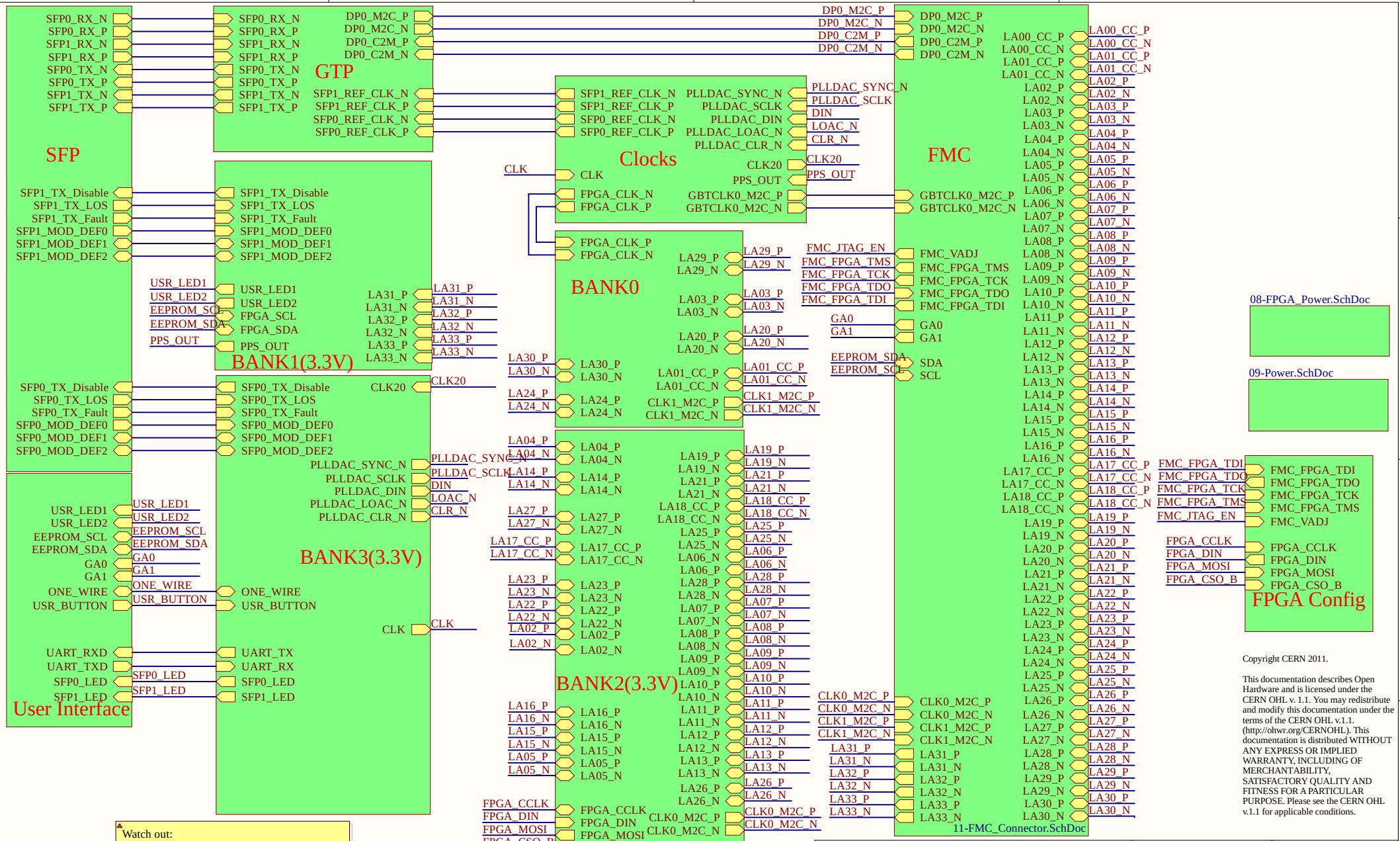

Title	CUTEWR-DP		
Size: A4	Number:14.	Revision: V2	
Date: 2017/02/14		13	
File: 00cutewr_dp.SchDoc			

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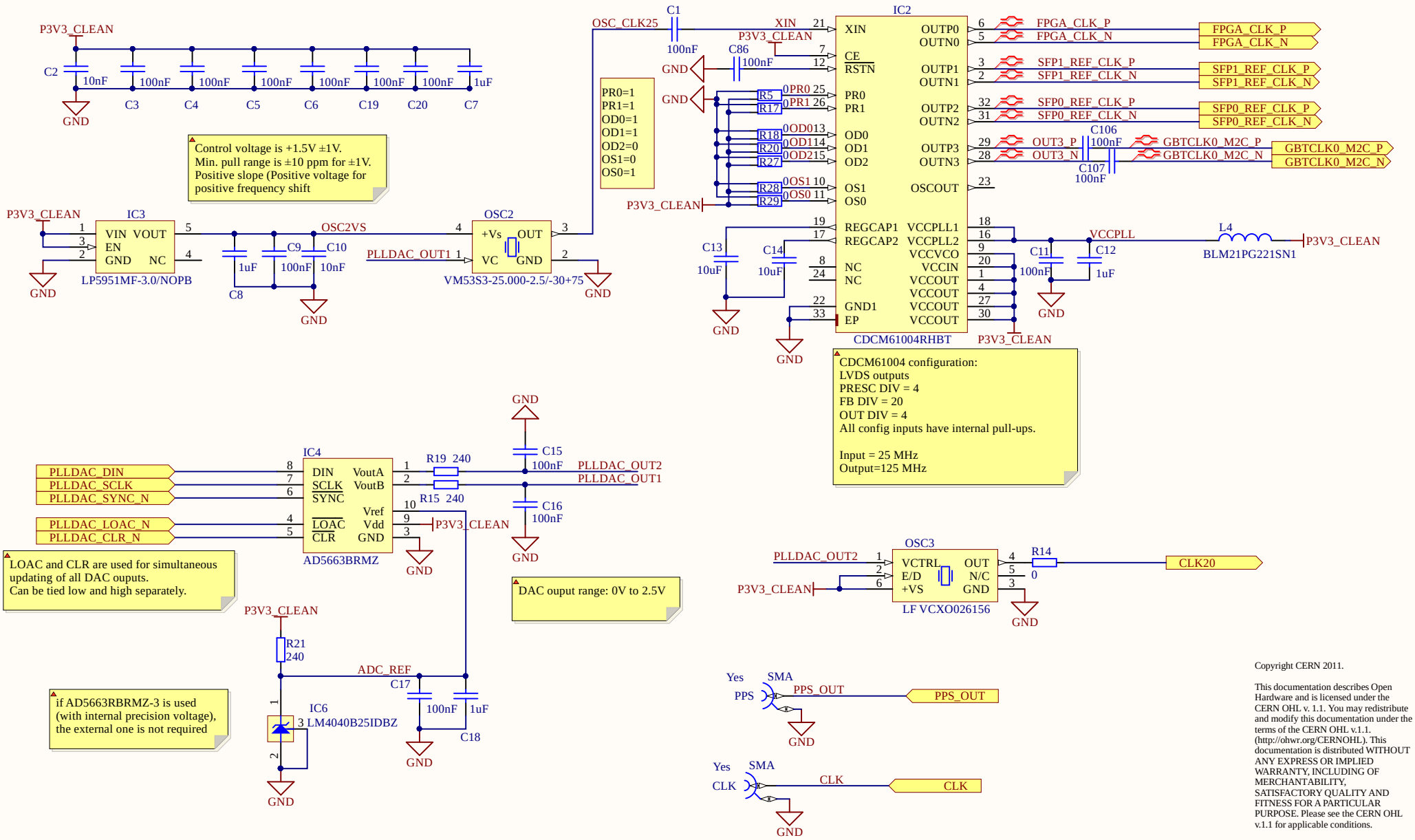
P3V3_CLEAN
C2
10nF
100nF
C3
C4
C5
C6
C19
C20
1uF
C7
GND
Control voltage is +1.5V ±1V.
Min. pull range is ±10 ppm for ±1V.
Positive slope (Positive voltage for positive frequency shift
IC3
VIN VOUT
EN
GND NC
LP5951MF-3.0/NOPB
C8
C9
C10
OSC2VS
OSC2
+Vs OUT
VC GND
VM53S3-25.000-2.5/-30+75
PLLDAC_OUT1
OSC_CLK25
C1
XIN
PR0=1
PR1=1
OD0=1
OD1=1
OD2=0
OS1=0
OS0=1
C86
R5
R17
R18
R20
R27
R28
R29
IC2
CE
RSTN
PR0
PR1
OD0
OD1
OD2
OS1
OS0
OUTP0
OUTN0
OUTP1
OUTN1
OUTP2
OUTN2
OUTP3
OUTN3
OSCOUT
REGCAP1
REGCAP2
NC
GND1
EP
VCCPLL1
VCCPLL2
VCCVCO
VCCIN
VCCOUT
CDCM61004RHBT
FPGA_CLK_P
FPGA_CLK_N
SFP1_REF_CLK_P
SFP1_REF_CLK_N
SFP0_REF_CLK_P
SFP0_REF_CLK_N
OUT3_P
OUT3_N
C106
C107
GBTCLK0_M2C_P
GBTCLK0_M2C_N
C13
C14
C11
C12
VCCPLL
L4
BLM21PG221SN1
CDCM61004 configuration:
LVDS outputs
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
All config inputs have internal pull-ups.
Input = 25 MHz
Output=125 MHz
IC4
PLLDAC_DIN
PLLDAC_SCLK
PLLDAC_SYNC_N
PLLDAC_LOAC_N
PLLDAC_CLR_N
DIN VoutA
SCLK VoutB
SYNC
Vref
LOAC Vdd
CLR GND
AD5663BRMZ
R19 240
R15 240
C15
C16
PLLDAC_OUT2
PLLDAC_OUT1
LOAC and CLR are used for simultaneous updating of all DAC ouputs.
Can be tied low and high separately.
DAC ouput range: 0V to 2.5V
R21
240
ADC_REF
C17
C18
IC6
LM4040B25IDBZ
if AD5663RBRMZ-3 is used (with internal precision voltage), the external one is not required
OSC3
VCTRL OUT
E/D N/C
+VS GND
LF VCXO026156
R14
CLK20
Yes
SMA
PPS
PPS_OUT
CLK
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Title CUTEWR-DP
Size: A4
Number:1.
Revision: V2
Date: 2017/02/14
13
File: 01-Clocks.SchDoc
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hongming
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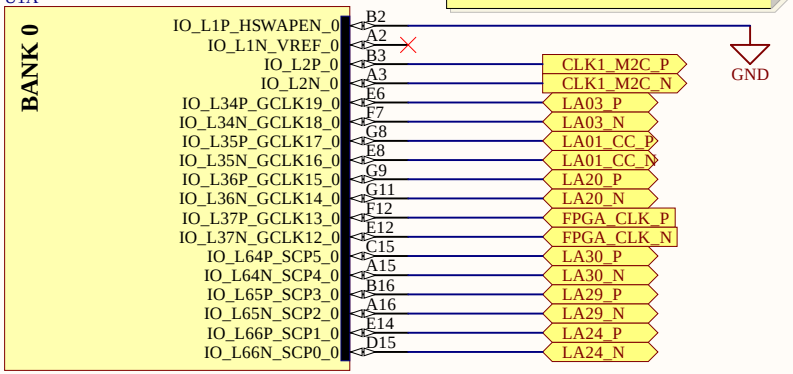
Bank 0 Supports differential output

VCCO_0 = 3.3V

FPGA IO pulled-up during configuration

U1A



XC6SLX45T-3CSG324C

Title	CUTEWR-DP		
Size: A4	Number:2.	Revision: V2	
Date: 2017/02/14		13	
File: 02-FPGA_bank0.SchDoc			

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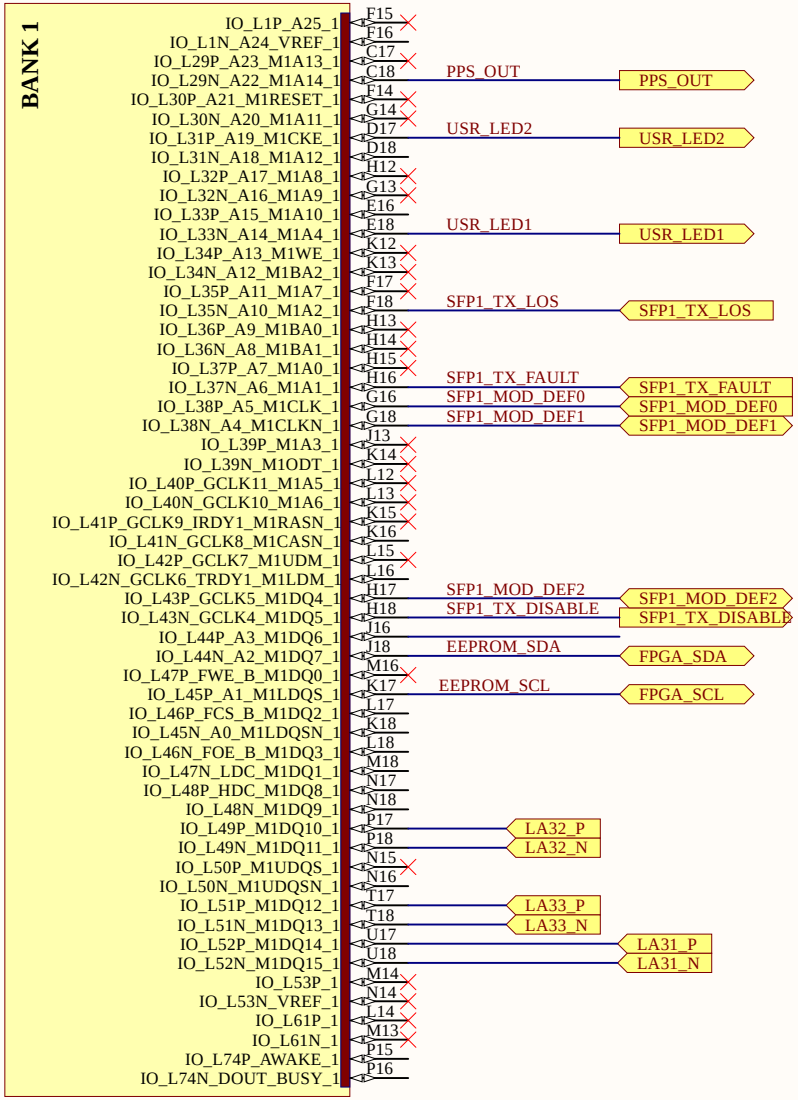
Bank 1 DOESN'T Supports differential output

VCCO_1 = 3.3V

U1B



XC6SLX45T-3CSG324C

Title	CUTEWR-DP		
Size: A4	Number:3.	Revision: V2	
Date: 2017/02/14		13	
File: 03-FPGA_bank1.SchDoc			

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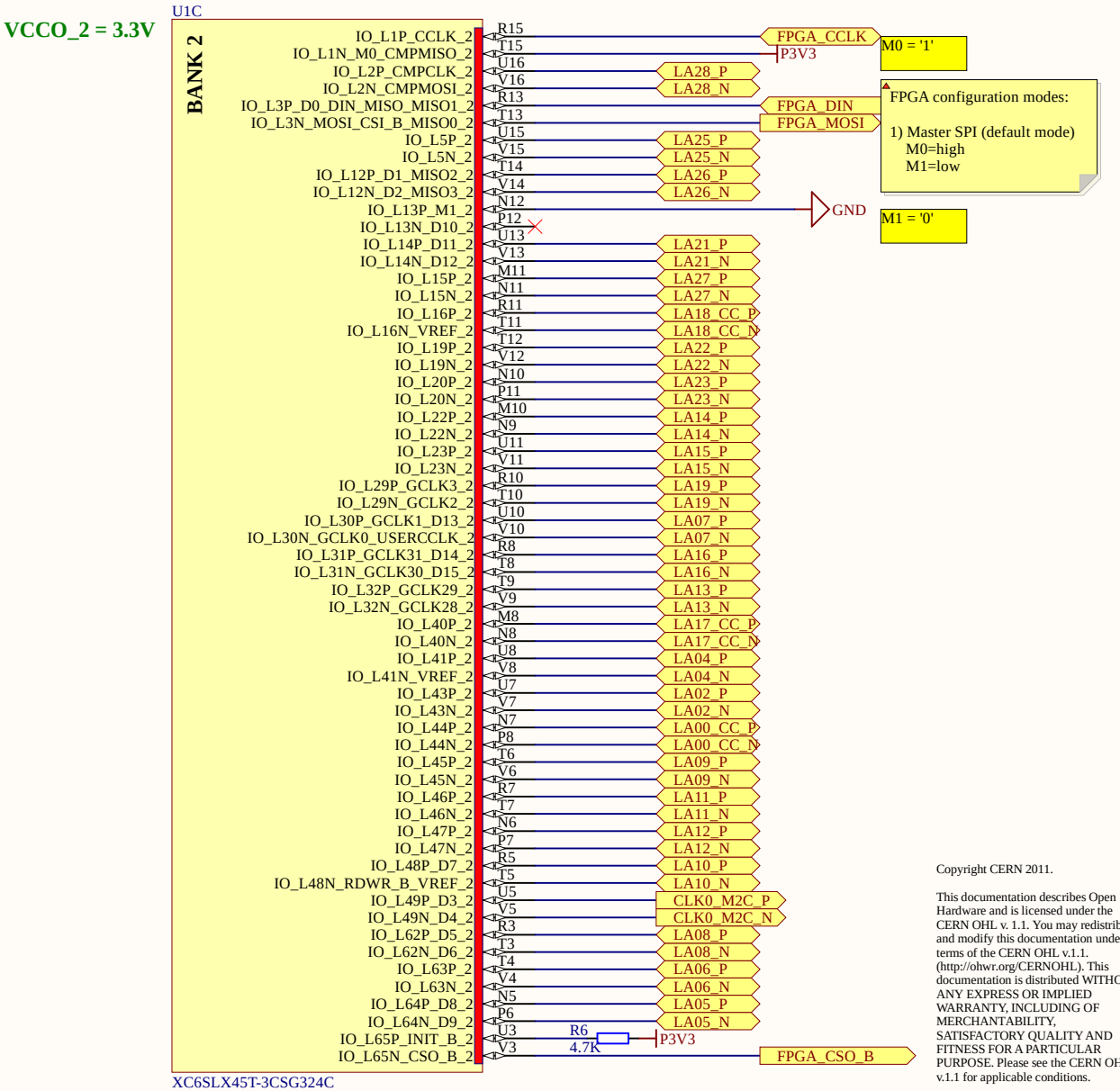

Title	CUTEWR-DP		
Size: A4	Number:4.	Revision: V2	
Date: 2017/02/14		13	
File: 04-FPGA_bank2.SchDoc			

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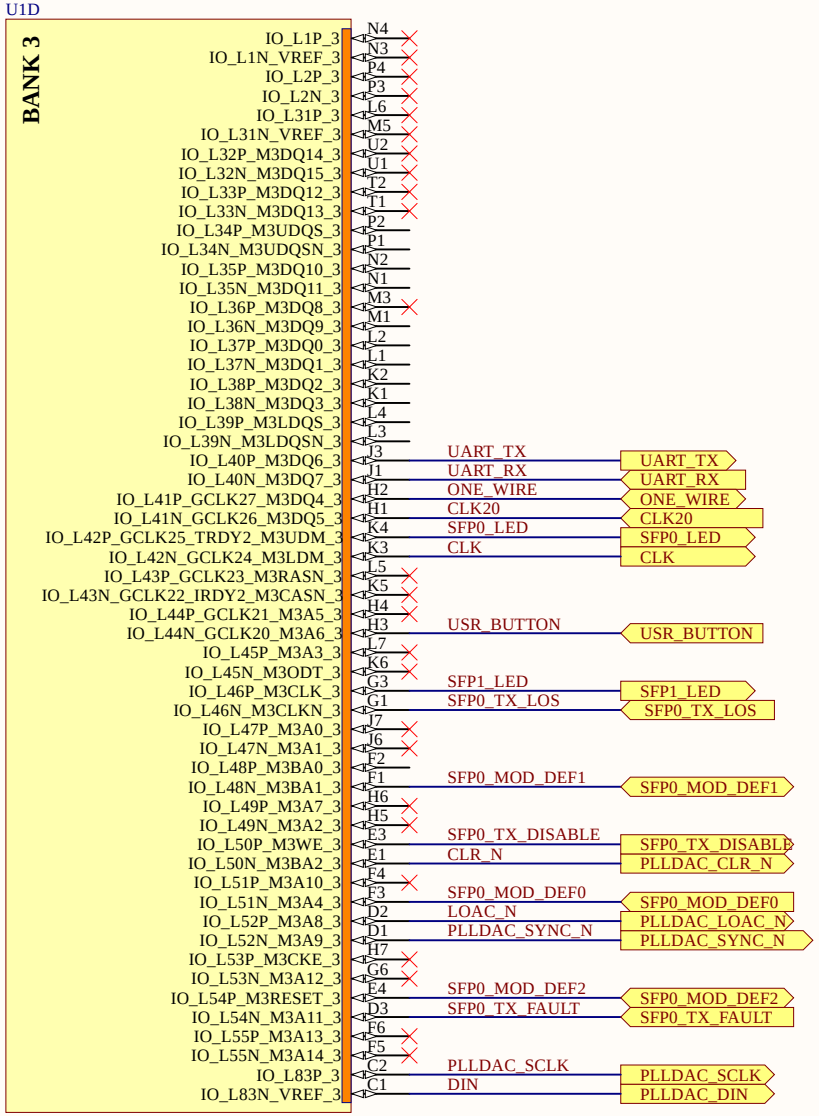
Bank 3 DOESN'T Supports differential output

VCCO_3 = 3.3V

U1D



XC6SLX45T-3CSG324C

Title	CUTEWR-DP		
Size: A4	Number:5.	Revision: V2	
Date: 2017/02/14		13	
File: 05-FPGA_bank3.SchDoc			

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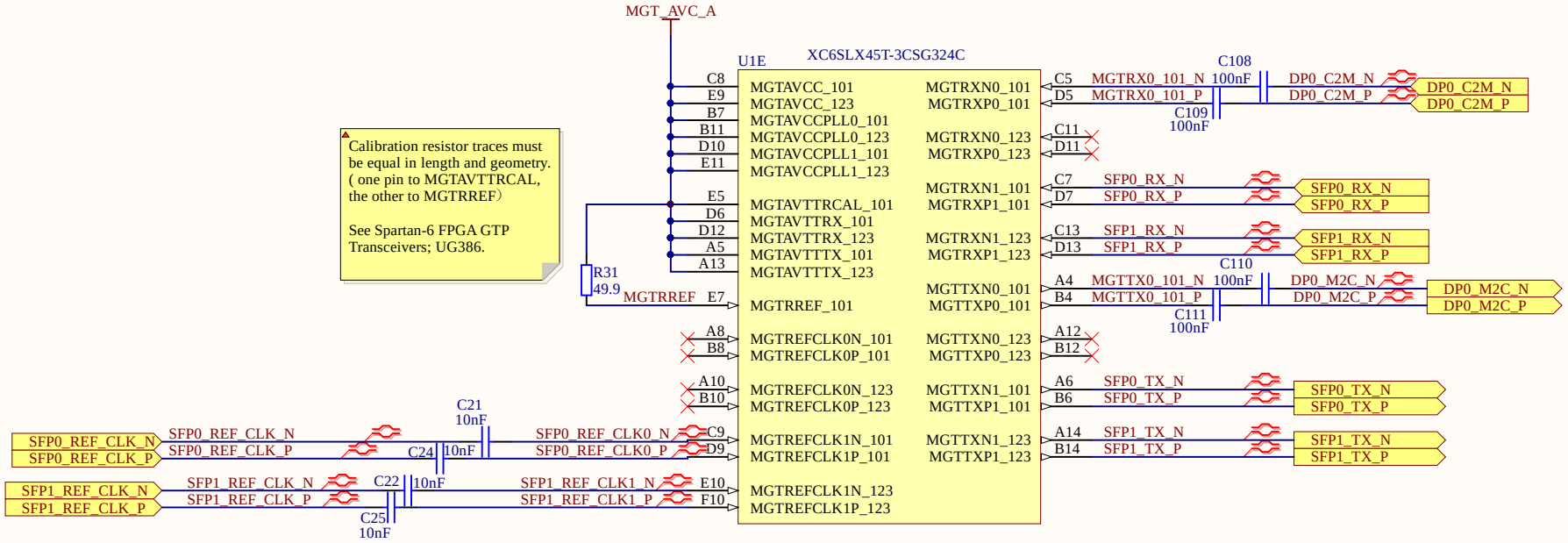

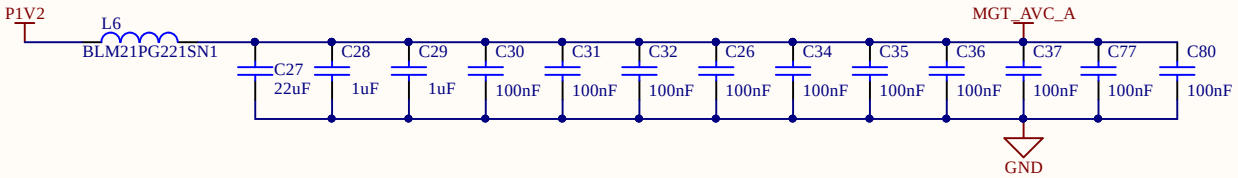

Title	CUTEWR-DP		
Size: A4	Number:6.	Revision: V2	
Date: 2017/02/14		13	
File: 06-FPGA_GTP.SchDoc			

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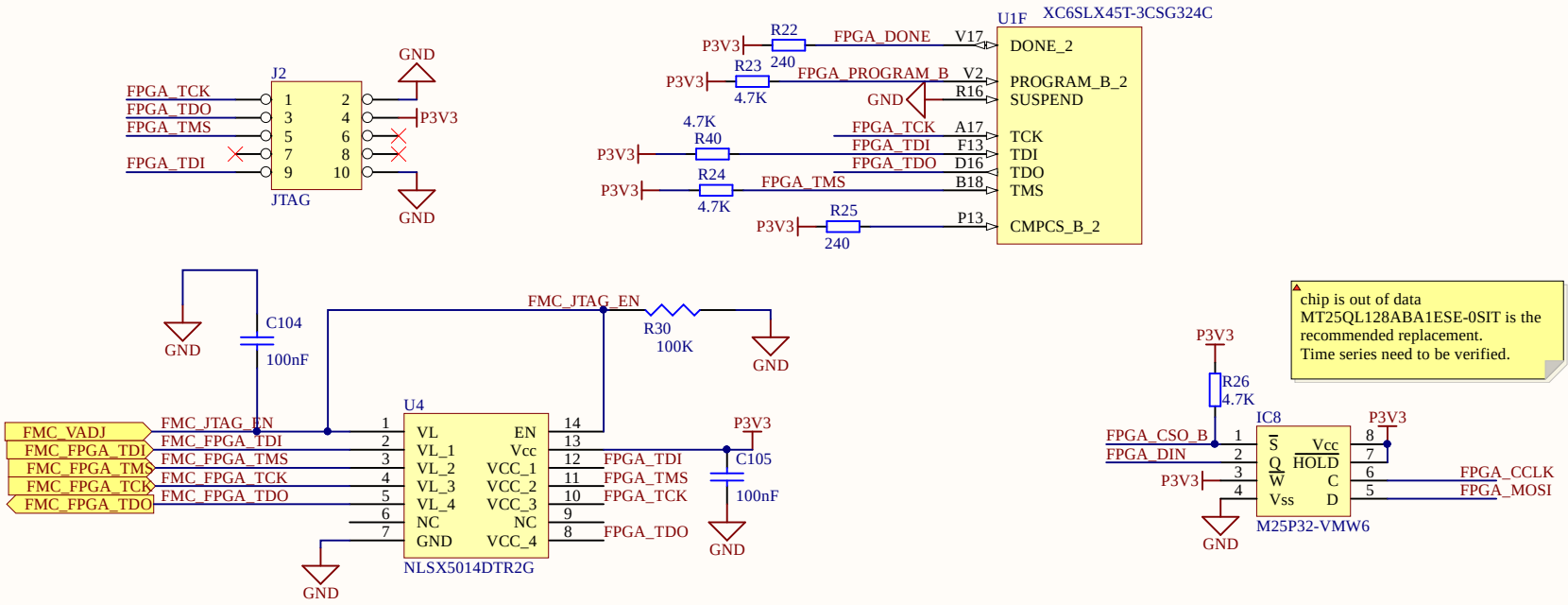

Title	CUTEWR-DP		
Size: A4	Number:7.	Revision: V2	
Date: 2017/02/14		13	
File: 07-FPGA_Config.SchDoc			

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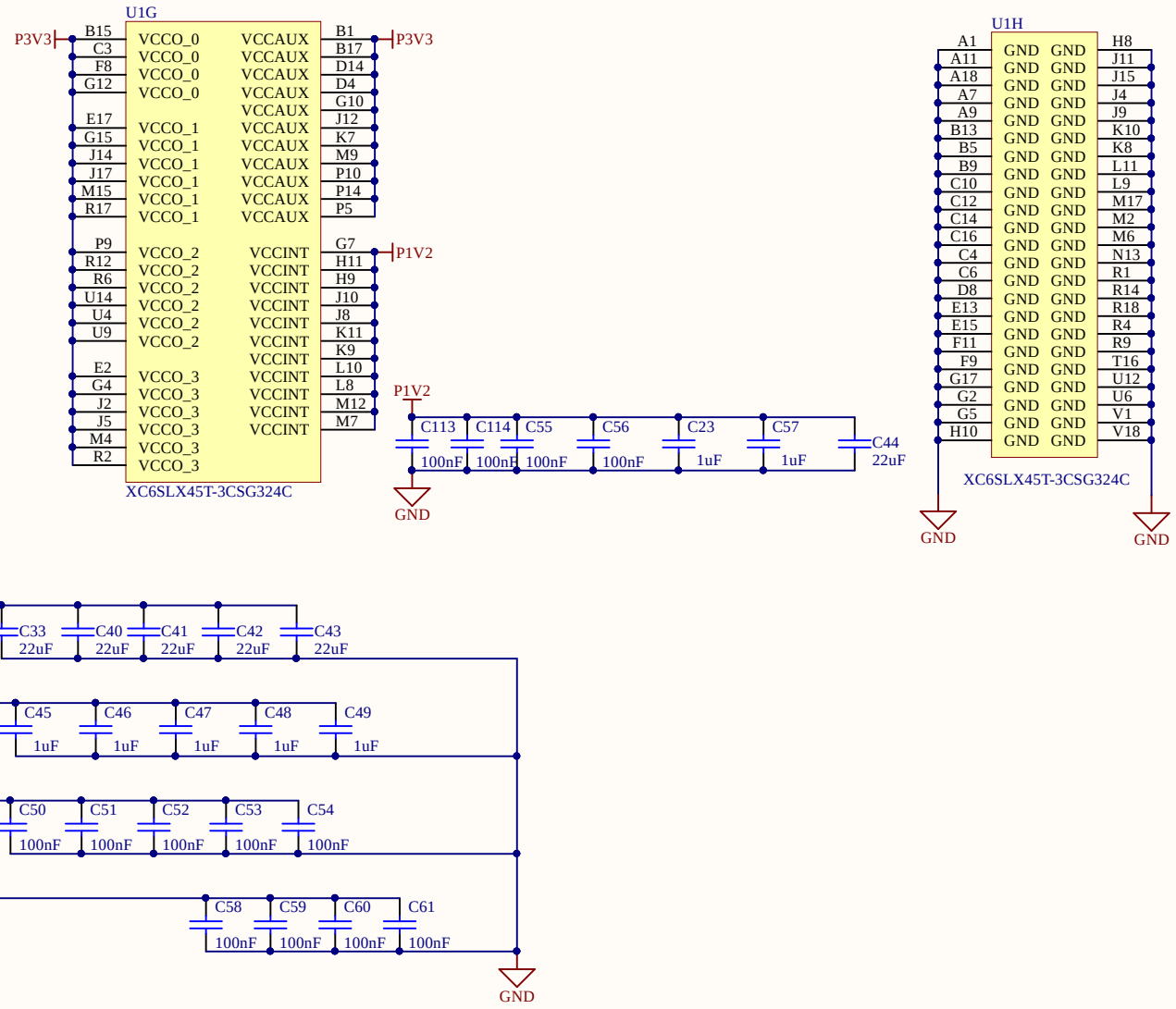

Title	CUTEWR-DP		
Size: A4	Number:8.	Revision: V3	
Date: 2017/02/14		13	
File: 08-FPGA_Power.SchDoc			

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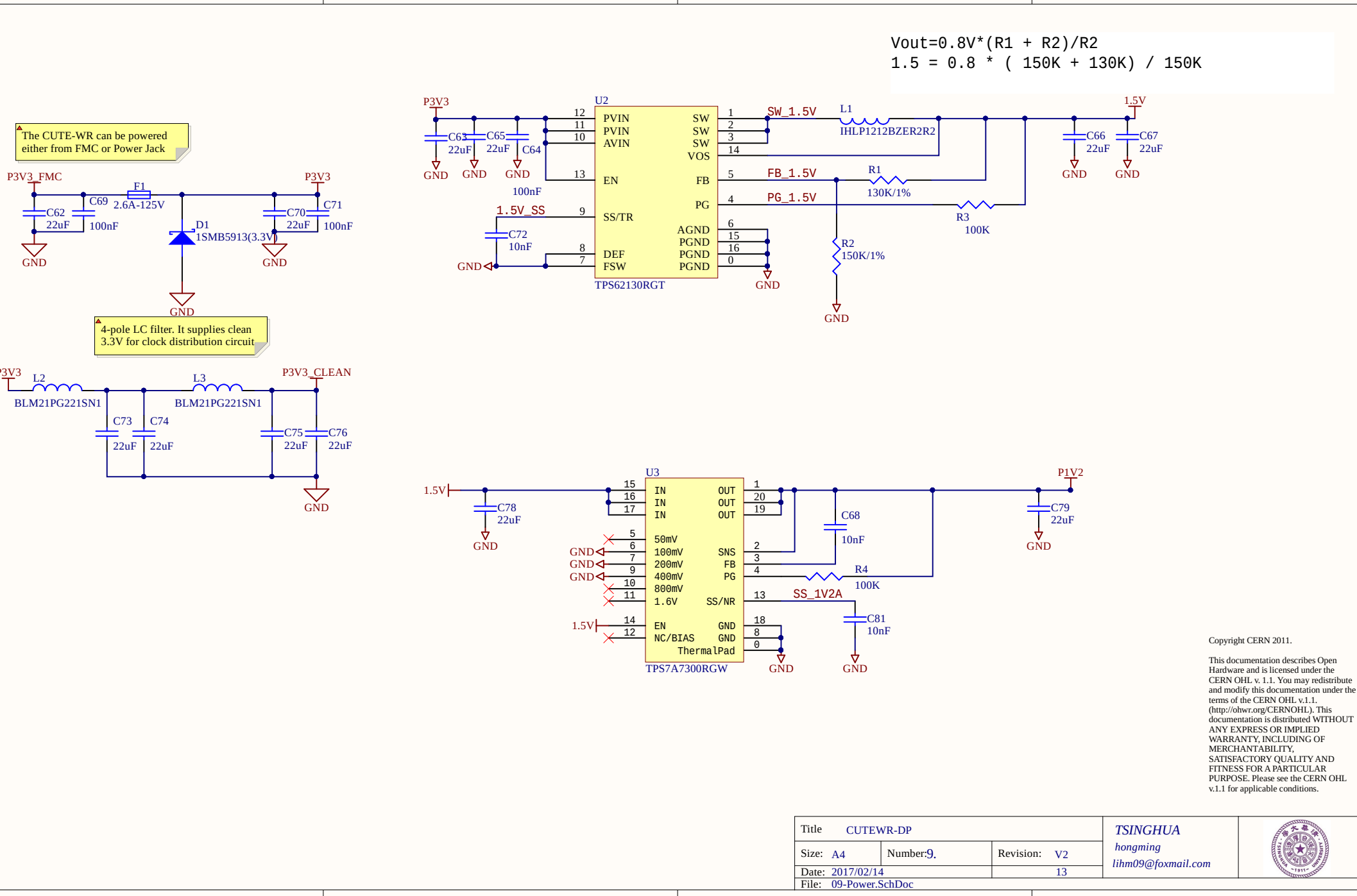
Vout=0.8V*(R1 + R2)/R2
1.5 = 0.8 * (150K + 130K) / 150K
The CUTE-WR can be powered either from FMC or Power Jack
P3V3_FMC
F1
2.6A-125V
C62 22uF
C69 100nF
D1 1SMB5913(3.3V)
C70 22uF
C71 100nF
P3V3
GND
4-pole LC filter. It supplies clean 3.3V for clock distribution circuit
P3V3
L2 BLM21PG221SN1
L3 BLM21PG221SN1
P3V3_CLEAN
C73 22uF
C74 22uF
C75 22uF
C76 22uF
U2
PVIN
PVIN
AVIN
EN
SS/TR
DEF
FSW
SW
SW
SW
VOS
FB
PG
AGND
PGND
PGND
PGND
TPS62130RGT
C63 22uF
C65 22uF
C64 100nF
1.5V_SS
C72 10nF
SW_1.5V
L1 IHLP1212BZER2R2
FB_1.5V
PG_1.5V
R1 130K/1%
R2 150K/1%
R3 100K
1.5V
C66 22uF
C67 22uF
U3
IN
IN
IN
50mV
100mV
200mV
400mV
800mV
1.6V
EN
NC/BIAS
ThermalPad
OUT
OUT
OUT
SNS
FB
PG
SS/NR
GND
GND
TPS7A7300RGW
C78 22uF
C68 10nF
R4 100K
SS_1V2A
C81 10nF
P1V2
C79 22uF
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Title CUTEWR-DP
Size: A4
Number:9.
Revision: V2
Date: 2017/02/14
File: 09-Power.SchDoc
13
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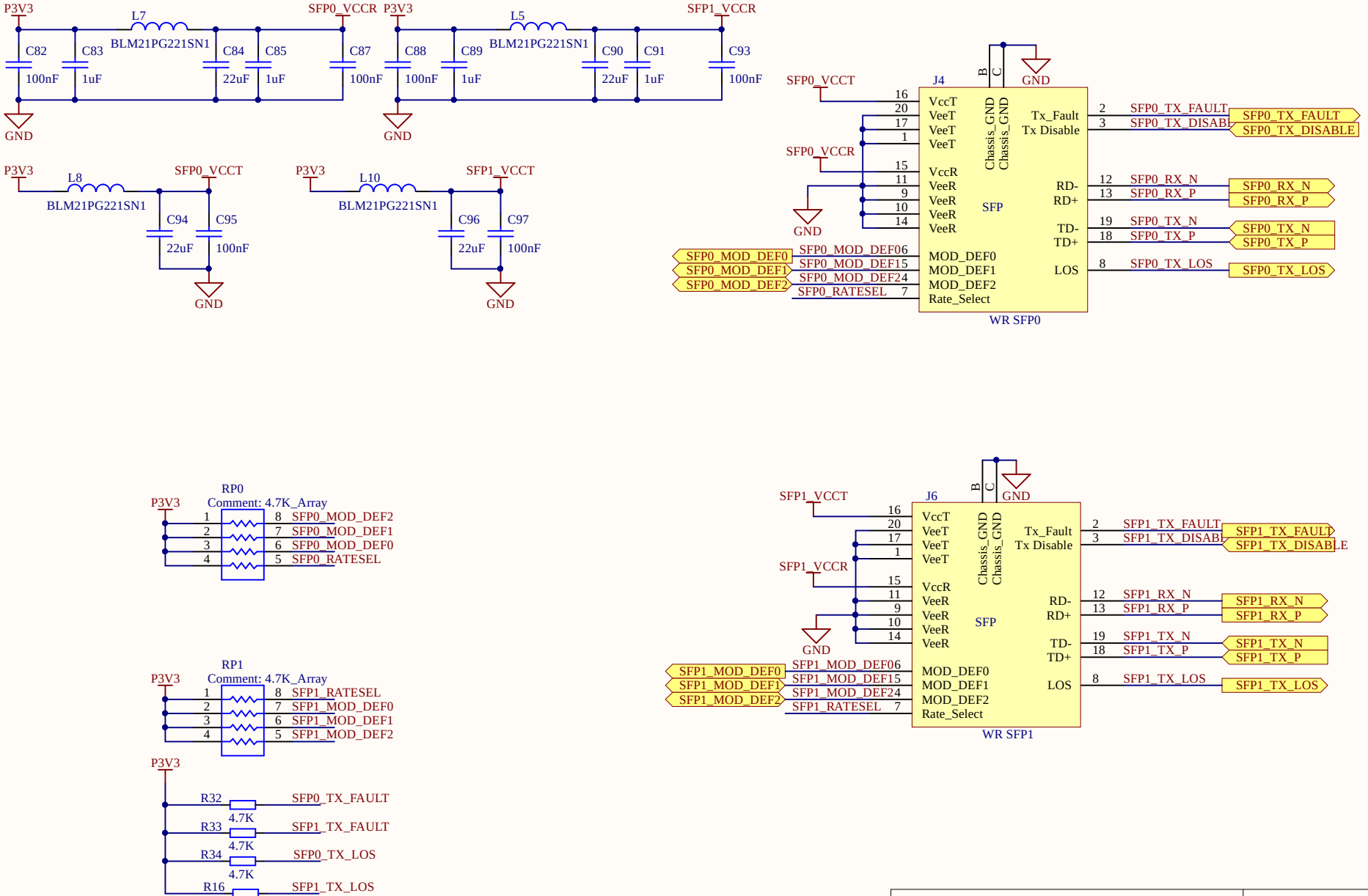
P3V3
L7
BLM21PG221SN1
SFP0_VCCR
C82
100nF
C83
1uF
C84
22uF
C85
1uF
C87
100nF
GND
P3V3
L5
BLM21PG221SN1
SFP1_VCCR
C88
100nF
C89
1uF
C90
22uF
C91
1uF
C93
100nF
GND
P3V3
L8
BLM21PG221SN1
SFP0_VCCT
C94
22uF
C95
100nF
GND
P3V3
L10
BLM21PG221SN1
SFP1_VCCT
C96
22uF
C97
100nF
GND
SFP0_VCCT
SFP0_VCCR
GND
J4
B
C
GND
Chassis_GND
Chassis_GND
16 VccT
20 VeeT
17 VeeT
1 VeeT
15 VccR
11 VeeR
9 VeeR
10 VeeR
14 VeeR
SFP
SFP0_MOD_DEF0
SFP0_MOD_DEF1
SFP0_MOD_DEF2
SFP0_MOD_DEF06
SFP0_MOD_DEF15
SFP0_MOD_DEF24
SFP0_RATESEL 7
MOD_DEF0
MOD_DEF1
MOD_DEF2
Rate_Select
Tx_Fault
Tx Disable
2 SFP0_TX_FAULT
3 SFP0_TX_DISABL
SFP0_TX_FAULT
SFP0_TX_DISABLE
RD-
RD+
12 SFP0_RX_N
13 SFP0_RX_P
SFP0_RX_N
SFP0_RX_P
TD-
TD+
19 SFP0_TX_N
18 SFP0_TX_P
SFP0_TX_N
SFP0_TX_P
LOS
8 SFP0_TX_LOS
SFP0_TX_LOS
WR SFP0
RP0
Comment: 4.7K_Array
P3V3
1 8 SFP0_MOD_DEF2
2 7 SFP0_MOD_DEF1
3 6 SFP0_MOD_DEF0
4 5 SFP0_RATESEL
RP1
Comment: 4.7K_Array
P3V3
1 8 SFP1_RATESEL
2 7 SFP1_MOD_DEF0
3 6 SFP1_MOD_DEF1
4 5 SFP1_MOD_DEF2
P3V3
R32 4.7K SFP0_TX_FAULT
R33 4.7K SFP1_TX_FAULT
R34 4.7K SFP0_TX_LOS
R16 4.7K SFP1_TX_LOS
SFP1_VCCT
SFP1_VCCR
GND
J6
B
C
GND
Chassis_GND
Chassis_GND
16 VccT
20 VeeT
17 VeeT
1 VeeT
15 VccR
11 VeeR
9 VeeR
10 VeeR
14 VeeR
SFP
SFP1_MOD_DEF0
SFP1_MOD_DEF1
SFP1_MOD_DEF2
SFP1_MOD_DEF06
SFP1_MOD_DEF15
SFP1_MOD_DEF24
SFP1_RATESEL 7
MOD_DEF0
MOD_DEF1
MOD_DEF2
Rate_Select
Tx_Fault
Tx Disable
2 SFP1_TX_FAULT
3 SFP1_TX_DISABL
SFP1_TX_FAULT
SFP1_TX_DISABLE
RD-
RD+
12 SFP1_RX_N
13 SFP1_RX_P
SFP1_RX_N
SFP1_RX_P
TD-
TD+
19 SFP1_TX_N
18 SFP1_TX_P
SFP1_TX_N
SFP1_TX_P
LOS
8 SFP1_TX_LOS
SFP1_TX_LOS
WR SFP1
Title CUTEWR-DP
Size: A4
Number:10.
Revision: V2
Date: 2017/02/14
13
File: 10-SFP.SchDoc
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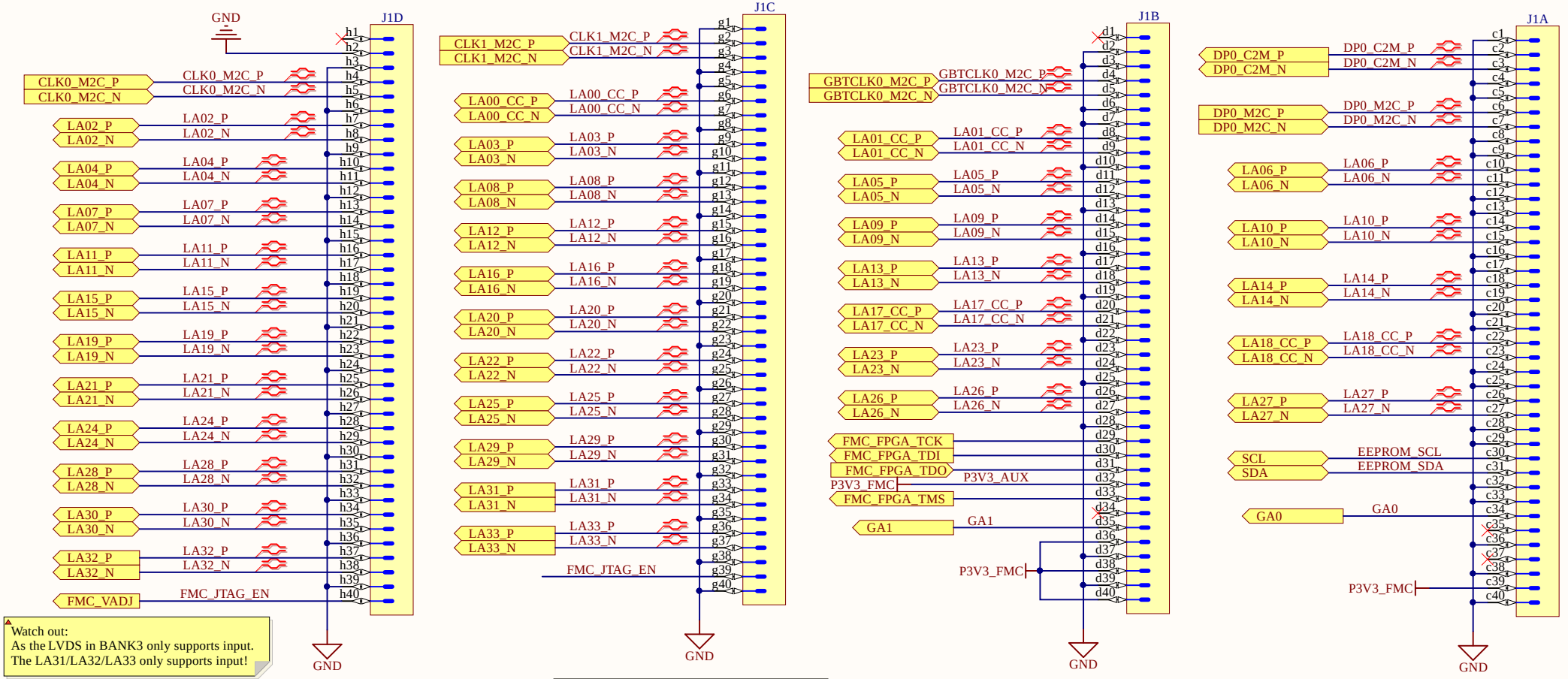

Watch out:
As the LVDS in BANK3 only supports input.
The LA31/LA32/LA33 only supports input!

NB: the LVDS pairs must have a differential impedance of 100 ohm (+/-10%) and be routed with no skew between the P and the N lines. The skew between the various LA pairs should be kept as low as possible (<200ps).

Title	CUTEWR-DP		
Size: A4	Number:11.	Revision: V2	
Date: 2017/02/14		13	
File: 11-FMC_Connector.SchDoc			

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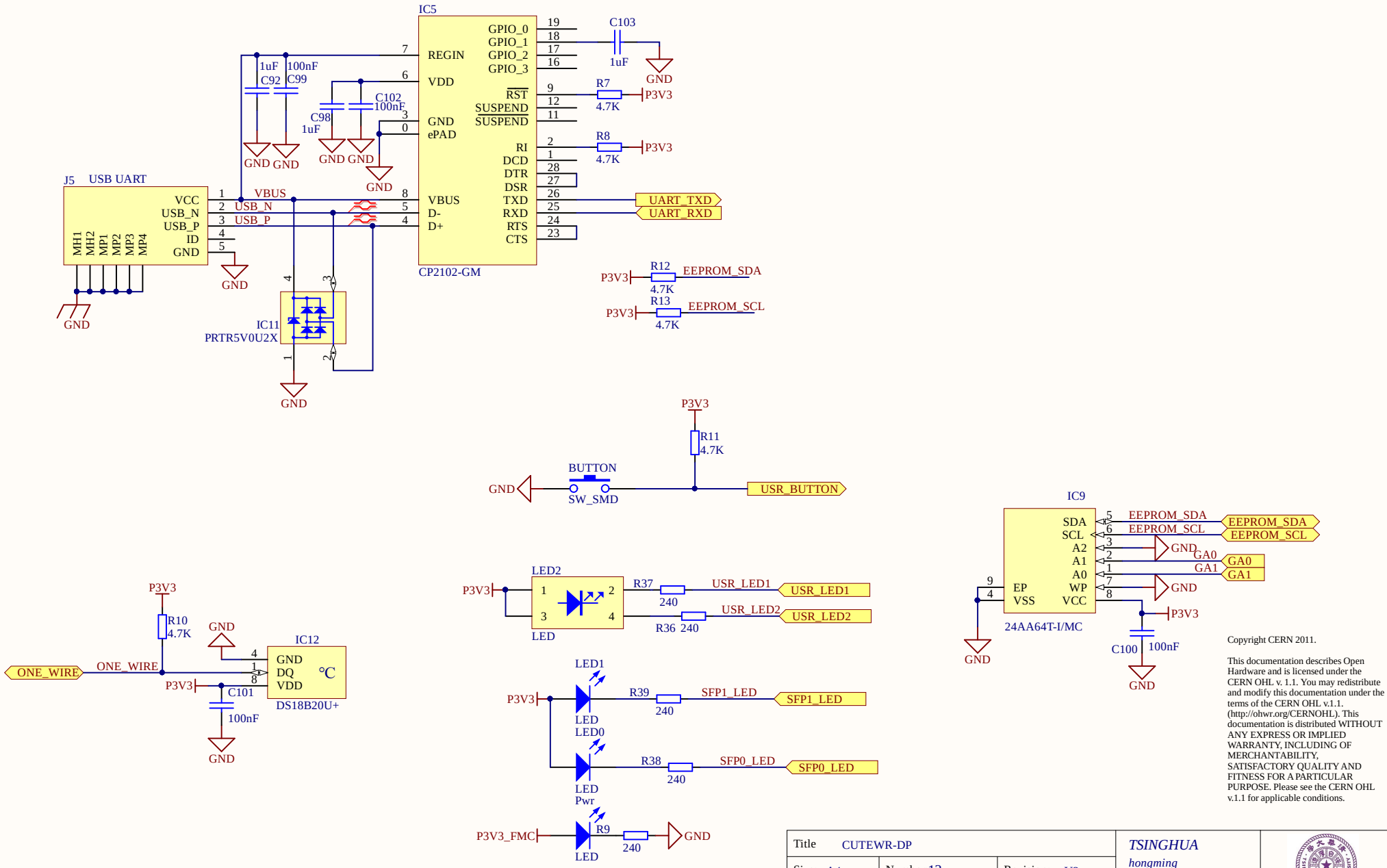

Title	CUTEWR-DP		
Size: A4	Number:13.	Revision: V2	
Date: 2017/02/14		13	
File: 13-User_Interface.SchDoc			

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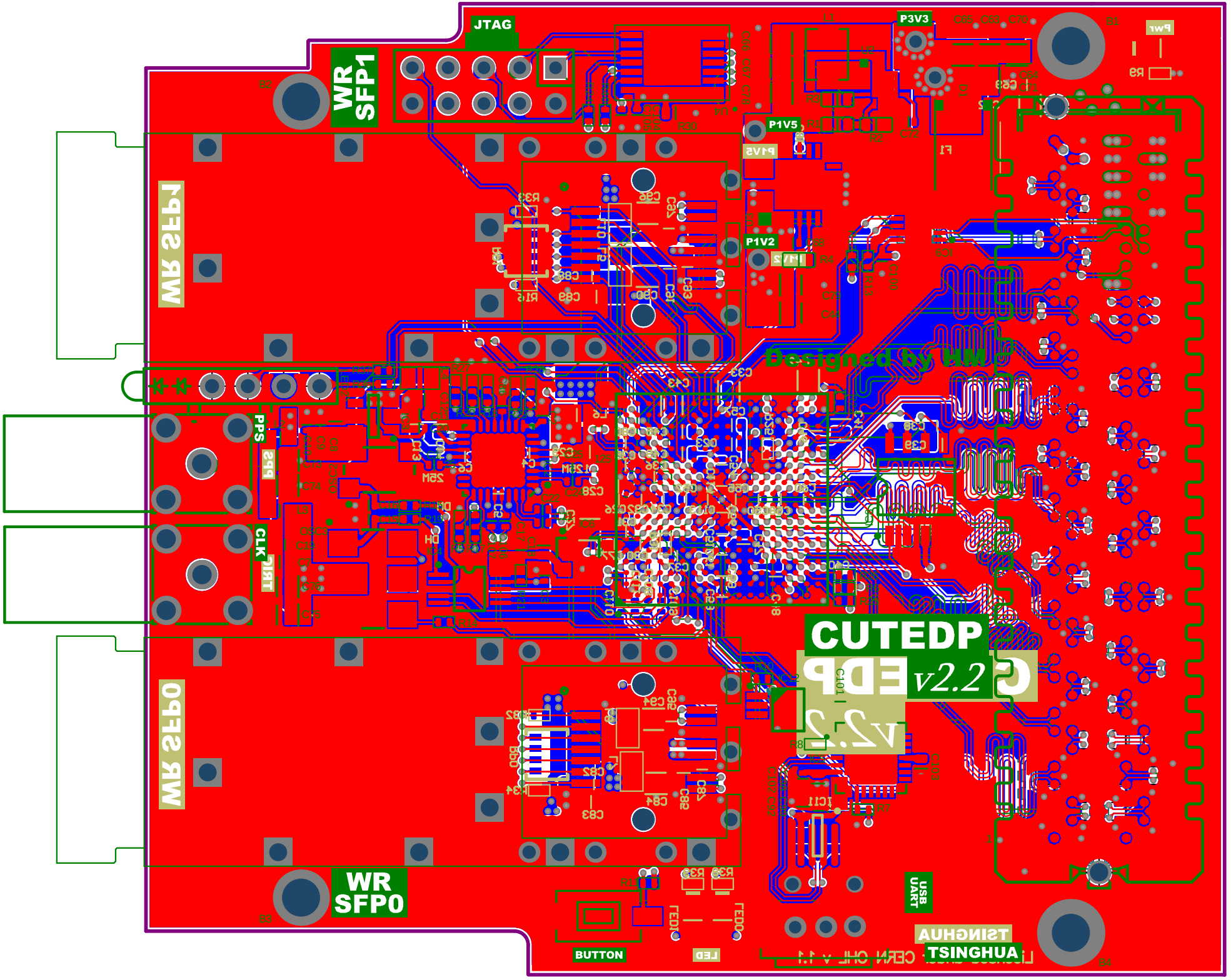
JTAG
WR SFP1
WR SFP0
P3V3
P1V5
P1V2
PPS
CLK
CUTEDP
v2.2
Designed by THU
TSINGHUA
USB UART
BUTTON
LED