Control voltage is \( \pm 1.5 \text{V} \). Min. pull range is \( \pm 10 \text{ppm} \) for \( \pm 1 \text{V} \). Positive slope (positive voltage for positive frequency shift).

Clock outputs, 125 MHz

DAC output range: 0V to 2.5V

If AD5663BRMZ-S is used (with on-chip reference), the external one is not required.
Compliant SFP devices see "http://www.ohwr.org/projects/white-rabbit/wiki/SFP"
Calibration resistor traces must be equal in length and geometry. See Spartan-6 FPGA GTP Transceivers, UG386.

Reference clock, 125 MHz

Power: GTPs power plane, and signal plane should be separated by a ground plane from any signal passing close.

The capacitor bank recommended for decoupling is described in: Xilinx user guide Spartan-6 FPGA GTP Transceivers (ug386.pdf), Chapter 5 Board Design Guidelines. Check Table 5-2: Recommended Minimum Decoupling for Spartan-6 FPGA GTPA1_DUAL Tiles and Figure 5-11: Stackup for GTP Power and Signal Layers.

Copyright Physik Institut Universitaet Zuerich 2014. Based on SPEC and CUTE-WR, see http://www.ohwr.org/projects. This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERN OHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

FPGA GTP Transceivers
System: Compact RIO Module - White Rabbit Node
Board: CRIO-WR
Created: 06-JAN-2014, Daniel Florin
Modified: 13-AUG-2014, Daniel Florin
Physik Institut Universitaet Zuerich Winterthurerstrasse 190 8057 Zuerich
VCCO_0 = 3.3V

Bank 0 supports differential inputs and outputs.
VCCO_1 = 3.3V

**FPGA Bank 1**

**Bank 1 supports ONLY differential inputs**

**System:** Compact RIO Module - White Rabbit Node

**Board:** CompactRIO

**Created:** 06-JUL-2014, Daniel Florin

**Modified:** 06-JAN-2014, Daniel Florin

**Sheet:** 6 of 13
Copyright Physik Institut Universitaet Zuerich 2014.
Based on FPGA and CPU/MEM, see http://www.ohwr.org
This documentation is described Open Hardware and is licensed under the CERN
OHL v.1.1. For more information and details, see documentation under the
terms of the CERN OHL v.1.1. (http://ohwr.org/CERN OHL). This documentation
is distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFY
QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the
CERN OHL v.1.1 for applicable conditions.

FPGA Bank 2

System: CompactRio Module - White Rabbit Node
Board: CRIO-RTH
Created: 06-JUN-2014, Daniel Florin
Revisions: 1.01
Modified: 13-JUL-2015, Daniel Florin

SPI_FLASH_CCLK
- Route as a 50R controlled impedance transmission line
- Drive H or L after configuration

SPI_FLASH_MISO

Bank 2 supports differential inputs and outputs

*Bank 2 supports differential inputs and outputs
**FPGA Bank 3**

System: Compact RIO Module - White Rabbit Node

Sheet: 1 of 13

<table>
<thead>
<tr>
<th>Bank 3 supports ONLY differential inputs</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bank 3</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>IO_L1P_3</th>
<th>IO_L1N_3</th>
<th>VCCO_3</th>
<th>VREF_3</th>
</tr>
</thead>
<tbody>
<tr>
<td>R7</td>
<td>R8</td>
<td>3.3V</td>
<td>3V</td>
</tr>
</tbody>
</table>

**Modified:** 06-JAN-2014, Daniel Florin

**Created:** 13-AUG-2014, Daniel Florin

Copyright Physik Institut Universitaet Zuerich 2014.

Based on SPEC and CUTE-WR, see http://www.ohwr.org/projects.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1.

You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1.

Please see the CERN OHL v.1.1 for applicable conditions.
Copyright Physik Institut Universitaet Zuerich 2014.
Based on JFPGA and CUTE-WR, see http://www.ohwr.org/projects
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1 (http://ohwr.org/CERN-OHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

FPGA Configuration, NV-Memory and Board ID
System: Compact RIO Module - White Rabbit Node
Board: CRIO-WR
Created: 06-JAN-2014, Daniel Florin
Revision: 1.01
Modified: 13-AUG-2014, Daniel Florin
Sheet: 10 of 13
Physik Institut Universitaet Zuerich Winterthurerstrasse 190 8057 Zuerich
User Interface

System: Compact RIO Module - White Rabbit Node
Board: CRIO-WR
Created: 06-JAN-2014, Daniel Florin
Modified: 13-AUG-2014, Daniel Florin
Physik Institut Universität Zürich Winterthurerstrasse 190 8057 Zürich

Copyright Physik Institut Universität Zürich 2014
Based on SPIF and CUTE-WR, see http://www.openhwi.org/projects
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v. 1.1. http://ohwr.org/CERN OHL This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v. 1.1 for applicable conditions.