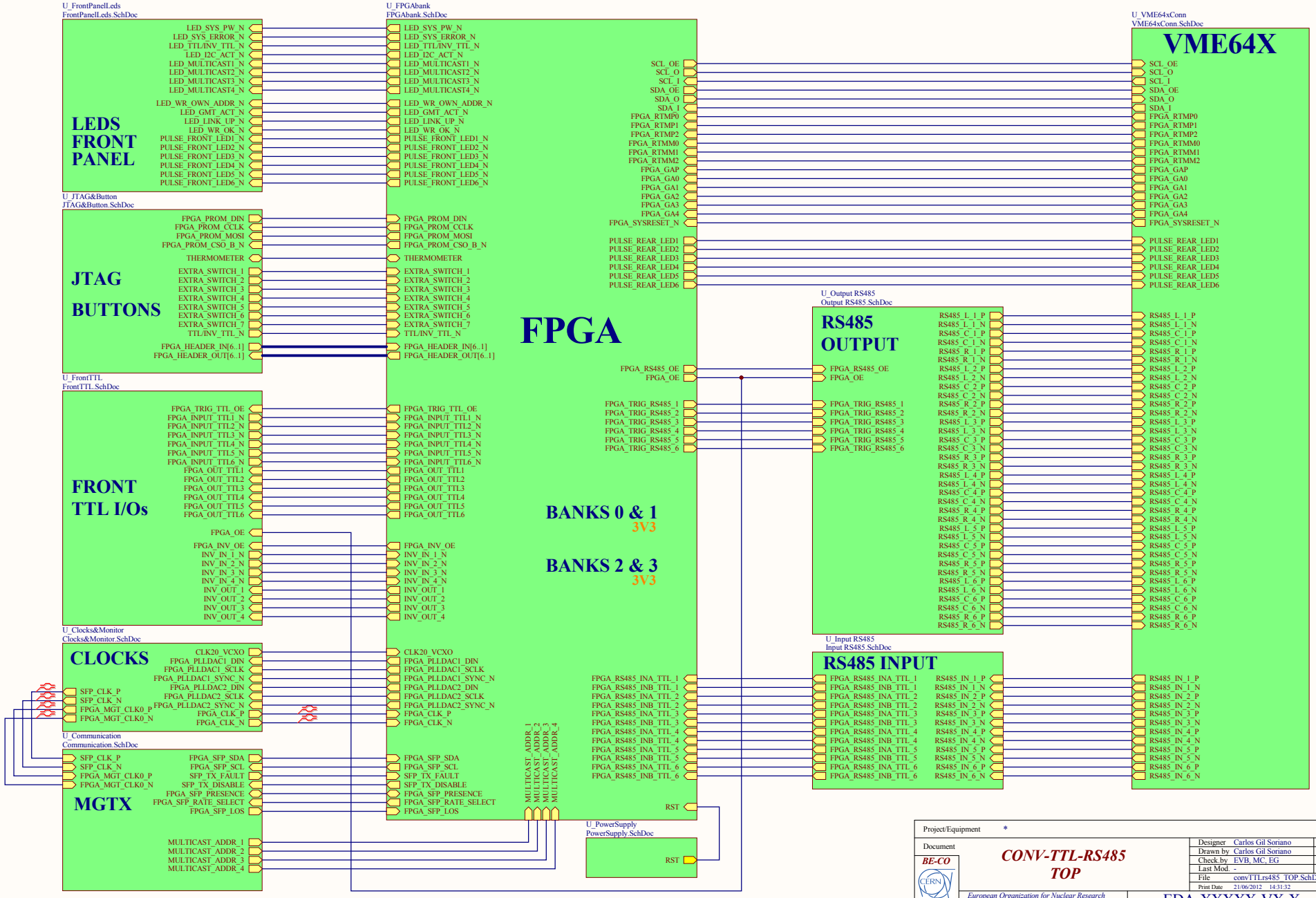
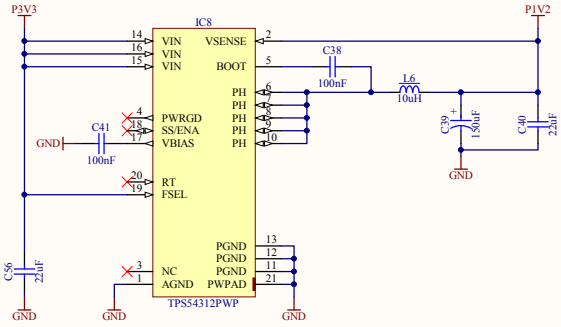
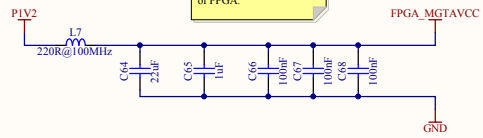


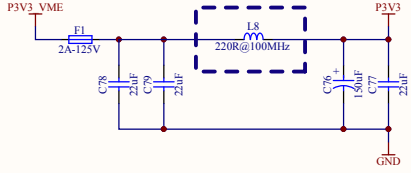
Efficiency of 85% and better



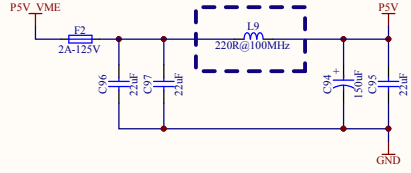
As close as possible to GTP DUAL pins --bank 0 of FPGA.

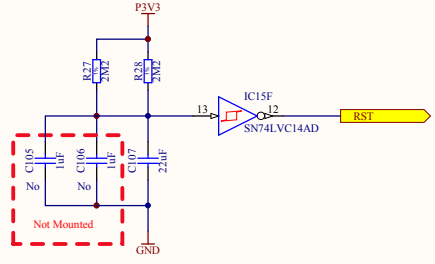


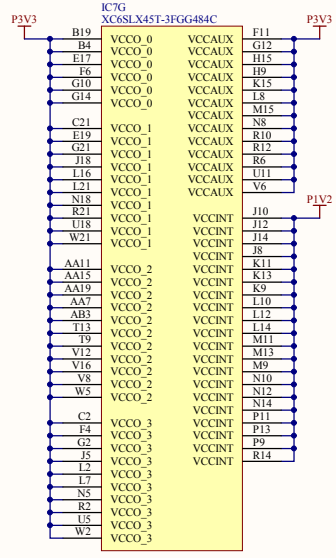
Change for BLM41PG181SN1L

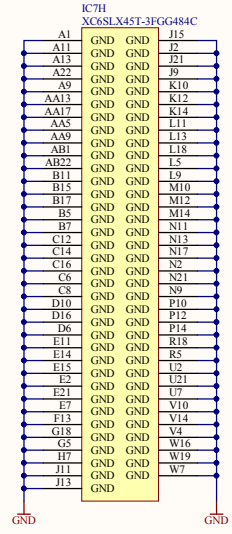


Change for BLM41PG181SN1L









Voltages are:

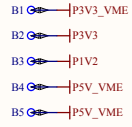
*** FPGA

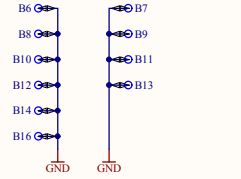
VCCO_0	3V3
VCCO_1	3V3
VCCO_2	3V3
VCCO_3	3V3
VCCaux	3V3
VCCint	1V2

*** PROM

VCCaux	3V3

Test points

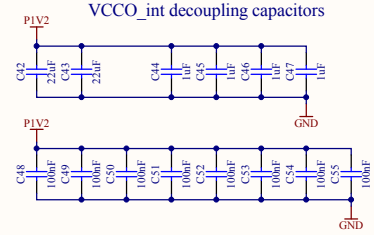




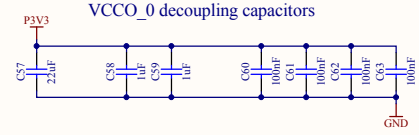
Nearby VME P2 RS485 inputs

Nearby Front Panel

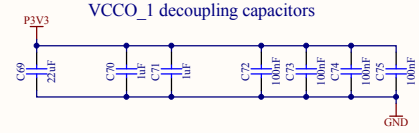
VCCO_int decoupling capacitors



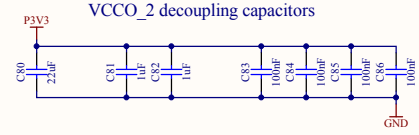
VCCO_0 decoupling capacitors



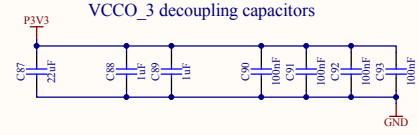
VCCO_1 decoupling capacitors



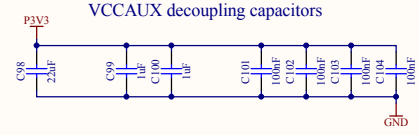
VCCO_2 decoupling capacitors



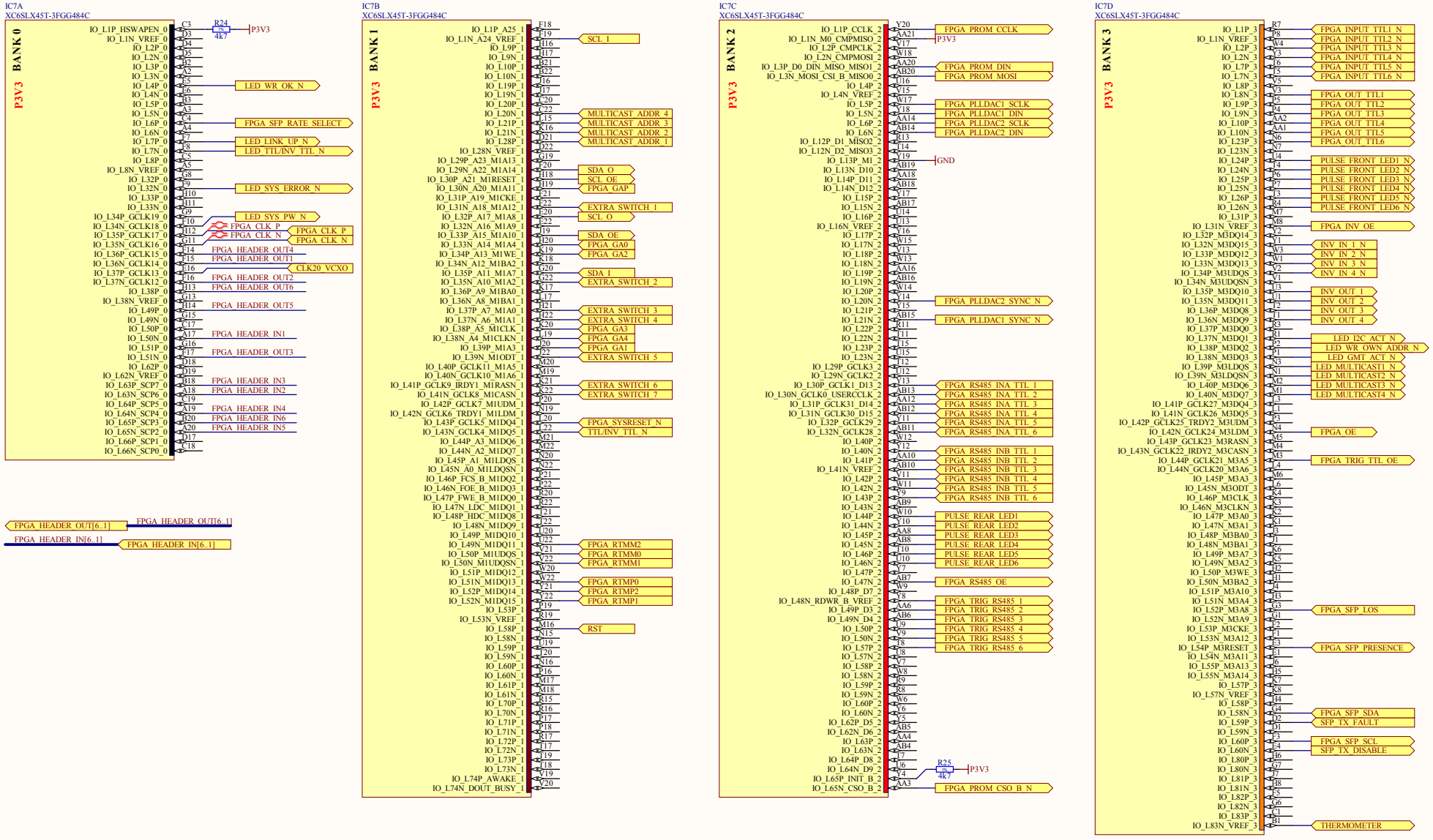
VCCO_3 decoupling capacitors



VCCAUX decoupling capacitors



Project/Equipment	*		
Document	CONV-TTL-RS485 Power Supply	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	12/03/2012
		Check by EVB, MC, EG	21/05/2012
		Last Mod. -	21/06/2012
		File PowerSupply.SchDoc	
		Print Date 21/06/2012 14:31:32	Sheet 2 of 13
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	Size A3 / Rev 3



Project/Equipment *

Document

CONV-TTL-RS485
FPGA BANK

BE-CO

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

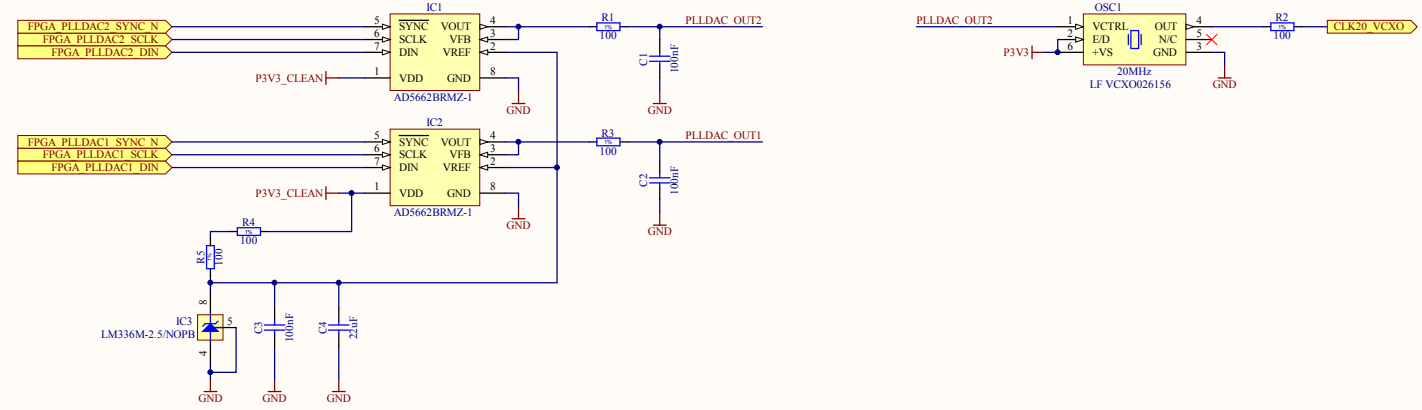
Designer	Carlos Gil Soriano	
Drawn by	Carlos Gil Soriano	12/03/2012
Check by	EVB, MC, EG	21/05/2012
Last Mod.	-	21/06/2012
File	FPGAbank.SchDoc	
Print Date	21/06/2012 14:31:32	Sheet 3 of 13

EDA-XXXXX-VX-X

Size A3 | Rev 3

DAC Vih = 2V so it accepts 2.5V CMOS signal
DAC ouput range: 0V to 2.5V

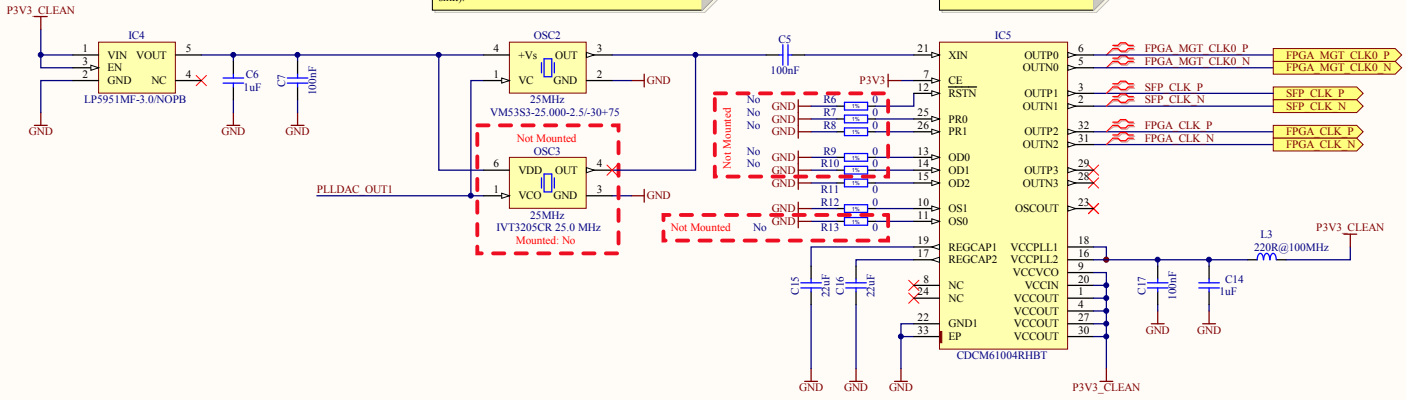
DAC Vih = 2V so it accepts 2.5V CMOS signal
DAC ouput range: 0V to 2.5V

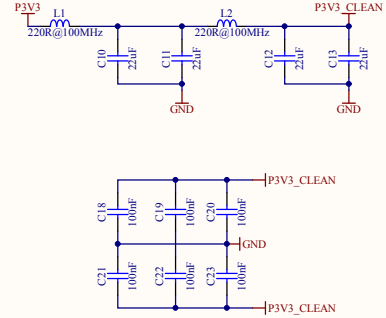


Control voltage is +1.5V ±1V.
Min. pull range is ±10 ppm for ±1V.
Positive slope (Positive voltage for positive frequency shift).

CDCM61004 configuration:
LVDS outputs
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
All config inputs have internal pull-ups.

Input = 25 MHz
Output=125 MHz



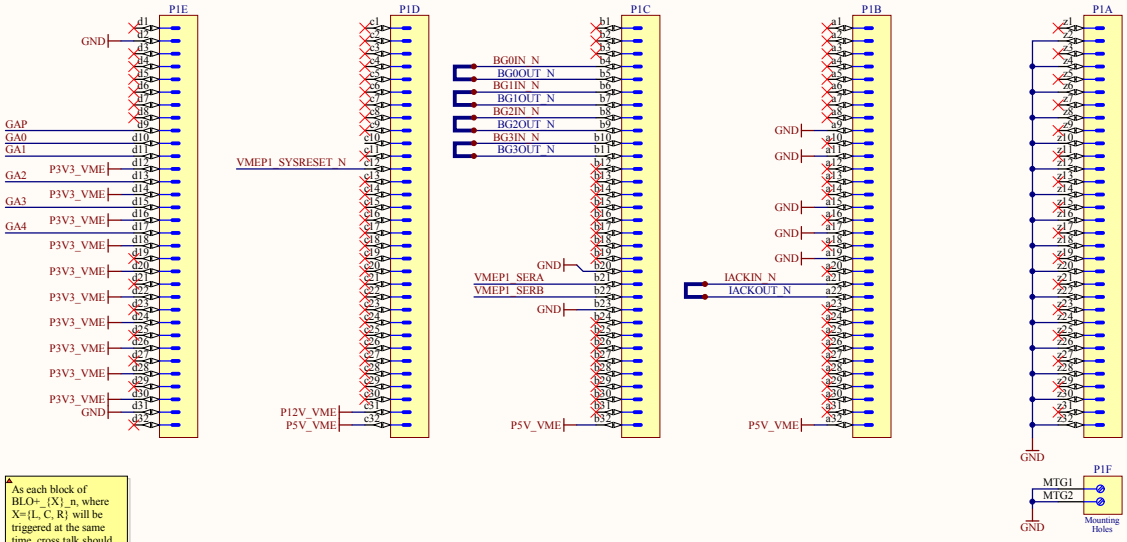


Project/Equipment	*	
Document	CONV-TTL-RS485 CLOCKS	
Designer	Carlos Gil Soriano	
Drawn by	Carlos Gil Soriano	12/03/2012
Check by	EVB, MC, EG	21/05/2012
Last Mod.	-	21/06/2012
File	Clocks&Monitor.SchDoc	
Print Date	21/06/2012 14:31:33	Sheet 4 of 13
BE-CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X
		Size A3 / Rev 3

Utility Bus Signal: see page 199
ANSI/VITA 1-1994

Output configurations in page 230

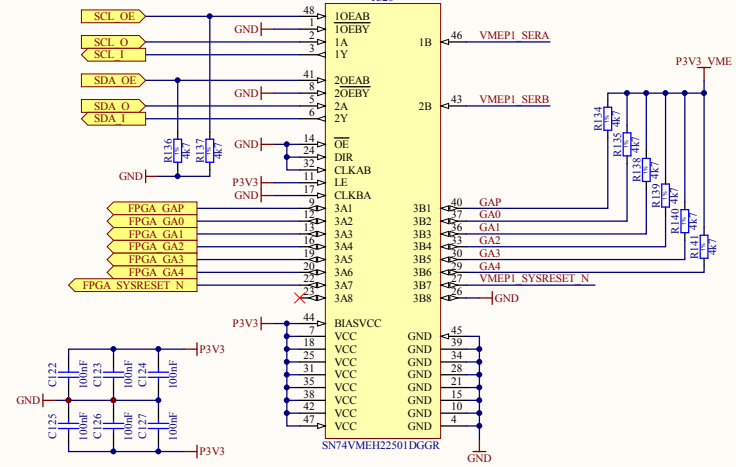
ACFAIL_N	Open collector
SYSFAIL_N	Open collector
SYSRESET_N	Open collector
SYSCLK	Totem-pole

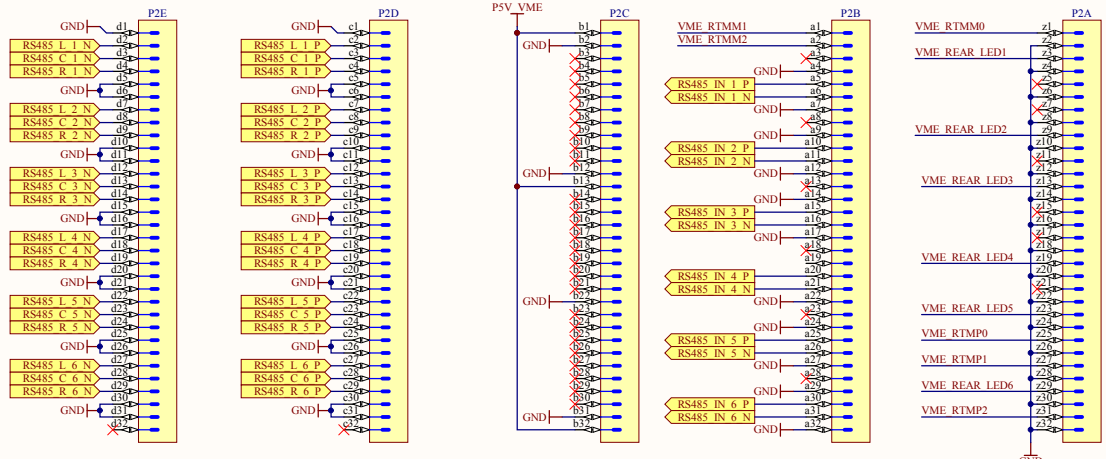


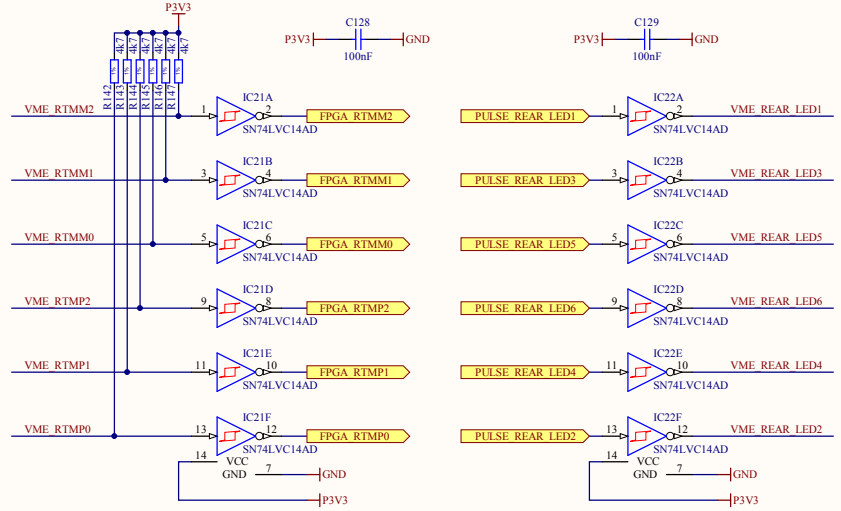
As each block of BLO+_{X}_n, where X={L, C, R} will be triggered at the same time, cross talk should not be so critical.
However, it would be better group the signals as it is shown and leave ground between sets of signals triggered by different sources.

As input signals come from far away, the spectrum of this signal will have less high frequency components that the spectrum of the generated Standard Blocking in conv-ttl-blo
Signals with more spectral power in higher frequencies should be routed more carefully,so it is better to leave the easiest paths to them.
In this case, outer pins should be available for output signals and inner pins to input ones.

As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64.
Hence, none of its pins can be used.
Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

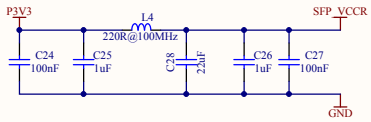


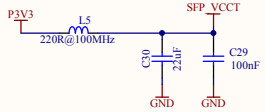


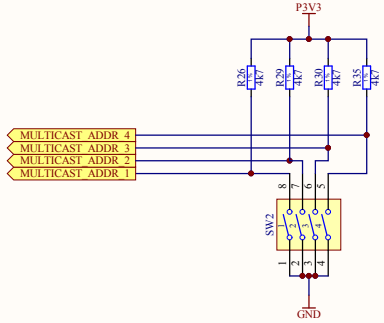


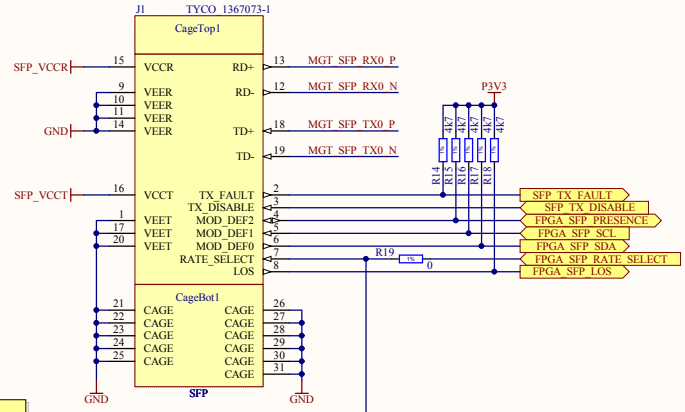
Project/Equipment	*
Document	CONV-TTL-RS485 VME64X
BE-CO	
European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	
EDA-XXXXX-VX-X	

Designer	Carlos Gil Soriano	
Drawn by	Carlos Gil Soriano	12/03/2012
Check by	EVB, MC, EG	21/05/2012
Last Mod.	-	21/06/2012
File	VME64xConn.SchDoc	
Print Date	21/06/2012 14:31:33	Sheet 5 of 13
Size	A3	Rev 3

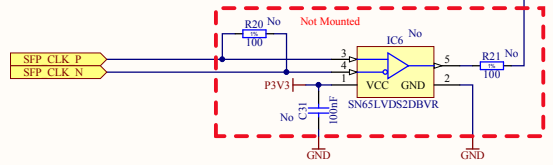




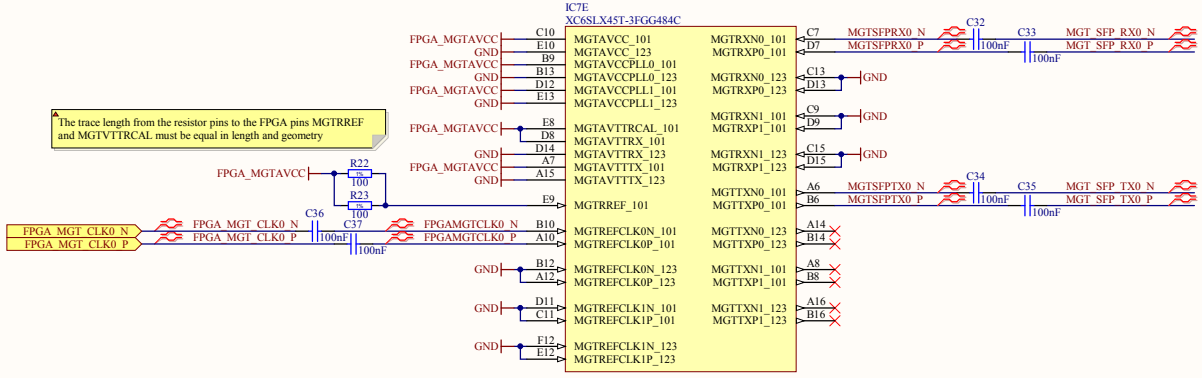




The LVDS receiver can be used to feed a clock to a "custom white rabbit copper SFP".

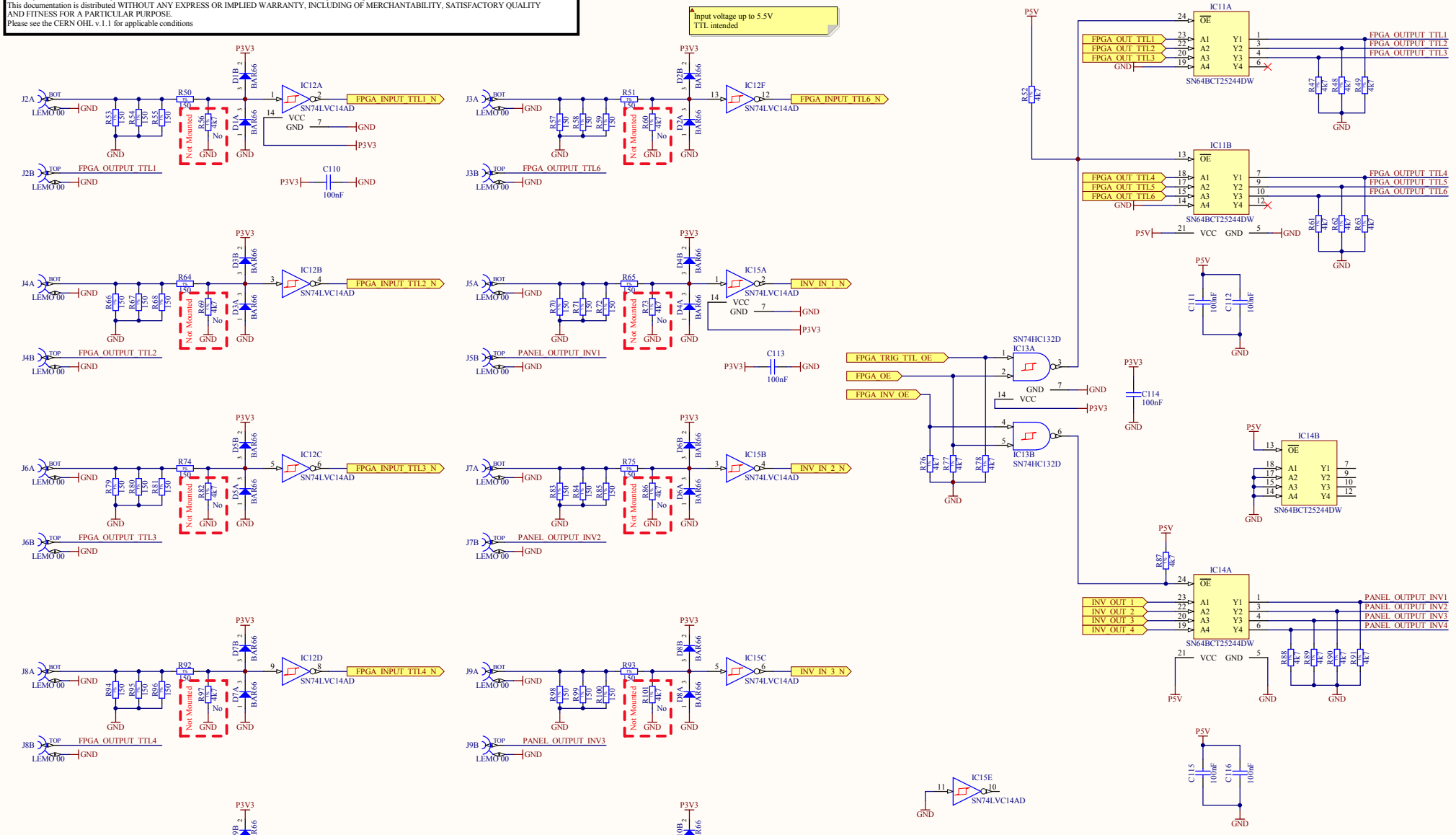


The trace length from the resistor pins to the FPGA pins MGTRREF and MGTVTTRCAL must be equal in length and geometry



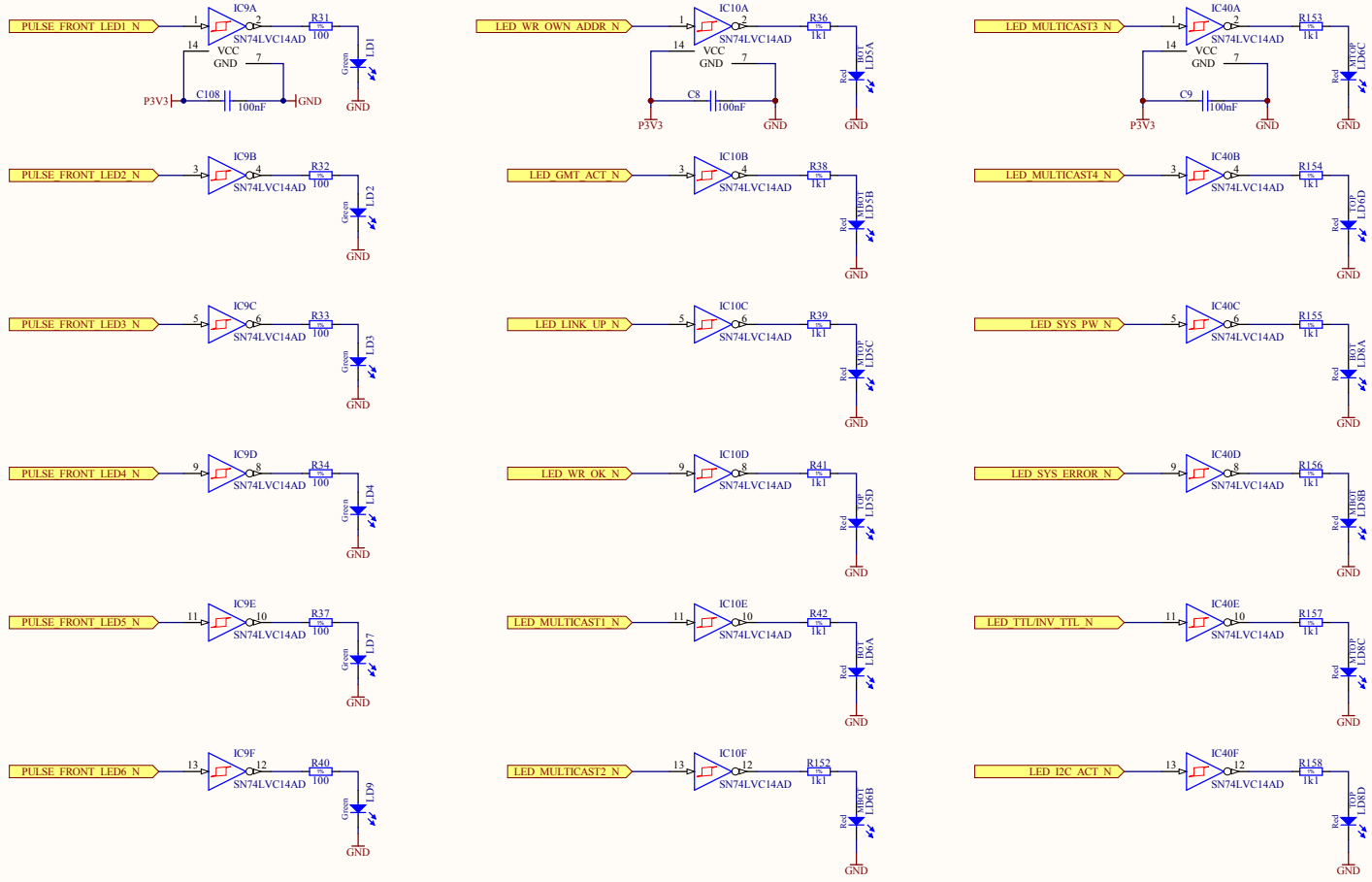
Project/Equipment	*		
Document	CONV-TTL-RS485 MGTX	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	21/05/2012
		Check by EVB, MC, EG	09/05/2012
		Last Mod. -	21/06/2012
		File Communication.SchDoc	
		Print Date 21/06/2012 14:31:34	Sheet 6 of 13
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev 3

Input voltage up to 5.5V
TTL intended

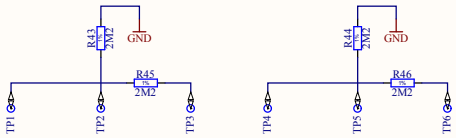


Project/Equipment	*		
Document	CONV-TTL-RS485 FRONT TTL	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	12/03/2012
		Check by EVB, MC, EG	21/05/2012
		Last Mod. -	21/06/2012
		File FrontTTL.SchDoc	
		Print Date 21/06/2012 14:31:34	Sheet 7 of 13
BE-CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev 3

BIVAR model
Red H485CHDL 1.8V@ 2mA



ESD discharge strips (top and bottom of the card)



FTG1 FTG2
FTG3 FTG4
FTG5 FTG6

Project/Equipment	*
Document	CONV-TTL-RS485 FRONT PANEL
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 12/03/2012
Check by	EVB, MC, EG 21/05/2012
Last Mod.	- 21/06/2012
File	FrontPanelLeds.SchDoc
Print Date	21/06/2012 14:31:35
Sheet	8 of 13
Size	A3
Rev	3

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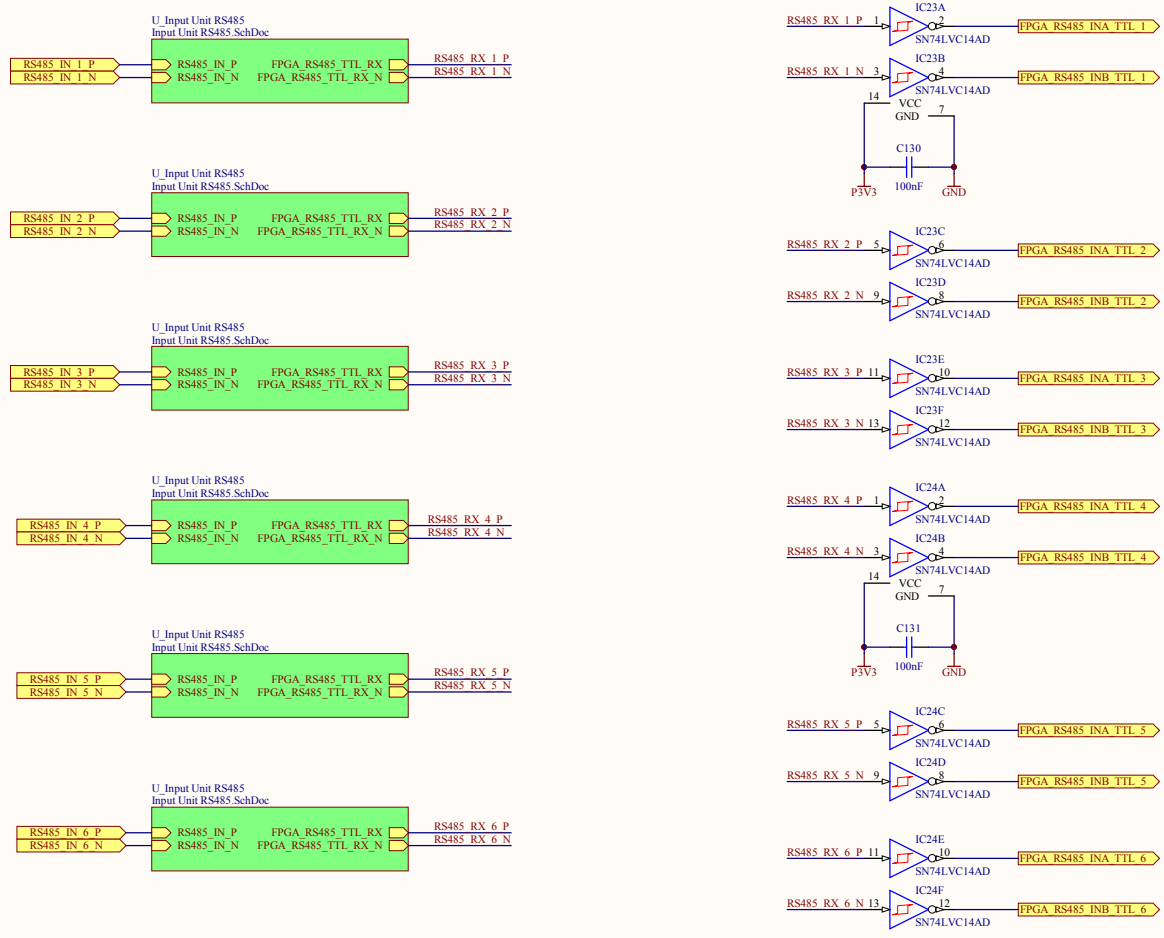
EDA-XXXXX-VX-X



Project/Equipment

Document

BE-CO

CONV-TTL-RS485 INPUT CHANNELS

Designer	Carlos Gil Soriano	
Drawn by	Carlos Gil Soriano	12/03/2012
Check by	EVB, MC, EG	21/05/2012
Last Mod.	-	21/06/2012
File	Input RS485.SchDoc	
Print Date	21/06/2012 14:31:35	Sheet 9 of 13

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EDA-XXXXX-VX-X

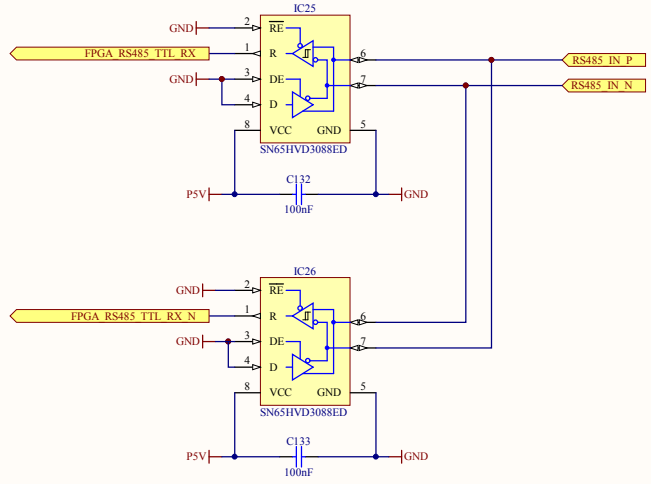
Size A3 | Rev 3

Extra functionality: DETECTION OF LOW DIFFERENTIAL SIGNAL

This extra feature can be used to monitor whether the input link is alive. Having not enough differential signal can be interpreted in several ways:
- We are experiencing a lot of attenuation in the link
- Cable is not connected
- DC supression device, such a transformer, has been connected in the link.

HOW TO IMPLEMENT
First, a glance to the SN65HVD3088ED shows that the input differential thresholds V+_in and V-_in are both negative. By connecting receivers
with the differential pins swapped we can define a voltage range between [-V-_in, V-_in] in which a fault detection can be issued by ANDing the
R pins of the two receivers (this will be internally done in the FPGA).

Further information can be found in Texas Instruments technical document slyt257.



Project/Equipment

Document

BE-CO

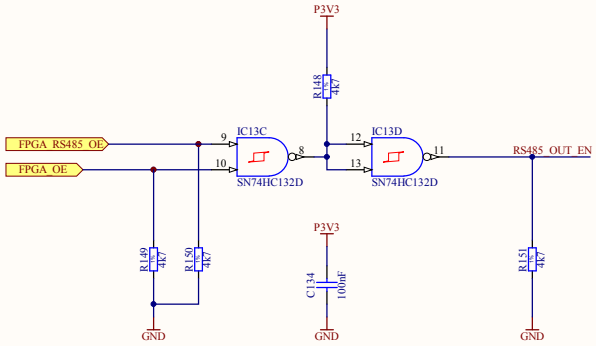
CONV-TTL-RS485
INPUT UNIT

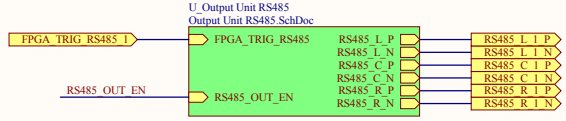
Designer	Carlos Gil Soriano	
Drawn by	Carlos Gil Soriano	12/03/2012
Check by	EVB, MC, EG	21/05/2012
Last Mod.	-	21/06/2012
File	Input Unit RS485.SchDoc	
Print Date	21/06/2012 14:31:36	Sheet 10 of 13

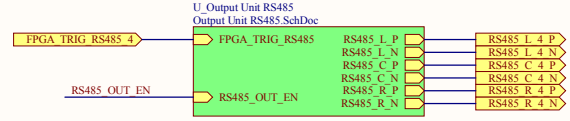
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

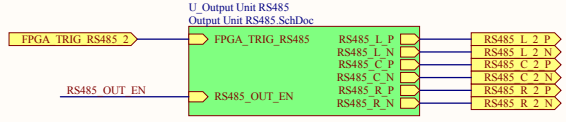
EDA-XXXXX-VX-X

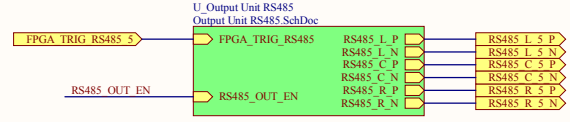
Size A3 | Rev 3

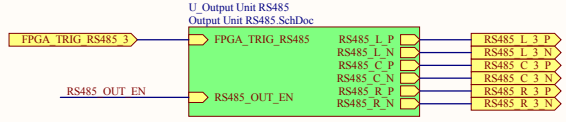


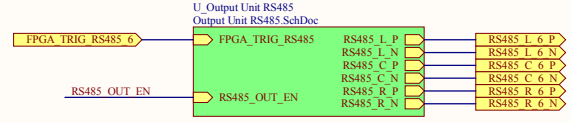












Project/Equipment

Document

CONV-TTL-RS485
OUTPUT CHANNELS

BE-CO

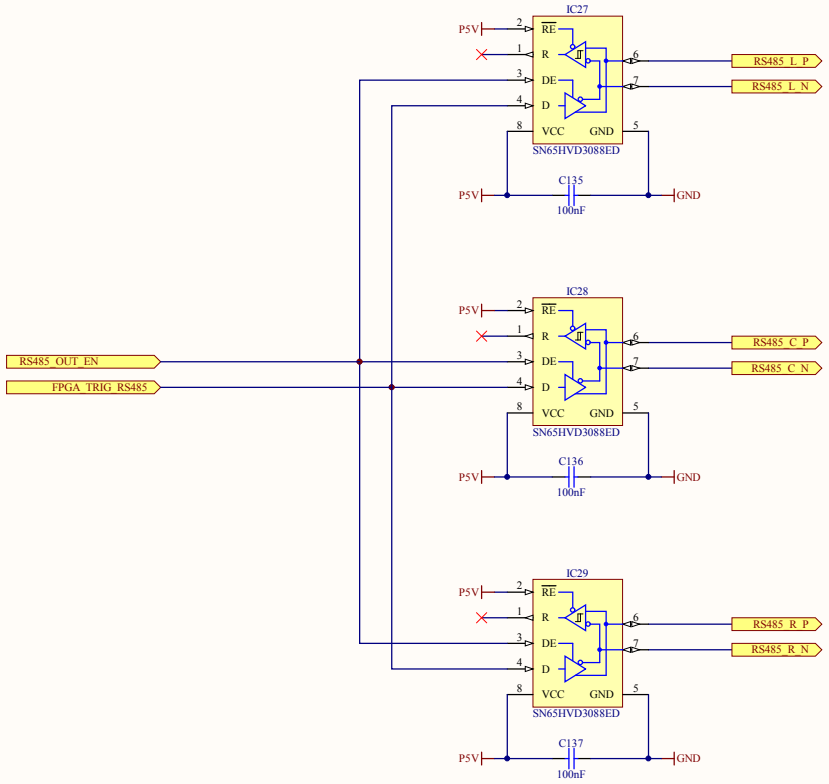
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

Designer	Carlos Gil Soriano	
Drawn by	Carlos Gil Soriano	12/03/2012
Check by	EVB, MC, EG	21/05/2012
Last Mod.	-	21/06/2012
File	Output RS485.SchDoc	
Print Date	21/06/2012 14:31:36	Sheet 11 of 13

EDA-XXXXX-VX-X

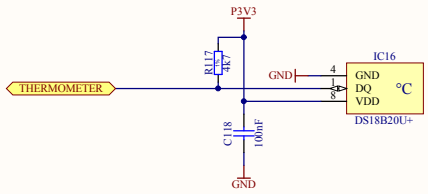
Size A3 | Rev 3

Every SN65HVD3088ED can drive up to 256 nodes

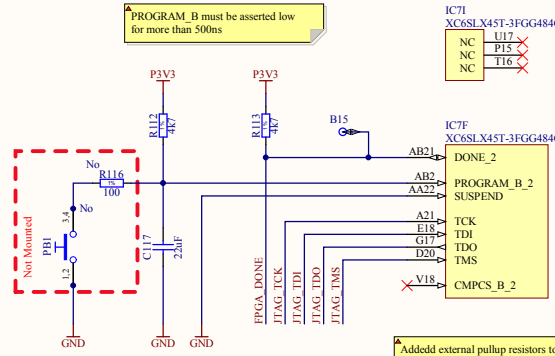


Project/Equipment		
Document	**CONV-TTL-RS485 OUTPUT UNIT**	Designer Carlos Gil Soriano
BE-CO		Drawn by Carlos Gil Soriano 12/03/2012
		Check by EVB, MC, EG 21/05/2012
		Last Mod. - 21/06/2012
		File Output Unit RS485.SchDoc
		Print Date 21/06/2012 14:31:36 Sheet 12 of 13
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev 3

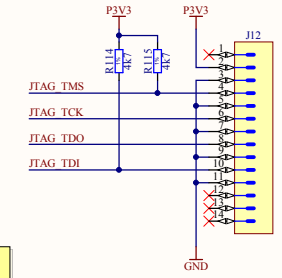
Thermometer will be used to have a FPGA unique ID

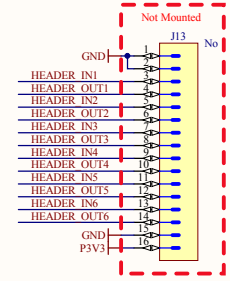


PROGRAM_B must be asserted low for more than 500ns



Addedd external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433
However as the JTAG TAP controller fsm is in reset always that TMS experiences two consecutives ones, we can leave it pulled up.
UG380 pg56: the four JTAG pins are internally pulled up.
Hence, there's no need of external ones.

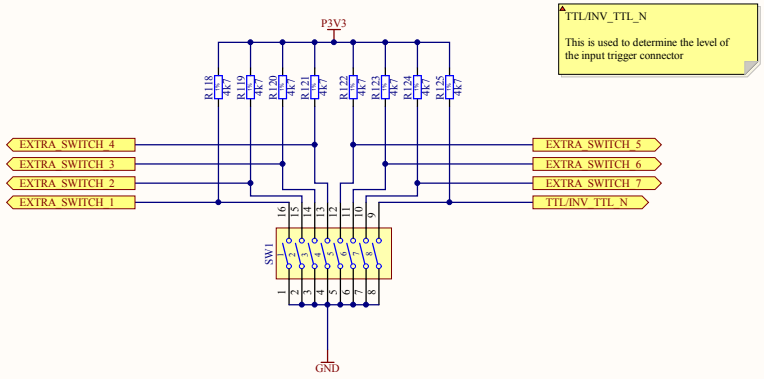


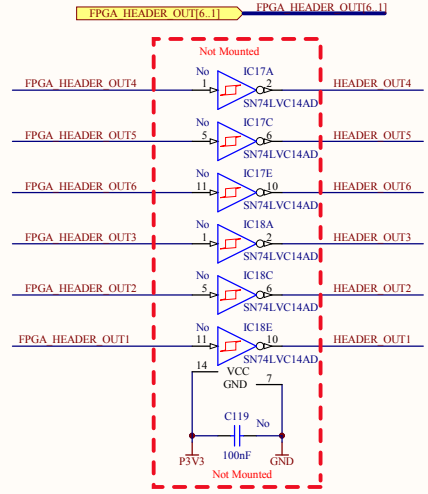


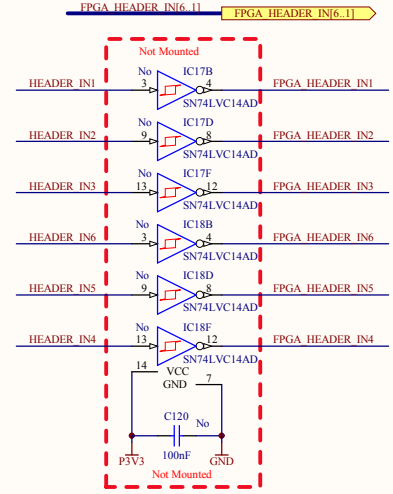
RFU switch

TTL/INV_TTL_N

This is used to determine the level of the input trigger connector

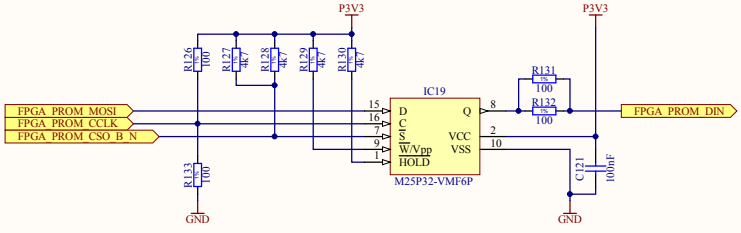






PROM MEMORY

W_N is 1 to allow writes in the memory



Project/Equipment	*
Document	CONV-TTL-RS485 JTAG
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 12/03/2012
Check by	EVB, MC, EG 21/05/2012
Last Mod.	- 21/06/2012
File	JTAG&Button.SchDoc
Print Date	21/06/2012 14:31:37
Sheet	13 of 13
Size	A3
Rev	3

BE-CO

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-XXXXX-VX-X

Comment	Description	Designator	Footprint	LibRef	Quantity
Test Point	Single Terminal Socket	B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16	VERO_20-2136	VERO_20-2136	16
100nF	Non-polarised capacitor	C1, C2, C3, C5, C7, C8, C9, C17, C18, C19, C20, C21, C22, C23, C24, C27, C29, C31, C32, C33, C34, C35, C36, C37, C38, C41, C48, C49, C50, C51, C52, C53, C54, C55, C60, C61, C62, C63, C66, C67, C68, C72, C73, C74, C75, C83, C84, C85, C86, C90, C91, C92, C93, C101, C102, C103, C104, C108, C110, C111, C112, C113, C114, C115, C116, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132_U_Input Unit RS4851, C132_U_Input Unit RS4852, C132_U_Input Unit RS4853, C132_U_Input Unit RS4854, C132_U_Input Unit RS4855, C132_U_Input Unit RS4856, C133_U_Input Unit RS4851, C133_U_Input Unit RS4852, C133_U_Input Unit RS4853, C133_U_Input Unit RS4854, C133_U_Input Unit RS4855, C133_U_Input Unit RS4856, C134, C135_U_Output Unit RS4851,	CAPC1005X55N	CC0402_100NF_16V_10%_X7R	110
22uF	Non-polarised capacitor	C4, C10, C11, C12, C13, C15, C16, C28, C30, C40, C42, C43, C56, C57, C64, C69, C77, C78, C79, C80, C87, C95, C96, C97, C98, C107, C117	CAPC3216X180N	CC1206_22UF_10V_10%_X7R	27
1uF	Non-polarised capacitor	C6, C14, C25, C26, C44, C45, C46, C47, C58, C59, C65, C70, C71, C81, C82, C88, C89, C99, C100, C105, C106	CAPC1608X87N	CC0603_1UF_16V_10%_X7R	21
150uF	Polarised capacitor	C39, C76, C94	CAPPR350-850X700	CAER_150UF_6.3V_20%_SANYO_6SEQP150M	3
SFP	SFP Cage Bottom (Small Form-factor Pluggable)	CageBot1	TYCO_6367034-1	TYCO_6367034-1	1
SFP	SFP Cage Top (Small Form-factor Pluggable)	CageTop1	TYCO_6367035-1	TYCO_6367035-1	1
BAR66	Serial Diode	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10	SOT95P240X110-3N	BAR66	10
2A-125V	Fuse	F1, F2	FUSE_LITTELFUSE_0154	FUSE_LITTELFUSE_0154002.DR	2
Use only in PCB	Fiducial Target	FTG1, FTG2, FTG3, FTG4, FTG5, FTG6	FIDUCIAL_TOP_S200-400	FIDUCIAL_TARGET_S200-400	6
AD5662BRMZ-1	2.7V to 5.5V, 250uA, Rail-to-Rail Output 16-Bit nanoDAC	IC1, IC2	SOP65P490X110-8N	AD5662BRMZ-1	2
LM336M-2.5/NOPB	Reference Diode	IC3	SOIC127P600X175-8N	LM336M-2.5/NOPB	1
LP5951MF-3.0/NOPB	150mA Micropower Low-Dropout CMOS Voltage Regulator	IC4	SOT95P284X122-5N	LP5951MF-3.0/NOPB	1
CDCM61004RHBT	Four Output, Integrated VCO, Low-Jitter Clock Generator	IC5	QFN50P500X500X100-33N-S355	CDCM61004RHBT	1
SN65LVDS2DBVR	High-Speed Differential Line Receiver	IC6	SOT95P280X145-5N	SN65LVDS2DBVR	1
XC6SLX45T-3FGG484C	Spartan-6 LXT 1.2V FPGA, 296 User I/Os, 484-Ball Fine-Pitch BGA (1.0mm Pitch), Speed Grade 3, Commercial Grade, Pb-Free	IC7	BGA484C100P22X22_2300X2300X260	XC6SLX45T-3FGG484C	1
TPS54312PWP	3V to 6V Input, 3A Output Synchronous-Buck PWM Switcher With Integrated FETs (SWIFT)	IC8	SOP65P640X120-21N-R240X340	TPS54312PWP	1
SN74LVC14AD	Hex Schmitt-Trigger Inverter	IC9, IC10, IC12, IC15, IC17, IC18, IC21, IC22, IC23, IC24, IC40	SOIC127P600X175-14N	SN74LVC14AD	11
SN64BCT25244DW	25-Ohm Octal Buffer/Driver with 3-State Outputs	IC11, IC14	SOIC127P1030X265-24N	SN64BCT25244DW	2
SN74HC132D	Quad Positive NAND Gate With Schmitt-Trigger Input	IC13	SOIC127P600X175-14N	SN74HC132D	1
DS18B20U+	Programmable Resolution 1-Wire Digital Thermometer	IC16	SOP65P490X110-8N	DS18B20U+	1
M25P32-VMF6P	32 Mbit, low-voltage, Serial Flash memory with 75-MHz SPI bus interface	IC19	SOIC127P1030X265-16N	M25P32-VMF6P	1
SN74VMEH22501DGGR	8-Bit Universal Bus Transceiver and Two 1-Bit Bus Transceivers with 3-State Outputs	IC20	SOP50P810X120-48N	SN74VMEH22501DGGR	1
SN65HVD3088ED	Low-Power RS-485 Transceiver	RS4851, IC25_U_Input Unit RS4852, IC25_U_Input Unit RS4853, IC25_U_Input Unit RS4854, IC25_U_Input Unit RS4855, IC25_U_Input Unit RS4856, IC26_U_Input Unit RS4851, IC26_U_Input Unit RS4852, IC26_U_Input Unit RS4853, IC26_U_Input Unit RS4854, IC26_U_Input Unit RS4855, IC26_U_Input Unit RS4856, IC27_U_Output Unit RS4851, IC27_U_Output Unit RS4852, IC27_U_Output Unit RS4853, IC27_U_Output Unit RS4854, IC27_U_Output Unit RS4855, IC27_U_Output Unit RS4856, IC28_U_Output Unit RS4851, IC28_U_Output Unit RS4852, IC28_U_Output Unit RS4853, IC28_U_Output Unit RS4854, IC28_U_Output Unit RS4855, IC28_U_Output Unit RS4856, IC29_U_Output Unit RS4851, IC29_U_Output Unit RS4852, IC29_U_Output Unit	SOIC127P600X175-8N	SN65HVD3088ED	30
SFP	20 Position SFP Connector (Small Form-factor Pluggable)	J1	TYCO_1367073-1	TYCO_1367073-1	1
LEMO 00	Dual Female Coax 1-2 Common Shield 3	J2, J3, J4, J5, J6, J7, J8, J9, J10, J11	LEMO_EPY.00.250.NTNY	LEMO_EPY.00.250.NTNY	10
Milli-Grid?	Connector 14 Male	J12	MOLEX_87832-1420	MOLEX_87832-1420	1
Header 16	Connector 16 Male	J13	COMATEL_389.0358.1.16.400	COMATEL_389.0358.1.16.400	1
220R@100MHz	Inductor	L1, L2, L3, L4, L5, L7, L8, L9	INDC2012X105N	IND0805_MURATA_BLM21PG221SN1D	8
10uH	Inductor With Magnetic core	L6	IND_COILCRAFT_DO3316	IND_10UH_20%_COILCRAFT_DO3316P-103MLD	1
Green	LED Green 1C 2A	LD1, LD2, LD3, LD4, LD7, LD9	LED_DIALIGHT_551-1307F	LED_DIALIGHT_551-1307F	6
HE Red	LED x4 Red 1C2A-BOT_3C4A_5C6A_7C8A-TOP	LD5, LD6, LD8	LED_BIVAR_H485CHDL	LED_BIVAR_H485CHDL	3
20MHz	3.3V ±100ppm 15pF HCMOS Tri-State Surface Mount Voltage Controlled Oscillator VCXO (CFPV-45 Serie)	OSC1	OSC_IQD_CFPV-45	OSC_20MHZ_IQD_LFVCXO026156	1
25MHz	Oscillator 4 pins 1=VC 2=GND 3=OUT 4=+Vs	OSC2	OSCCC320X500X160-4N	OSC_25MHZ_MERCURY_VM53S3-25.000-2.5/-30+75	1
25MHz	Oscillator 4 pins 1=VCO 3=GND 4=OUT 6=VDC	OSC3	OSC_RAKON_IVT3200C	OSC_25MHZ_RAKON_IVT3205CR	1
HAR-BUS 64	Connector 160zabcd Male (5x32)	P1, P2	HARTING_02 01 160 2101	HARTING_02 01 160 2101	2
Push Button	Push-Button Switch SPDT	PB1	PB_TYCO_ALCOSWITCH_FSM2JSMA	PB_TYCO_ALCOSWITCH_FSM2JSMA	1
100	Resistor - 1%	R1, R2, R3, R4, R5, R20, R21, R22, R23, R31, R32, R33, R34, R37, R40, R116, R126, R131, R132, R133	RESC1608X55N	R0603_100R_1%_0.1W_100PPM	20
0	Resistor - 1%	R6, R7, R8, R9, R10, R11, R12, R13, R19	RESC1608X55N	R0603_0R_JUMPER	9
4k7	Resistor - 1%	R14, R15, R16, R17, R18, R24, R25, R26, R29, R30, R35, R47, R48, R49, R52, R56, R60, R61, R62, R63, R69, R73, R76, R77, R78, R82, R86, R87, R88, R89, R90, R91, R97, R101, R107, R111, R112, R113, R114, R115, R117, R118, R119, R120, R121, R122, R123, R124, R125, R127, R128, R129, R130, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151	RESC1608X55N	R0603_4K7_1%_0.1W_100PPM	71
2M2	Resistor - 1%	R27, R28, R43, R44, R45, R46	RESC3216X65N	R1206_2M2_1%_0.25W_100PPM	6
1k1	Resistor - 1%	R36, R38, R39, R41, R42, R152, R153, R154, R155, R156, R157, R158	RESC1608X55N	R0603_1K1_1%_0.1W_100PPM	12
150	Resistor - 1%	R50, R51, R53, R54, R55, R57, R58, R59, R64, R65, R66, R67, R68, R70, R71, R72, R74, R75, R79, R80, R81, R83, R84, R85, R92, R93, R94, R95, R96, R98, R99, R100, R102, R103, R104, R105, R106, R108, R109, R110	RESC3216X65N	R1206_150R_1%_0.25W_100PPM	40
Switch	8 Ways SPST DIP Switch	SW1	SW_TYCO_1-1571983-0	SW_TYCO_1-1571983-0	1
Switch	4 Ways SPST DIP Switch	SW2	SW_TYCO_1571983-4	SW_TYCO_1571983-4	1
Test Point	Test Point	TP1, TP2, TP3, TP4, TP5	TPS127	SMD_PAD_1.27X1.27MM	6