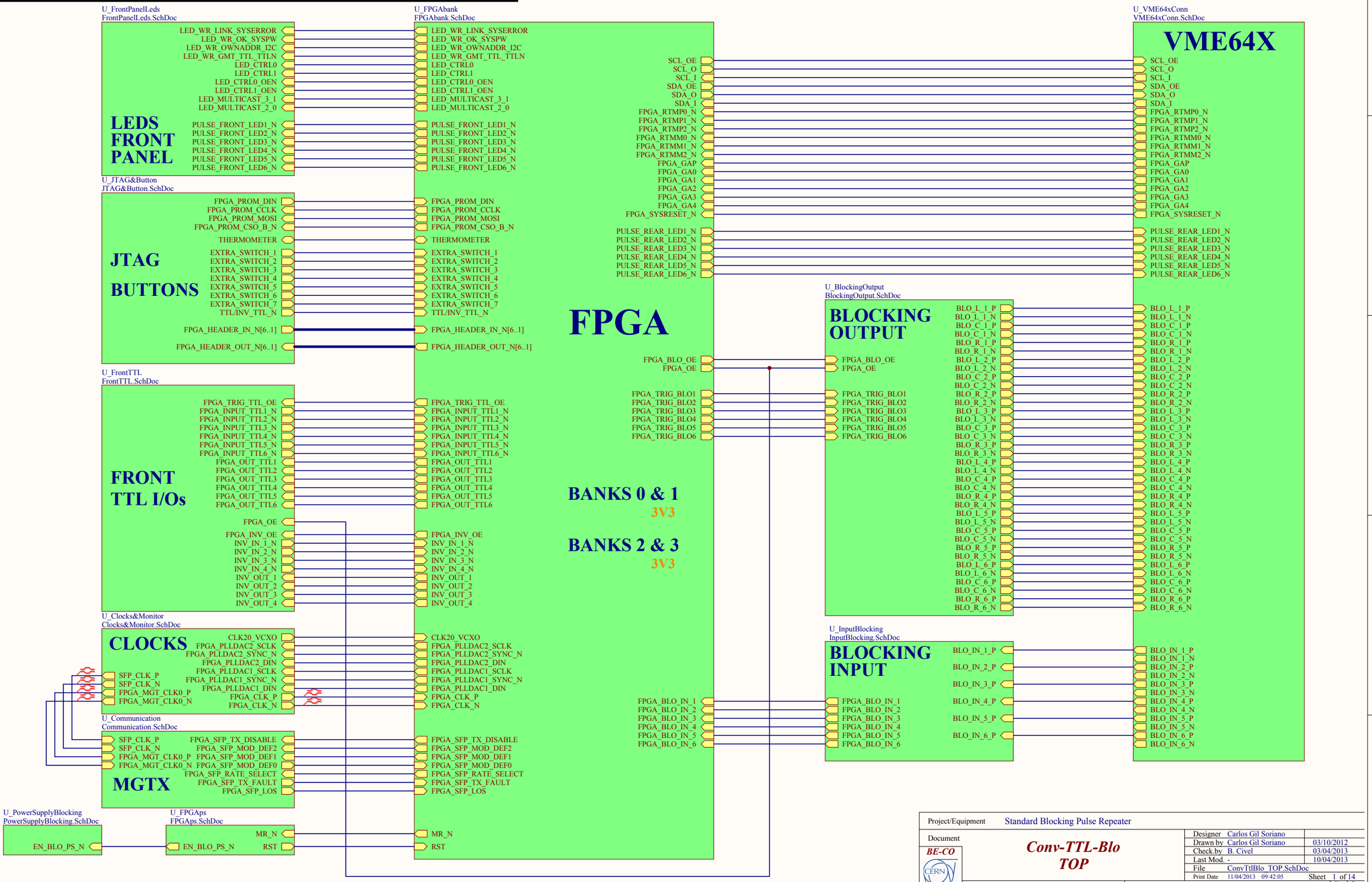


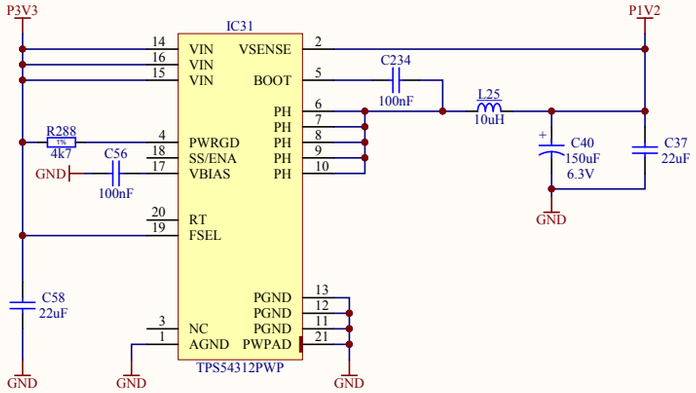
Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo TOP
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check.by	B. Civel 03/04/2013
Last Mod.	- 10/04/2013
File	ConvTtlBlo_TOP.SchDoc
Print Date	11/04/2013 09:42:05 Sheet 1 of 14
Size	A3
Rev	1

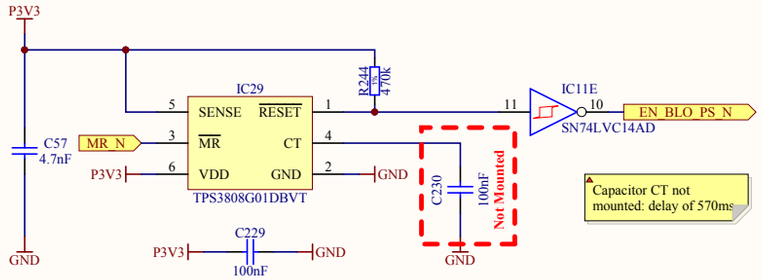
BE-CO

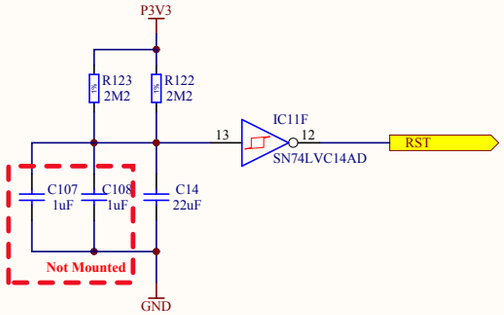
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-02446-V2-1

Efficiency of 85% and better

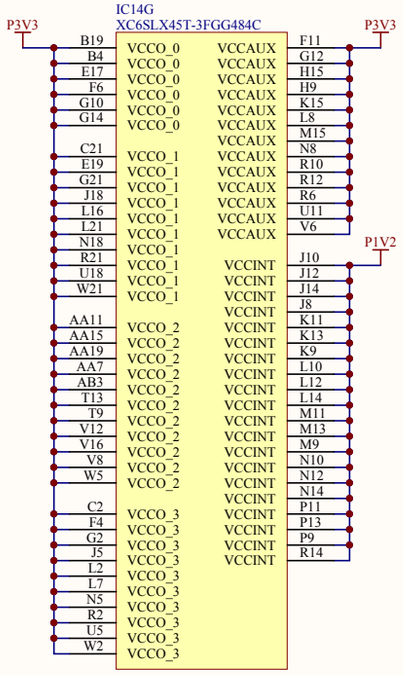


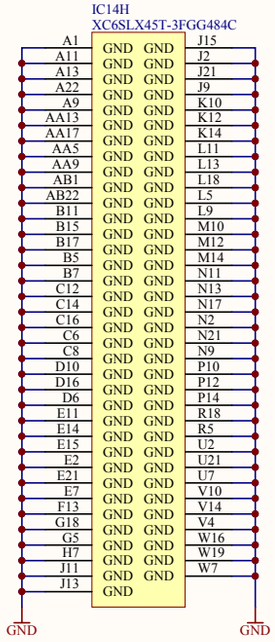




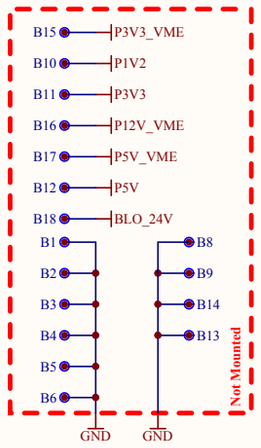
Voltages are:

*** FPGA	
VCCO_0	3V3
VCCO_1	3V3
VCCO_2	3V3
VCCO_3	3V3
VCCaux	3V3
VCCint	1V2
*** PROM	
VCCaux	3V3



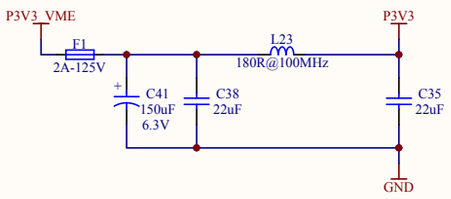


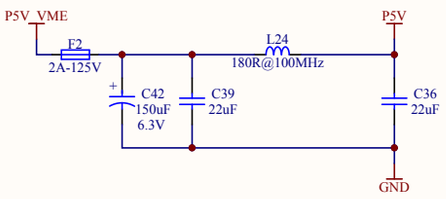
Test points



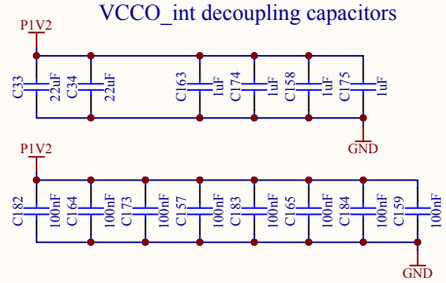
PI filters for decoupling noise in the band of 50 MHz to 150 MHz in 3V3 and 5V rails.

BLM41PG181SN1L is a ferrite with low DCR (max 10mOhm) targeted for high current (power rails).

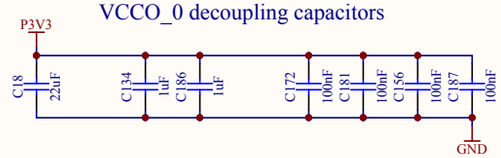




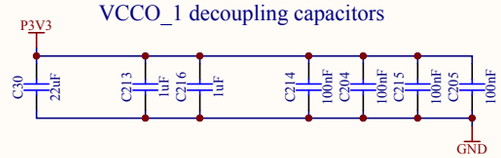
VCCO_int decoupling capacitors



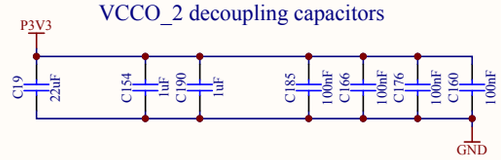
VCCO_0 decoupling capacitors



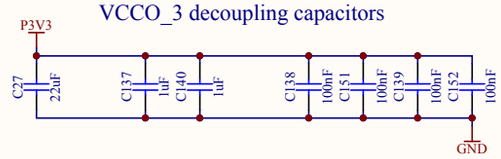
VCCO_1 decoupling capacitors



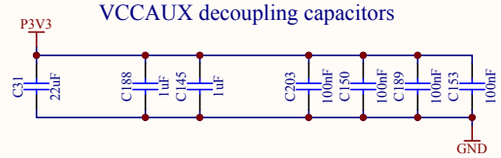
VCCO_2 decoupling capacitors



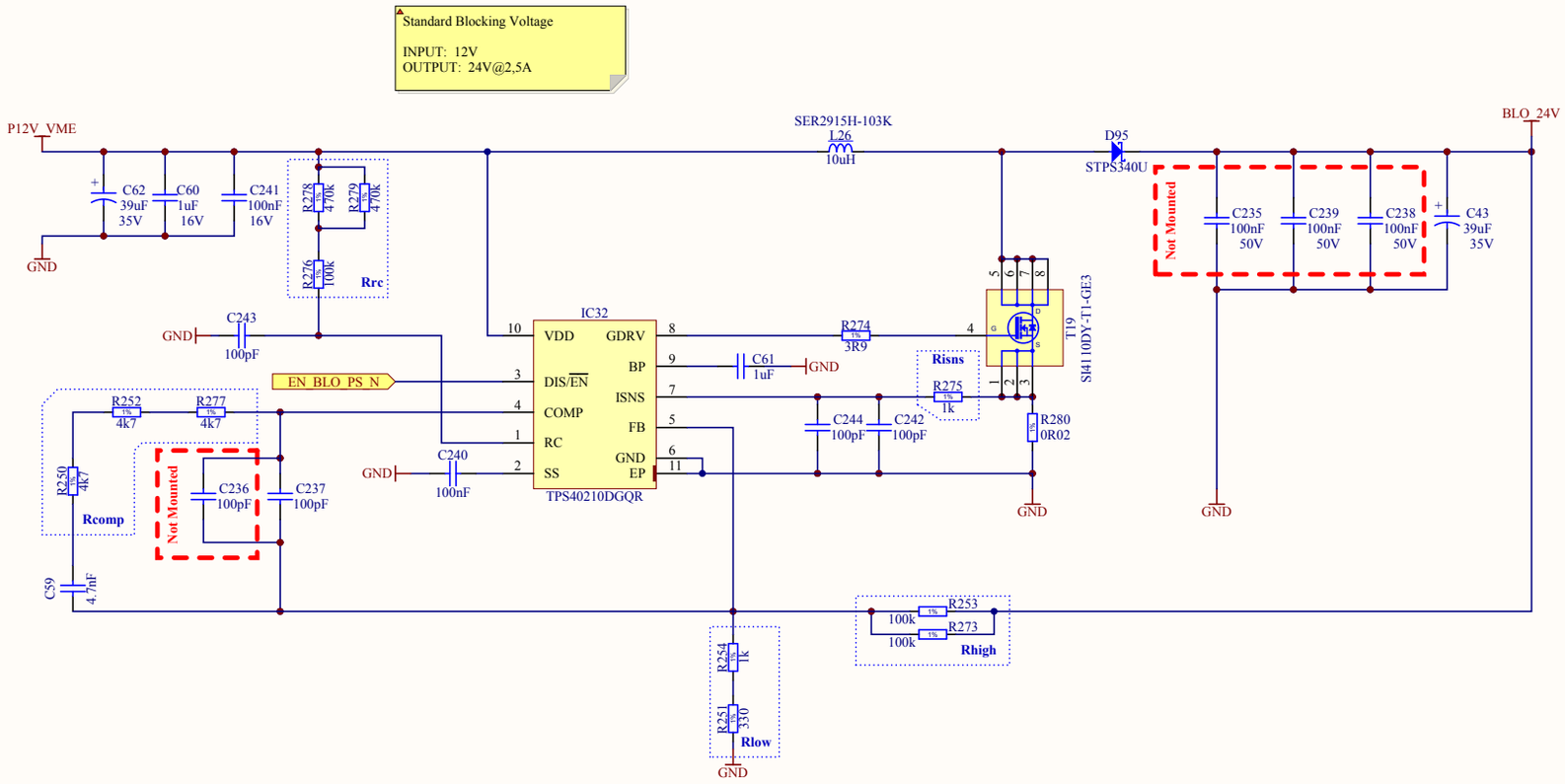
VCCO_3 decoupling capacitors



VCCAUX decoupling capacitors



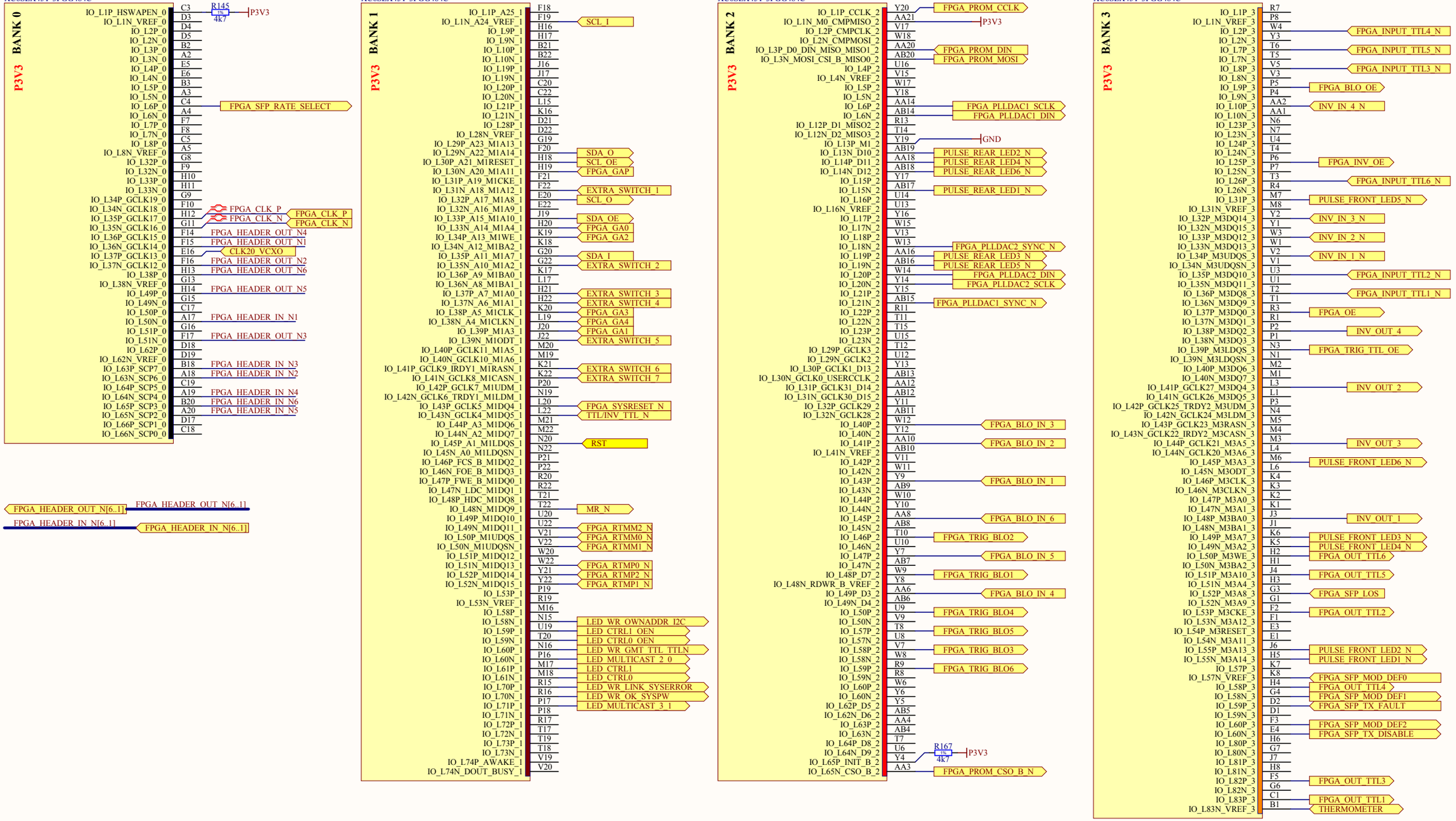
Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo FPGA PS**	Designer	Carlos Gil Soriano
BE-CO		Drawn by	Carlos Gil Soriano 03/10/2012
		Check.by	B. Civel 03/04/2013
		Last Mod.	- 10/04/2013
		File	FPGAps.SchDoc
		Print Date	11/04/2013 09:42:06
		Sheet	2 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-1	Size	A3
		Rev	1



Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo BLOCKING PS
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check.by	B. Civel 03/04/2013
Last Mod.	- 10/04/2013
File	PowerSupplyBlocking.SchDoc
Print Date	11/04/2013 09:42:06 Sheet 3 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-1 Size A3 Rev 1

To allow high SerDes ratios, leave all the trigger inputs and outputs in _P pins.

See Xilinx's document UG381, chapter 3 for further information.

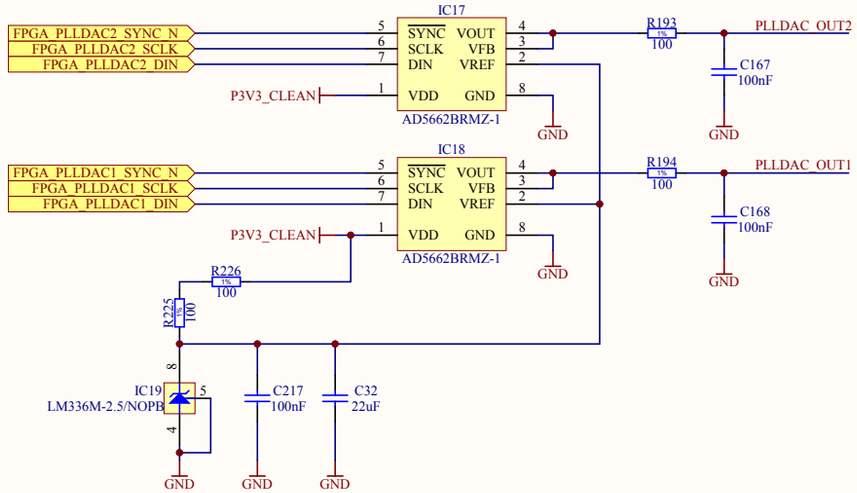


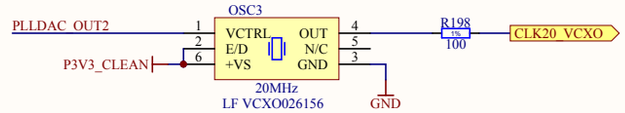
Project/Equipment	Standard Blocking Pulse Repeater
Document	**Conv-TTL-Blo FPGA BANK**
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check.by	B. Civel 03/04/2013
Last Mod.	- 10/04/2013
File	FPGAbank.SchDoc
Print Date	11/04/2013 09:42:06
Sheet	4 of 14
Size	A3
Rev	1

BE-CO

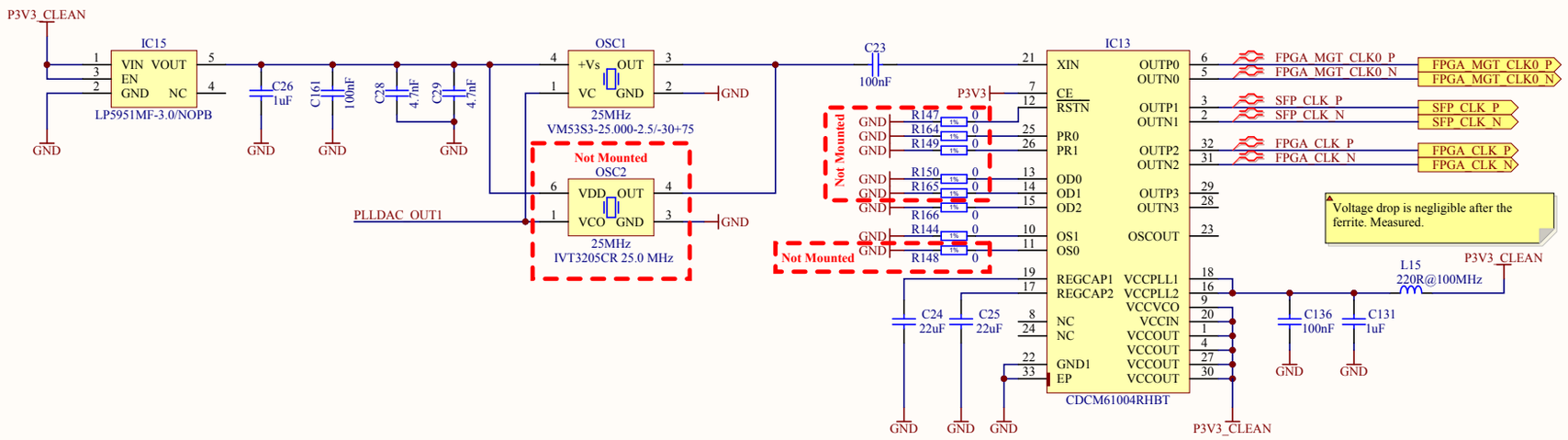
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-02446-V2-1



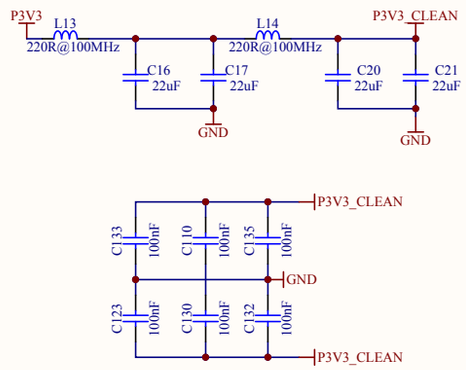


Control voltage is +1.5V ±1V.
Min. pull range is ±10 ppm for ±1V.
Positive slope (Positive voltage for positive frequency shift).

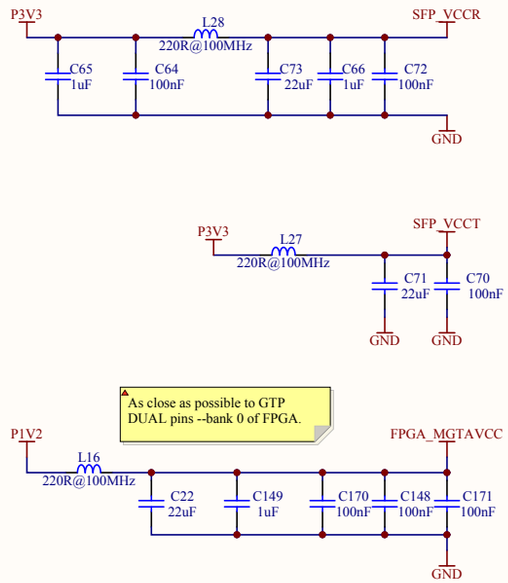


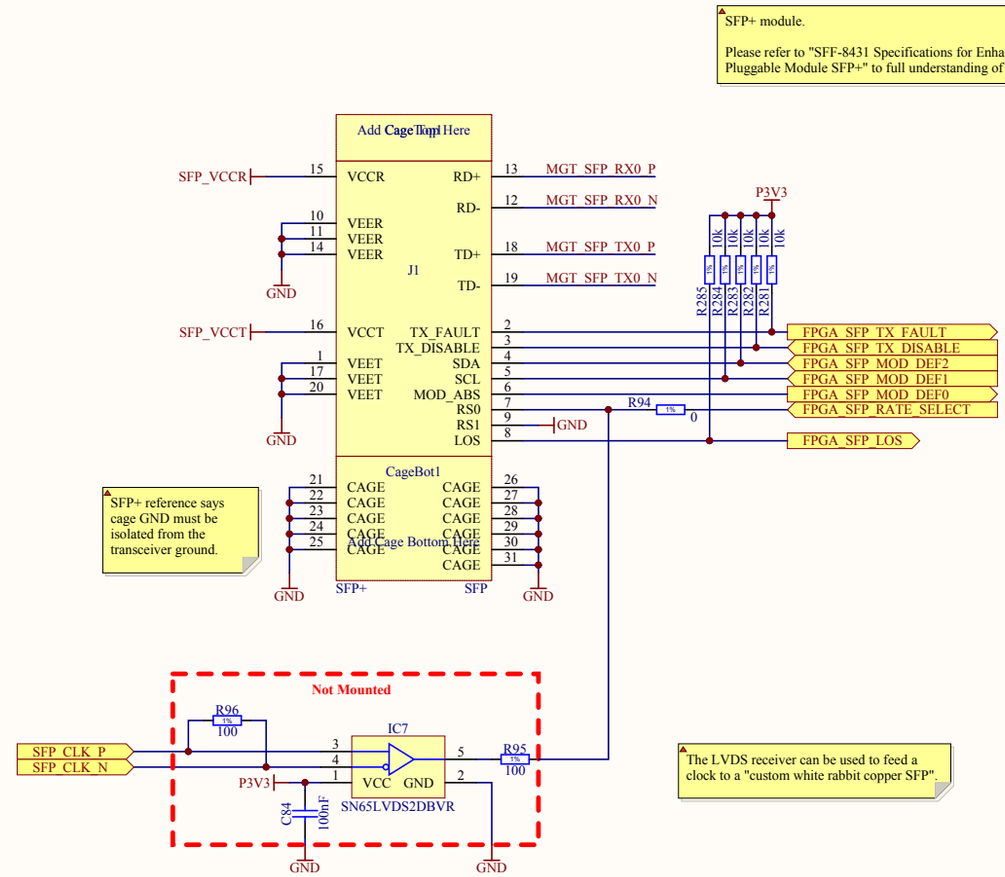
CDCM61004 configuration:
LVDS outputs
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
All config inputs have internal pull-ups.

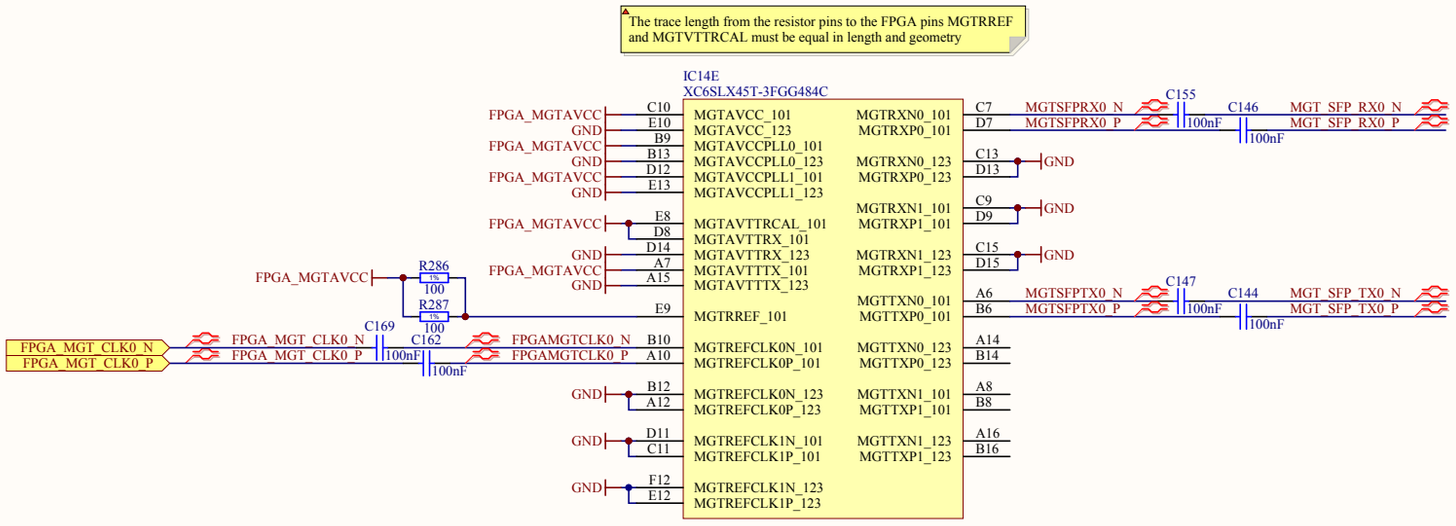
Input = 25 MHz
Output=125 MHz



Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo CLOCKS	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check.by B. Civel	03/04/2013
		Last Mod. -	10/04/2013
		File Clocks&Monitor.SchDoc	
		Print Date 11/04/2013 09:42:06	Sheet 5 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-1	Size A3	Rev 1

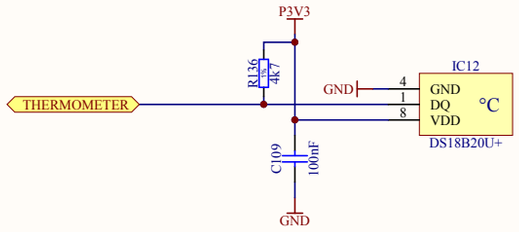




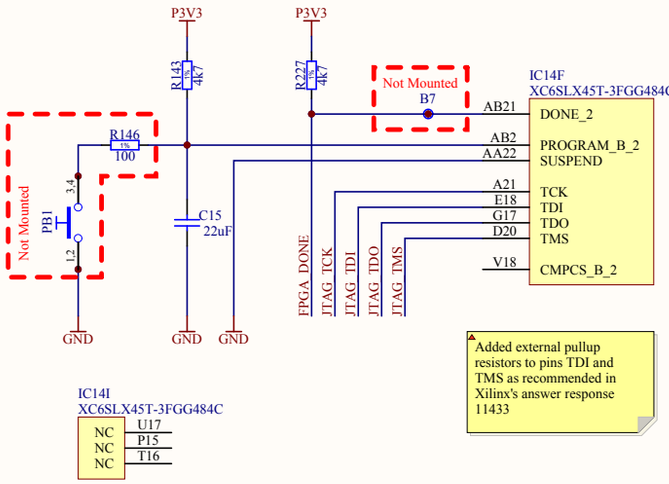


Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo MGTX
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check.by	B. Civel 03/04/2013
Last Mod.	- 10/04/2013
File	Communication.SchDoc
Print Date	11/04/2013 09:42:07 Sheet 6 of 14
BE-CO	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland
EDA-02446-V2-1	Size A3 Rev 1

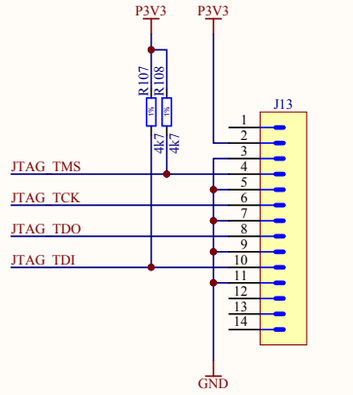
Thermometer will be used to have a FPGA unique ID

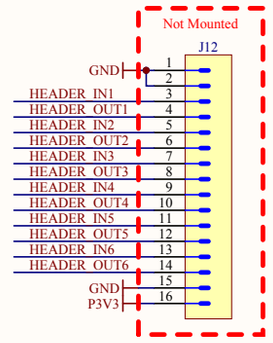


PROGRAM_B must be asserted low for more than 500ns



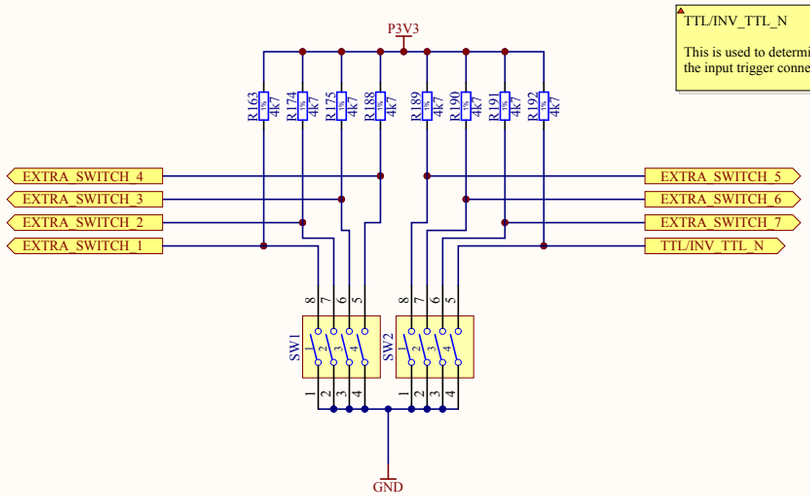
Added external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433

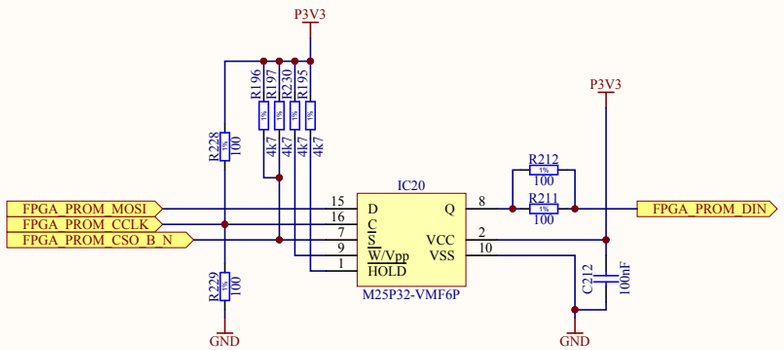


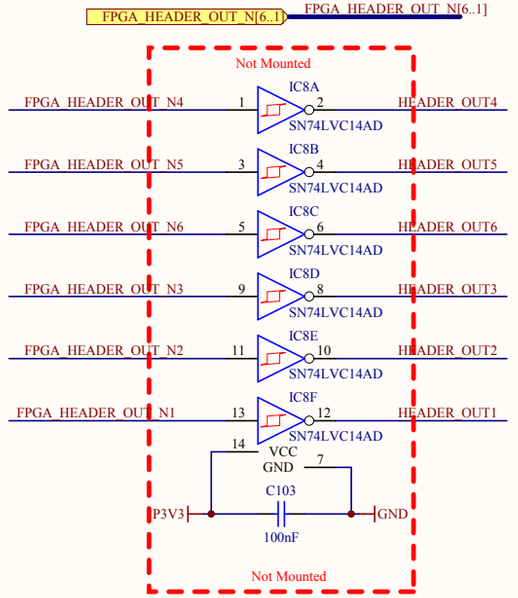


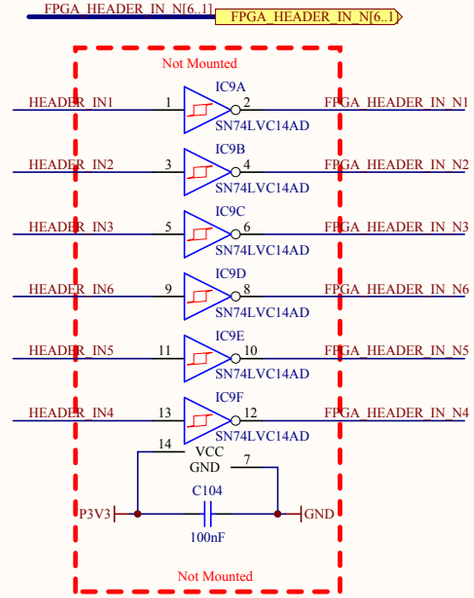
TTL/INV_TTL_N

This is used to determine the level of the input trigger connector









Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo JTAG**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check.by B. Civel	03/04/2013
		Last Mod. -	11/04/2013
		File JTAG&Button.SchDoc	
		Print Date 11/04/2013 09:42:07	Sheet 7 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-1	Size A3	Rev 1

Utility Bus Signal: see page 199
ANSI/VITA 1-1994

Output configurations in page 230
SYSRESET_N Open collector

P1E: GND, GAP, GA0, GA1, GA2, GA3, GA4, P3V3_VME

P1D: VMEP1_SYSRESET_N, P12V_VME, P5V_VME

P1C: BG0IN_N, BG0OUT_N, BG1IN_N, BG1OUT_N, BG2IN_N, BG2OUT_N, BG3IN_N, BG3OUT_N, VMEP1_SERA, VMEP1_SERB, P5V_VME

P1B: GND, IACKIN_N, IACKOUT_N, P5V_VME

P1A: GND

P1F: MTG1, MTG2, GND — Mounting Holes

As each block of BLO+_{X}_n, where X={L, C, R} will be triggered at the same time, cross talk should not be so critical. However, it would be better group the signals as it is shown and leave ground between sets of signals triggered by different sources.

As input signals come from far away, the spectrum of this signal will have less high frequency components that the spectrum of the generated Standard Blocking in conv-ttl-blo
Signals with more spectral power in higher frequencies should be routed more carefully,so it is better to leave the easiest paths to them.
In this case, outer pins should be available for output signals and inner pins to input ones.

As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used.
Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

P2E: GND, BLO_L_1_N, BLO_C_1_N, BLO_R_1_N, BLO_L_2_N, BLO_C_2_N, BLO_R_2_N, BLO_L_3_N, BLO_C_3_N, BLO_R_3_N, BLO_L_4_N, BLO_C_4_N, BLO_R_4_N, BLO_L_5_N, BLO_C_5_N, BLO_R_5_N, BLO_L_6_N, BLO_C_6_N, BLO_R_6_N

P2D: GND, BLO_L_1_P, BLO_C_1_P, BLO_R_1_P, BLO_L_2_P, BLO_C_2_P, BLO_R_2_P, BLO_L_3_P, BLO_C_3_P, BLO_R_3_P, BLO_L_4_P, BLO_C_4_P, BLO_R_4_P, BLO_L_5_P, BLO_C_5_P, BLO_R_5_P, BLO_L_6_P, BLO_C_6_P, BLO_R_6_P

P2C: GND

P2B: VME_RTMM1, VME_RTMM2, BLO_IN_1_P, BLO_IN_1_N, BLO_IN_2_P, BLO_IN_2_N, BLO_IN_3_P, BLO_IN_3_N, BLO_IN_4_P, BLO_IN_4_N, BLO_IN_5_P, BLO_IN_5_N, BLO_IN_6_P, BLO_IN_6_N

P2A: VME_RTMM0, VME_REAR_LED1, VME_REAR_LED2, VME_REAR_LED3, VME_REAR_LED4, VME_REAR_LED5, VME_RTMP0, VME_RTMP1, VME_REAR_LED6, VME_RTMP2

P2F: MTG1, MTG2, GND — Mounting Holes

IC30 — SN74VMEH22501DGGR

SCL_OE	48	1OEAB	
	1	1OEBY	
SCL_O	2	1A	1B 46 VMEP1_SERA
SCL_I	3	1Y	
SDA_OE	41	2OEAB	
	8	2OEBY	
SDA_O	5	2A	2B 43 VMEP1_SERB
SDA_I	6	2Y	
	14	OE	
	24	DIR	
	32	CLKAB	
P3V3	11	LE	
	17	CLKBA	
FPGA_GAP	9	3A1	3B1 40 GAP
FPGA_GA0	12	3A2	3B2 37 GA0
FPGA_GA1	13	3A3	3B3 36 GA1
FPGA_GA2	16	3A4	3B4 33 GA2
FPGA_GA3	19	3A5	3B5 30 GA3
FPGA_GA4	20	3A6	3B6 29 GA4
FPGA_SYSRESET_N	22	3A7	3B7 27 VMEP1_SYSRESET_N
	23	3A8	3B8 26 GND
P3V3	44	BIASVCC	
	7	VCC	GND 45
	18	VCC	GND 39
	25	VCC	GND 34
	31	VCC	GND 28
	35	VCC	GND 21
	38	VCC	GND 15
	42	VCC	GND 10
	47	VCC	GND 4

R290, R289: 4k7 (GND); R291–R296: 4k7 (P3V3_VME)

P3V3: 100nF C225, C233, C231, C226, C228, C232 — GND

R231–R247: 4k7 (P3V3)

VME_RTMM2	13	IC28F	FPGA_RTMM2_N
VME_RTMM1	11	IC28E	FPGA_RTMM1_N
VME_RTMM0	9	IC28D	FPGA_RTMM0_N
VME_RTMP2	5	IC28C	FPGA_RTMP2_N
VME_RTMP1	3	IC28B	FPGA_RTMP1_N
VME_RTMP0	1	IC28A	FPGA_RTMP0_N

SN74LVC14AD; VCC 14, GND 7

PULSE_REAR_LED1_N	1	IC21A	2 VME_REAR_LED1
PULSE_REAR_LED3_N	3	IC21B	4 VME_REAR_LED3
PULSE_REAR_LED5_N	5	IC21C	6 VME_REAR_LED5
PULSE_REAR_LED6_N	9	IC21D	8 VME_REAR_LED6
PULSE_REAR_LED4_N	11	IC21E	10 VME_REAR_LED4
PULSE_REAR_LED2_N	13	IC21F	12 VME_REAR_LED2

SN74LVC14AD; VCC 14, GND 7

C227 100nF (P3V3 — GND); C218 100nF (P3V3 — GND)

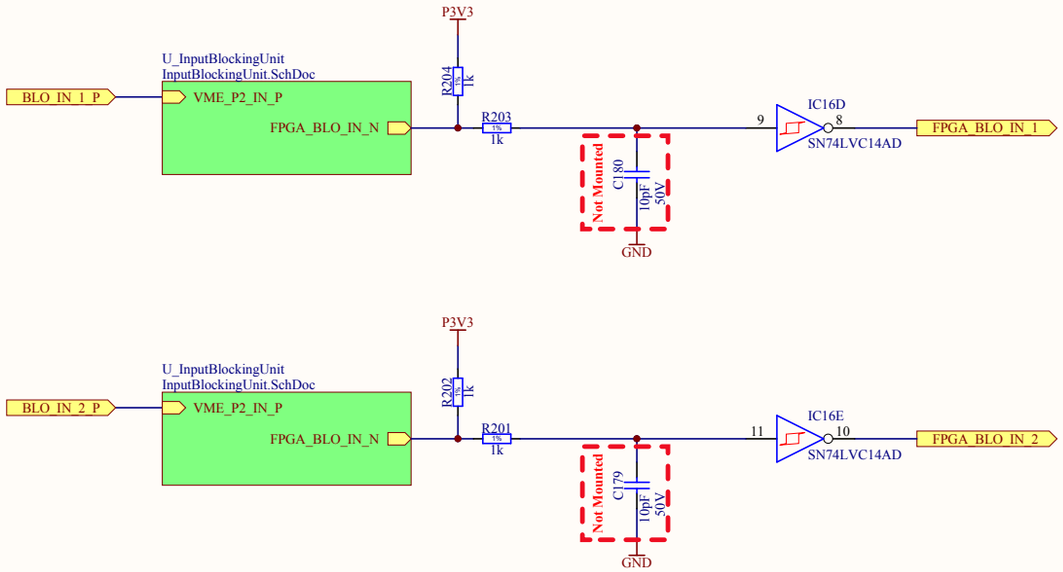
Fixing for P1 & P2: M2.5, PCB, D5xd2.7, M2.5x10 x4

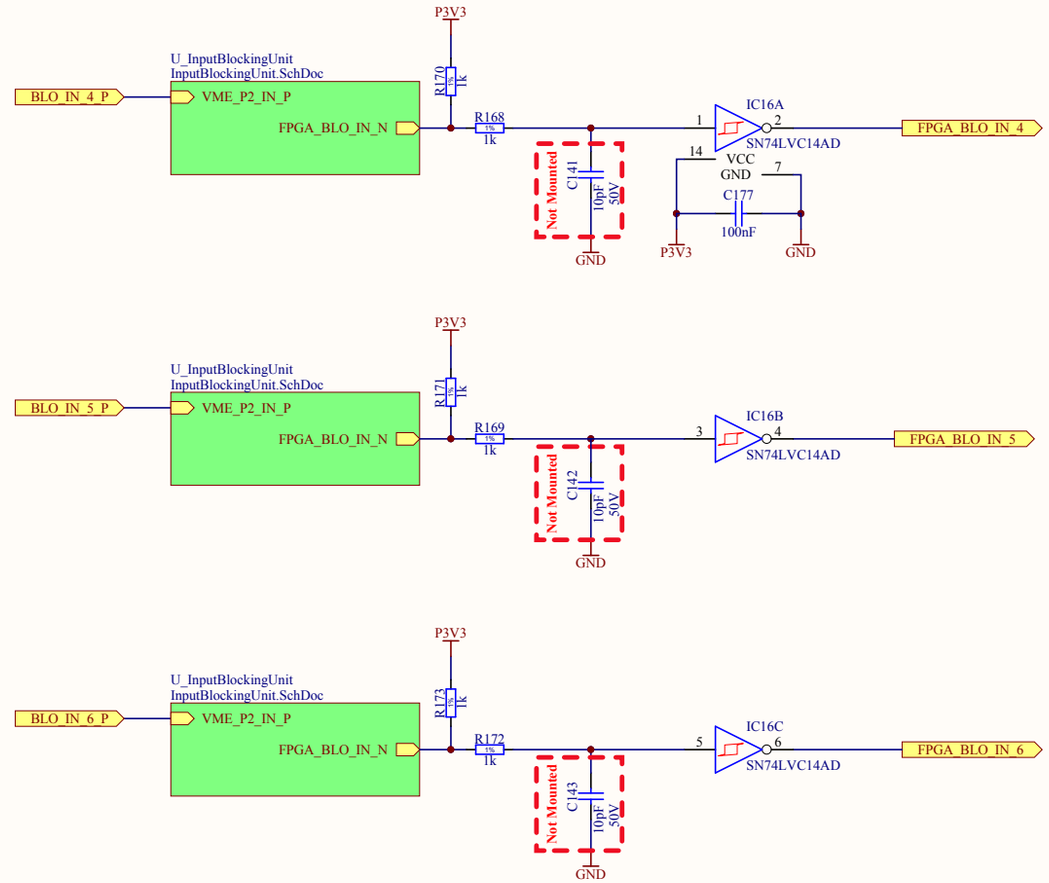
Project/Equipment: Standard Blocking Pulse Repeater
Document: Conv-TTL-Blo VME64X

Designer	Carlos Gil Soriano	
Drawn by	Carlos Gil Soriano	03/10/2012
Check.by	B. Civel	03/04/2013
Last Mod.	-	10/04/2013
File	VME64xConn.SchDoc	
Print Date	11/04/2013 09:42:07	Sheet 8 of 14

BE-CO — CERN
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-02446-V2-1 — Size A3 — Rev 1





Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo INPUT BLO**	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check.by B. Civel	03/04/2013
		Last Mod. -	10/04/2013
		File InputBlocking.SchDoc	
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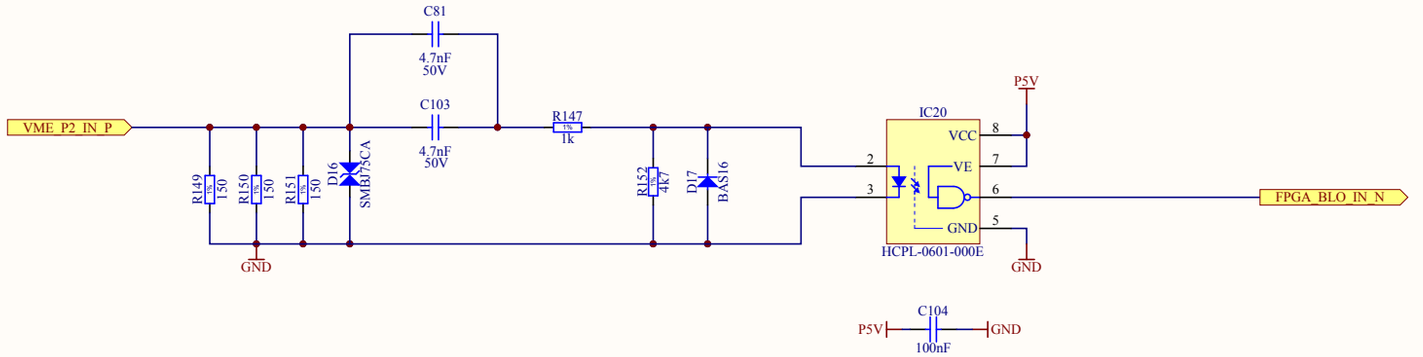
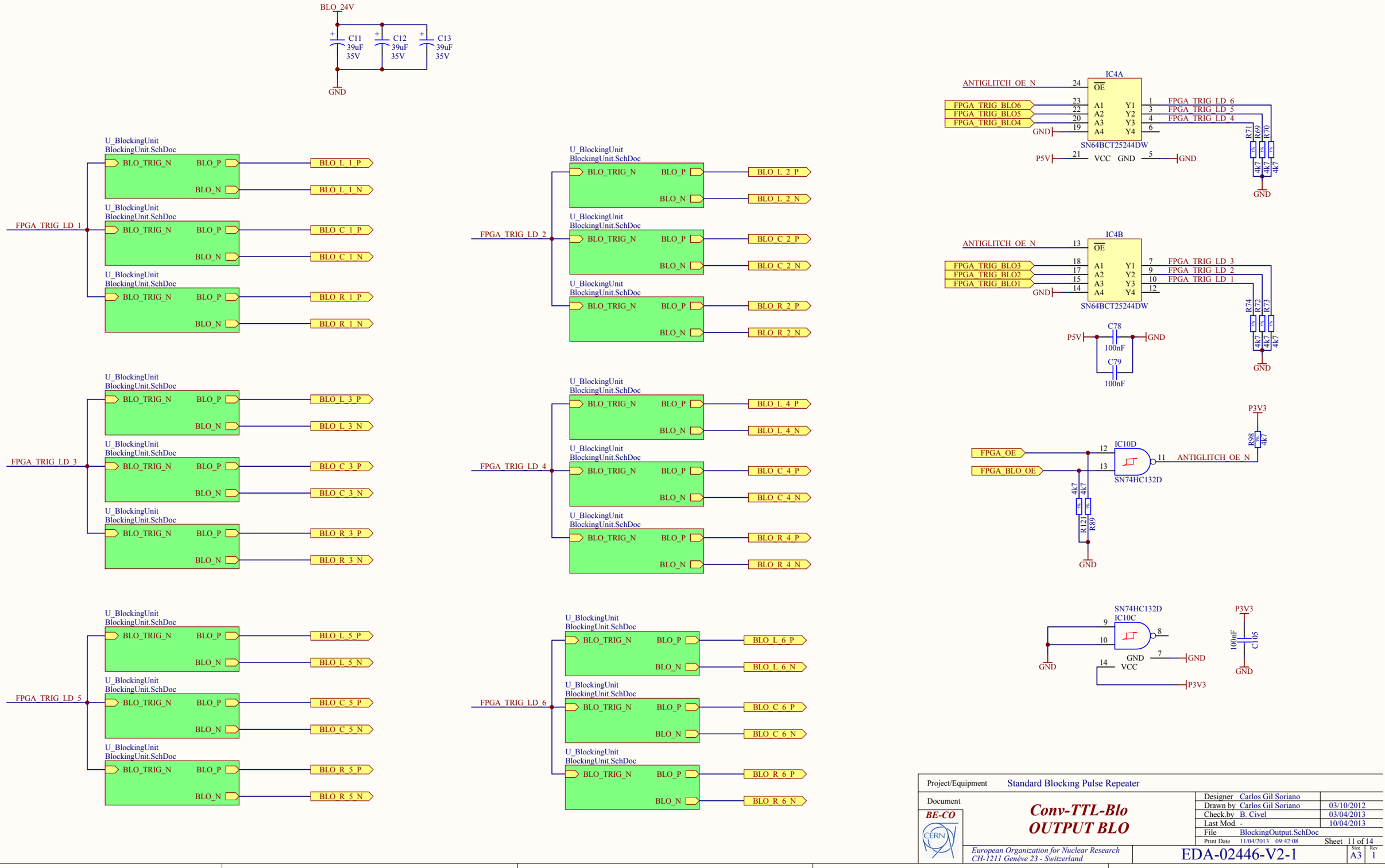
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-1	Size A3	Rev 1

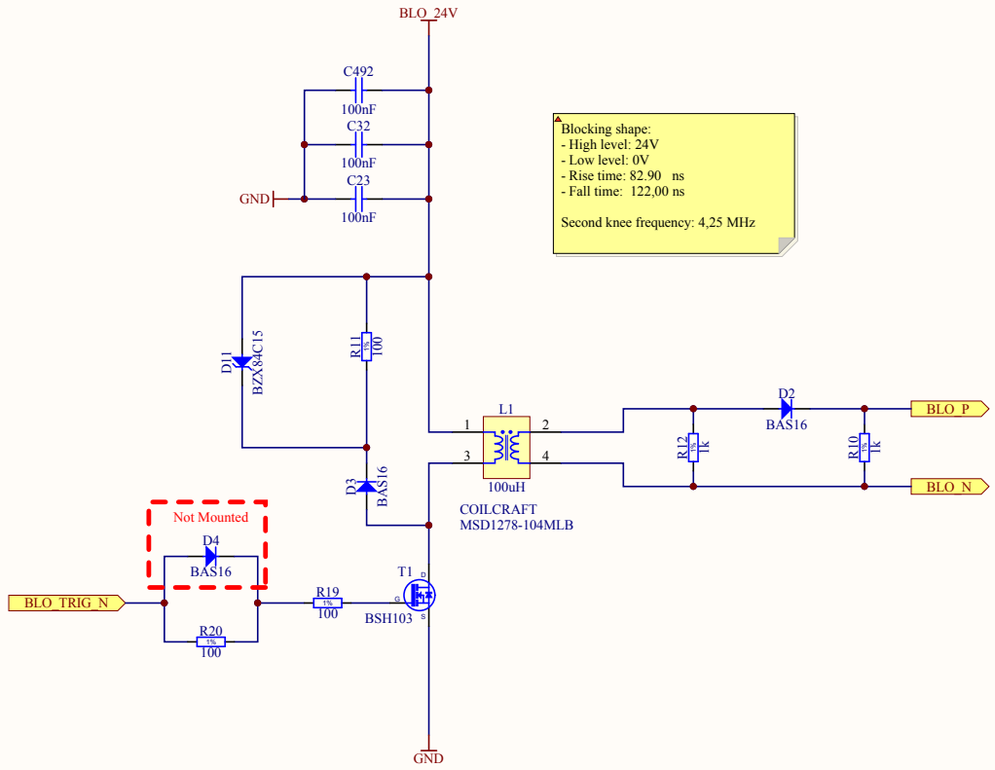
Input waveforms:
nominal 24V Std.Blocking
minimum 5V Std.Blocking



Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo INPUT UNIT	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check.by B. Civel	03/04/2013
		Last Mod. -	10/04/2013
		File InputBlockingUnit.SchDoc	
		Print Date 11/04/2013 09:42:08	Sheet 10 of 14
BE-CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-1	Size A3 / Rev 1



Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo OUTPUT BLO
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check.by	B. Civel 03/04/2013
Last Mod.	- 10/04/2013
File	BlockingOutput.SchDoc
Print Date	11/04/2013 09:42:08 Sheet 11 of 14
BE-CO	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland
EDA-02446-V2-1	Size A3, Rev 1



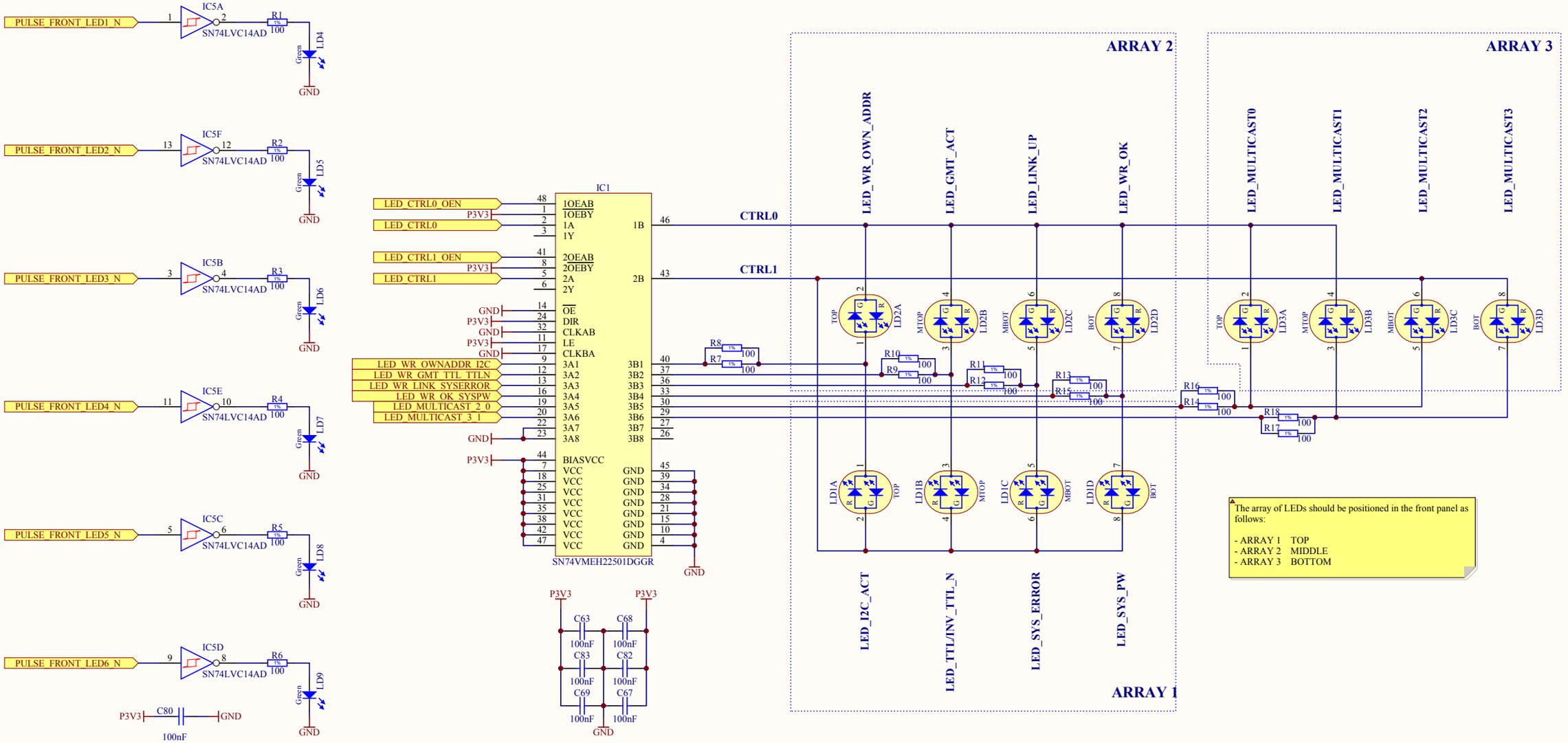
Project/Equipment	Standard Blocking Pulse Repeater		
Document	*Conv-TTL-Blo OUTPUT UNIT*	Designer	Carlos Gil Soriano
		Drawn by	Carlos Gil Soriano 03/10/2012
		Check.by	B. Civel 03/04/2013
		Last Mod.	- 10/04/2013
		File	BlockingUnit.SchDoc
		Print Date	11/04/2013 09:42:09 Sheet 12 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-1	Size	A3
		Rev	1

Input voltage up to 5.5V
TTL intended

Low pass filter

Gain 1
Knee frequency 16MHz

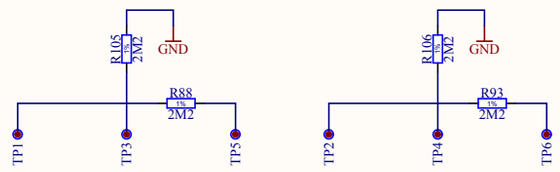
Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo FRONT TTL**	Designer	Carlos Gil Soriano
		Drawn by	Carlos Gil Soriano 03/10/2012
		Check.by	B. Civel 03/04/2013
		Last Mod.	- 10/04/2013
		File	FrontTTL.SchDoc
		Print Date	11/04/2013 09:42:09 Sheet 13 of 14
BE-CO	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	EDA-02446-V2-1	Size A3 Rev 1



The array of LEDs should be positioned in the front panel as follows:

- ARRAY 1 TOP
- ARRAY 2 MIDDLE
- ARRAY 3 BOTTOM

ESD discharge strips (top and bottom of the card)



FTG1 FTG4
FTG3 FTG6
FTG2 FTG5

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo FRONT PANEL**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check.by B. Civel	03/04/2013
		Last Mod. -	10/04/2013
		File FrontPanelLeds.SchDoc	
		Print Date 11/04/2013 09:42:09	Sheet 14 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-1	Size A3	Rev 1