CONV-TTL-BLO Hardware Guide

July 4, 2013

Theodor-Adrian Stana (CERN/BE-CO-HT)

Revision history

Date	Version	Change
date	0.1	First draft

Contents

1 Introduction **1**

2 Front module **2**
2.1 Power supplies 2
2.2 Clock circuits 3
2.3 FPGA 4
2.4 TTL pulse repetition 4
2.4.1 Input stage 4
2.4.2 Output stage 5
2.5 Blocking pulse repetition 5
2.5.1 Input stage 6
2.5.2 Output stage 6
2.6 SFP connector 6
2.7 Thermometer and flash chip 6

3 Rear-Transition Module **6**
3.1 RTM Motherboard 6
3.2 RTM Piggyback 6

Appendices **7**

A Blocking input stage calculations **7**
A.1 Minimum blocking pulse level 7
A.2 Maximum blocking pulse width calculation 8

List of Figures

1 TTL to blocking pulse conversion system 1
2 Block diagram of CONV-TTL-BLO board 2
3 TTL pulse input stage 5
4 Blocking input stage 7

List of Tables

1 Voltage levels on CONV-TTL-BLO 3
2 Clocks on CONV-TTL-BLO 3

List of Abbreviations

RTM	Rear-Transition Module
IC	Integrated Circuit
PLL	Phase-Locked Loop
SFP	Small-Form-factor Pluggable (transceiver)

1 Introduction

This document presents the hardware of the TTL to blocking converter system (Figure 1). A full pulse conversion system consists of three distinct boards:

- CONV-TTL-BLO – active front module, containing the circuits necessary to achieve all functionality of the system
- CONV-TTL-RTM – passive rear-transition module (RTM) motherboard, providing the connections from the CONV-TTL-BLO VME P2 connector to the rear panel
- CONV-TTL-RTM-BLO – piggyback board on the RTM, providing the LEMO connectors pulse LEDs, and the screws to fix the rear panel

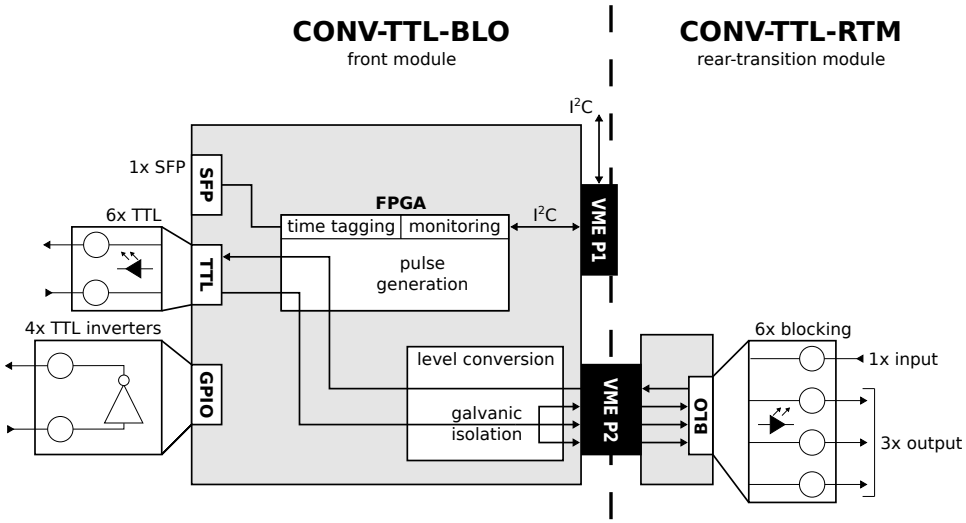

Figure 1: TTL to blocking pulse conversion system

The CONV-TTL-BLO can be used standalone without any RTM, if no blocking pulse replication is needed. This board contains all active circuitry needed to implement the functionalty of the system, from blocking pulse detection and generation, to communication over I^2C and time-tagging via White Rabbit [1].

An RTM system usually consists of both motherboard and piggyback and provide the connections to input blocking pulses to the CONV-TTL-BLO.

board pics

Additional documentation

!!!

- CONV-TTL-BLO User Guide [2]

2 Front module

A block diagram of the CONV-TTL-BLO board is shown in Figure 2. The board contains all active circuitry needed within a converter system. The various blocks in Figure 2 are presented in subsections that follow.

The schematics of the CONV-TTL-BLO board can be found at [3].

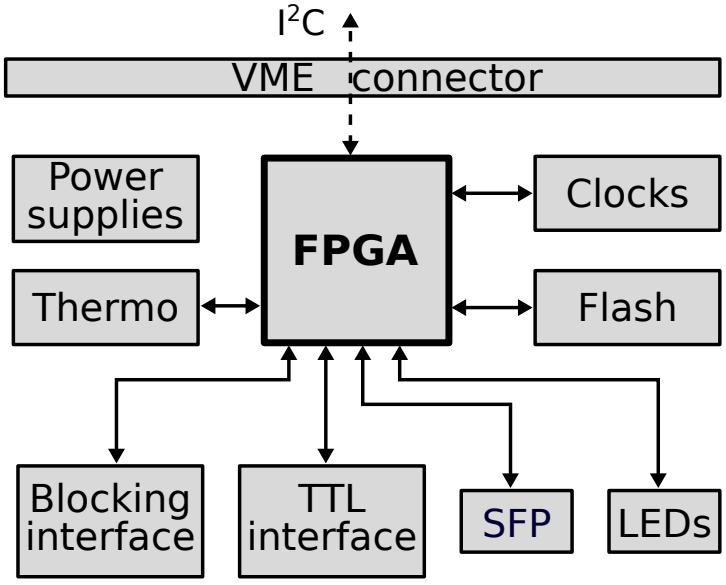

Figure 2: Block diagram of CONV-TTL-BLO board

2.1 Power supplies

Schematics: pages 2, 3

Various power levels are needed on the CONV-TTL-BLO board. They are listed in Table 1. All power supplies on the board are derived in some way from the 3.3 V, 5 V and 12 V VME power supplies.

First, the 5 V and 3.3 V VME supplies arriving on the VME connectors are filtered using two PI filters (schematic page 2). These filters assure noise immunity in the 50 MHz to 150 MHz band. The filtered power supplies are used throughout the logic.

Table 1: Voltage levels on CONV-TTL-BLO

Level	Description
1.2 V	Low-voltage power supply for the FPGA logic
3.3 V	V_{CC} for most of the devices on the board
5 V	Power supply for some circuits on-board (blocking input optocouplers, blocking output buffers, etc.)
24 V	Blocking-level power supply

Table 2: Clocks on CONV-TTL-BLO

Clock	Frequency	Description
CLK20_VCXO	$20MHz$	FPGA clock (from VCXO)
FPGA_CLK	$125MHz$	FPGA clock (from PLL IC)
SFP_CLK	$125MHz$	Dedicated SFP clock
FPGA_MGT_CLK	$125MHz$	Dedicated clock for FPGA transceiver

The 1.2 V logic power supply is generated by a Texas Instruments TPS54312PWP Buck converter. This circuit can be found in page 2 of the schematics.

Finally, the 24 V blocking power supply (schematics page 3) uses a Texas Instruments TPS40210DGQR. It was calculated using the first design example in the device's datasheet [4].

2.2 Clock circuits

Schematics: page 5

There are multiple clock signals on the CONV-TTL-BLO (Table 2). A 20 MHz clock for the FPGA is generated directly from a tunable VCXO (OSC3). The second FPGA clock is a 125 MHz signal generated from a 25 MHz VCXO by means of a Texas Instruments CDCM61004RHBT PLL IC. Two of the other PLL's output channels are used to output dedicated 125 MHz dedicated clocks to the SFP and FPGA transceiver.

Both VCXOs can be tuned by means of two Analog Devices AD5662BRMZ-1 DACs (IC17 and IC18). The DACs can be controlled via a 3-wire SPI interface from the FPGA.

The 3.3 V power supply used by ICs on the clock generation part is a cleaner version of the board-wide 3.3 V supply. The cleaning is done by a four-pole LC filter.

2.3 FPGA

Schematics: page 4

A Xilinx XC6SLX45T Spartan-6 FPGA is present on the CONV-TTL-BLO board. It is the core part of the blocking conversion system, since it is the device controlling all the components on the board.

The intended functionality of the FPGA is:

- generating output pulses as response to input pulse
- pulse logging
- clock conditioning
- remote reprogramming
- controlling the various panel LEDs to inform the user either of pulse arrival, or the status of the system.

For more details on the FPGA firmware and functionality, refer to the CONV-TTL-BLO HDL Guide **REFER**.

2.4 TTL pulse repetition

Schematics: page 13

TTL and TTL-BAR pulses may arrive on front panels of CONV-TTL-BLO boards. The two signal types are described in Sections 4.1 and 4.2 of [2]. Signals arriving on an input channel go through an input stage consisting of Schmitt trigger circuits; they are then input to the FPGA, where the pulse gets regenerated and passed to the output stage.

2.4.1 Input stage

The input stage on a TTL pulse channel is shown in Figure 3. Pulses go through a Texas Instruments SN74LVC14AD Schmitt trigger inverter which smooths the edges of the input signal and helps isolate the FPGA from the channel input. The inverter is 5 V tolerant at the input, so TTL signals may be up to 5 V high. Anything above 5.6 V opens the BAS66 diode to the 5 V and protects the Schmitt trigger.

The input stage is 50 Ω terminated (the three 150 Ω resistors). Note that when no wire is plugged into the LEMO connector, the termination pulls the line low which becomes a continuous high-level when it comes out of the Schmitt trigger.

This input stage is repeated on each of the six TTL pulse replication channels of the CONV-TTL-BLO, as well as the four inverter channels.

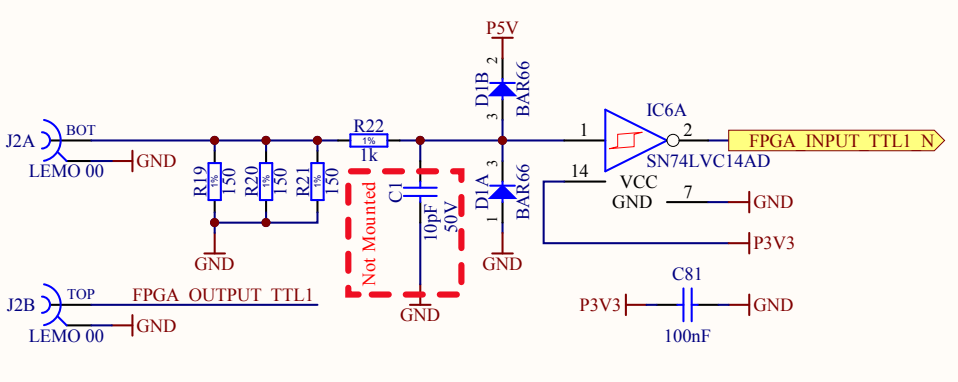

Figure 3: TTL pulse input stage

2.4.2 Output stage

The output stage consists of Texas Instruments SN64BCT25244DW tri-state buffers driven from the FPGA. The purpose of the buffers is two-fold. First, they isolate the FPGA outputs from the actual channel outputs. Second, they assure the line can drive a 50 Ω load.

The buffers' enable signals are controlled by two signals from the FPGA. These signals are NANDed together (IC10 NAND gate) and connected to the output enable active-low signals. When the FPGA does not drive the output enable line, it is pulled high by a pull-up resistor, to safeguard against spurious signals on the output of the channel.

Pull-down resistors at the output of the tri-state buffers assure a continuous low level at the output when the buffers are not enabled.

2.5 Blocking pulse repetition

Schematics: pages 9-12

Blocking pulses arrive through the LEMO connectors on the rear panel. Through the RTM and the P2 connector, they arrive at the blocking input stage on the CONV-TTL-BLO, where an optocoupler is used to isolate the input signal from the logic levels of the FPGA. The input pulse then goes into the FPGA, where the pulse is regenerated in the same manner as TTL pulses. The regenerated pulse signal goes through a flyback converter output stage, where the logic levels of the FPGA are converted back into blocking level.

The blocking input stage can be found on pages 9 and 10 of the schematics; the blocking output stage can be found on pages 11 and 12.

2.5.1 Input stage

Schematics: pages 9, 10

The blocking input stage contains the 50 Ω termination, a transient voltage suppressor diode to protect against high-voltage spikes, a high-pass RC filter which prevents DC signals from passing to the Avago optocoupler. Finally, the optocoupler isolates the blocking-level stage from the logic stage on the FPGA side. Since the optocoupler is powered from 5 V, a Schmitt trigger (not shown in Figure 4) adapts the 5 V level to the 3.3 V level needed by the FPGA.

The minimum pulse level for this circuit is 3.8 V (see Appendix A.1).

The maximum pulse width that can be safely sustained by the input stage is 2 μs (see Appendix A.2).

2.5.2 Output stage

Schematics: pages 11, 12

details about output circuit
galvanic isolation
max outp. PW calculation
danger in case of no firmware

2.6 SFP connector

Schematics: page 6

The small form-factor pluggable (SFP) connector on the CONV-TTL-BLO front panel can be used to input an optic fiber cable that may be used for pulse tagging using White Rabbit.

2.7 Thermometer and flash chip

Schematics: page 7

3 Rear-Transition Module

3.1 RTM Motherboard

3.2 RTM Piggyback

Appendices

A Blocking input stage calculations

Figure 4 shows the blocking input stage, as a reference for the calculations below.

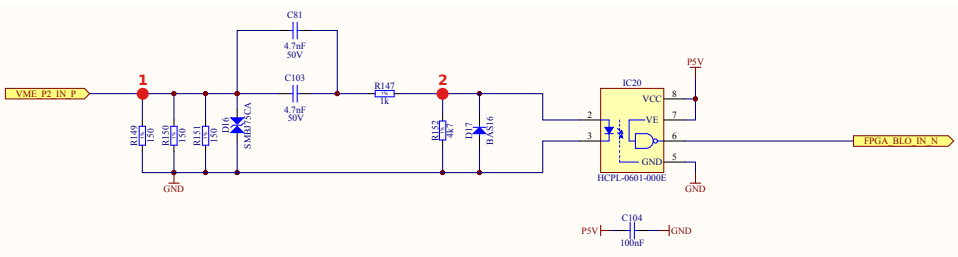

Figure 4: Blocking input stage

A.1 Minimum blocking pulse level

The optocoupler LED has a forward voltage of 1.5 V and therefore when the LED is on, the voltage in point 2 of Figure 4 is

$$V_2 = 1.5V \tag{1}$$

This means that for the LED to turn on, only

$$V_2 = \frac{R_{152}}{R_{152} + R_{147}} V_1 \tag{2}$$

$$V_1 = \frac{R_{152} + R_{147}}{R_{152}} V_2 \tag{3}$$

$$V_1 = \frac{5k7}{4k7} \times 1.5 = 1.82V \tag{4}$$

are needed at the blocking input. However, the LED needs to reach a certain intensity level before it triggers the output of the optocoupler. This translates into a threshold current for the LED, which is given in the optocoupler datasheet to have a typical value of

$$I_{TH} = 2mA \tag{5}$$

Inputting this into the circuit calculation above, and knowing that when the LED is on a 0.31 mA current passes through R_{152} (1.5 V / 4k7Ω), this yields a current of 2.31 mA passing through R_{147} (I_{LED}+$I_{R_{152}}$). This results in a minimum pulse level of

$$V_1 - V_2 = 2.31mA \times 1k\Omega \tag{6}$$

$$V_{1,min} = 3.8V \tag{7}$$

This value has been verified in practice to be the minimum input pulse level for which a pulse is generated at the output.

A.2 Maximum blocking pulse width calculation

Considering $24V$ pulses at the blocking input (point 1 in Figure 4) and the fact that the forward voltage of the LED when conducting is $1.5V$ ($V_2 = 1.5V$), this yields a $22.5mA$ current going through R_{147}

$$I_{R_{147}} = \frac{24 - 1.5}{1k} = 22.5mA \tag{8}$$

Since this current is divided among R_{152} and the optocoupler LED and the current through R_{152} is

$$I_{R_{152}} = \frac{V_2}{R_{152}} = \frac{1.5}{4k7} = 0.31mA \tag{9}$$

the current through the LED is

$$I_{LED} = I_{R_{147}} - I_{R_{152}} \cong 22.2mA \tag{10}$$

Now, by selecting a recommended input RMS current of $15mA$ from the optocoupler's datasheet, and knowing that the RMS current for the pulse wave is

$$I_{LED,RMS} = I_{LED}\sqrt{\delta} \tag{11}$$

this gives a maximum duty cycle of

$$\delta \cong 0.46 \tag{12}$$

With the $1.2\mu s$ pulse width at the output and the minimum $4.8\mu s$ pulse period, this gives a maximum pulse width at the input of

$$t_{p,max} = 2.2\mu s \tag{13}$$

References

[1] "White Rabbit." http://www.ohwr.org/projects/white-rabbit.

[2] T.-A. Stana, "CONV-TTL-BLO User Guide." http://www.ohwr.org/documents/263, 06 2013.

[3] "CONV-TTL-BLO Schematics." https://edms.cern.ch/file/1278535/1/EDA-02446-V2-1_sch.pdf.

[4] Texas Instruments, "TPS40210, TPS40211, 4.5 V to 52 V Input Current Mode Boost Controller." http://www.ohwr.org/documents/227.