U_CITY_FMC
CITY_FMC.SchDoc

U_CITY_Soc_top
CITY_Soc_top.SchDoc

FMC1_LA_P[33..0]
FMC1_LA_N[33..0]
FMC1_CLK0M2C_P
FMC1_CLK0M2C_N
FMC1_CLK0C2M_P
FMC1_CLK0C2M_N
FMC1_GBTCLK0M2C_P
FMC1_GBTCLK0M2C_N
FMC1_DP0M2C_P
FMC1_DP0M2C_N
FMC1_DP0C2M_P
FMC1_DP0C2M_N
FMC1_PRSNTM2C_N
FMC1_VREFAM2C
FMC1_SCL
FMC1_SDA
FMC1_TCK
FMC1_TDI
FMC1_TMS
FMC1_TDO
FMCx_PGC2M

FMC connectors

FMC2_LA_P[33..0]
FMC2_LA_N[33..0]
FMC2_CLK0M2C_P
FMC2_CLK0M2C_N
FMC2_CLK0C2M_P
FMC2_CLK0C2M_N
FMC2_DP0M2C_P
FMC2_DP0M2C_N
FMC2_DP0C2M_P
FMC2_DP0C2M_N
FMC2_PRSNTM2C_N
FMC2_VREFAM2C
FMC2_SCL
FMC2_SDA
FMC2_TCK
FMC2_TDI
FMC2_TMS
FMC2_TDO

Zynq SoC

PS_POR_N
SFP_RX2_P
SFP_RX2_N
SFP_TX2_P
SFP_TX2_N
WRC_LED_LINK
WRC_LED_ACT
WRC_SFP_MOD_DEF0
WRC_SFP_MOD_DEF2
WRC_SFP_MOD_DEF1
WRC_SFP_TX_FAULT
WRC_SFP_TX_LOS
I2C_PMBus_d_hv
I2C_PMBus_clk_hv
PMBus_alert_N
WRC_SDA
WRC_SCL
WRC_PPS_P
WRC_PPS_N
DIN_P[1..4]
DIN_N[1..4]
DOUTB_P[1..6]
DOUTB_N[1..6]
DOUTA_P[1..6]
DOUTA_N[1..6]
RF_FPGA_P
RF_FPGA_N
CLK_SYNTH_P
CLK_SYNTH_N
DAC_DAT
ADC_SCK
ADC_SDI
ADC_SDO
ADC_CNV
PD_CLK
PD_DAT
PD_LE
PD_LockDetect
RF_PLL_STATUS
SPI_SS0
SPI_SCLK
SPI_MOSI
SPI_MISO
SPI_SS1

U_CITY_SFP
CITY_SFP.SchDoc

SFP_RX2_P
SFP_RX2_N
SFP_TX2_P
SFP_TX2_N
WRC_LED_LINK
WRC_LED_ACT
WRC_SFP_MOD_DEF0
WRC_SFP_MOD_DEF2
WRC_SFP_MOD_DEF1
WRC_SFP_TXFAULT
WRC_SFP_LOS

SFP

U_CITY_misc
CITY_misc.SchDoc

I2C_PMBus_d_hv
I2C_PMBus_clk_hv
PMBus_alert_N
USR_CLK_SEL0
USR_CLK_SEL1
PPS
BIAS[1..4]
IN_TERM_EN[1..4]
AD2[1..6]
AD1[1..6]
AD0[1..6]
FDEL_TUNE[1..6]

Misc.

GND
J4
LEMO 00

U_CITY_DDS_top
CITY_DDS_top.SchDoc

SOC_SDA
SOC_SCL
RF_FPGA_P
RF_FPGA_N
CLK_SYNTH_P
CLK_SYNTH_N
DAC_DAT
ADC_SCK
ADC_SDI
ADC_SDO
ADC_CNV
PD_CLK
PD_DATA
PD_LE
PD_LockDetect
RF_PLL_STATUS
RF_PLL_CS
PLL_SCLK
PLL_SDI
PLL_SDO

RFoWR - DDS

RF_SYNC_P[1..6]
RF_SYNC_N[1..6]
RF_OUT
DAC_CLK_P
DAC_CLK_N
RF_OUT1_P
RF_OUT1_N
DAC_OUT_P
DAC_OUT_N
RF_IN

J17
GND
SMA
J21
GND
SMA

U_CITY_user_clock
CITY_user_clock.SchDoc

RF_OUT_P
RF_OUT_N
RFDAC_OUT_P
RFDAC_OUT_N
WR_USR_CLK_P
WR_USR_CLK_N
SEL0
SEL1
CLK_OUT

User Clk

USR_CLK_SEL0
USR_CLK_SEL1
C430
100nF
J24
SMA
GND

U_CITY_WR_clocking
CITY_WR_clocking.SchDoc

CLK_REF_125MHZ_FPGA_P
CLK_REF_125MHZ_FPGA_N
CLK_REF_125MHZ_GTX_P
CLK_REF_125MHZ_GTX_N
CLK_VCXO_20MHZ
WR_DAC_SCLK
WR_DAC_DIN
WR_DAC_CS1
WR_DAC_CS2
WR_PLL_RESET_N
WR_PLL_STATUS
WR_PLL_CS
PLL_SCLK
PLL_SDI
PLL_SDO
DAC_CLK_P
DAC_CLK_N
WR_CLK_USER_P
WR_CLK_USER_N
WR_REF_10MHZ

WR clocking

J2
BNC
GND

FPGA_CLK_P
FPGA_CLK_N
FPGA_MGTREFCLK1_P
FPGA_MGTREFCLK1_N
CLK20_VCXO
WRC_PLLDAC_SCLK
WRC_PLLDAC_DIN
WRC_PLL25DAC_CS_N
WRC_PLL20DAC_CS_N
WR_PLL_RESET_N
WR_PLL_STATUS

U_CITY_power-controller
CITY_power-controller.SchDoc

I2C_PMBus_d_hv
I2C_PMBus_clk_hv
VCCINT_I_MON
P3V3_I_MON
PMBus_alert_N
P1V8_VCCAUXIO_PG
P1V8_VCCPAUX_PG
P1V2_PG
P1V0_MGTAVCC_PG
SEQ2_GO
SEQ3_GO
SEQ4_GO
SEQ5_GO
SEQ6_GO

Power Controller

U_CITY_power-supplies-3
CITY_power-supplies-3.SchDoc

PS_POR_N
FMCx_PG
SEQ_EXTPS_PG
P1V8_I_MON
P2V5_I_MON
SEQ_P1V8_EN
SEQ_P2V5_EN

Supplies (3)

U_CITY_power-supplies
CITY_power-supplies.SchDoc

SEQ_P3V3_EN
SEQ_VTT_DDR_EN
SEQ_EXTPS_PG
VCCINT_I_MON
P3V3_I_MON
P3V3_PG
P1V0_PG

Supplies (1)

U_CITY_power-supplies-2
CITY_power-supplies-2.SchDoc

P1V8_VCCAUXIO_PG
P1V8_VCCPAUX_PG
P1V2_PG
P1V0_MGTAVCC_PG
SEQ2_GO
SEQ3_GO
SEQ4_GO
SEQ5_GO
SEQ6_GO
SEQ_4_EN
SEQ_6_EN
SEQ_EXTPS_PG

Supplies (2)

REPEAT(DI,1,4)
CITY_DI_1channel.SchDoc

BIAS2
IN_TERM_EN4
DIN_P1
DIN_N4
Repeat(BIAS)
Repeat(IN_TERM_EN)
Repeat(OUT_P)
Repeat(OUT_N)
Repeat(IN)
IN1

DI

IN1 BOT J6A
IN2 TOP J6B
IN3 BOT J9A
IN4 TOP J9B
LEMO 00
GND

REPEAT(DO,1,6)
CITY_DO_2channels.SchDoc

FDEL_TUNE5
SOC_SDA
SOC_SCL
DOUTB_P1
DOUTB_N5
DOUTA_P2
DOUTA_N3
RF_SYNC_P2
RF_SYNC_N4
Repeat(FDEL_TUNE)
Repeat(IN1_P)
Repeat(IN1_N)
Repeat(IN0_P)
Repeat(IN0_N)
Repeat(RF_SYNC_P)
Repeat(RF_SYNC_N)
Repeat(I2C_AD0)
Repeat(I2C_AD1)
Repeat(I2C_AD2)
Repeat(OUT0)
Repeat(OUT1)

DO

AD26
AD13
AD06
OUT06
OUT16

OUT01 BOT J11A
OUT02 BOT J15A
OUT03 BOT J16A
OUT04 BOT J18A
OUT05 BOT J20A
OUT06 BOT J22A
LEMO 00
GND

J11B TOP OUT11
J15B TOP OUT12
J16B TOP OUT13
J18B TOP OUT14
J20B TOP OUT15
J22B TOP OUT16
LEMO 00
GND

Based on FASEC design
EDA-03288-V3

FTG1 FTG4
FTG2 FTG5
FTG3 FTG6

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Project: CITY
Sheet: Top Level
File: CITY_top.SchDoc

Rev.	Date	Author
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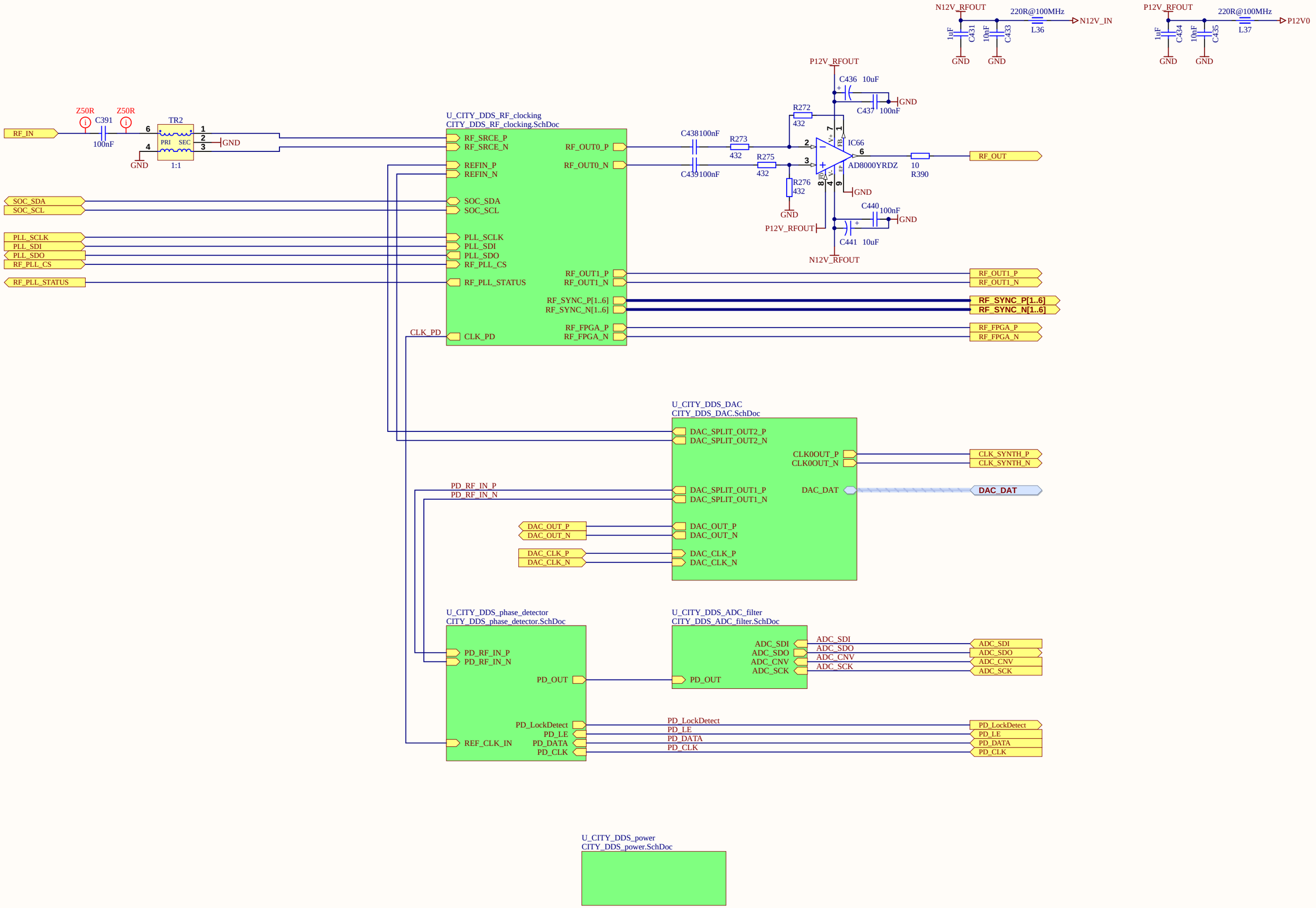
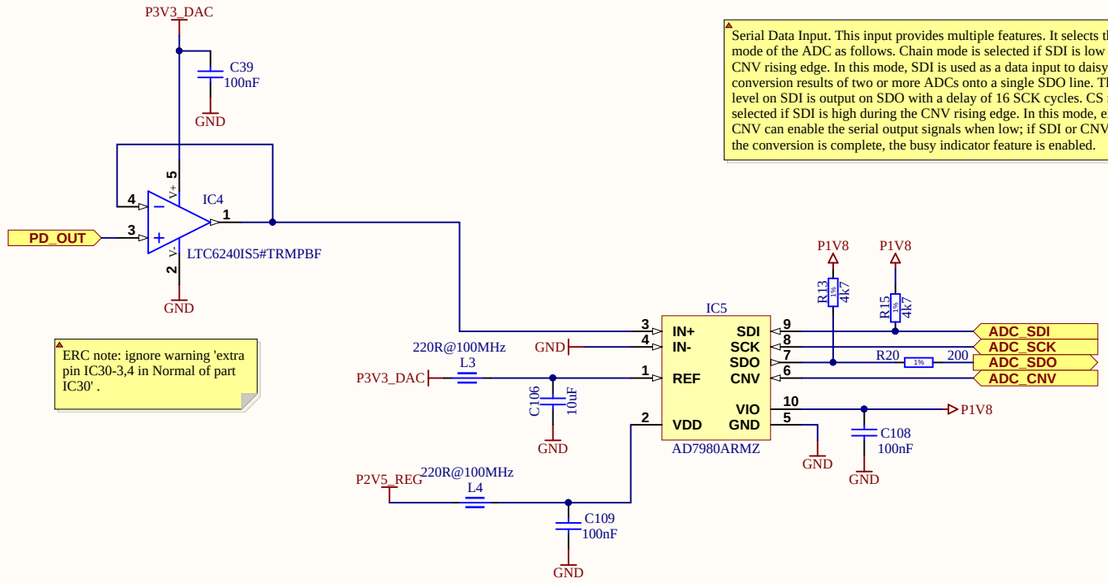
SVN: 89f9589d8aaca0a25e422de51e6



ESRF The European Synchrotron	Doc. Num.:	Ver.: A	Sheet: 2 of 36
	Project: CITY		
	Sheet: DDS Top	Rev.	Date / Author
	File: CITY_DDS_top.SchDoc	0	05/2019 broquet
		SVN: 89f9589d8aaca0a25e422de51e6	



Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows. Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. CS mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low; if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.

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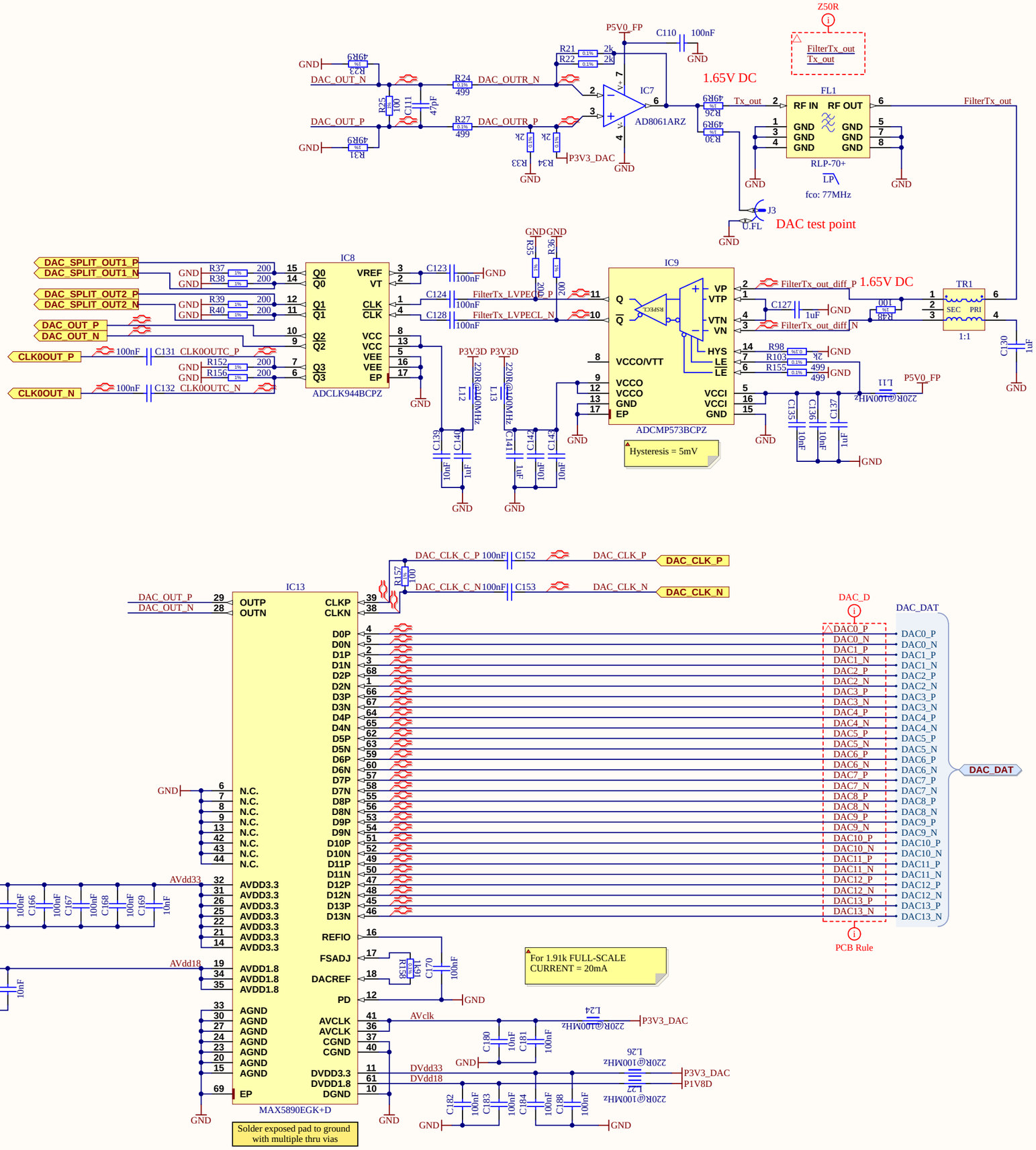
Project: CITY			
Sheet: DDS ADC	Rev.	Date	Author
	0	05/2019	broquet
File: CITY_DDS_ADC_filter.SchDoc	SVN: b29a393685549acd64523545bec		

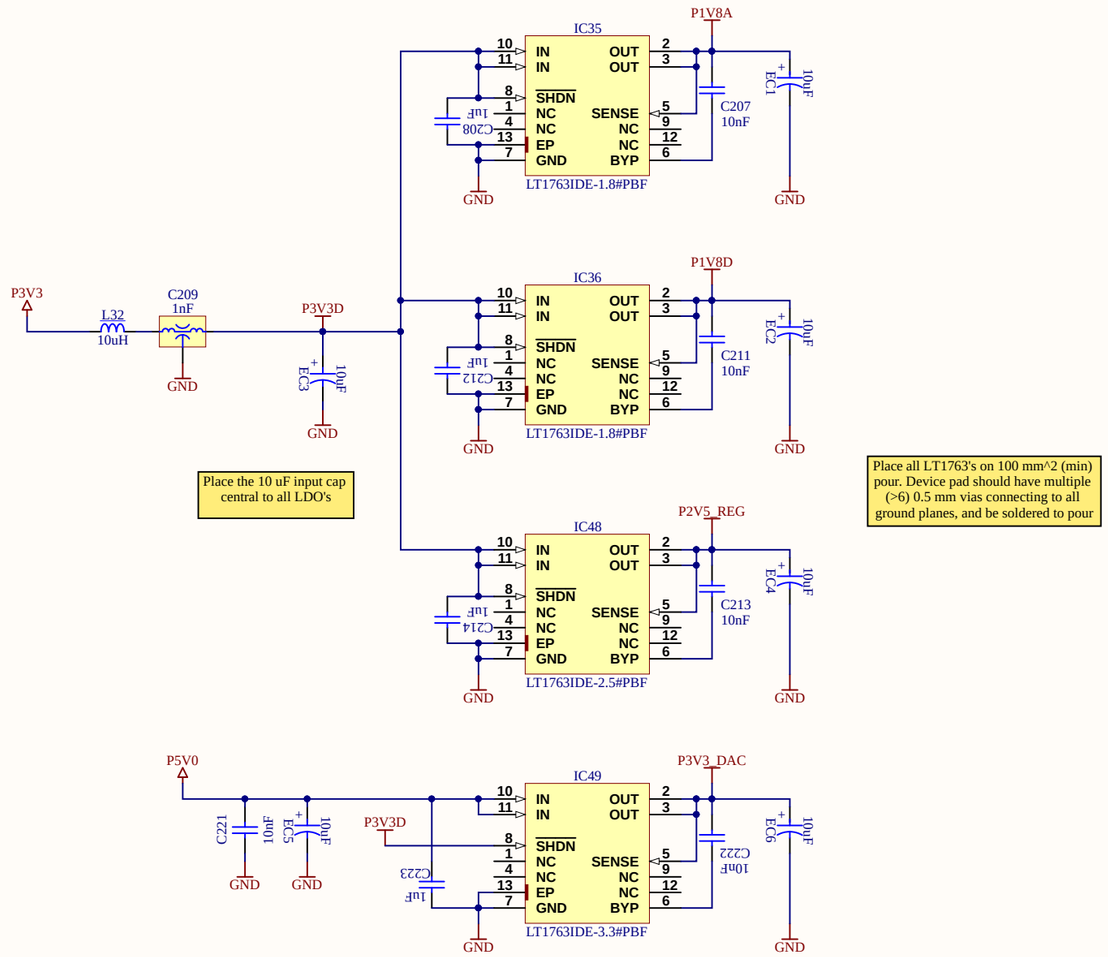


Doc. Num.:	Ver.: A	Sheet: 4 of 36	
Project: CITY			
Sheet: DDS DAC & Filter	Rev. 0	Date 05/2019	Author broquet
File: CITY_DDS_DAC.SchDoc	SVN: 89f9589d8aaca0a25e422de51e6		

ESRF The European Synchrotron	Doc. Num.:	Ver.: A	Sheet: 5 of 36
	Project: CITY		
	Sheet: DDS Phase Detector		
	File: CITY_DDS_phase_detector.SchDoc		

Rev.	Date	Author
0	05/2019	broquet

SVN: 89f9589d8aaca0a25e422de51e6



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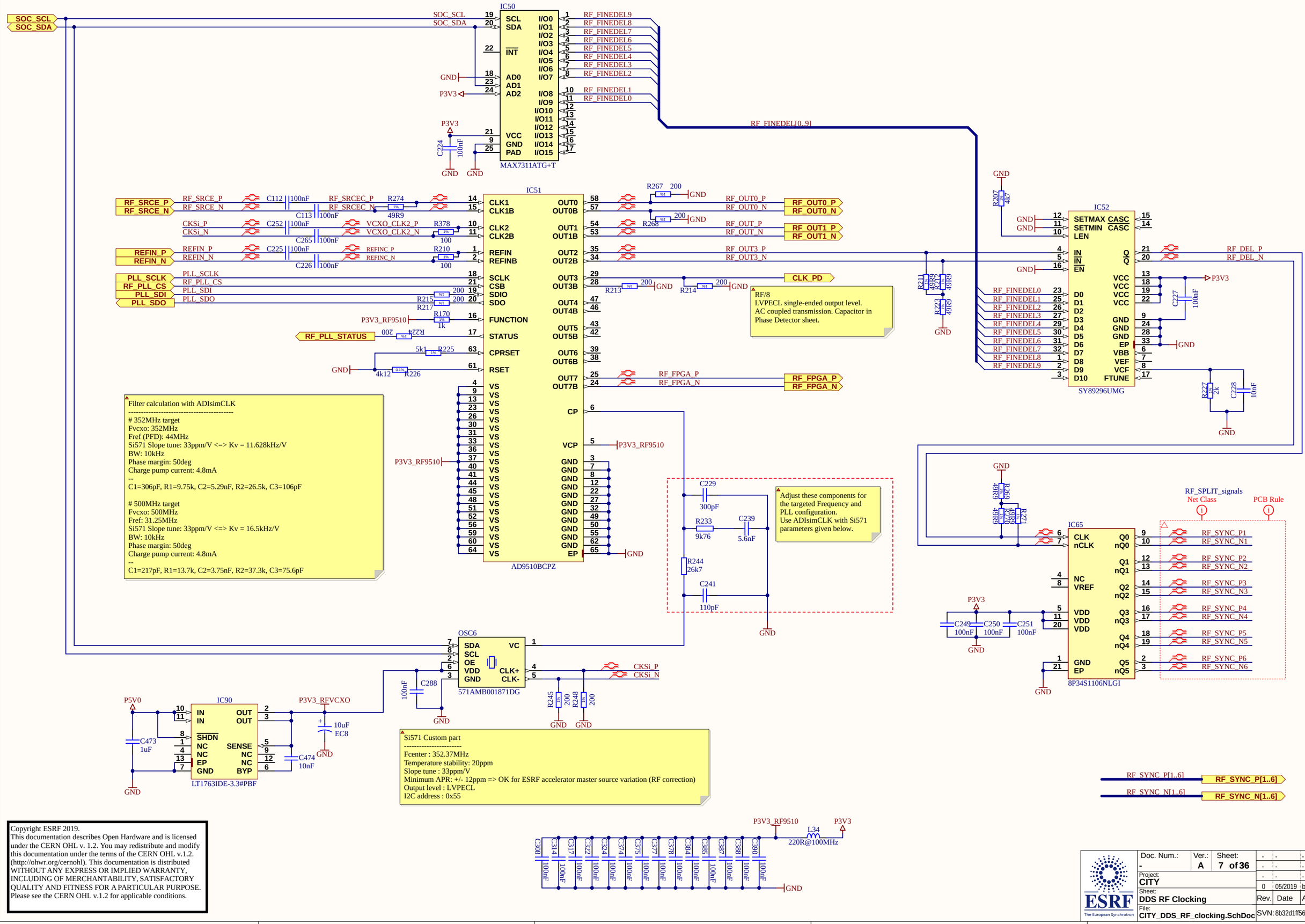
Project: CITY

Sheet: DDS Power Supply Regulators

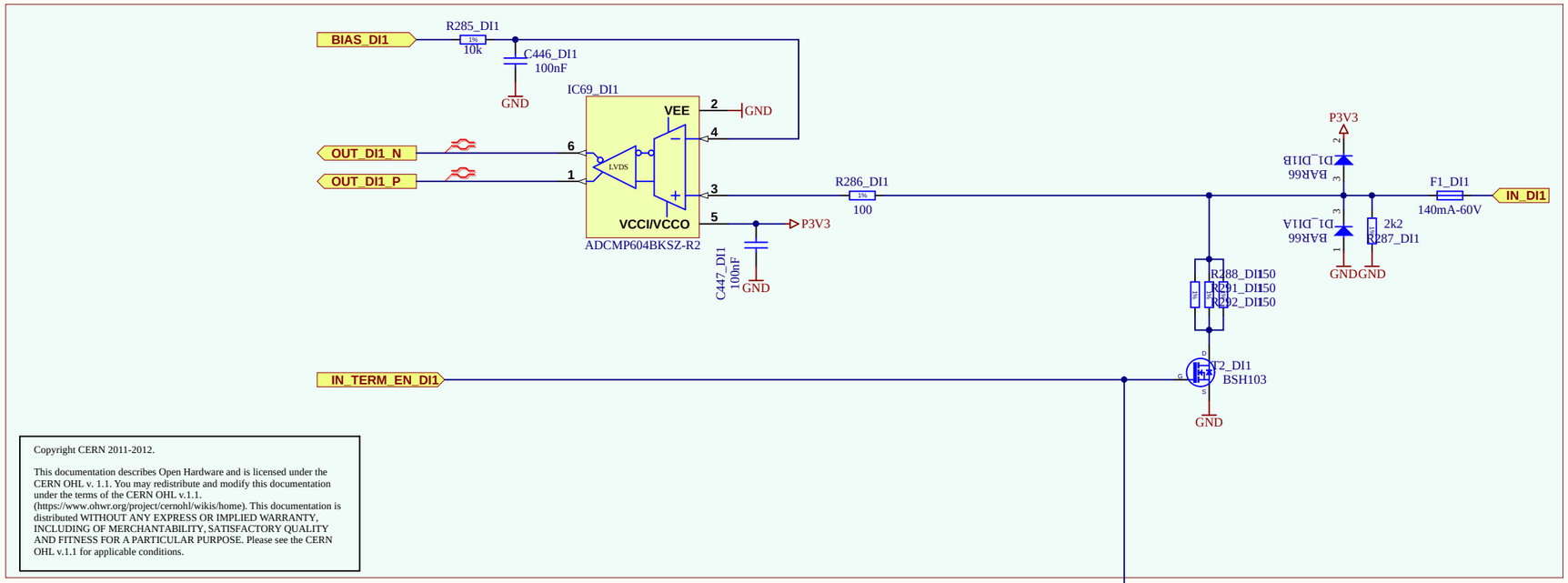
File: CITY_DDS_power.SchDoc

Rev.	Date	Author
0	05/2019	broquet

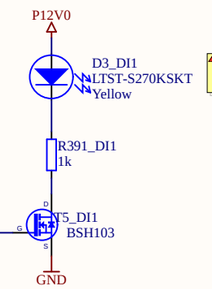
SVN: 89f9589d8aaca0a25e422de51e6



ESRF The European Synchrotron	Doc. Num.: -	Ver.: A	Sheet: 7 of 36
	Project: CITY		
	Sheet: DDS RF Clocking	Rev. 0	Date 05/2019 Author broquet
	File: CITY_DDS_RF_clocking.SchDoc	SVN: 8b32d1ff56bec64e17ac727dd233	



Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0



Place LED under LEMO connector.

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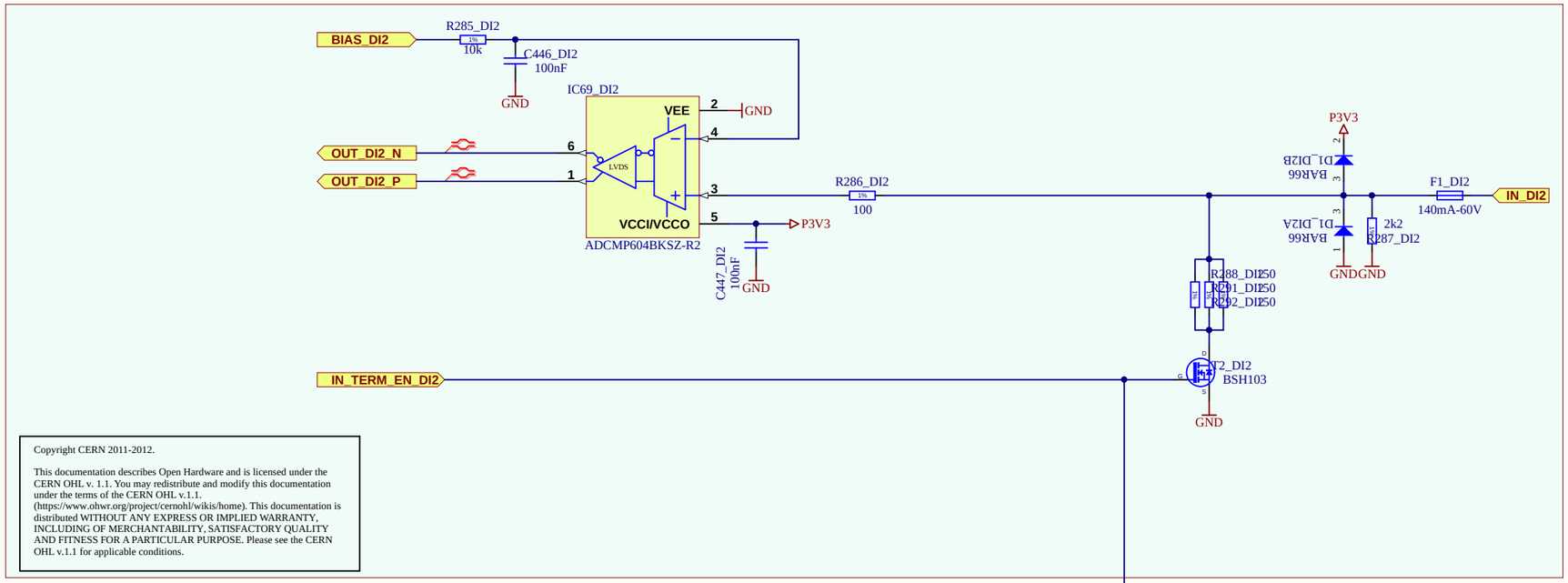
	Project: CITY		
	Sheet: DI 2 channels	Rev. 0	Date 05/2019 Author broquet
	File: CITY_DI_1channel.SchDoc	SVN: ebd898e7ae22b92c77af7210a03	



Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

Place LED under LEMO connector.

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	Project: CITY		
	Sheet: DI 2 channels	Rev. 0	Date 05/2019
	File: CITY_DI_1channel.SchDoc		Author broquet
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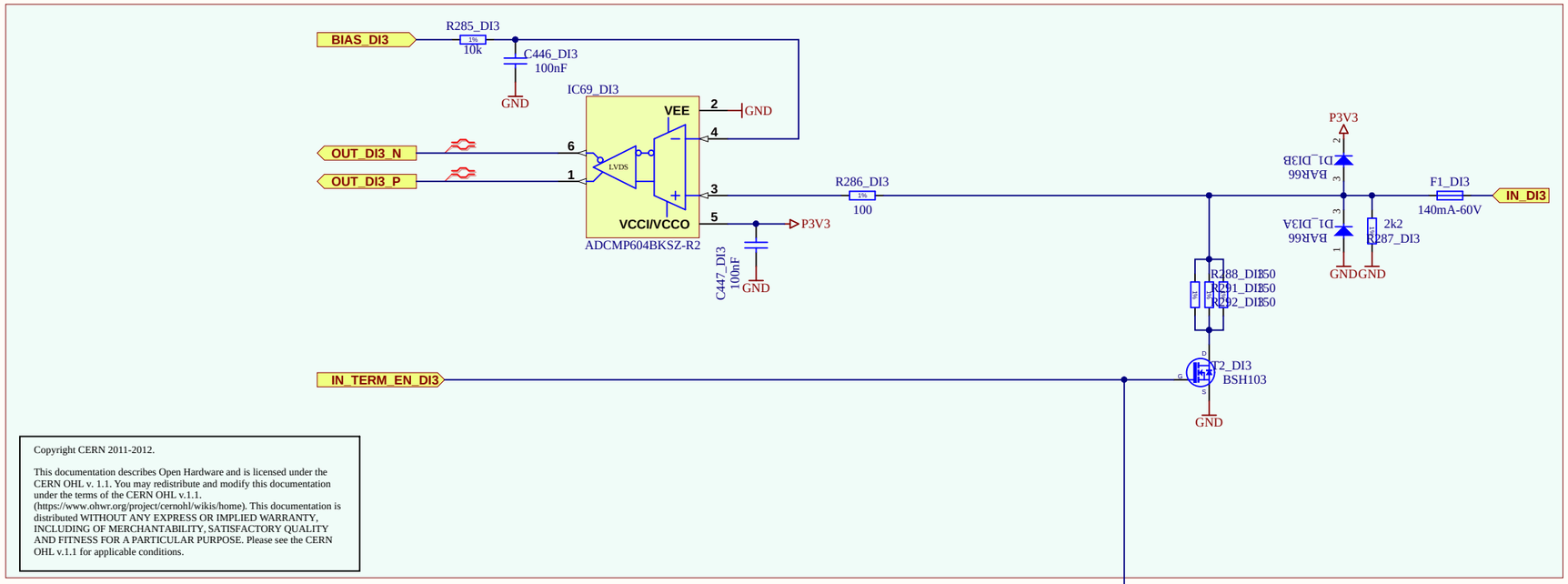

Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

ESRF The European Synchrotron	Doc. Num.:	Ver.: A	Sheet: 8.3 of 36	
	Project: CITY			
	Sheet: DI 2 channels	Rev.	Date	Author
	File: CITY_DI_1channel.SchDoc	0	05/2019	broquet
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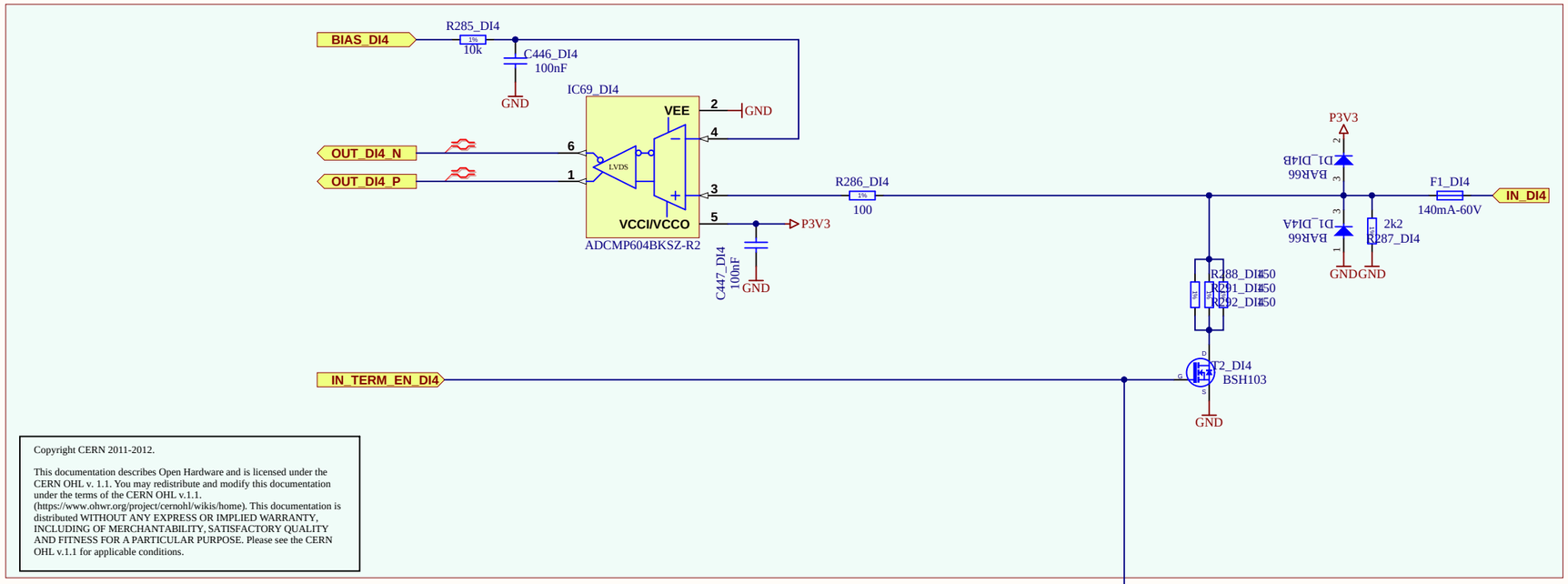

Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

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	Project: CITY			
	Sheet: DI 2 channels	Rev.	Date	Author
	File: CITY_DI_1channel.SchDoc	0	05/2019	broquet
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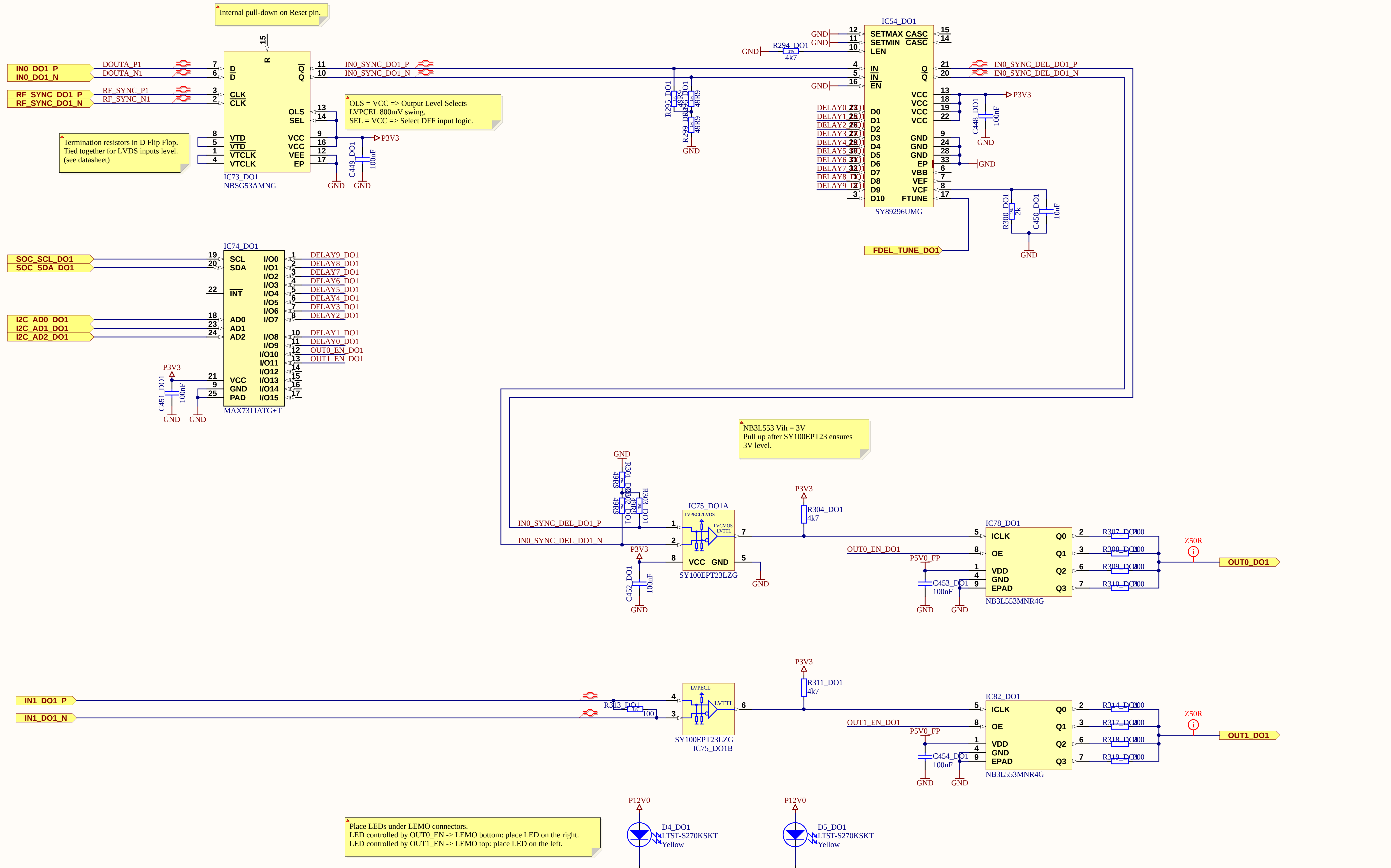

Internal pull-down on Reset pin.
IN0_DO1_P
IN0_DO1_N
RF_SYNC_DO1_P
RF_SYNC_DO1_N
DOUTA_P1
DOUTA_N1
RF_SYNC_P1
RF_SYNC_N1
Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)
IC73_DO1
NBSG53AMNG
OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.
IN0_SYNC_DO1_P
IN0_SYNC_DO1_N
C449_DO1
100nF
P3V3
GND
R294_DO1
4k7
R295_DO1
R299_DO1
49R9
IC54_DO1
SETMAX
SETMIN
LEN
CASC
IN
EN
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10
VCC
GND
EP
VBB
VEF
VCF
FTUNE
SY89296UMG
IN0_SYNC_DEL_DO1_P
IN0_SYNC_DEL_DO1_N
C448_DO1
100nF
R300_DO1
2k
C450_DO1
10nF
FDEL_TUNE_DO1
SOC_SCL_DO1
SOC_SDA_DO1
I2C_AD0_DO1
I2C_AD1_DO1
I2C_AD2_DO1
IC74_DO1
SCL
SDA
INT
AD0
AD1
AD2
PAD
MAX7311ATG+T
DELAY9_DO1
DELAY8_DO1
DELAY7_DO1
DELAY6_DO1
DELAY5_DO1
DELAY4_DO1
DELAY3_DO1
DELAY2_DO1
DELAY1_DO1
DELAY0_DO1
OUT0_EN_DO1
OUT1_EN_DO1
C451_DO1
100nF
NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.
R301_DO1
R302_DO1
R303_DO1
IC75_DO1A
LVPECL/LVDS
LVCMOS LVTTL
SY100EPT23LZG
C452_DO1
100nF
R304_DO1
4k7
IC78_DO1
ICLK
OE
VDD
EPAD
Q0 Q1 Q2 Q3
NB3L553MNR4G
P5V0_FP
C453_DO1
100nF
R307_DO1
R308_DO1
R309_DO1
R310_DO1
200
Z50R
OUT0_DO1
IN1_DO1_P
IN1_DO1_N
R313_DO1
100
LVPECL
LVTTL
SY100EPT23LZG
IC75_DO1B
R311_DO1
4k7
IC82_DO1
C454_DO1
100nF
R314_DO1
R317_DO1
R318_DO1
R319_DO1
OUT1_DO1
Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.
P12V0
D4_DO1
LTST-S270KSKT
Yellow
D5_DO1
R392_DO1
1k
R393_DO1
1k
BSH103
R394_DO1
2k2
R395_DO1
2k2

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Project: CITY

Sheet: DO 2 channels

File: CITY_DO_2channels.SchDoc

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-	-	-
0	05/2019	broquet

SVN: 89f9589d8aaca0a25e422de51e6

Internal pull-down on Reset pin.

IN0_DO2_P
IN0_DO2_N
RF_SYNC_DO2_P
RF_SYNC_DO2_N

DOUTA_P2
DOUTA_N2
RF_SYNC_P2
RF_SYNC_N2

IC73_DO2
NBSG53AMNG
D D CLK CLK VTD VTD VTCLK VTCLK R Q Q OLS SEL VCC VCC VEE EP

IN0_SYNC_DO2_P
IN0_SYNC_DO2_N

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

P3V3
C449_DO2 100nF
GND

IC54_DO2
SY89296UMG
SETMAX SETMIN LEN CASC CASC IN IN EN Q Q VCC VCC VCC GND GND GND EP VBB VEF VCF FTUNE D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10

R294_DO2 4k7
R295_DO2 49R9
R296_DO2 49R9
R299_DO2 49R9

IN0_SYNC_DEL_DO2_P
IN0_SYNC_DEL_DO2_N

C448_DO2 100nF
R300_DO2 2k
C450_DO2 10nF

DELAY0_DO2
DELAY1_DO2
DELAY2_DO2
DELAY3_DO2
DELAY4_DO2
DELAY5_DO2
DELAY6_DO2
DELAY7_DO2
DELAY8_DO2
DELAY9_DO2

FDEL_TUNE_DO2

SOC_SCL_DO2
SOC_SDA_DO2
I2C_AD0_DO2
I2C_AD1_DO2
I2C_AD2_DO2

IC74_DO2
MAX7311ATG+T
SCL SDA INT AD0 AD1 AD2 I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8 I/O9 I/O10 I/O11 I/O12 I/O13 I/O14 I/O15 VCC GND PAD

C451_DO2 100nF

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

IC75_DO2A
SY100EPT23LZG
LVPECL/LVDS LVCMOS LVTTL VCC GND

R304_DO2 4k7
C452_DO2 100nF

IC78_DO2
NB3L553MNR4G
ICLK OE VDD GND EPAD Q0 Q1 Q2 Q3

R307_DO2 200
R308_DO2 200
R309_DO2 200
R310_DO2 200

Z50R
OUT0_DO2
OUT0_EN_DO2
P5V0_FP
C453_DO2 100nF

IN1_DO2_P
IN1_DO2_N
R313_DO2 100

IC75_DO2B
SY100EPT23LZG
LVPECL LVTTL

R311_DO2 4k7

IC82_DO2
NB3L553MNR4G
ICLK OE VDD GND EPAD Q0 Q1 Q2 Q3

R314_DO2 200
R317_DO2 200
R318_DO2 200
R319_DO2 200

OUT1_DO2
OUT1_EN_DO2
C454_DO2 100nF

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

P12V0
D4_DO2 LTST-S270KSKT Yellow
R392_DO2 1k
Q0_DO2 BSH103
R394_DO2 2k2

D5_DO2 LTST-S270KSKT Yellow
R393_DO2 1k
Q2_DO2 BSH103
R395_DO2 2k2

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Project: CITY			
Sheet: DO 2 channels			
File: CITY_DO_2channels.SchDoc			

Rev.	Date	Author
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SVN: 89f9589d8aaca0a25e422de51e6

Internal pull-down on Reset pin.

IC73_DO3
NBSG53AMNG

IN0_DO3_P
IN0_DO3_N
DOUTA_P3
DOUTA_N3
IN0_SYNC_DO3_P
IN0_SYNC_DO3_N

RF_SYNC_DO3_P
RF_SYNC_DO3_N
RF_SYNC_P3
RF_SYNC_N3

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

P3V3
C449_DO3 100nF
GND

IC54_DO3
SY89296UMG

IN0_SYNC_DEL_DO3_P
IN0_SYNC_DEL_DO3_N

R294_DO3 4k7
R295_DO3 49R9
R296_DO3 49R9
R299_DO3 49R9

DELAY0_DO3
DELAY1_DO3
DELAY2_DO3
DELAY3_DO3
DELAY4_DO3
DELAY5_DO3
DELAY6_DO3
DELAY7_DO3
DELAY8_DO3
DELAY9_DO3

C448_DO3 100nF
R300_DO3 2k
C450_DO3 10nF
FDEL_TUNE_DO3

IC74_DO3
MAX7311ATG+T

SOC_SCL_DO3
SOC_SDA_DO3
I2C_AD0_DO3
I2C_AD1_DO3
I2C_AD2_DO3
C451_DO3 100nF

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

R301_DO3 49R9
R303_DO3 49R9

IC75_DO3A
SY100EPT23LZG

R304_DO3 4k7
C452_DO3 100nF

IC78_DO3
NB3L553MNR4G

OUT0_EN_DO3
R307_DO3 200
R308_DO3 200
R309_DO3 200
R310_DO3 200
Z50R
OUT0_DO3
C453_DO3 100nF

IN1_DO3_P
IN1_DO3_N
R313_DO3 100

IC75_DO3B
SY100EPT23LZG

R311_DO3 4k7

IC82_DO3
NB3L553MNR4G

OUT1_EN_DO3
R314_DO3 200
R317_DO3 200
R318_DO3 200
R319_DO3 200
Z50R
OUT1_DO3
C454_DO3 100nF

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

D4_DO3
D5_DO3
LTST-S270KSKT
Yellow
R392_DO3 1k
R393_DO3 1k
Q0_DO3
Q2_DO3
BSH103
R394_DO3 2k2
R395_DO3 2k2

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	Sheet: DO 2 channels		
	File: CITY_DO_2channels.SchDoc		

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0	05/2019	broquet

SVN: 89f9589d8aaca0a25e422de51e6

Internal pull-down on Reset pin.

IC73_DO4
NBSG53AMNG

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

IC54_DO4
SY89296UMG

IC74_DO4
MAX7311ATG+T

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

IC75_DO4A
SY100EPT23LZG

IC75_DO4B
SY100EPT23LZG

IC78_DO4
NB3L553MNR4G

IC82_DO4
NB3L553MNR4G

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

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SVN: 89f9589d8aaca0a25e422de51e6

Internal pull-down on Reset pin.

IC73_DO5
NBSG53AMNG

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

IC54_DO5
SY89296UMG

IC74_DO5
MAX7311ATG+T

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

IC75_DO5A
SY100EPT23LZG

IC78_DO5
NB3L553MNR4G

IC75_DO5B
SY100EPT23LZG

IC82_DO5
NB3L553MNR4G

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

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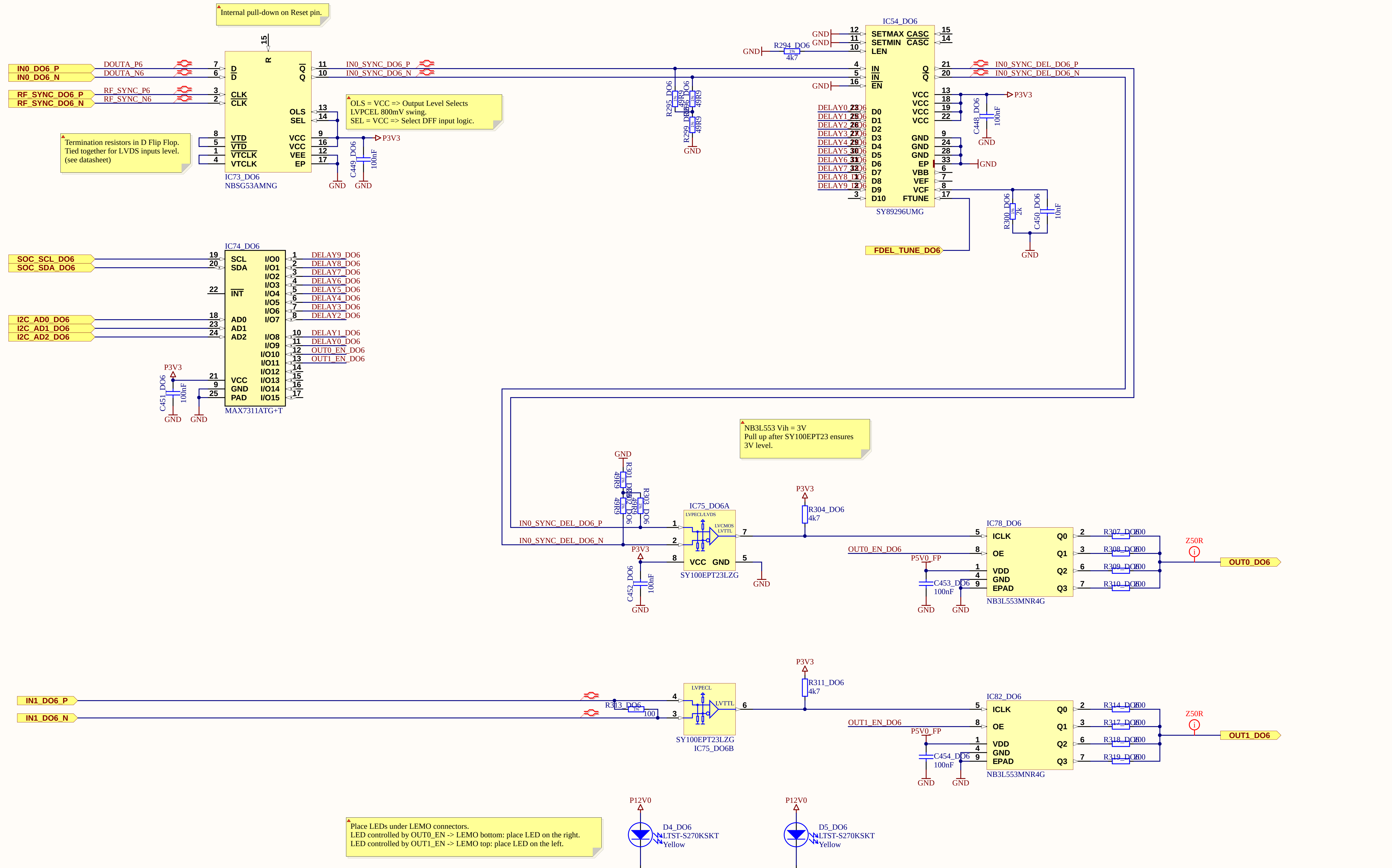
SVN: 89f9589d8aaca0a25e422de51e6



Internal pull-down on Reset pin.

Termination resistors in D Flip Flop. Tied together for LVDS inputs level. (see datasheet)

OLS = VCC => Output Level Selects LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures 3V level.

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

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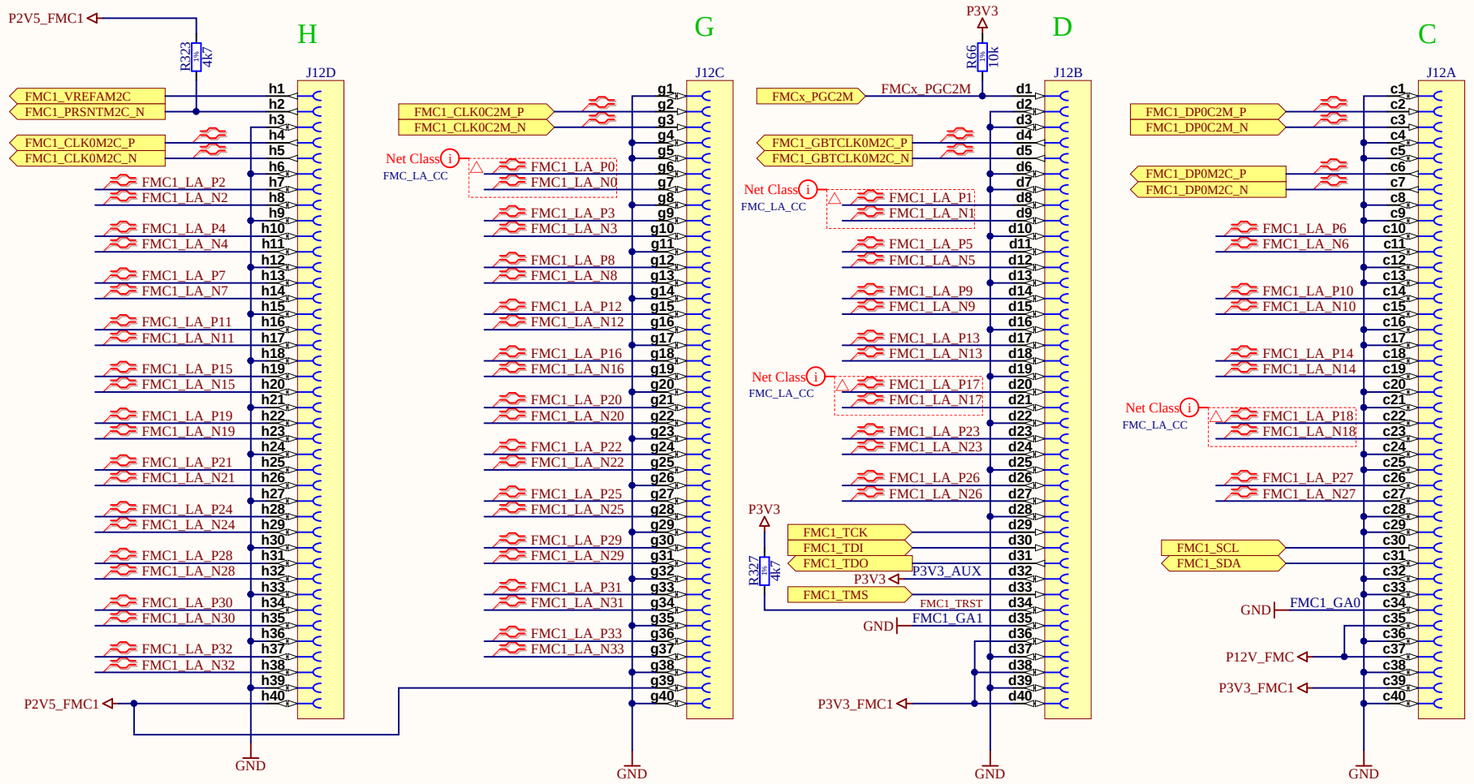
SVN: 89f9589d8aaca0a25e422de51e6



VADJ = 2.5V

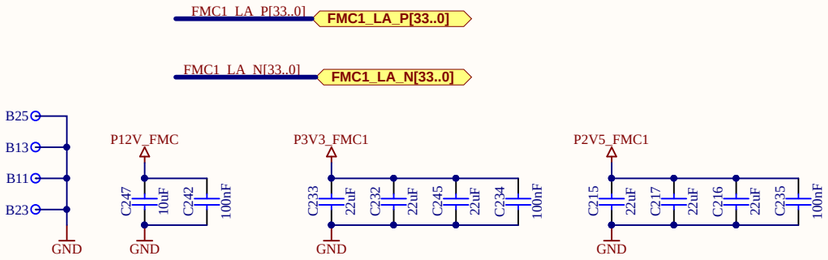
GA = '00'

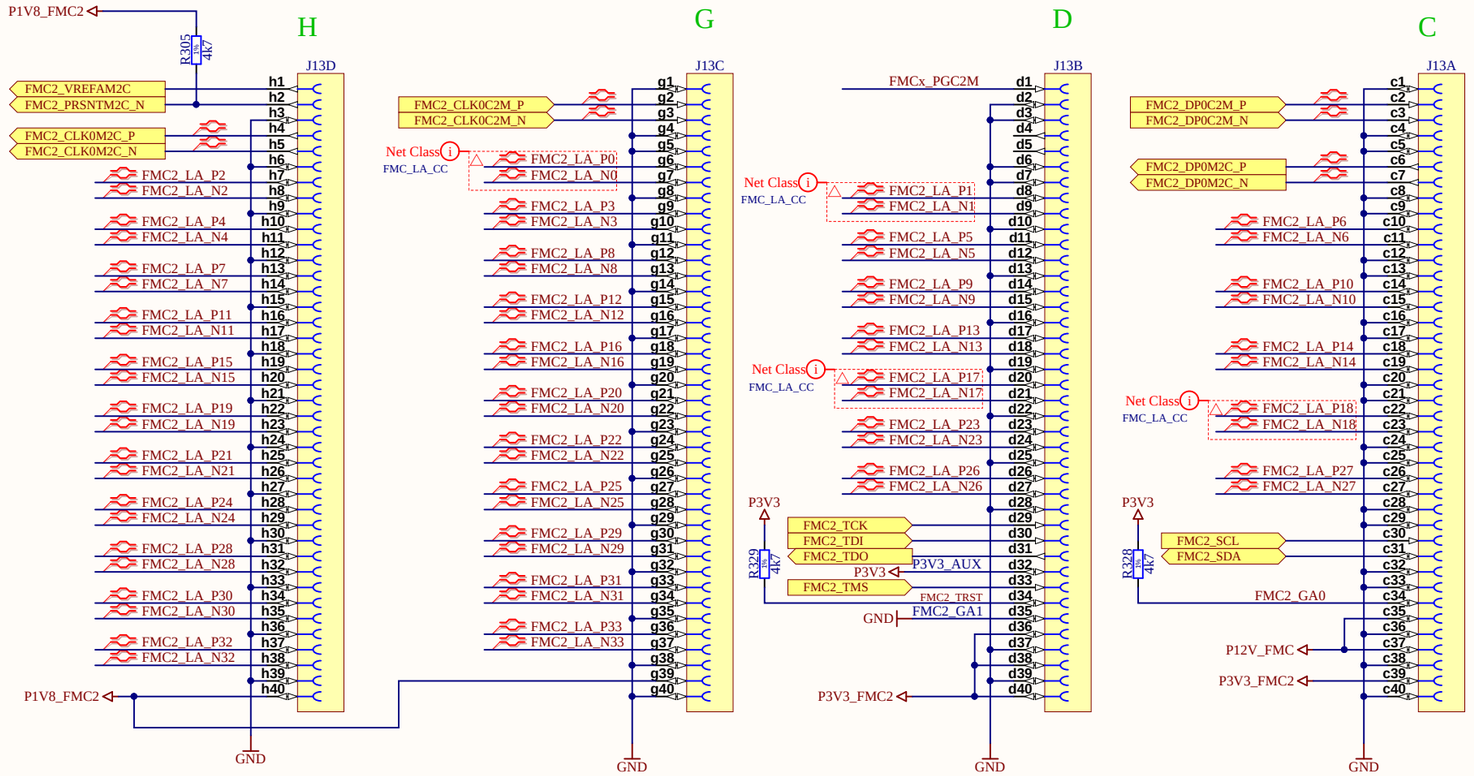
ANSI/VITA 57.1:
For all differential pairs:
Recommendation 5.3: When signals are routed differentially each pair should provide a differential impedance of 100Ω +/- 10%

For FMCx_CLK0M2C and FMCx_CLK0C2M pairs:
Rule 5.22: Clock traces shall provide a differential impedance of 100Ω +/-10%
Rule 5.23: The differential length mismatch on each differential clock pair shall be a maximium 11ps.

For the FMCx_DP0 pairs:
Rule 5.43: The differential length mismatch on each differential data pair shall 1ps.

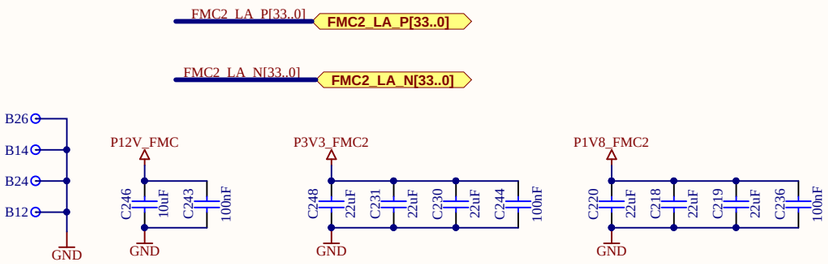
For the FMCx_GBTCLK0M2C pairs:
Rule 5.48: Clock traces shall provide a differential impedance of 100Ω +/-10%
Rule 5.49: The differential length mismatch on each differential clock pair shall 11ps.





VADJ = 1.8V

GA = '01'



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Sheet: FMC Connectors 1 & 2

File: CITY_FMC.SchDoc

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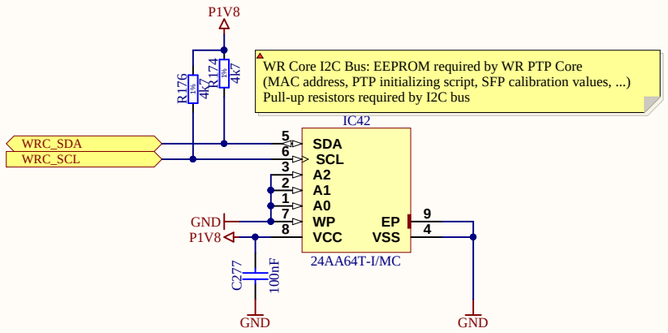
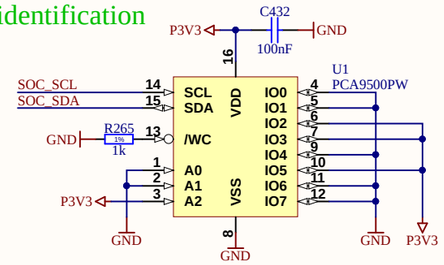
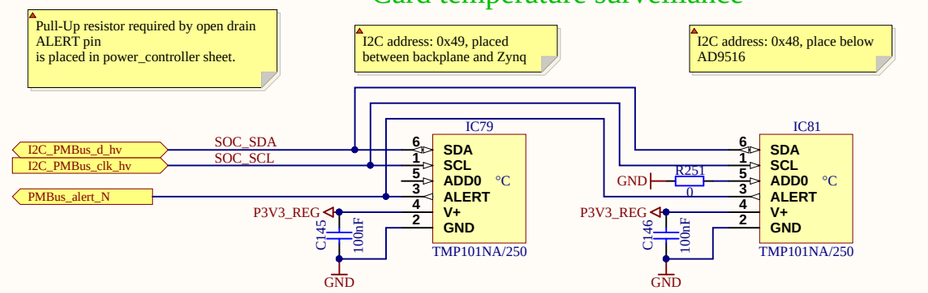
64 Kbit EEPROM (I2C @ 100 kHz max)



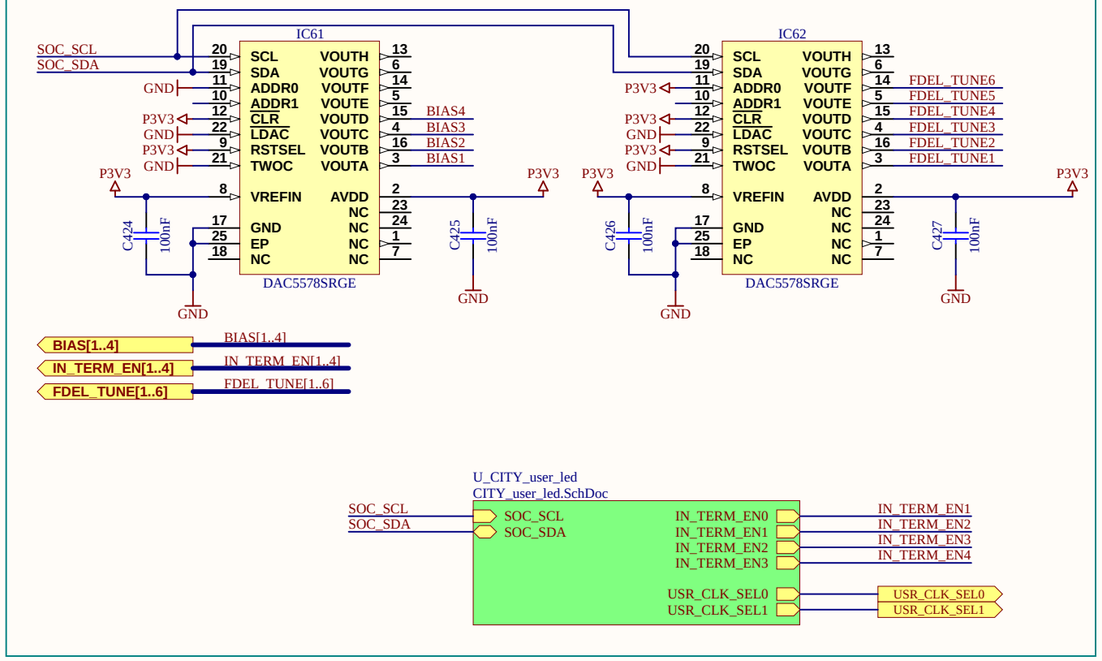
Board identification



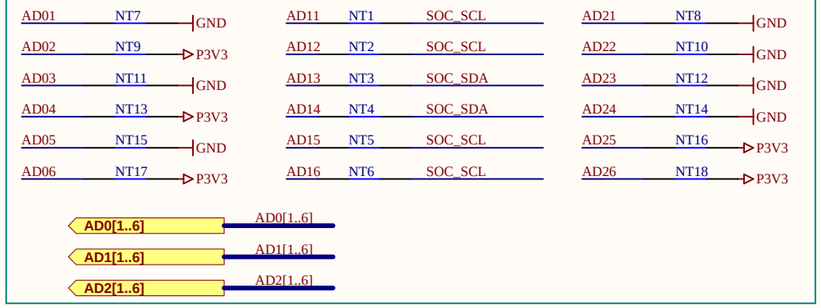
Card temperature surveillance



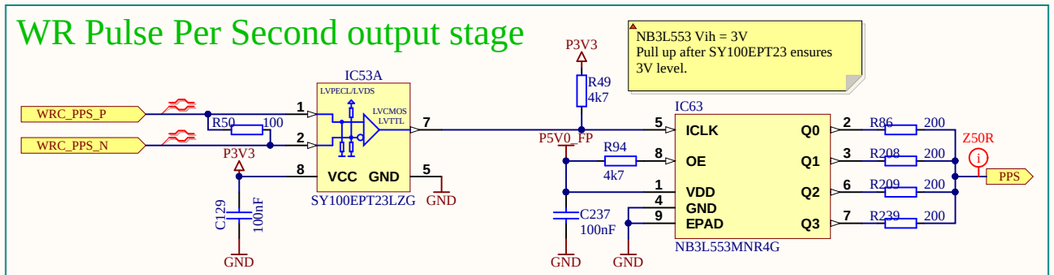
DACs for Inputs BIAS and Fine Delay Tune / User LED + GPIO



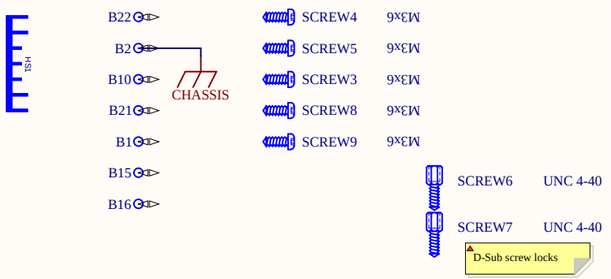
I2C address bus for DO channel IO registers



WR Pulse Per Second output stage



PCB mounting holes, screws & heatsink



changelog

V2-0:
* several small component changes, not documented here
* power supply sequence improved
* bank 501 and all connected chips changed to 1.8V for full RGMII support
* PHY SPI wired to bank 35, in addition to existing MDIO
* UART changed to FT230X
* power controller UCD90120 GPIO rewired cause pull-downs; 2nd connecter added for use of TI adapter

V3-0:
* few small component changes, not documented here
* external patch-panel interrupt line to SoC
* i2c level converter ADUM1250 turned around cause i2c compliance problems
* D-sub 15 wiring change to follow CERN cabling convention
* TMP101 thermal sensors added

CITY V1-0:
* See the CHANGES.TXT document provided in the project

I2C addresses

I2C addresses hex number are given in the 7bit format aligned to LSb (without R/W bit).
Example: I2C addr = 0x74 (1 1 1 0 1 0 0) --> Read access = 1 1 1 0 1 0 0 1 (0xE9)

WR Core I2C:
========
24AA64T -> 0x50

SoC I2C (I2C PMBus):
==========
CITY_power-controller.SchDoc
UCD90120ARGC -> 0x5B

CITY_misc.SchDoc
TMP101(1) -> 0x48 (with ADD0 = 0)
TMP101(2) -> 0x49 (with ADD0 = Float)
DAC5578(1) -> 0x4C (with ADDR0 = GND, ADDR1 = float)
DAC5578(2) -> 0x4D (with ADDR0 = VCC, ADDR1 = float)
BOARD ID I/O -> 0x24 (with A0 = A1 = GND, A2 = VCC)
BOARD ID EEPROM -> 0x54 (with A0 = A1 = GND, A2 = VCC)

CITY_user_led.SchDoc
General IO control -> 0x25 (AD0 = VCC, AD1 = GND, AD2 = VCC)

DO_2channels.SchDoc (I/Os control: Finde delay, Output drivers enable)
0 -> 0x10 (AD0 = GND, AD1 = SCL, AD2 = GND)
1 -> 0x11 (AD0 = VCC, AD1 = SCL, AD2 = GND)
2 -> 0x12 (AD0 = GND, AD1 = SDA, AD2 = GND)
3 -> 0x13 (AD0 = VCC, AD1 = SDA, AD2 = GND)
4 -> 0x14 (AD0 = GND, AD1 = SCL, AD2 = VCC)
5 -> 0x15 (AD0 = VCC, AD1 = SCL, AD2 = VCC)

RF_Clocking.SchDoc
RF clock delay for outputs synchronization -> 0x16 (AD0 = GND, AD1 = SDA, AD2 = VCC)
Si571 -> 0x55 (default, fixed).

ESRF
LOGO PCB

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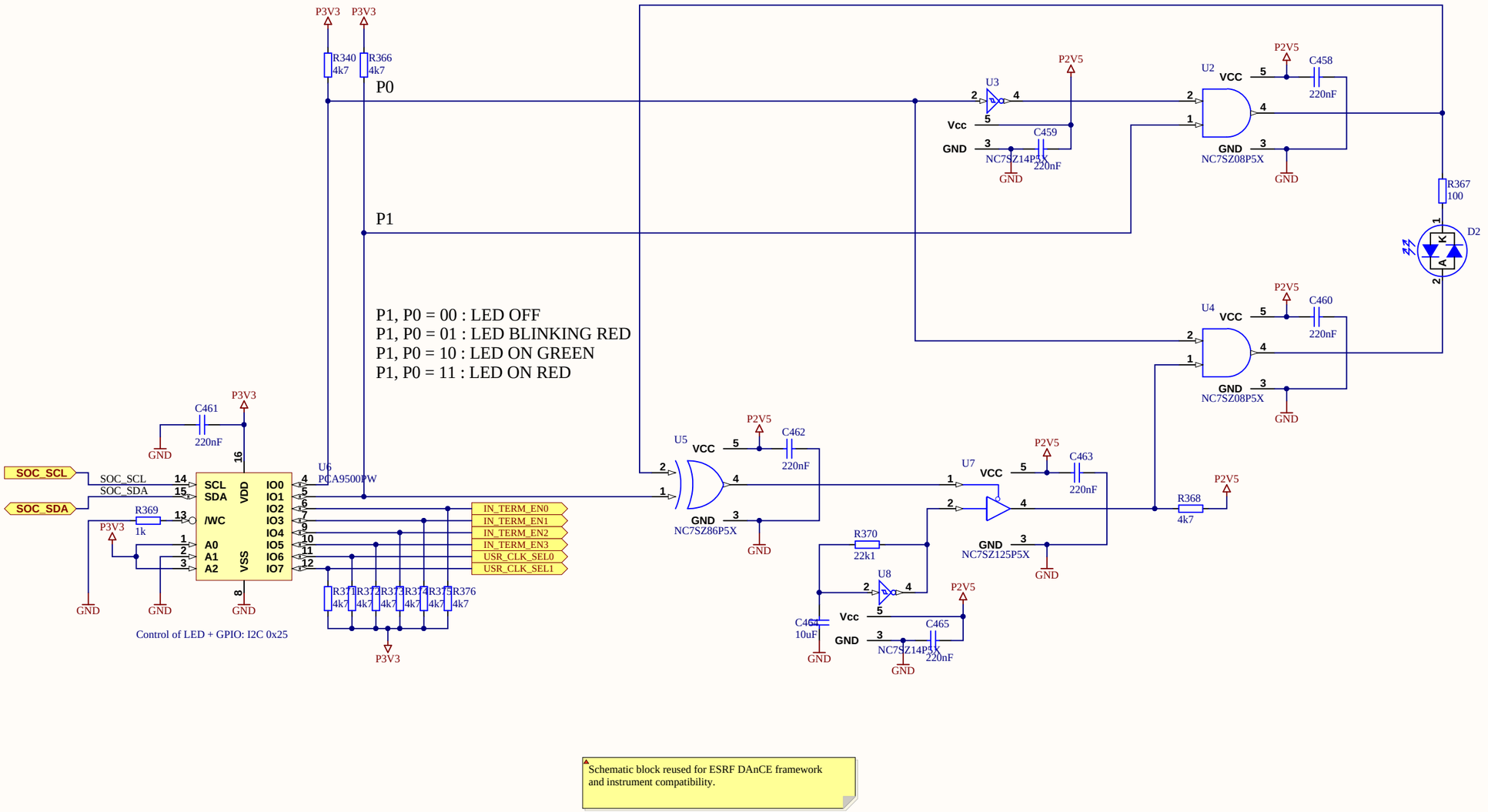
	File: CITY_misc.SchDoc	SVN: 08ea0502fc00b004fc6fb5e91983	



Schematic block reused for ESRF DAnCE framework and instrument compatibility.

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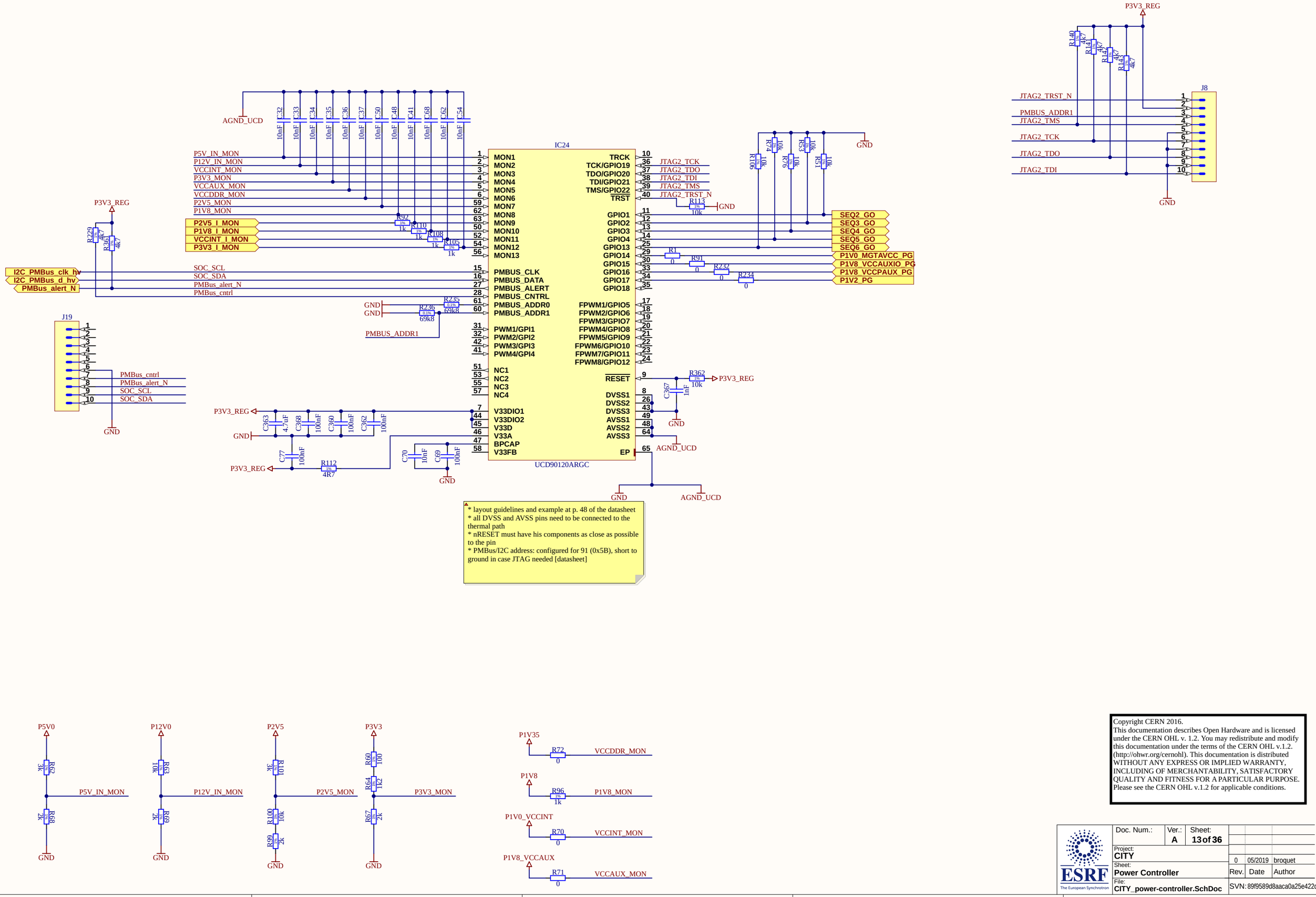
	Sheet: User LED	Rev. 0	Date 05/2019 Author broquet
	File: CITY_user_led.SchDoc	SVN: 89f9589d8aaca0a25e422de51e6	



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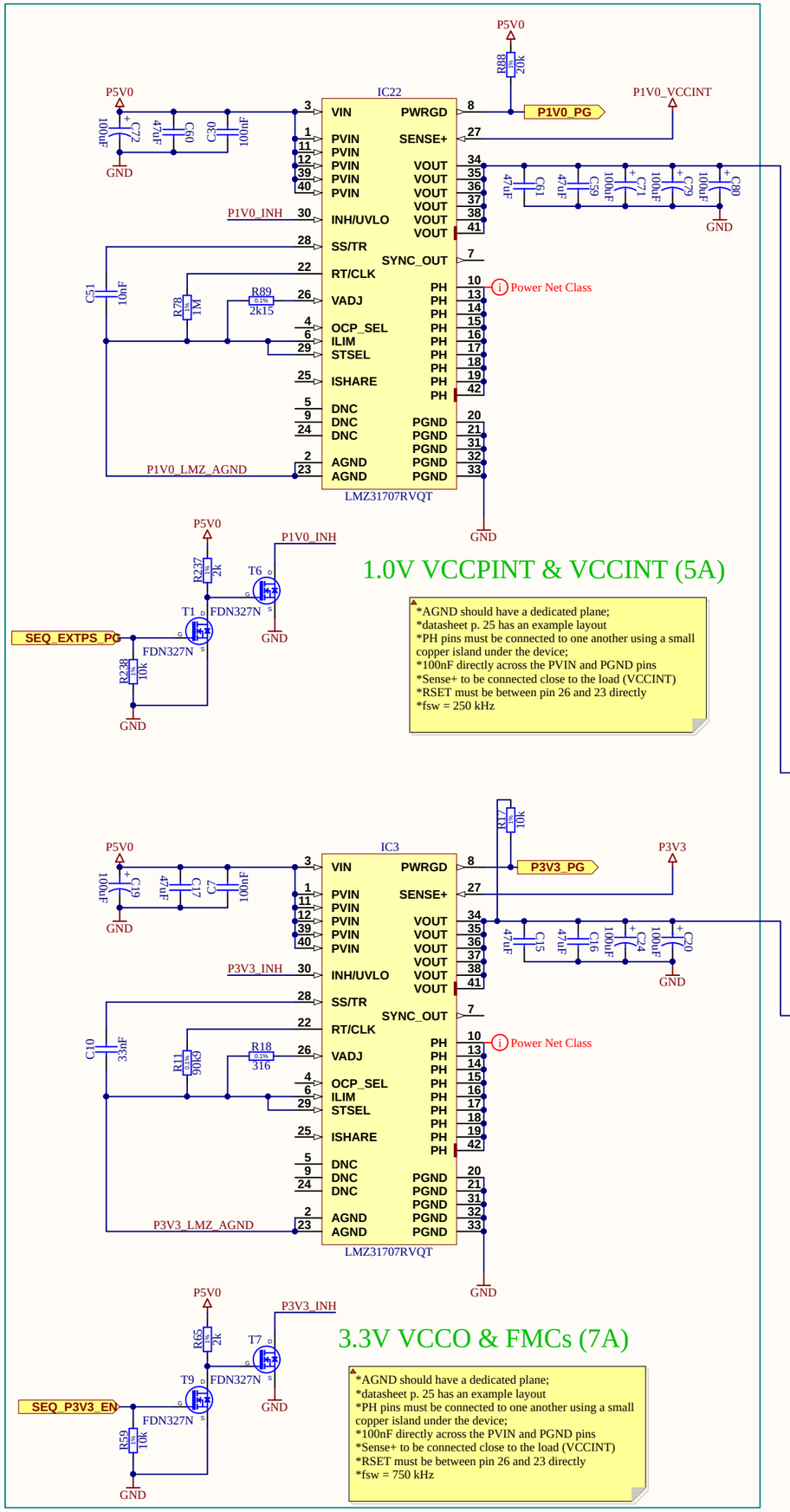
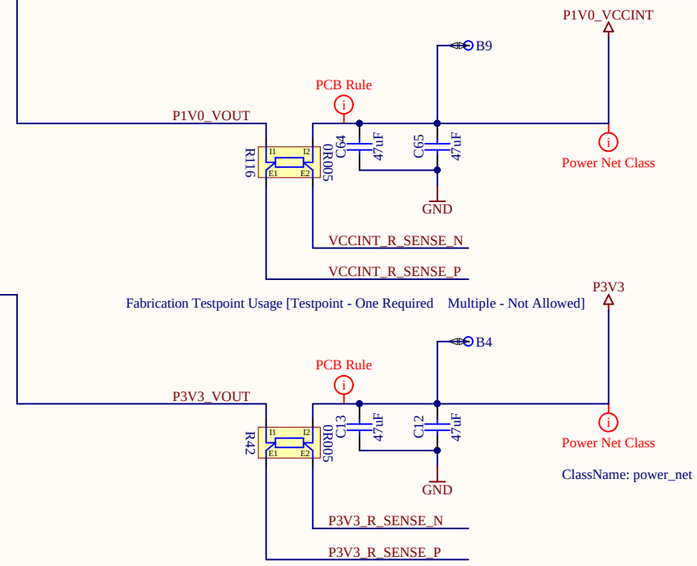
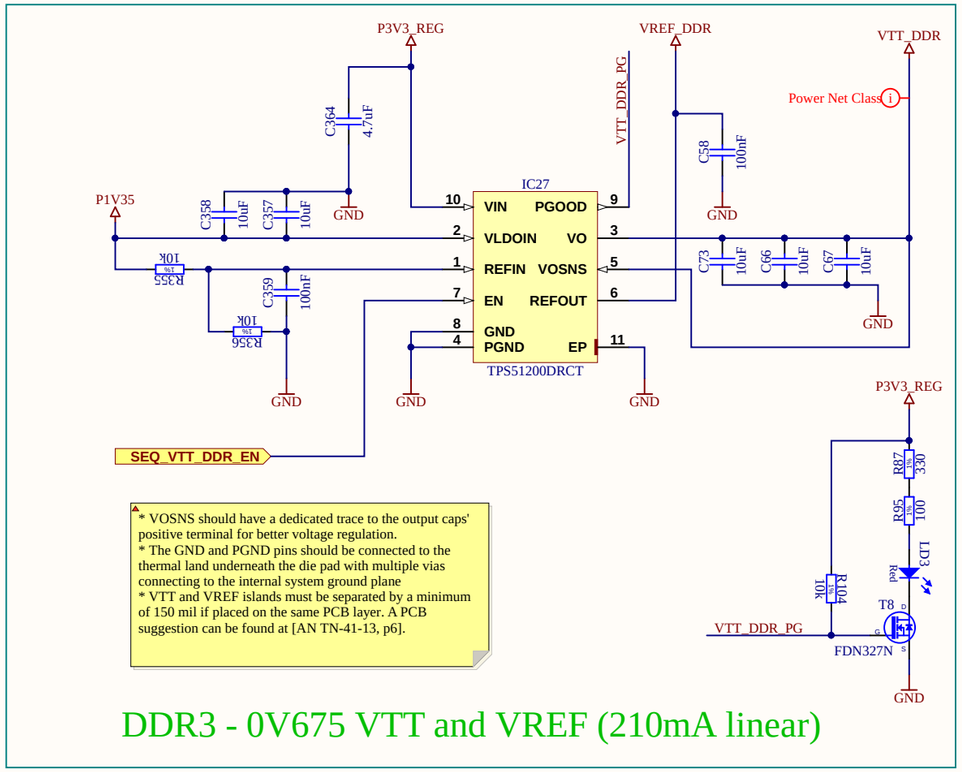
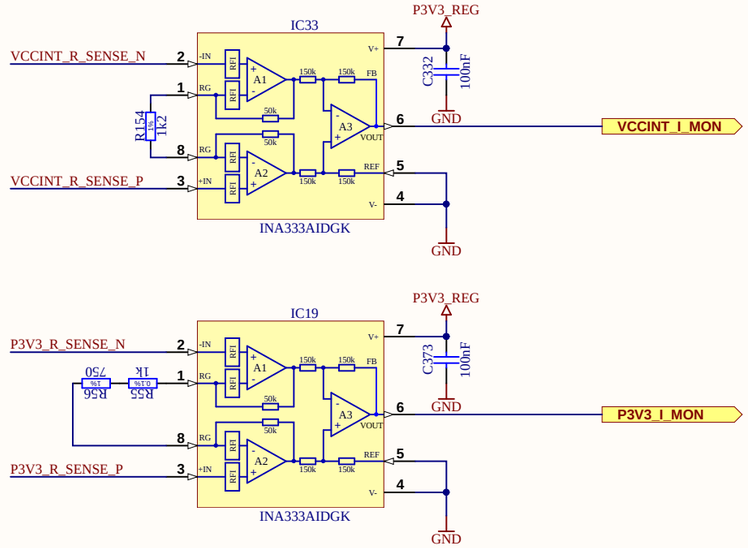
	Sheet: Power Controller	Rev. 0	Date 05/2019 Author broquet
	File: CITY_power-controller.SchDoc	SVN: 89f9589d8aaca0a25e422de51e6	









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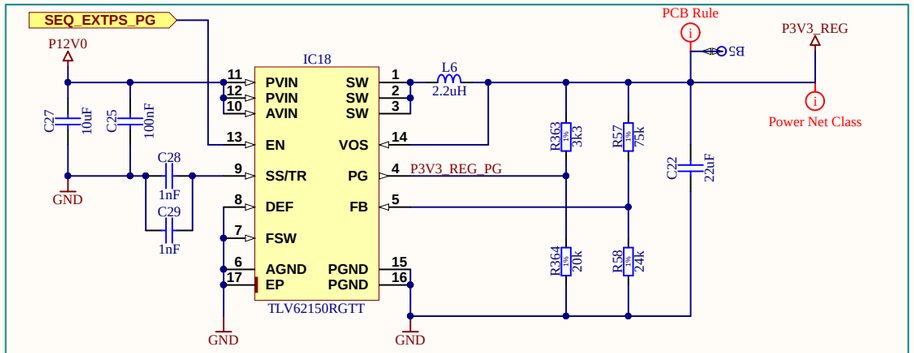
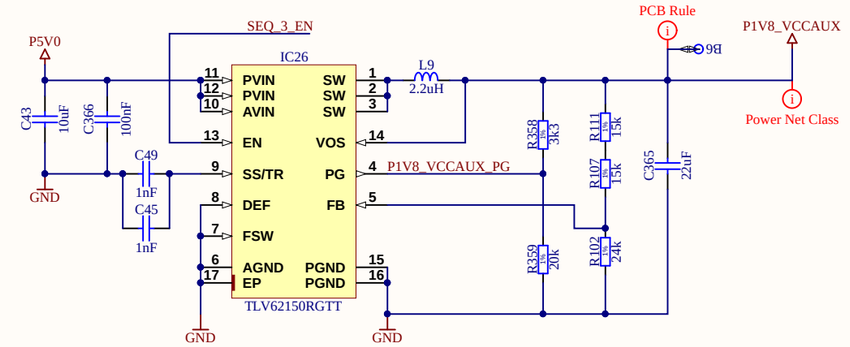
	Project: CITY		
	Sheet: Supplies 1	Rev. 0	Date 05/2019 Author broquet
	File: CITY_power-supplies.SchDoc	SVN: 89f9589d8aaca0a25e422de51e6	



3.3V VREG (1A)

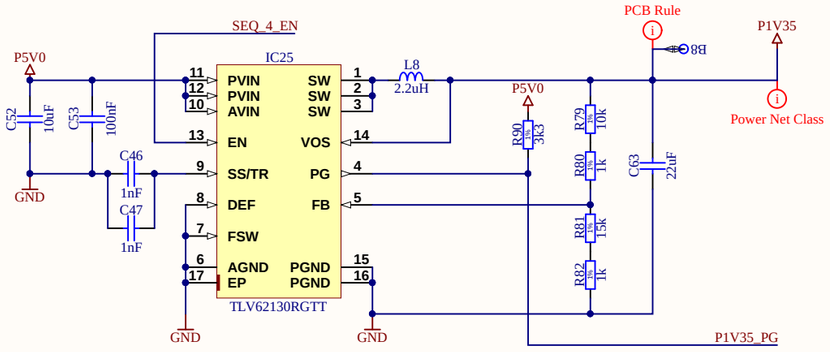
*fsw = 2.5 MHz
*layout example at datasheet p.21
*100nF directly across the AVIN and AGND pins
* Not only used for the LDOs at this page!

Fabrication Testpoint Usage [Testpoint - One Required Multiple - Not Allowed]



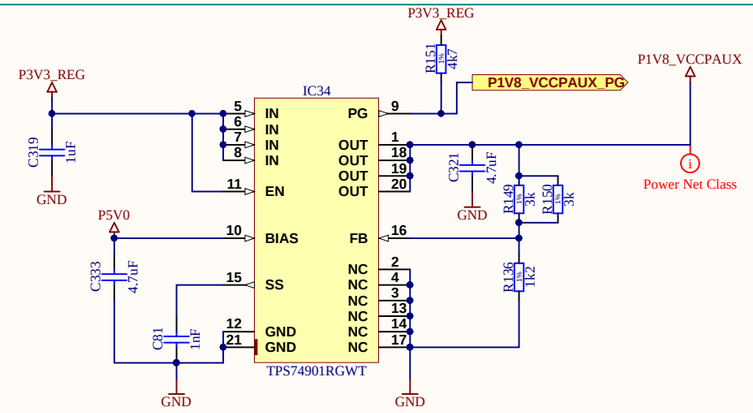
1.8V VCCAUX (800mA)

*fsw = 2.5 MHz
*layout example at datasheet p.21
*100nF directly across the AVIN and AGND pins



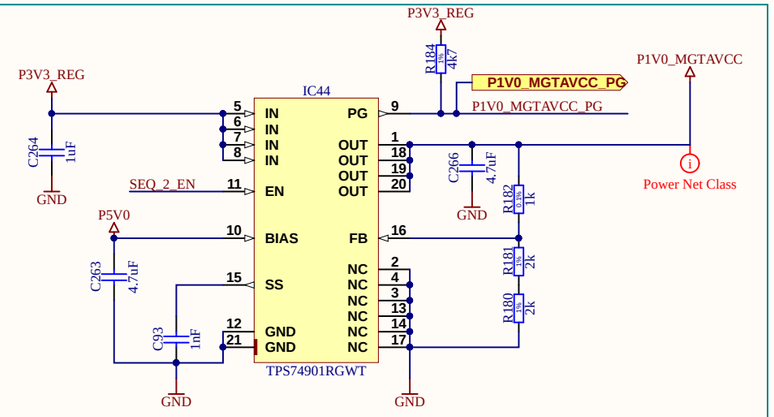
1.35V VCCDDR (1.1A)

*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins



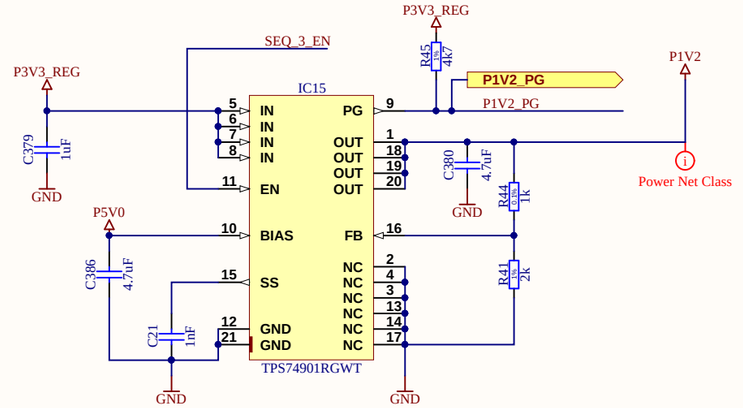
1.8V VCCPAUX (120mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; only 180 mW dissipation with a theta_JA of 120 °C/W.



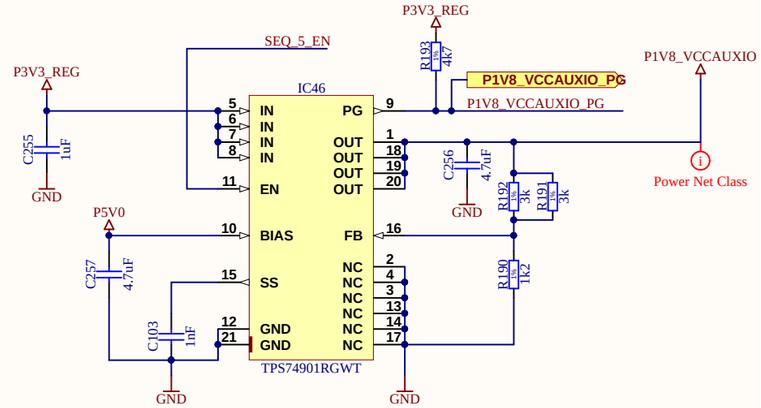
1.0V MGTAVCC (150mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 345 mW dissipation with a theta_JA of 120 °C/W.



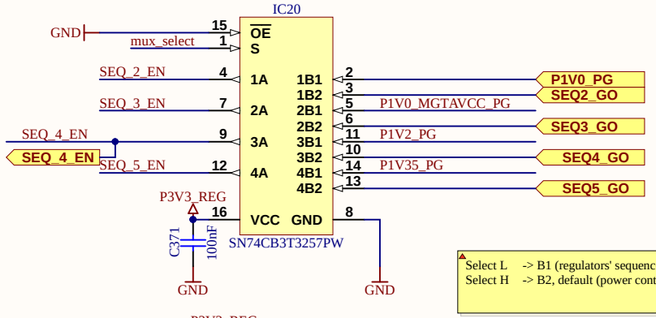
1.2V all (130mA linear)

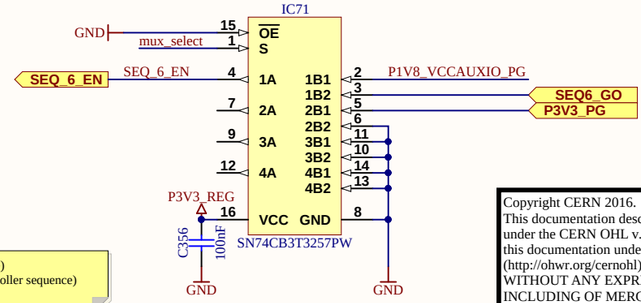
*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a theta_JA of 120 °C/W.

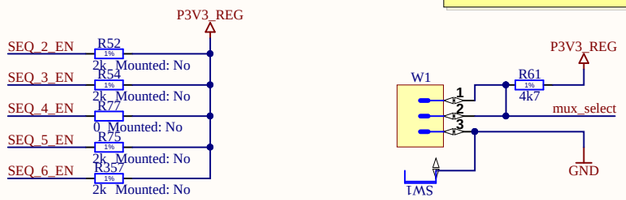


1.8V VCCAUX_IO (130mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a theta_JA of 120 °C/W.







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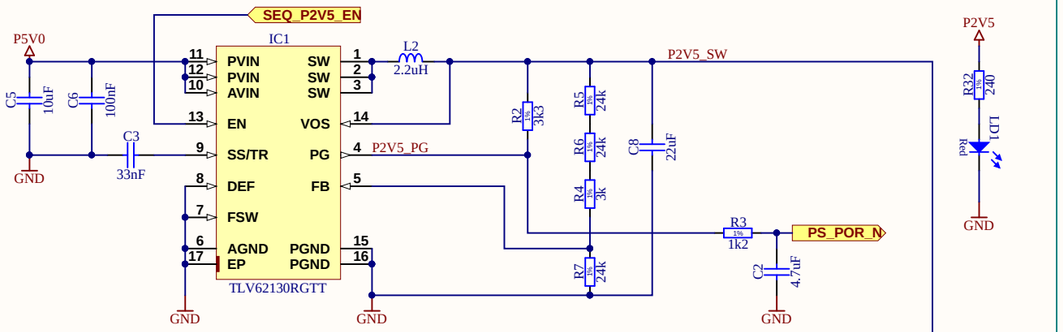
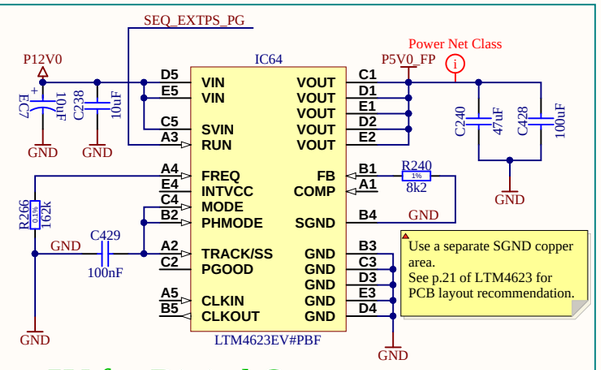


2.5V all (3A max)

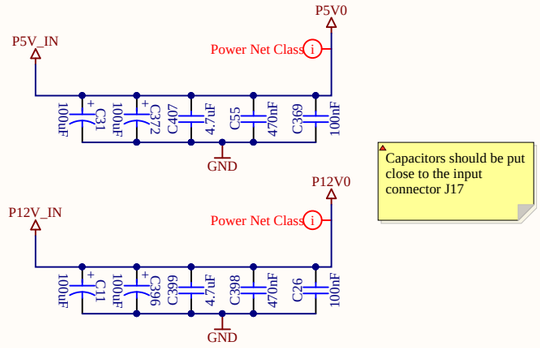
*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins

RC delay (tau=21ms) to provide the required 40ms after VCCO_0 assertion before deasserting PS_POR_B [DS191 p.18] to 2.31V (Vcc*0.7).

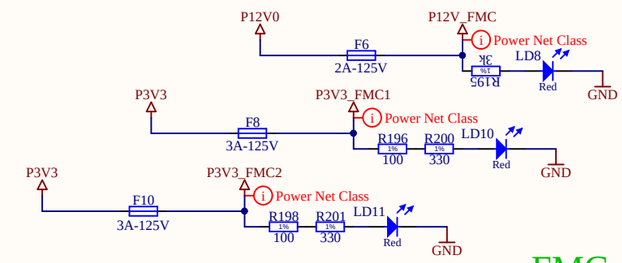
Power ON LED

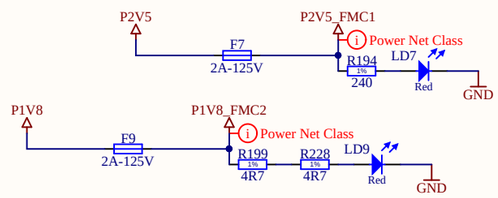


5V for Digital Output stages

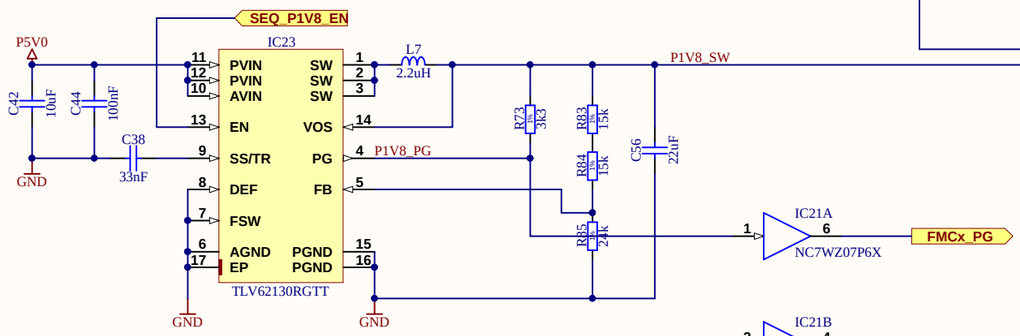


Power supply decoupling



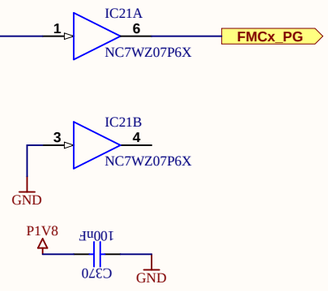


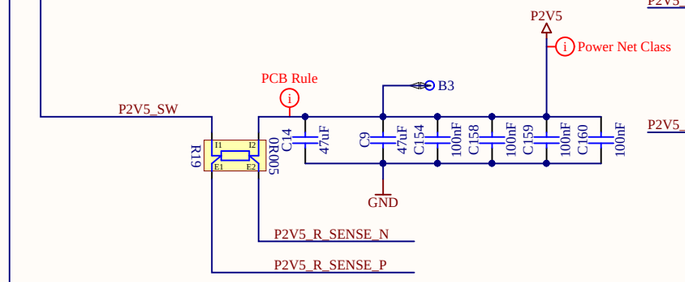
FMC power & fuses

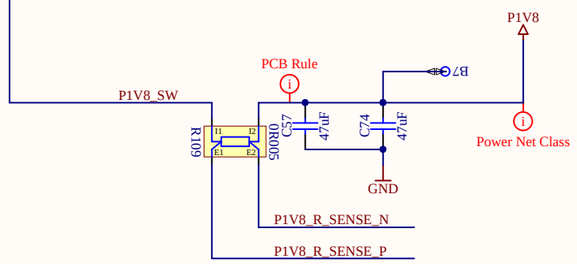


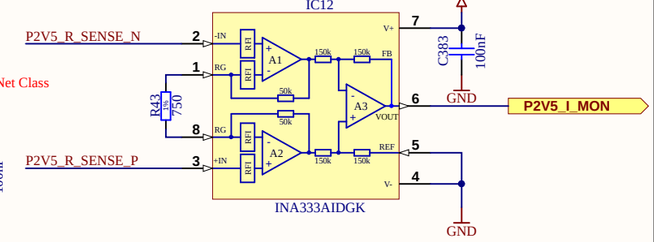
1.8V all (3A max)

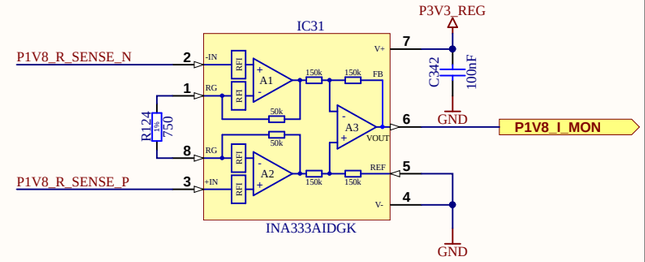
*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins

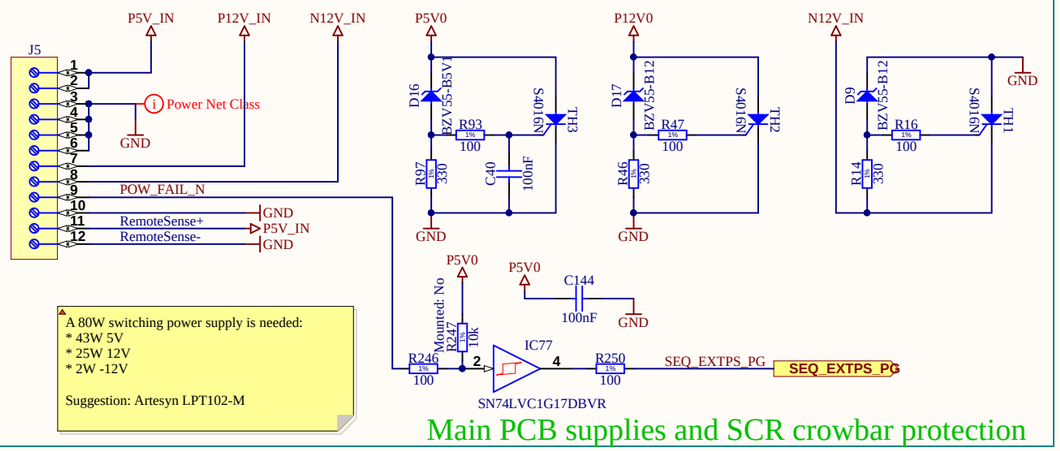




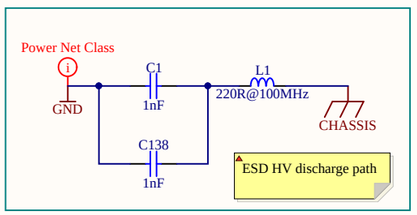








Main PCB supplies and SCR crowbar protection



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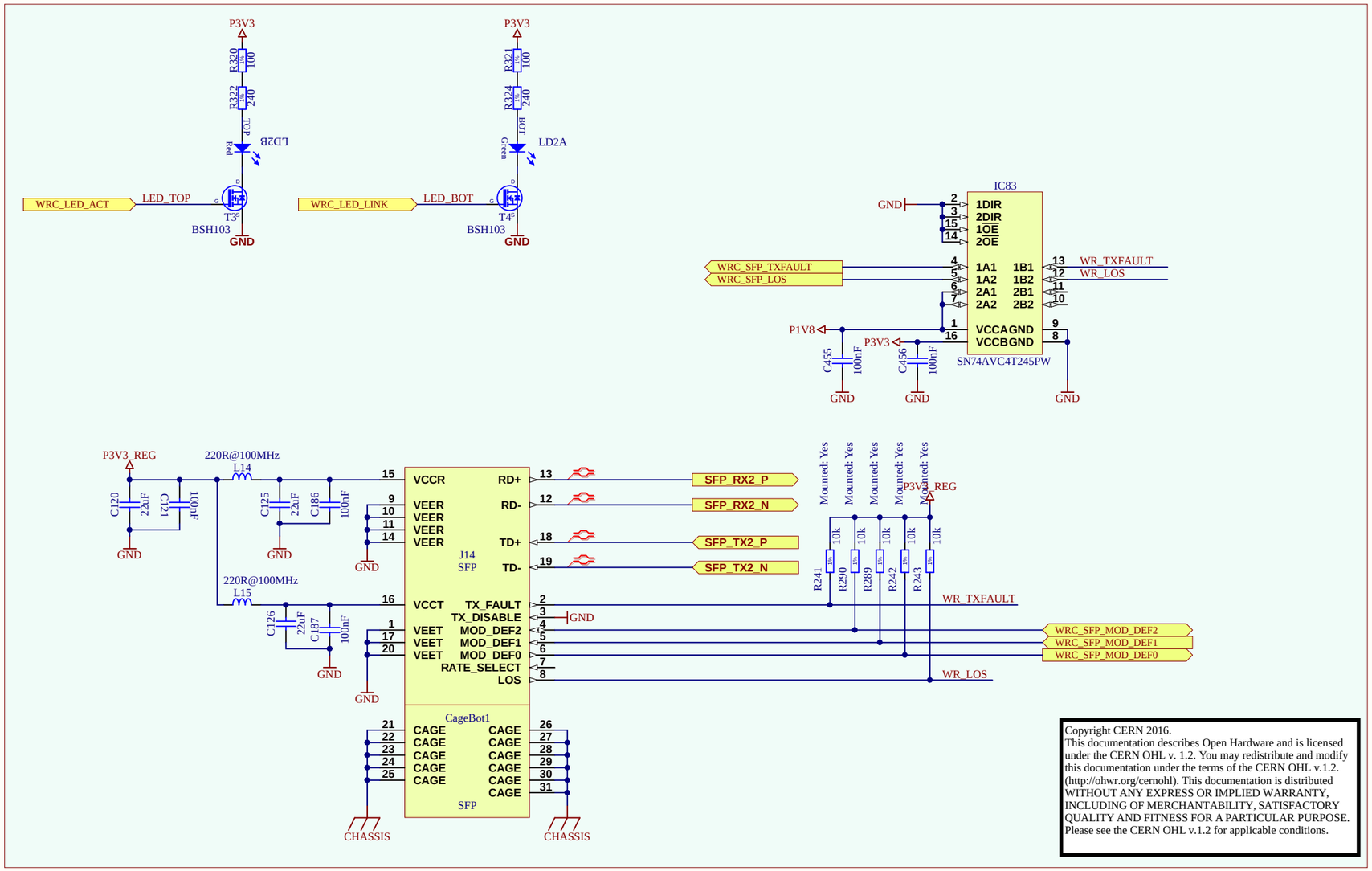
Project: CITY			
Sheet: Supplies 3			
File: CITY_power-supplies-3.SchDoc			

Rev.	Date	Author
0	05/2019	broquet

SVN: 89f9589d8aaca0a25e422de51e6



Based on SPEC schematics, EDA-02189-V4-0 p. 2 & 16

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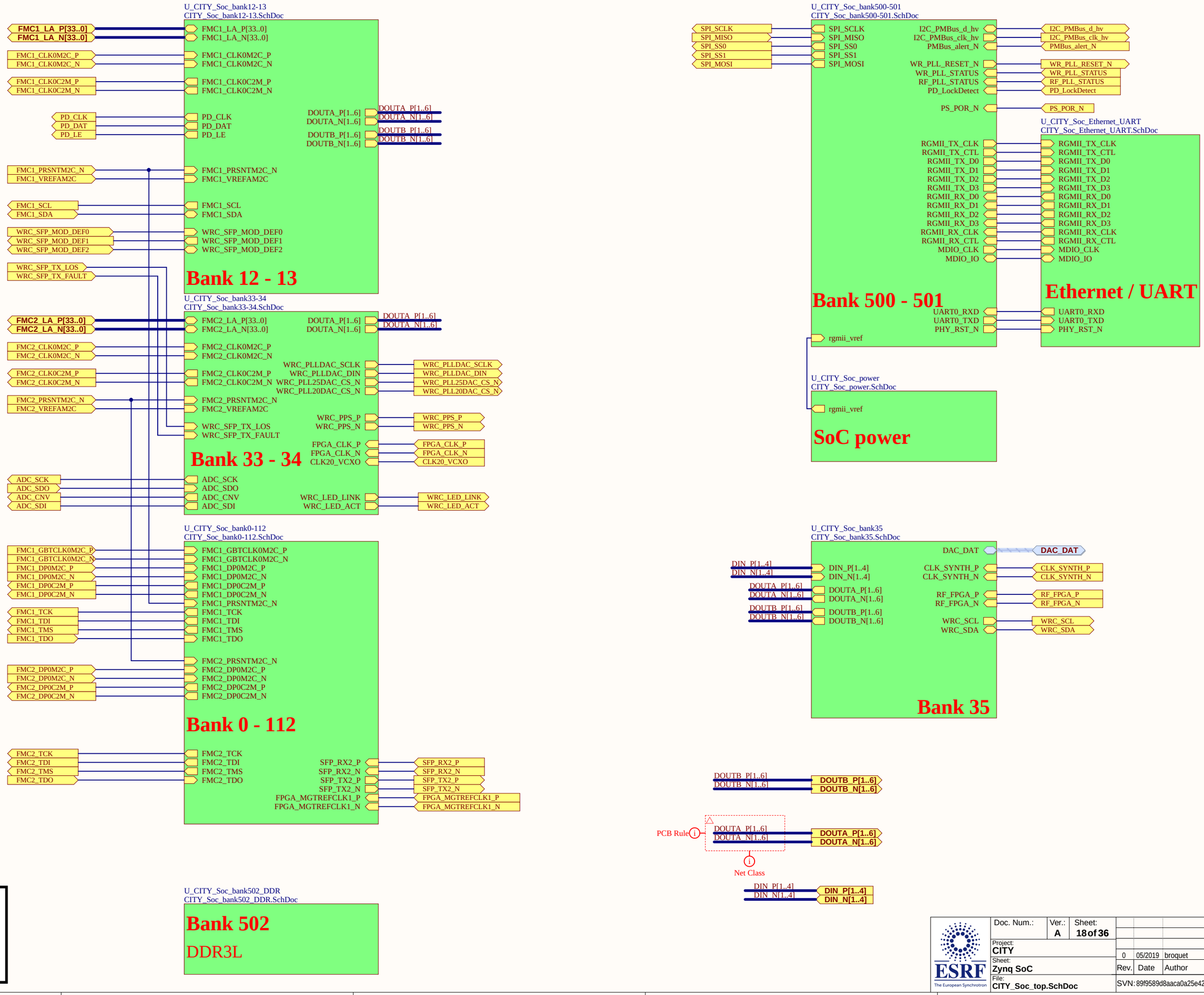
	Sheet: SFP	Rev. 0	Date 05/2019 Author broquet
	File: CITY_SFP.SchDoc	SVN: be6245708ce70bfd0ddb55c0ab5	



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	Sheet: Zynq SoC	Rev. 0	Date 05/2019 Author broquet
	File: CITY_Soc_top.SchDoc	SVN: 89f9589d8aaca0a25e422de51e6	

VCCO_0=2.5V

IC37F
XC7Z030-2FFG676I

JTAG_TDI — V11 TDI_0
ZYNQ_TDO — W10 TDO_0
JTAG_TCK_BUFF1 — W12 TCK_0
JTAG_TMS_BUFF1 — W11 TMS_0
DONE — W9 DONE_0
P2V5 — 4k7 R179 — R8 INIT_B_0
4k7 R178 — V9 PROGRAM_B_0
T7 CFGBVS_0
GND — N14 VP_0
P13 VN_0
P14 VREFP_0
N13 VREFN_0
GND — R14 DXP_0
R13 DXN_0

Bank 0 configuration

The traces from MGTAVTTRCAL_112 and MGTRREF_112 to the resistor should have the same length and geometry [UG476 p. 303].

PCB Rule
Matched Net Lengths [Tolerance = 62mil]
Maximum Via Count Constraint [Max Count = 2]

Net Class GTX_CLK

IC37I
XC7Z030-2FFG676I

FMC1_GBTCLK0M2C_P — 100nF C98 — 100nF C97 MGT_CLK0_P — R6 MGTREFCLK0P_112 — MGTAVTTRCAL_112 — AB7
FMC1_GBTCLK0M2C_N — MGT_CLK0_N — R5 MGTREFCLK0N_112
FPGA_MGTREFCLK1_P — 100nF C102 — MGT_CLK1_P — U6 MGTREFCLK1P_112 — MGTRREF_112 — AB8
FPGA_MGTREFCLK1_N — 100nF C101 — MGT_CLK1_N — U5 MGTREFCLK1N_112

MGT_AVTT — R175 100

FMC1_DP0M2C_P — 100nF C100 — 100nF C99 mgtxrx0_p — AB4 MGTXRXP0_112 — MGTXTXP0_112 — AA2 — FMC1_DP0C2M_P
FMC1_DP0M2C_N — mgtxrx0_n — AB3 MGTXRXN0_112 — MGTXTXN0_112 — AA1 — FMC1_DP0C2M_N
MGT_RX1_P — Y4 MGTXRXP1_112 — MGTXTXP1_112 — W2 MGT_TX1_P
MGT_RX1_N — Y3 MGTXRXN1_112 — MGTXTXN1_112 — W1 MGT_TX1_N

Net Class GTX_RXTX

SFP_RX2_P — V4 MGTXRXP2_112 — MGTXTXP2_112 — U2 — SFP_TX2_P
SFP_RX2_N — V3 MGTXRXN2_112 — MGTXTXN2_112 — U1 — SFP_TX2_N
FMC2_DP0M2C_P — 100nF C95 — mgtxrx3_p — T4 MGTXRXP3_112 — MGTXTXP3_112 — R2 — FMC2_DP0C2M_P
FMC2_DP0M2C_N — 100nF C96 — mgtxrx3_n — T3 MGTXRXN3_112 — MGTXTXN3_112 — R1 — FMC2_DP0C2M_N

PCB Rule
Matched Net Lengths [Tolerance = 6mil]
Maximum Via Count Constraint [Max Count = 2]

MGT_AVCC — IC37J XC7Z030-2FFG676I — MGT_AVTT

R4 T6 U4 Y6 AA4 AA8 AB6 AC8 AD6 AE8 — MGTAVCC — MGTAVTT — T2 V2 W4 Y2 AB2 AC4 AD2 AE4 AF2 AF6
MGT_VCCAUX — V6 MGTVCCAUX

P1V2 — L20 220R@100MHz — MGT_AVTT
C257 100nF — C268 4.7uF — GND

P1V0_MGTAVCC — L21 220R@100MHz — MGT_AVCC
C271 100nF — C278 4.7uF — GND

P1V8 — L22 220R@100MHz — MGT_VCCAUX
C272 100nF — C273 4.7uF — GND

DONE is open-drain but has an internal 10k pull-up resistor. Kept at GND when the configuration sequence has not finished (i.e. FPGA not programmed).

FPGA done

P2V5 — R185 240 — LD6 Green — T11 DONE — FDN327N — GND

JTAG at 2.5V

P2V5 — R189 4k7 — R188 4k7 — R187 4k7 — R186 4k7

J10
1 JTAG_TMS
2 JTAG_TCK
3 JTAG_TDO
4 JTAG_TDI
5 6 7 8 9 10 11 12 13 14
GND

JTAG_TCK — IC47 CDCLVC1102PW — JTAG_TCK_BUFF1 — JTAG_TCK_BUFF2 — FMC1_TCK — FMC2_TCK
P2V5 — L18 220R@100MHz — C253 1uF — C254 100nF — GND GND

JTAG_TMS — IC45 CDCLVC1102PW — JTAG_TMS_BUFF1 — JTAG_TMS_BUFF2 — FMC1_TMS — FMC2_TMS
P2V5 — L19 220R@100MHz — C262 1uF — C258 100nF — GND GND

TCK and TMS trace lengths should be kept as short as possible - the clock buffer somewhere in the middle.

FMC1_PRSNTM2C_N — FMC1_PRSNTM2C_N
FMC2_PRSNTM2C_N — FMC2_PRSNTM2C_N

FMC1_TDO
FMC1_TDI
ZYNQ_TDO — IC85 NC7SZ66P5X — FMC1_TDO_MUX
FMC1_PRSNTM2C_N
P2V5 — C210 100nF — GND

FMC2_TDO
FMC2_TDI
FMC1_TDO_MUX — IC84 NC7SZ66P5X — JTAG_TDO
FMC2_PRSNTM2C_N
P2V5 — C198 100nF — GND

MGT_TX1_P C148 — 100nF — SATA_TX_P
MGT_TX1_N C149 — 100nF — SATA_TX_N
MGT_RX1_N C150 — 100nF — SATA_RX_N
MGT_RX1_P C151 — 100nF — SATA_RX_P

J25 SATA
1 GND
2 A+
3 A-
4 GND
5 B-
6 B+
7 GND
SHIELD
GND

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File: CITY_Soc_bank0-112.SchDoc

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SVN: d31ec2226c449ee6e0322007c15

VCCO_12=2.5V

IC37A
XC7Z030-2FFG676I

BANK 12

IO_0_12	W14	WRC_SFP_MOD_DEF1
IO_L1P_T0_12	Y12	FMC1_LA_P2
IO_L1N_T0_12	Y11	FMC1_LA_N2
IO_L2P_T0_12	AB12	FMC1_LA_P3
IO_L2N_T0_12	AC11	FMC1_LA_N3
IO_L3P_T0_DQS_12	Y10	FMC1_LA_P4
IO_L3N_T0_DQS_12	AA10	FMC1_LA_N4
IO_L4P_T0_12	AB11	FMC1_LA_P6
IO_L4N_T0_12	AB10	FMC1_LA_N6
IO_L5P_T0_12	W13	FMC1_LA_P5
IO_L5N_T0_12	Y13	FMC1_LA_N5
IO_L6P_T0_12	AA13	FMC1_PRSNTM2C_N
IO_L6N_T0_VREF_12	AA12	FMC1_VREFAM2C
IO_L7P_T1_12	AE10	FMC1_LA_P8
IO_L7N_T1_12	AD10	FMC1_LA_N8
IO_L8P_T1_12	AE12	FMC1_LA_P10
IO_L8N_T1_12	AF12	FMC1_LA_N10
IO_L9P_T1_DQS_12	AE11	FMC1_LA_P9
IO_L9N_T1_DQS_12	AF10	FMC1_LA_N9
IO_L10P_T1_12	AE13	FMC1_LA_P7
IO_L10N_T1_12	AF13	FMC1_LA_N7
IO_L11P_T1_SRCC_12	AC12	
IO_L11N_T1_SRCC_12	AD11	FMC1_CLK0M2C_P
IO_L12P_T1_MRCC_12	AC13	FMC1_CLK0M2C_N
IO_L12N_T1_MRCC_12	AD13	FMC1_CLK0C2M_P
IO_L13P_T2_MRCC_12	AC14	FMC1_CLK0C2M_N
IO_L13N_T2_MRCC_12	AD14	FMC1_LA_P0
IO_L14P_T2_SRCC_12	AB15	FMC1_LA_N0
IO_L14N_T2_SRCC_12	AB14	FMC1_LA_P1
IO_L15P_T2_DQS_12	AD16	FMC1_LA_N1
IO_L15N_T2_DQS_12	AD15	FMC1_LA_P16
IO_L16P_T2_12	AF15	FMC1_LA_N16
IO_L16N_T2_12	AF14	FMC1_LA_P13
IO_L17P_T2_12	AE16	FMC1_LA_N13
IO_L17N_T2_12	AE15	FMC1_LA_P14
IO_L18P_T2_12	AE17	FMC1_LA_N14
IO_L18N_T2_12	AF17	FMC1_LA_P15
IO_L19P_T3_12	Y17	FMC1_LA_N15
IO_L19N_T3_VREF_12	AA17	WRC_SFP_MOD_DEF0
IO_L20P_T3_12	AB17	FMC1_VREFAM2C
IO_L20N_T3_12	AB16	DOUTB_P5
IO_L21P_T3_DQS_12	AC17	DOUTB_N5
IO_L21N_T3_DQS_12	AC16	FMC1_LA_P11
IO_L22P_T3_12	AA15	FMC1_LA_N11
IO_L22N_T3_12	AA14	FMC1_LA_P12
IO_L23P_T3_12	Y16	FMC1_LA_N12
IO_L23N_T3_12	Y15	DOUTA_P5
IO_L24P_T3_12	W16	DOUTA_N5
IO_L24N_T3_12	W15	DOUTB_P4
IO_25_12	W17	DOUTB_N4
		WRC_SFP_MOD_DEF2

C283 100nF → GND

C298 100nF → GND

VCCO_13=2.5V

IC37B
XC7Z030-2FFG676I

BANK 13

IO_0_13	V19	PD_DAT
IO_L1P_T0_13	AA25	FMC1_LA_P33
IO_L1N_T0_13	AB25	FMC1_LA_N33
IO_L2P_T0_13	AB26	FMC1_LA_P28
IO_L2N_T0_13	AC26	FMC1_LA_N28
IO_L3P_T0_DQS_13	AE25	FMC1_LA_P25
IO_L3N_T0_DQS_13	AE26	FMC1_LA_N25
IO_L4P_T0_13	AD25	FMC1_LA_P24
IO_L4N_T0_13	AD26	FMC1_LA_N24
IO_L5P_T0_13	AF24	FMC1_LA_P26
IO_L5N_T0_13	AF25	FMC1_LA_N26
IO_L6P_T0_13	AA24	
IO_L6N_T0_VREF_13	AB24	FMC1_VREFAM2C
IO_L7P_T1_13	AE22	FMC1_LA_P21
IO_L7N_T1_13	AF22	FMC1_LA_N21
IO_L8P_T1_13	AE23	FMC1_LA_P27
IO_L8N_T1_13	AF23	FMC1_LA_N27
IO_L9P_T1_DQS_13	AB21	FMC1_LA_P30
IO_L9N_T1_DQS_13	AB22	FMC1_LA_N30
IO_L10P_T1_13	AA22	FMC1_LA_P32
IO_L10N_T1_13	AA23	FMC1_LA_N32
IO_L11P_T1_SRCC_13	AD23	FMC1_LA_P17
IO_L11N_T1_SRCC_13	AD24	FMC1_LA_N17
IO_L12P_T1_MRCC_13	AC23	DOUTB_P6
IO_L12N_T1_MRCC_13	AC24	DOUTB_N6
IO_L13P_T2_MRCC_13	AD20	FPGA_SCL1
IO_L13N_T2_MRCC_13	AD21	FPGA_SDA1
IO_L14P_T2_SRCC_13	AC21	FMC1_LA_P18
IO_L14N_T2_SRCC_13	AC22	FMC1_LA_N18
IO_L15P_T2_DQS_13	AF19	FMC1_LA_P22
IO_L15N_T2_DQS_13	AF20	FMC1_LA_N22
IO_L16P_T2_13	AE20	DOUTA_P6
IO_L16N_T2_13	AE21	DOUTA_N6
IO_L17P_T2_13	AD18	FMC1_LA_P23
IO_L17N_T2_13	AD19	FMC1_LA_N23
IO_L18P_T2_13	AE18	FMC1_LA_P19
IO_L18N_T2_13	AF18	FMC1_LA_N19
IO_L19P_T3_13	W20	PD_LE
IO_L19N_T3_VREF_13	Y20	FMC1_VREFAM2C
IO_L20P_T3_13	AA20	FMC1_LA_P31
IO_L20N_T3_13	AB20	FMC1_LA_N31
IO_L21P_T3_DQS_13	AC18	FMC1_LA_P29
IO_L21N_T3_DQS_13	AC19	FMC1_LA_N29
IO_L22P_T3_13	AA19	DOUTB_P3
IO_L22N_T3_13	AB19	DOUTB_N3
IO_L23P_T3_13	W18	FMC1_LA_P20
IO_L23N_T3_13	W19	FMC1_LA_N20
IO_L24P_T3_13	Y18	DOUTA_P4
IO_L24N_T3_13	AA18	DOUTA_N4
IO_25_13	V18	PD_CLK

C311 100nF → GND

C305 100nF → GND

DOUTA_P[1..6] → DOUTA_P[1..6]
DOUTA_N[1..6] → DOUTA_N[1..6]
DOUTB_P[1..6] → DOUTB_P[1..6]
DOUTB_N[1..6] → DOUTB_N[1..6]

FMC1_LA_P[33..0] → FMC1_LA_P[33..0]
FMC1_LA_N[33..0] → FMC1_LA_N[33..0]
FMC1_VREFAM2C → FMC1_VREFAM2C

P2V5
P3V3
R315 1K2
R316 1K2
R297 1K2
R298 1K2
IC80
FPGA_SDA1 → 3
FPGA_SCL1 → 2
SDAA 3 | SDAB 6 → FMC1_SDA
SCLA 2 | SCLB 7 → FMC1_SCL
5 EN
1 VCCA | VCCB 8 | GND 4
TCA9517DGKR
C195 100nF → GND
C185 100nF → GND

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File: CITY_Soc_bank12-13.SchDoc	SVN: 89f9589d8aaca0a25e422de51e6		

VCCO_33=1.8V

IC37C
XC7Z030-2FFG676I

BANK 33

IO_0_VRN_33	L9	
IO_L1P_T0_33	G4	FMC2_LA_P3
IO_L1N_T0_33	F4	FMC2_LA_N3
IO_L2P_T0_33	D4	FMC2_LA_P2
IO_L2N_T0_33	D3	FMC2_LA_N2
IO_L3P_T0_DQS_33	G2	FMC2_LA_P5
IO_L3N_T0_DQS_33	F2	FMC2_LA_N5
IO_L4P_T0_33	D1	FMC2_LA_P4
IO_L4N_T0_33	C1	FMC2_LA_N4
IO_L5P_T0_33	E2	FMC2_LA_P6
IO_L5N_T0_33	E1	FMC2_LA_N6
IO_L6P_T0_33	F3	
IO_L6N_T0_VREF_33	E3	FMC2_VREFAM2C
IO_L7P_T1_33	J1	FMC2_LA_P9
IO_L7N_T1_33	H1	FMC2_LA_N9
IO_L8P_T1_33	H4	FMC2_LA_P8
IO_L8N_T1_33	H3	FMC2_LA_N8
IO_L9P_T1_DQS_33	K2	FMC2_LA_P10
IO_L9N_T1_DQS_33	K1	FMC2_LA_N10
IO_L10P_T1_33	H2	FMC2_LA_P7
IO_L10N_T1_33	G1	FMC2_LA_N7
IO_L11P_T1_SRCC_33	L3	
IO_L11N_T1_SRCC_33	K3	
IO_L12P_T1_MRCC_33	J4	
IO_L12N_T1_MRCC_33	J3	
IO_L13P_T2_MRCC_33	M6	FMC2_LA_P0
IO_L13N_T2_MRCC_33	M5	FMC2_LA_N0
IO_L14P_T2_SRCC_33	L5	FMC2_LA_P1
IO_L14N_T2_SRCC_33	L4	FMC2_LA_N1
IO_L15P_T2_DQS_33	N3	FMC2_LA_P14
IO_L15N_T2_DQS_33	N2	FMC2_LA_N14
IO_L16P_T2_33	M2	FMC2_LA_P13
IO_L16N_T2_33	L2	FMC2_LA_N13
IO_L17P_T2_33	N4	FMC2_LA_P11
IO_L17N_T2_33	M4	FMC2_LA_N11
IO_L18P_T2_33	N1	FMC2_LA_P16
IO_L18N_T2_33	M1	FMC2_LA_N16
IO_L19P_T3_33	M7	
IO_L19N_T3_VREF_33	L7	FMC2_VREFAM2C
IO_L20P_T3_33	K5	
IO_L20N_T3_33	J5	
IO_L21P_T3_DQS_33	M8	FMC2_LA_P15
IO_L21N_T3_DQS_33	L8	FMC2_LA_N15
IO_L22P_T3_33	K6	FMC2_LA_P12
IO_L22N_T3_33	J6	FMC2_LA_N12
IO_L23P_T3_33	N7	
IO_L23N_T3_33	N6	
IO_L24P_T3_33	K8	
IO_L24N_T3_33	K7	
IO_25_VRP_33	N8	

WRC_LED_ACT
FMC2_PRSNTM2C_N
FMC2_CLK0M2C_P
FMC2_CLK0M2C_N
FMC2_CLK0C2M_P
FMC2_CLK0C2M_N
ADC_SDI
ADC_SCK
ADC_SDO
WRC_PPS_P
WRC_PPS_N
ADC_CNV

C269 100nF → GND
C280 100nF → GND

VCCO_34=1.8V

IC37D
XC7Z030-2FFG676I

BANK 34

IO_0_VRN_34	K11	
IO_L1P_T0_34	J11	FMC2_LA_P25
IO_L1N_T0_34	H11	FMC2_LA_N25
IO_L2P_T0_34	G6	FMC2_LA_P23
IO_L2N_T0_34	G5	FMC2_LA_N23
IO_L3P_T0_DQS_PUDC_B_34	H9	
IO_L3N_T0_DQS_34	G9	
IO_L4P_T0_34	H7	FMC2_LA_P22
IO_L4N_T0_34	H6	FMC2_LA_N22
IO_L5P_T0_34	J10	FMC2_LA_P26
IO_L5N_T0_34	J9	FMC2_LA_N26
IO_L6P_T0_34	J8	
IO_L6N_T0_VREF_34	H8	FMC2_VREFAM2C
IO_L7P_T1_34	F5	FMC2_LA_P27
IO_L7N_T1_34	E5	FMC2_LA_N27
IO_L8P_T1_34	D9	FMC2_LA_P28
IO_L8N_T1_34	D8	FMC2_LA_N28
IO_L9P_T1_DQS_34	F9	FMC2_LA_P29
IO_L9N_T1_DQS_34	E8	FMC2_LA_N29
IO_L10P_T1_34	E6	FMC2_LA_P24
IO_L10N_T1_34	D5	FMC2_LA_N24
IO_L11P_T1_SRCC_34	F8	FMC2_LA_P17
IO_L11N_T1_SRCC_34	E7	FMC2_LA_N17
IO_L12P_T1_MRCC_34	G7	
IO_L12N_T1_MRCC_34	F7	
IO_L13P_T2_MRCC_34	C8	
IO_L13N_T2_MRCC_34	C7	
IO_L14P_T2_SRCC_34	D6	FMC2_LA_P18
IO_L14N_T2_SRCC_34	C6	FMC2_LA_N18
IO_L15P_T2_DQS_34	C9	DOUTA_P3
IO_L15N_T2_DQS_34	B9	DOUTA_N3
IO_L16P_T2_34	B10	FMC2_LA_P32
IO_L16N_T2_34	A10	FMC2_LA_N32
IO_L17P_T2_34	A9	FMC2_LA_P33
IO_L17N_T2_34	A8	FMC2_LA_N33
IO_L18P_T2_34	B7	
IO_L18N_T2_34	A7	
IO_L19P_T3_34	C4	
IO_L19N_T3_VREF_34	C3	FMC2_VREFAM2C
IO_L20P_T3_34	B5	FMC2_LA_P31
IO_L20N_T3_34	B4	FMC2_LA_N31
IO_L21P_T3_DQS_34	B6	FMC2_LA_P30
IO_L21N_T3_DQS_34	A5	FMC2_LA_N30
IO_L22P_T3_34	A4	FMC2_LA_P21
IO_L22N_T3_34	A3	FMC2_LA_N21
IO_L23P_T3_34	C2	FMC2_LA_P20
IO_L23N_T3_34	B1	FMC2_LA_N20
IO_L24P_T3_34	B2	FMC2_LA_P19
IO_L24N_T3_34	A2	FMC2_LA_N19
IO_25_VRP_34	K10	TEMPID_DQ

WRC_LED_LINK
WRC_SFP_TX_FAULT
WRC_SFP_TX_LOS
FPGA_CLK_P
FPGA_CLK_N
CLK20_VCXO
WRC_PLL20DAC_CS_N
WRC_PLLDAC_SCLK
WRC_PLLDAC_DIN
WRC_PLL25DAC_CS_N

P1V8 → R339 750 → WRC_SFP_TX_FAULT
R341 750 → GND (Mounted: No)
C281 100nF → GND
C270 100nF → GND

P1V8 → R342 750 → TEMPID_DQ

IC41
DS2411R+
pin 1: I/O
pin 3: GND
pin 2: VCC
P1V8 → C282 100nF → GND

Unique 64-bit ID (Maxim 1-Wire)

FMC2_LA_P[33..0] — FMC2_LA_P[33..0]
FMC2_LA_N[33..0] — FMC2_LA_N[33..0]
FMC2_VREFAM2C — FMC2_VREFAM2C

DOUTA_P[1..6] — DOUTA_P[1..6]
DOUTA_N[1..6] — DOUTA_N[1..6]

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File: CITY_Soc_bank33-34.SchDoc			

Rev.	Date	Author
0	05/2019	broquet

SVN: 89f9589d8aaca0a25e422de51e6

VCCO_35=1.8V

IC37E
XC7Z030-2FFG676I

BANK 35

IO_0_VRN_35	H16	WRC_SDA
IO_L1P_T0_AD0P_35	F12	DAC6_P
IO_L1N_T0_AD0N_35	E12	DAC6_N
IO_L2P_T0_AD8P_35	E10	DAC8_P
IO_L2N_T0_AD8N_35	D10	DAC8_N
IO_L3P_T0_DQS_AD1P_35	G10	DAC9_P
IO_L3N_T0_DQS_AD1N_35	F10	DAC9_N
IO_L4P_T0_35	E11	DAC7_P
IO_L4N_T0_35	D11	DAC7_N
IO_L5P_T0_AD9P_35	G12	DAC10_P
IO_L5N_T0_AD9N_35	G11	DAC10_N
IO_L6P_T0_35	F13	DAC5_P
IO_L6N_T0_VREF_35	E13	DAC5_N
IO_L7P_T1_AD2P_35	H13	DAC12_P
IO_L7N_T1_AD2N_35	H12	DAC12_N
IO_L8P_T1_AD10P_35	K13	DAC13_P
IO_L8N_T1_AD10N_35	J13	DAC13_N
IO_L9P_T1_DQS_AD3P_35	K15	DAC3_P
IO_L9N_T1_DQS_AD3N_35	J15	DAC3_N
IO_L10P_T1_AD11P_35	G16	DAC1_P
IO_L10N_T1_AD11N_35	G15	DAC1_N
IO_L11P_T1_SRCC_35	G14	DAC11_P
IO_L11N_T1_SRCC_35	F14	DAC11_N
IO_L12P_T1_MRCC_35	J14	
IO_L12N_T1_MRCC_35	H14	CLK_SYNTH_P
IO_L13P_T2_MRCC_35	D15	CLK_SYNTH_N
IO_L13N_T2_MRCC_35	D14	RF_FPGA_P
IO_L14P_T2_AD4P_SRCC_35	F15	RF_FPGA_N
IO_L14N_T2_AD4N_SRCC_35	E15	DAC4_P
IO_L15P_T2_DQS_AD12P_35	C17	DAC4_N
IO_L15N_T2_DQS_AD12N_35	C16	DAC0_P
IO_L16P_T2_35	E16	DAC0_N
IO_L16N_T2_35	D16	DAC2_P
IO_L17P_T2_AD5P_35	B16	DAC2_N
IO_L17N_T2_AD5N_35	B15	DIN_P2
IO_L18P_T2_AD13P_35	B17	DIN_N2
IO_L18N_T2_AD13N_35	A17	DIN_P1
IO_L19P_T3_35	D13	DIN_N1
IO_L19N_T3_VREF_35	C13	DIN_P4
IO_L20P_T3_AD6P_35	C14	DIN_N4
IO_L20N_T3_AD6N_35	B14	DOUTB_P1
IO_L21P_T3_DQS_AD14P_35	A15	DOUTB_N1
IO_L21N_T3_DQS_AD14N_35	A14	DIN_P3
IO_L22P_T3_AD7P_35	C12	DIN_N3
IO_L22N_T3_AD7N_35	B12	DOUTA_P2
IO_L23P_T3_35	C11	DOUTA_N2
IO_L23N_T3_35	B11	DOUTB_P2
IO_L24P_T3_AD15P_35	A13	DOUTB_N2
IO_L24N_T3_AD15N_35	A12	DOUTA_P1
IO_25_VRP_35	K12	DOUTA_N1
		WRC_SCL

DAC_DAT

DAC0_P	DAC0_P	DAC_DAT
DAC0_N	DAC0_N	
DAC1_P	DAC1_P	
DAC1_N	DAC1_N	
DAC2_P	DAC2_P	
DAC2_N	DAC2_N	
DAC3_P	DAC3_P	
DAC3_N	DAC3_N	
DAC4_P	DAC4_P	
DAC4_N	DAC4_N	
DAC5_P	DAC5_P	
DAC5_N	DAC5_N	
DAC6_P	DAC6_P	
DAC6_N	DAC6_N	
DAC7_P	DAC7_P	
DAC7_N	DAC7_N	
DAC8_P	DAC8_P	
DAC8_N	DAC8_N	
DAC9_P	DAC9_P	
DAC9_N	DAC9_N	
DAC10_P	DAC10_P	
DAC10_N	DAC10_N	
DAC11_P	DAC11_P	
DAC11_N	DAC11_N	
DAC12_P	DAC12_P	
DAC12_N	DAC12_N	
DAC13_P	DAC13_P	
DAC13_N	DAC13_N	

DOUTB_P[1..6] → DOUTB_P[1..6]
DOUTB_N[1..6] → DOUTB_N[1..6]
DOUTA_P[1..6] → DOUTA_P[1..6]
DOUTA_N[1..6] → DOUTA_N[1..6]

DIN_P[1..4] → DIN_P[1..4]
DIN_N[1..4] → DIN_N[1..4]

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Rev.	Date	Author
0	05/2019	broquet

SVN: 89f9589d8aaca0a25e422de51e6

VCCO_500=3.3V

VCCO_501=1.8V

rgmii_vref RGMII_VREF

IC37G
XC7Z030-2FFG676I

PS_CLK_500	B24	OSC_33
PS_POR_B_500	C23	PS_POR_OR_N
PS_SRST_B_501	A22	PS_SRST_OR_N
PS_MIO_VREF_501	H18	RGMII_VREF
	E26	QSPI1_CS
PS_MIO1_500	D26	QSPI0_CS
PS_MIO2_500	E25	QSPI0_DQ0
PS_MIO3_500	D25	QSPI0_DQ1
PS_MIO4_500	F24	QSPI0_DQ2
PS_MIO5_500	C26	QSPI0_DQ3
PS_MIO6_500	F23	QSPI0_SCLK
PS_MIO7_500	E23	MIO_BANK0_VMODE
PS_MIO8_500	A24	MIO_BANK1_VMODE
PS_MIO9_500	D24	QSPI1_SCLK
PS_MIO10_500	A25	QSPI1_DQ0
PS_MIO11_500	B26	QSPI1_DQ1
PS_MIO12_500	A23	QSPI1_DQ2
PS_MIO13_500	B25	QSPI1_DQ3
PS_MIO14_500	D23	PMBus_alert_N
PS_MIO15_500	C24	WR_PLL_RESET_N
PS_MIO16_501	G21	RGMII_TX_CLK / RGMII_TX_CLK
PS_MIO17_501	G17	RGMII_TX_D0 / RGMII_TX_D0
PS_MIO18_501	G20	RGMII_TX_D1 / RGMII_TX_D1
PS_MIO19_501	G19	RGMII_TX_D2 / RGMII_TX_D2
PS_MIO20_501	H19	RGMII_TX_D3 / RGMII_TX_D3
PS_MIO21_501	F22	RGMII_TX_CTL / RGMII_TX_CTL
PS_MIO22_501	G22	RGMII_RX_CLK / RGMII_RX_CLK
PS_MIO23_501	F20	RGMII_RX_D0 / RGMII_RX_D0
PS_MIO24_501	J19	RGMII_RX_D1 / RGMII_RX_D1
PS_MIO25_501	F19	RGMII_RX_D2 / RGMII_RX_D2
PS_MIO26_501	H17	RGMII_RX_D3 / RGMII_RX_D3
PS_MIO27_501	F18	RGMII_RX_CTL / RGMII_RX_CTL
PS_MIO28_501	J18	SPI_SCLK
PS_MIO29_501	E20	SPI_MISO
PS_MIO30_501	K19	SPI_SS0
PS_MIO31_501	E21	SPI_SS1
PS_MIO32_501	K17	SPI_SS2
PS_MIO33_501	E22	SPI_MOSI
PS_MIO34_501	J16	
PS_MIO35_501	D19	WR_PLL_STATUS
PS_MIO36_501	K16	RF_PLL_STATUS
PS_MIO37_501	D20	PD_LockDetect
PS_MIO38_501	D21	I2C_PMBus_clk
PS_MIO39_501	C21	I2C_PMBus_d
PS_MIO40_501	C22	40R2 R343 SD_CLK_VL
PS_MIO41_501	C19	SD_CMD_VL
PS_MIO42_501	F17	SD_D0_VL
PS_MIO43_501	D18	SD_D1_VL
PS_MIO44_501	E18	SD_D2_VL
PS_MIO45_501	C18	SD_D3_VL
PS_MIO46_501	E17	SD_CD_VL
PS_MIO47_501	B19	SD_WP_VL
PS_MIO48_501	B21	UART0_TXD
PS_MIO49_501	A18	UART0_RXD
PS_MIO50_501	B22	
PS_MIO51_501	B20	
PS_MIO52_501	A20	MDIO_CLK
PS_MIO53_501	A19	MDIO_IO

Net Class HSSD_VL

PCB Rule

P3V3 R139 330 R153 330 R349 20k R350 20k R348 20k R345 20k R344 20k GND

ALL QSPI 20k resistors should be placed near the middle of the QSPI0 traces while keeping their stubs as short as possible, in any case < 10 mm.

P3V3 OSC3 VDD OUT E/D GND 33.333MHz R162 100 OSC_33 C313 100nF GND

Boot Mode MIO strapping pins:
MIO[2] : '0' (PD) : JTAG Cascade mode
MIO[3] : '0' (PD) : no NOR boot, not on board
MIO[4-5] : see below (user selectable)
MIO[6] : '0' (PD) : PLL enabled
MIO[7-8] : '01' : Bank 0/1 at 3.3V/1.8V

MIO[4] SW1A	MIO[5] SW2A	=> Boot Mode
0	0	=> JTAG cascade
0	1	=> QUAD-SPI
1	0	=> NAND (not on board)
1	1	=> SD Card

microSD card

P3V3 R360 4k7 Mounted: No HSSD Net Class SD_D2 SD_D3 SD_CMD SD_CLK SD_D0 SD_D1 PCB Rule C361 100nF GND

J7: DAT2 DAT3 CMD VDD CLK VSS DAT0 DAT1 DETSW DETLEV

IC16 MAX13035EETE+: I/OVL1 I/OVL2 I/OVL3 I/OVL4 I/OVL5 CLKVL CLK_RET VL GND EP I/OVCC1 I/OVCC2 I/OVCC3 I/OVCC4 I/OVCC5 CLKVCC VCC

SD_D0_VL SD_D1_VL SD_D2_VL SD_D3_VL SD_CMD_VL SD_CLK_VL

P1V8 C115 100nF C116 100nF C117 1uF P3V3 R114 0 R127 4k7 SD_CD_VL SD_WP_VL R165 0 GND

* PCB and package delay skew for SD_D[0:3] and SD_CMD relative to SD_CLK must be between 50–200 ps [UG933].
* SI analysis for the SD_CLK line highly suggested
* Write Protect (WP) pulldown for linux driver compatibility
* SD_CMD pull-up not required but seen in MZ & ZC706

SoC POR (PB and PG VCCO_0)

* boot strap pins are sampled
* BootROM is executed

P3V3 R28 4k7 Mounted: No C309 100nF GND R164 4k7

PS_POR_N C89 100nF GND IC38B IC38A NC7WZ07P6X PS_POR_OR_N

Short trace between supervisory IC and Zynq SoC required.

P3V3 R278 4k7 C157 1nF GND IC76 SENSE RESET MR CT VDD GND TPS3808G33DBVT PB3 CHASSIS C155 100nF C156 100nF PHY_RST_N

POR reset deassertion delay time: 20 ms
2.6 ms RC for pushbutton
threshold voltage = 3.07V

SoC SRST (PB)

* boot strap pins are not sampled
* BootROM is executed
* debug environment is not disturbed

P3V3 R173 4k7 R167 4k7 R168 4k7 IC40B IC40A NC7WZ07P6X PS_SRST_OR_N

P3V3 R172 4k7 C285 1nF GND IC39 SENSE RESET MR CT VDD GND TPS3808G33DBVT PB1 C90 100nF C284 100nF C287 100nF

SRST reset deassertion delay time: 20 ms
2.6 ms RC for pushbutton
threshold voltage = 3.07V

QSPI at 3.3V

Net Class QSPI PCB Rule

IC87 IC32 S25FL128SAGMFI001: SCK SI/IO0 SO/IO1 WP/IO2 HOLD/IO3 CS RESET/RFU RFU NC VIO/RFU VCC VSS

QSPI0_SCLK QSPI0_DQ0 QSPI0_DQ1 QSPI0_DQ2 QSPI0_DQ3 QSPI0_CS

QSPI1_SCLK QSPI1_DQ0 QSPI1_DQ1 QSPI1_DQ2 QSPI1_DQ3 QSPI1_CS

P3V3 C320 100nF C351 100nF GND

SW2 SW3 R148 20k R159 20k MIO-4 MIO-5

SPI bus level translator

IC89 SN74AVC4T245PW: 1DIR 2DIR 1OE 2OE 1A1 1A2 2A1 2A2 1B1 1B2 2B1 2B2 VCCA GND VCCB GND

SPI_MISO C470 100nF C471 100nF P1V8 P3V3 GND

IC88 SN74AVC4T245PW: SPI_SCLK SPI_MOSI SPI_SS0 SPI_SS1 C468 100nF C469 100nF

I2C PMBus level translator

Pull-up to P1V8, bank 500's vcco!

P1V8 P3V3 R230 4k7 R231 4k7 R249 4k7 R252 4k7 IC70 TCA9517DGKR: SDAA SCLA SDAB SCLB EN VCCA VCCB GND

I2C_PMBus_d I2C_PMBus_clk I2C_PMBus_d_hv I2C_PMBus_clk_hv C133 100nF C134 100nF

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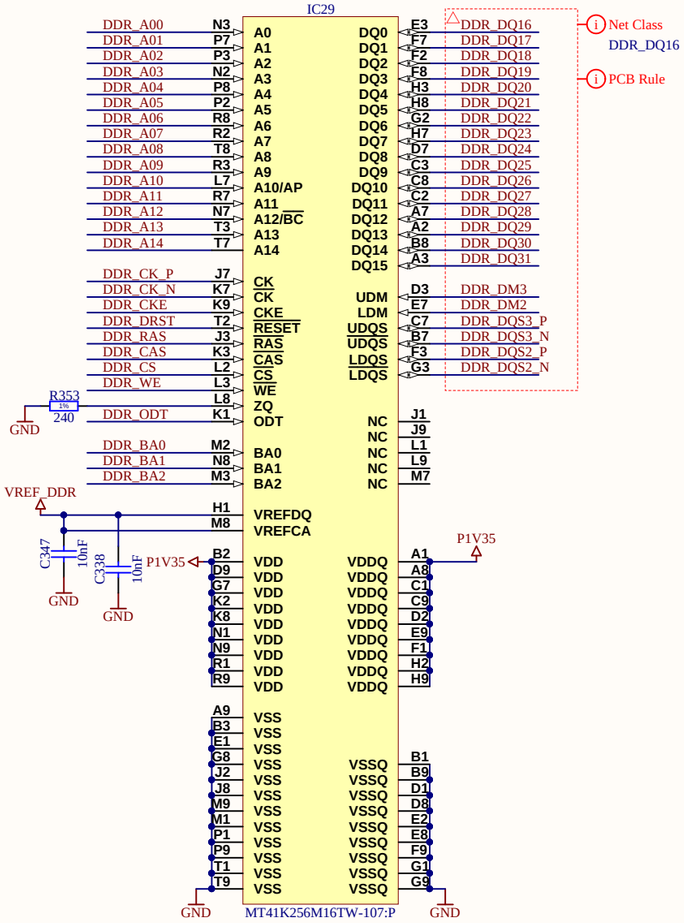
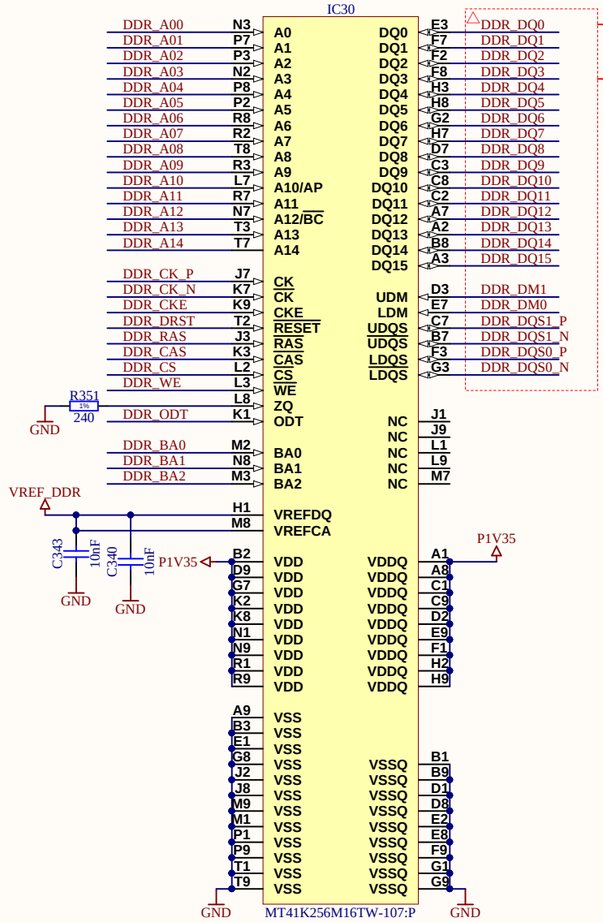
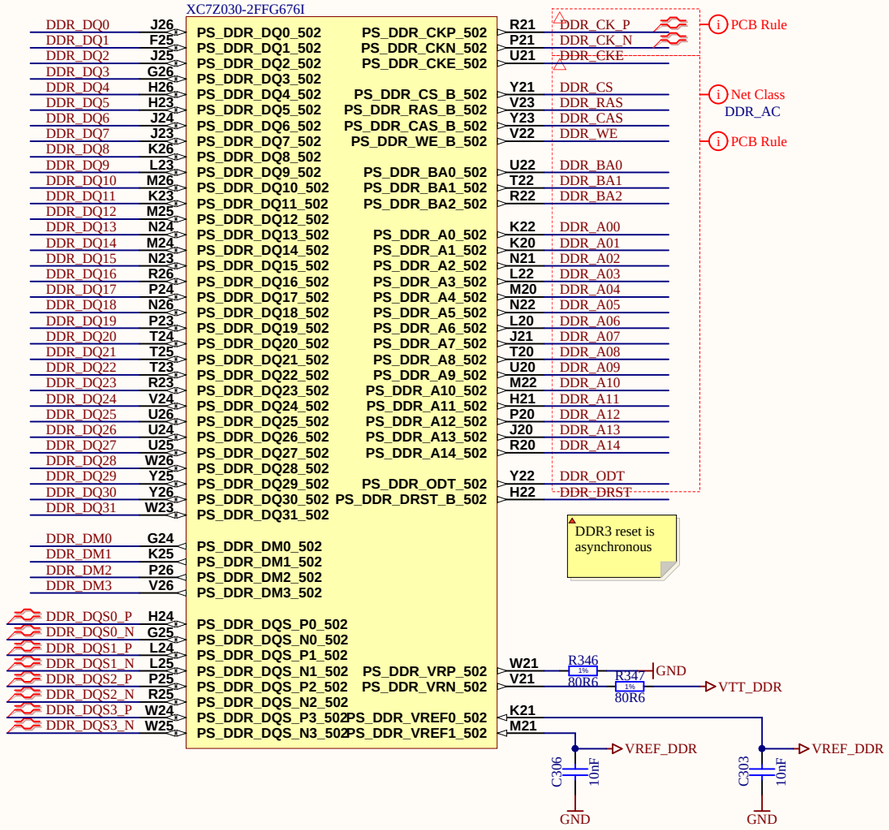
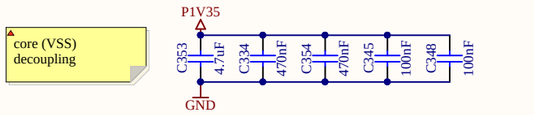
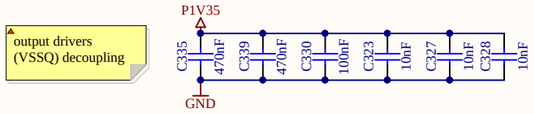
	Project: CITY			
	Sheet: Zynq SoC - Bank 500 & 501	Rev. 0	Date 05/2019	Author broquet
	File: CITY_Soc_bank500-501.SchDoc	SVN: 9e52f5b42aef8146190977f77afa5		



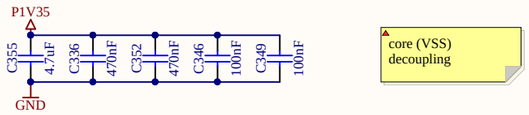


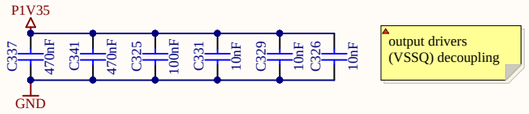


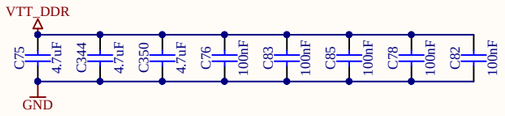


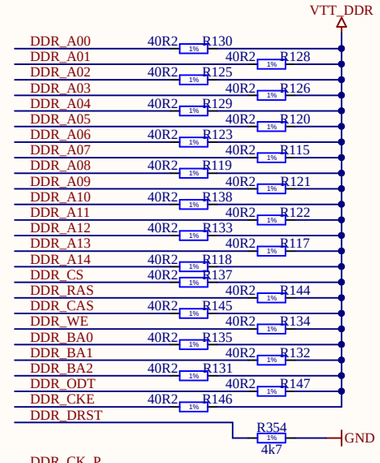


* Use separate vias for VSS and VSSQ as well as for VDD and VDDQ.
* No traces for VDD(Q) and VSS(Q), only planes; vias should have 8 mils traces [TN-46-14]
* For capacitor & terminating resistor placement, see Fig. 3, page 9 in Micrel TN-41-13 _and_ Fig. 4, page 6 in Micrel TN-46-14.
* Trace spacing constraints in Micrel TN-46-14 Table 1 (p. 8).
* VTT decoupling to be placed close to the terminated signals









* DDR3 trace lengths must include Zynq package flight time (generated in ISE using partgen -v xc7z030ffg676-2), see Documentation folder in this project.
* For DDR_AC, trace impedance should be 40 Ohms for single ended and 80 Ohms for differential signals; 50/100 Ohms is allowed if 40/80 is not achievable.
* For the DDR_DQ and DDR_DQS signals, On-Die Termination (ODT) is used and can be set to 40 or 60 Ohm (single ended) - one of these values has to be used for ALL traces.
* The two DDR3 devices should be routed and terminated in fly-by architecture, see Micrel TN-41-13 p. 20. Termination resistors should be placed past the last memory device.

Add following rules:
* 100 mil max skew between DDR_DQ and DDR_DQS
* DDR_AC hard to constrain, see [88AP510 p. 56]

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Project: CITY
Sheet: Zynq SoC - Bank 502 (DDR3L)
File: CITY_Soc_bank502_DDR.SchDoc

Rev.	Date	Author
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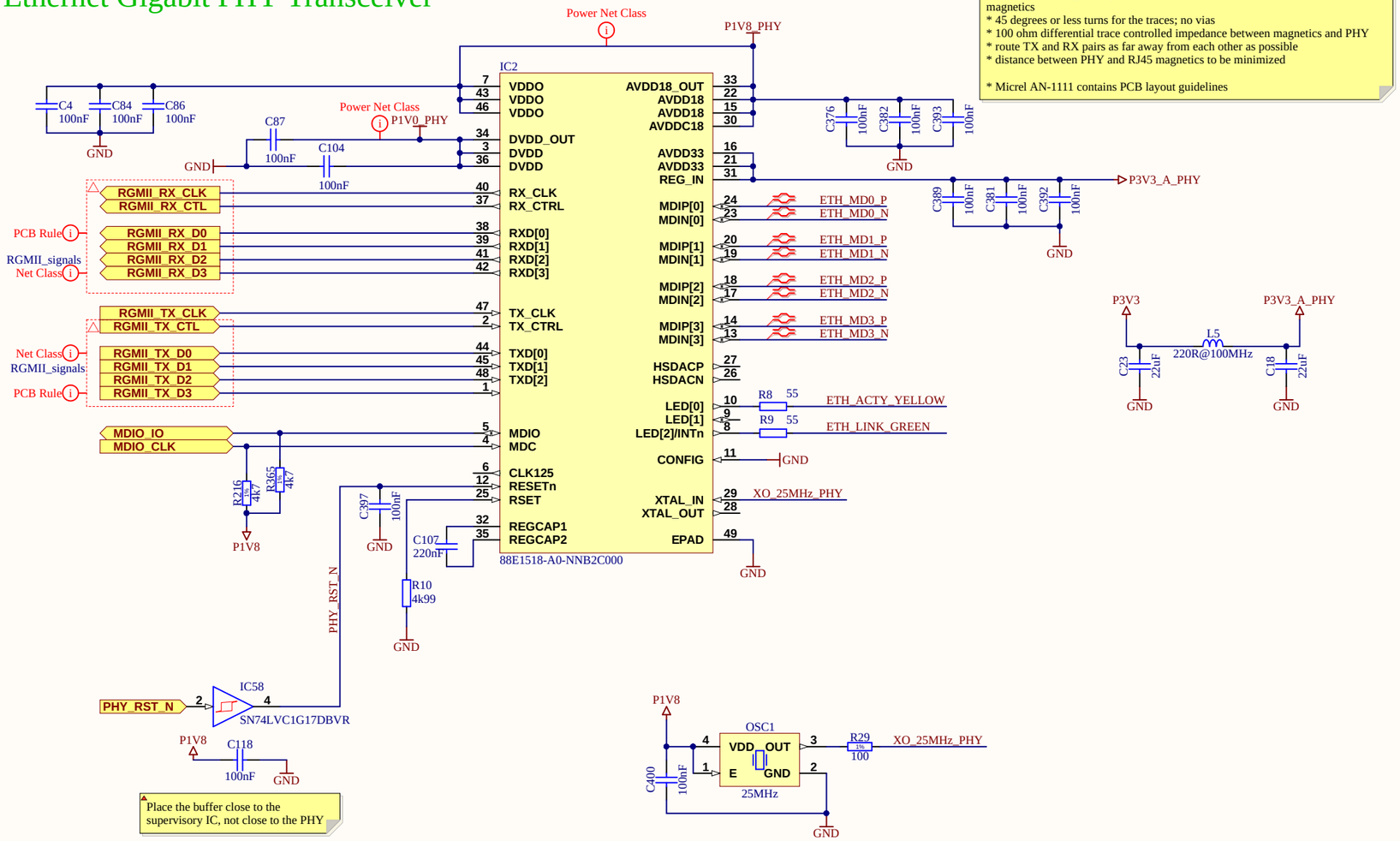
SVN: 89f9589d8aaca0a25e422de51e6

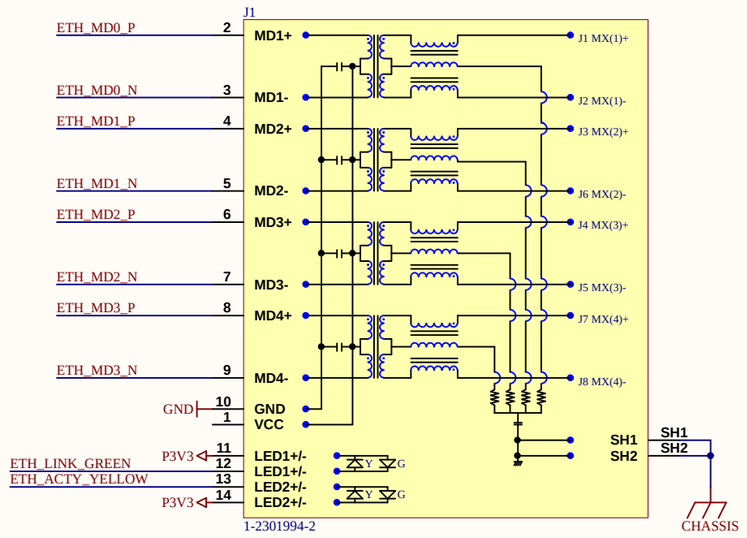
Ethernet Gigabit PHY Transceiver



* void power and ground planes on all layers underneath the RJ45 connector and magnetics
* 45 degrees or less turns for the traces; no vias
* 100 ohm differential trace controlled impedance between magnetics and PHY
* route TX and RX pairs as far away from each other as possible
* distance between PHY and RJ45 magnetics to be minimized

* Micrel AN-1111 contains PCB layout guidelines

Ethernet RJ45 connector

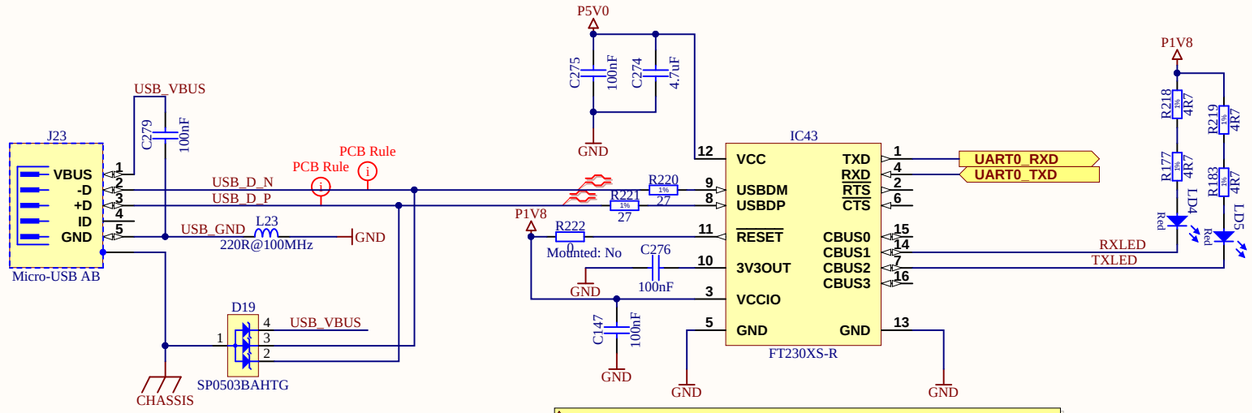


LED status (Marvell datasheet)

By default (HW reset), MODE3 dual LED is used:
LED1: OFF
LED0: OFF <=> No Link
LED0: ON <=> 1000Mbps Link / No activity
LED0: BLINK <=> 1000Mbps Link / Activity

LED2: ON <=> Link
LED2: OFF <=> No Link

USB UART



* void power and ground planes on all layers underneath the USB connector
* 45 degrees or less turns for the traces; no vias
* place chip as close as possible to the USB connector
* 90 ohms differential trace controlled impedance between connector and FT232

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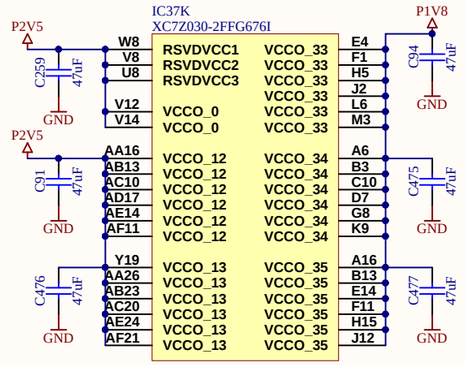
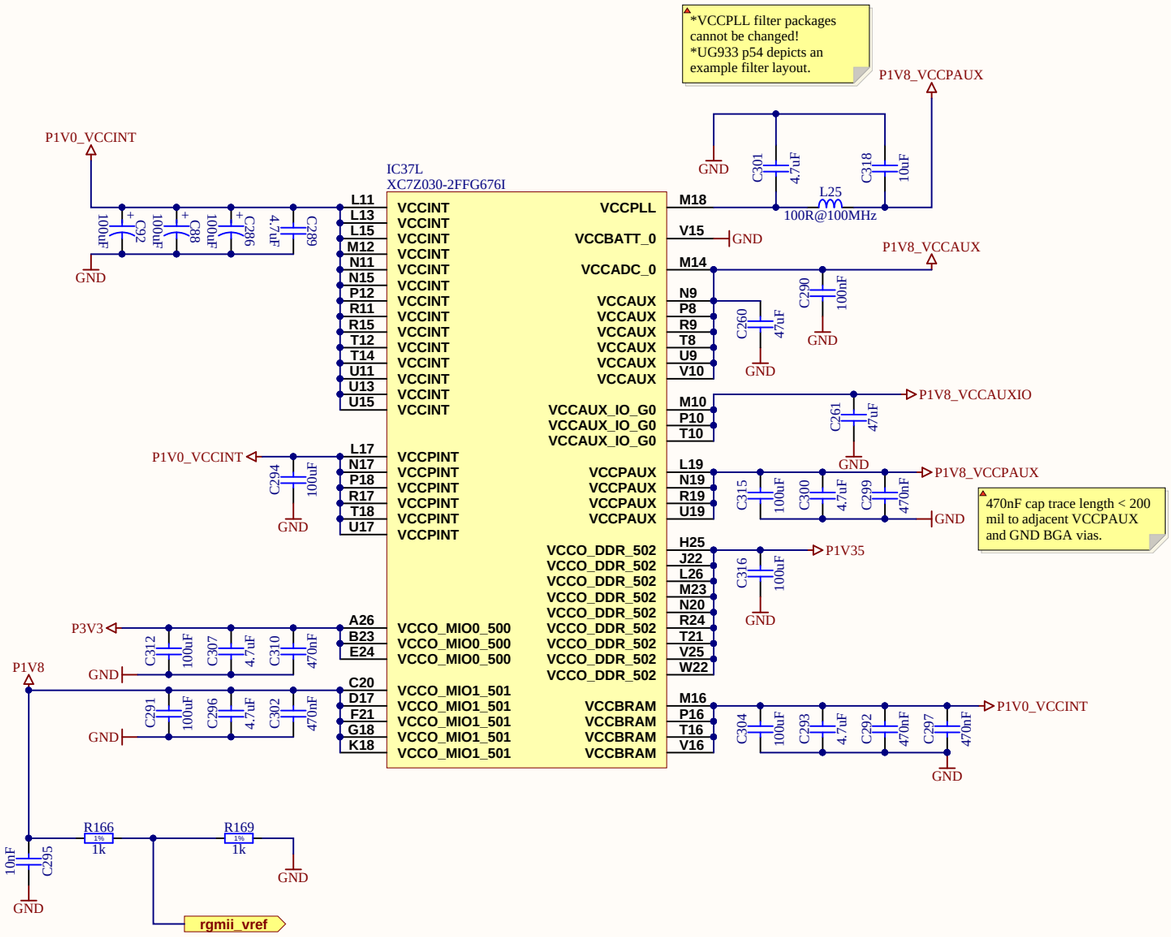
Project: CITY
Sheet: Ethernet, UART
File: CITY_Soc_Ethernet_UART.SchDoc

Rev.	Date	Author
0	05/2019	broquet

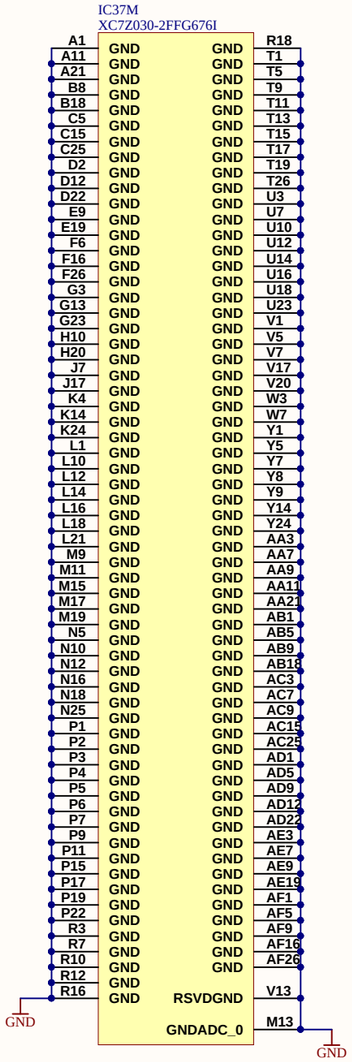
SVN: 0b7dfecaa4df95dd84a6b3f094c4

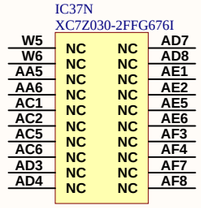




*VCCPLL filter packages cannot be changed!
*UG933 p54 depicts an example filter layout.

470nF cap trace length < 200 mil to adjacent VCCPAUX and GND BGA vias.





testpoints for probe, divide over the board

TP1
TP2
TP3
GND

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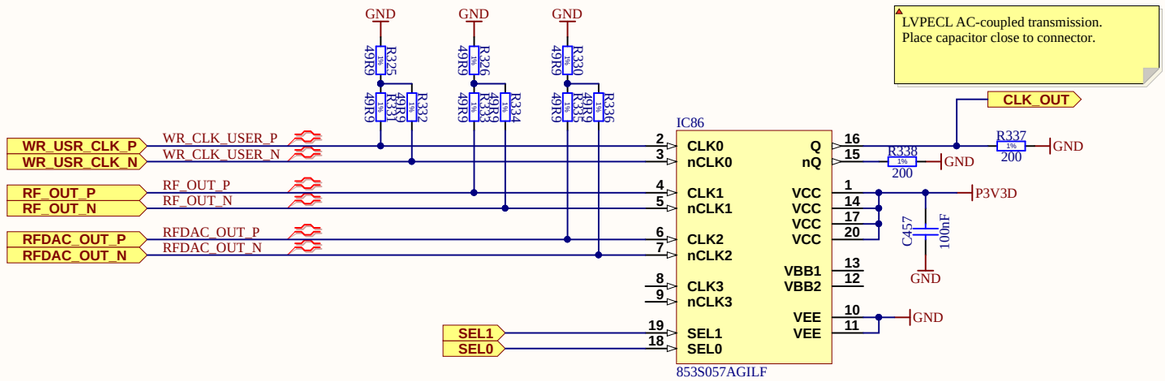
Project: CITY			
Sheet: Zynq SoC - Power	Rev. 0	Date 05/2019	Author broquet
File: CITY_Soc_power.SchDoc	SVN: 89f9589d8aaca0a25e422de51e6		



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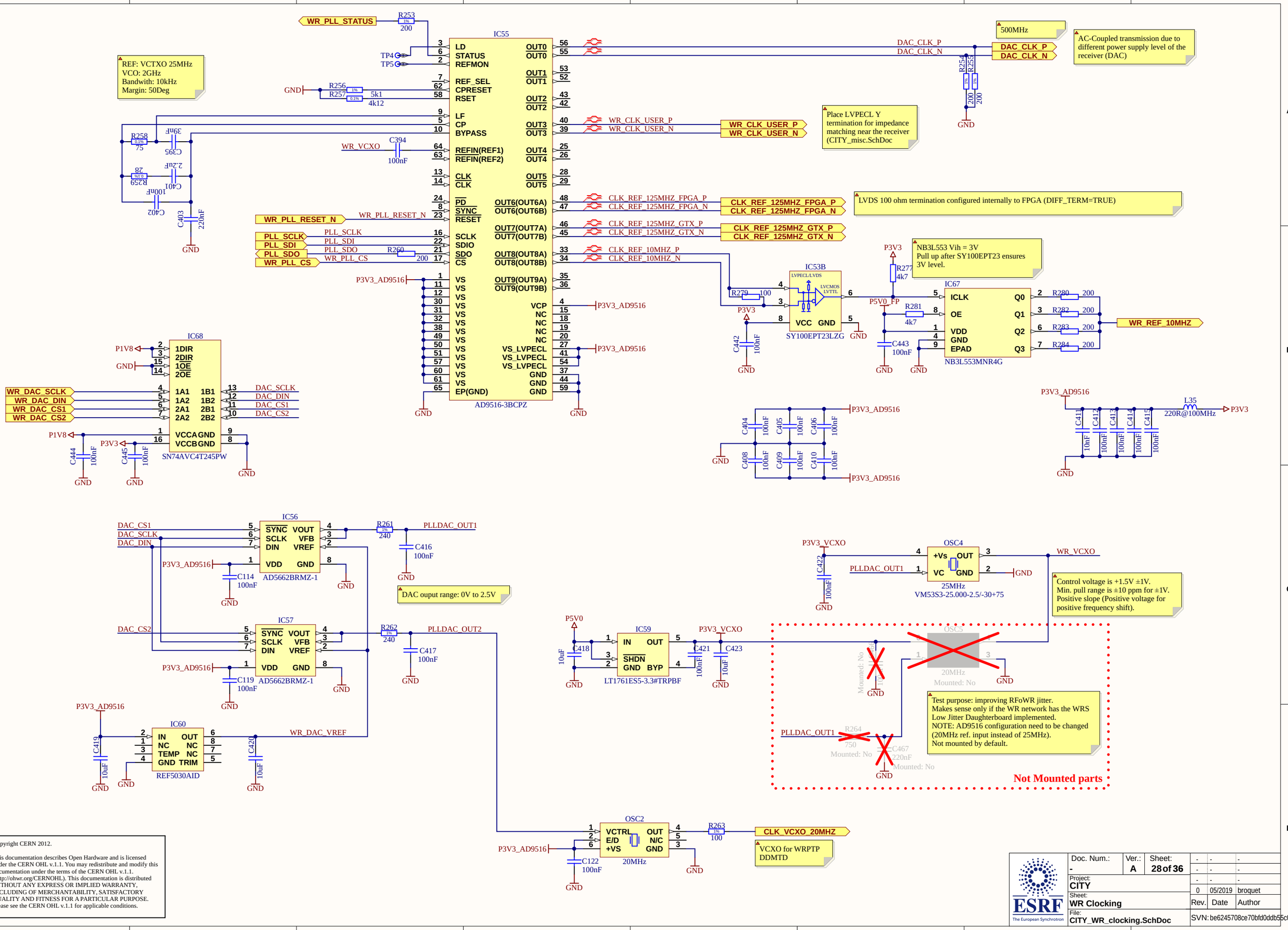
	Project: CITY		
	Sheet: User Clock	Rev. 0	Date 05/2019 Author broquet
	File: CITY_user_clock.SchDoc	SVN: 89f9589d8aaca0a25e422de51e6	



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	Sheet: WR Clocking			0 05/2019 broquet	
	File: CITY_WR_clocking.SchDoc			Rev. Date Author	
				SVN: be6245708ce70bfd0ddb55c0ab	