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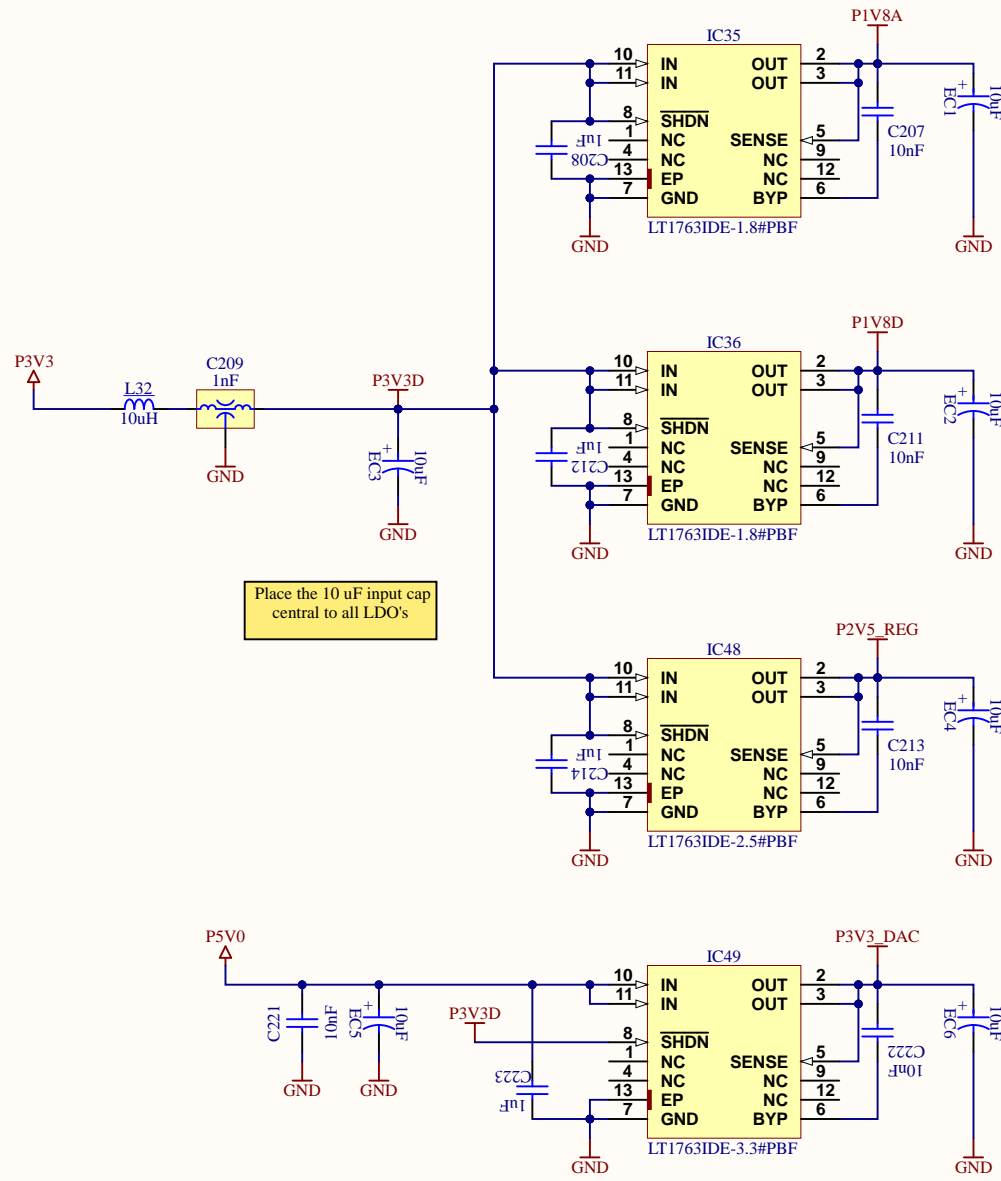
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	Doc. Num.:	Ver.:	Sheet:	
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	Project:	CITY		
	Sheet:	DDS Phase Detector		
File:	CITY_DDS_phase_detector.SchDoc	Rev.:	Date:	Author:

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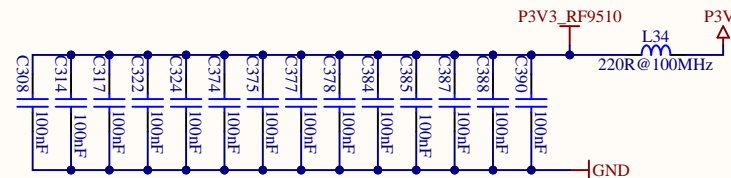
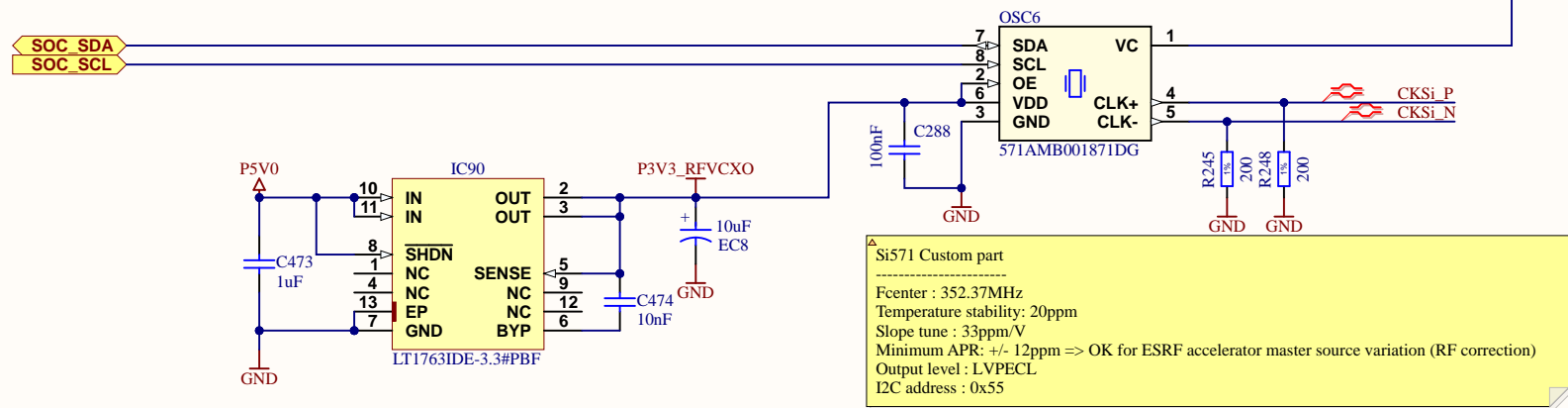
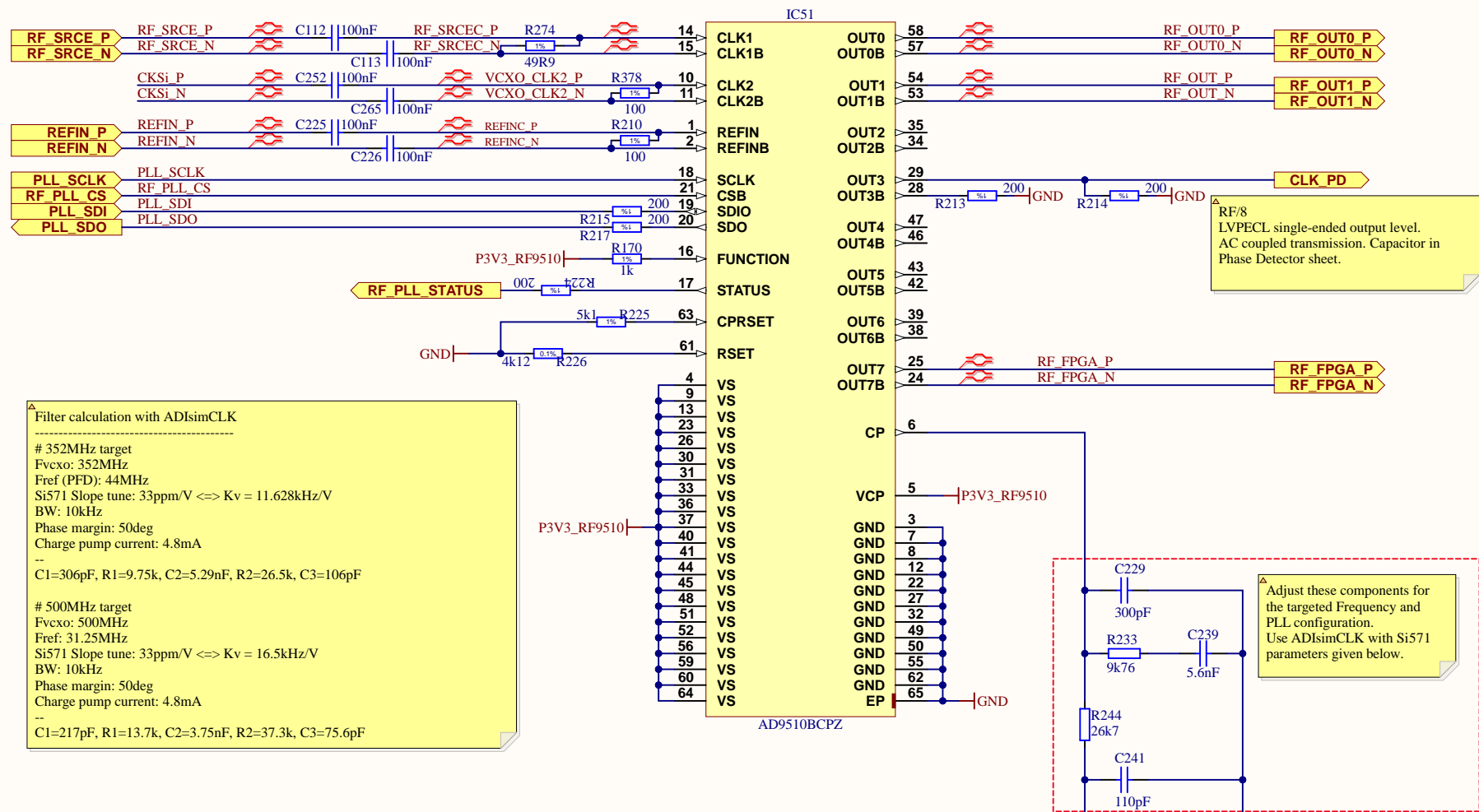
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		Rev.	Date	Author		




Place the 10 uF input cap central to all LDO's

Place all LT1763's on 100 mm^2 (min) pour. Device pad should have multiple (>6) 0.5 mm vias connecting to all ground planes, and be soldered to pour

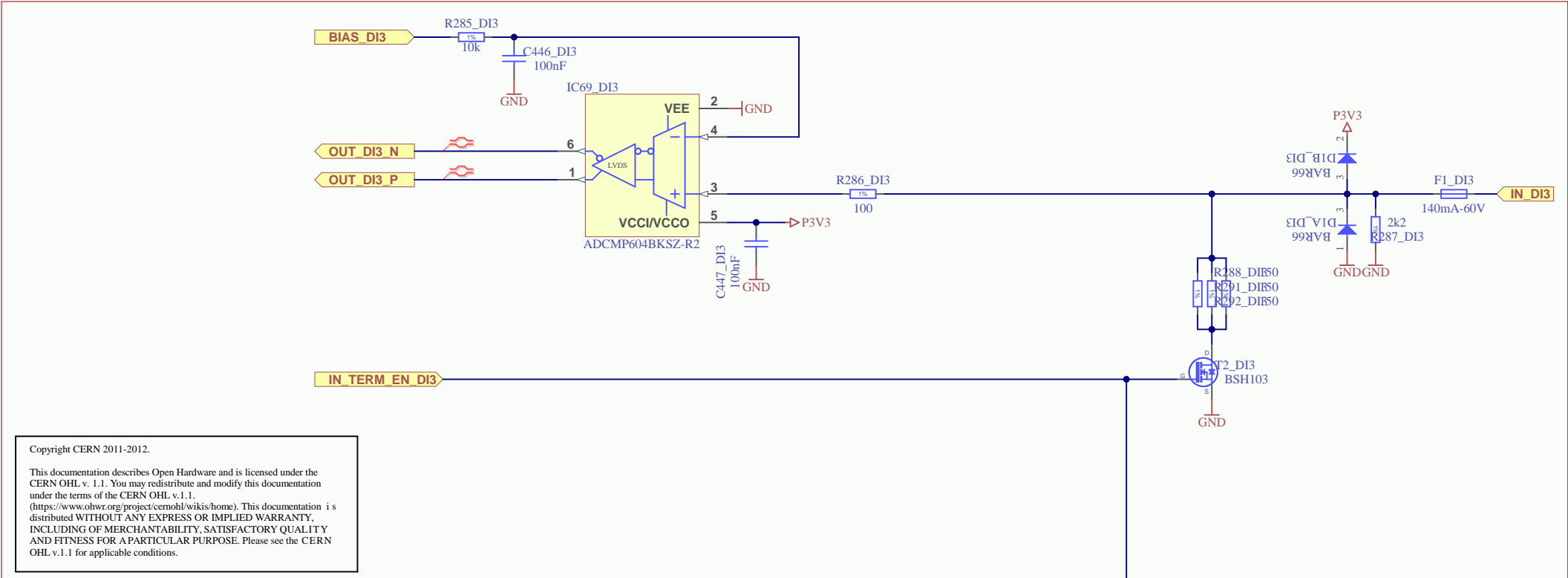


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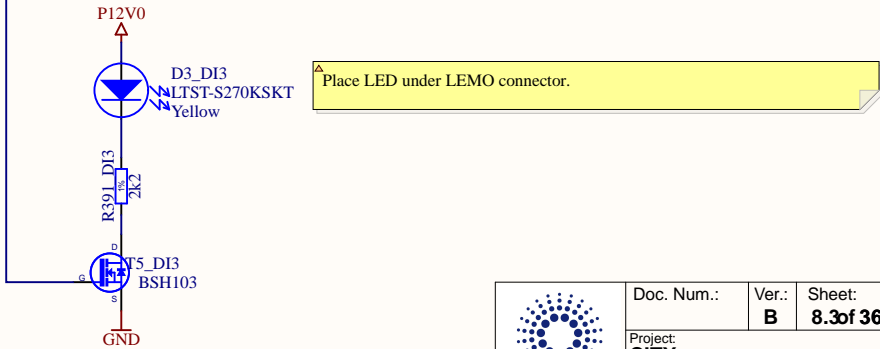
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	File:	CITY_DDS_RF_clocking.SchDoc				
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						broquet
				SVN:		







Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0





**A**

**A**

B

E

C

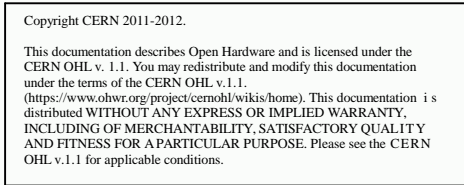
C

D

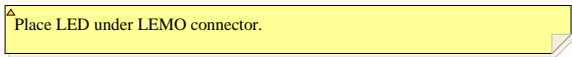
□

E

E

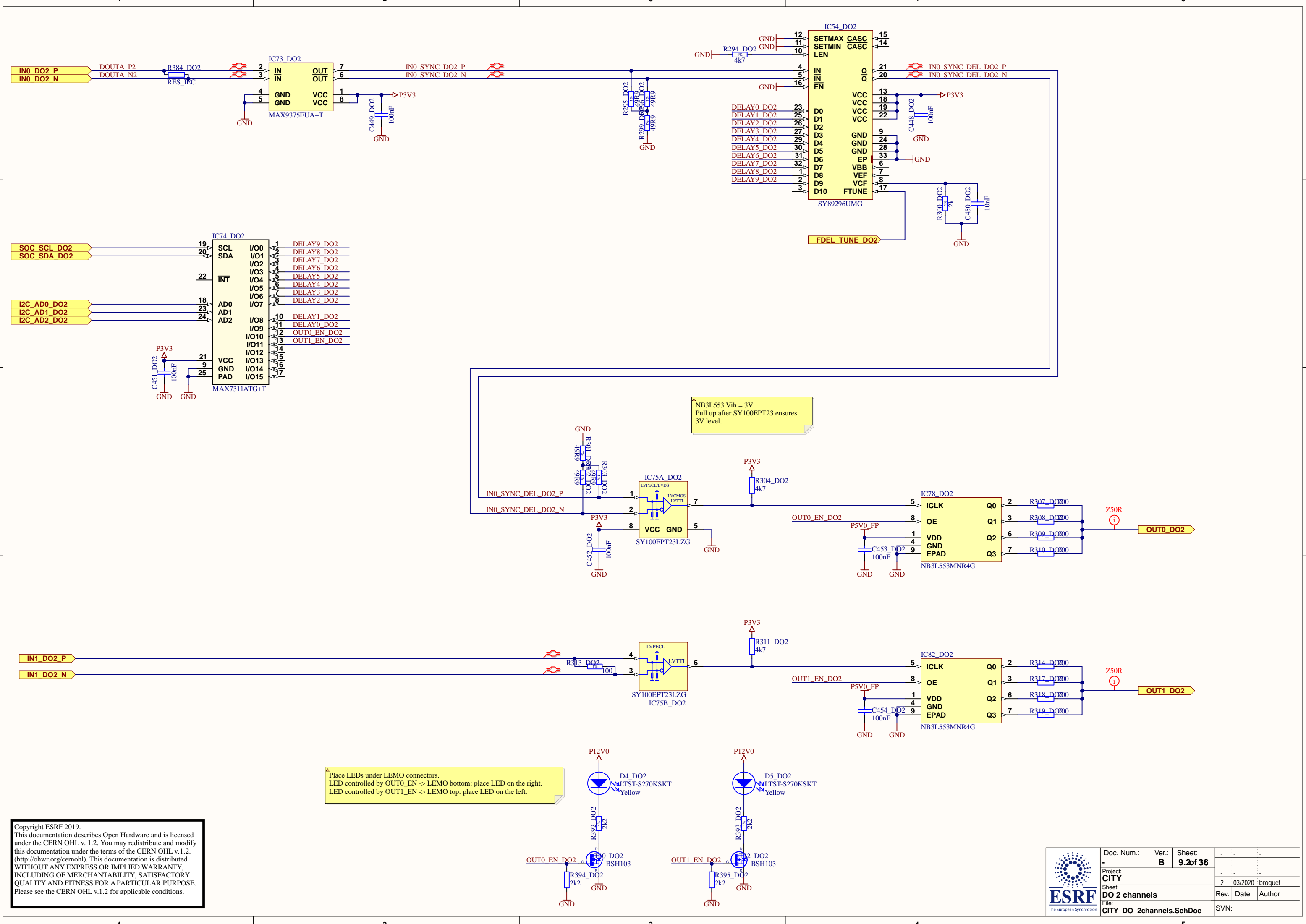


Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0




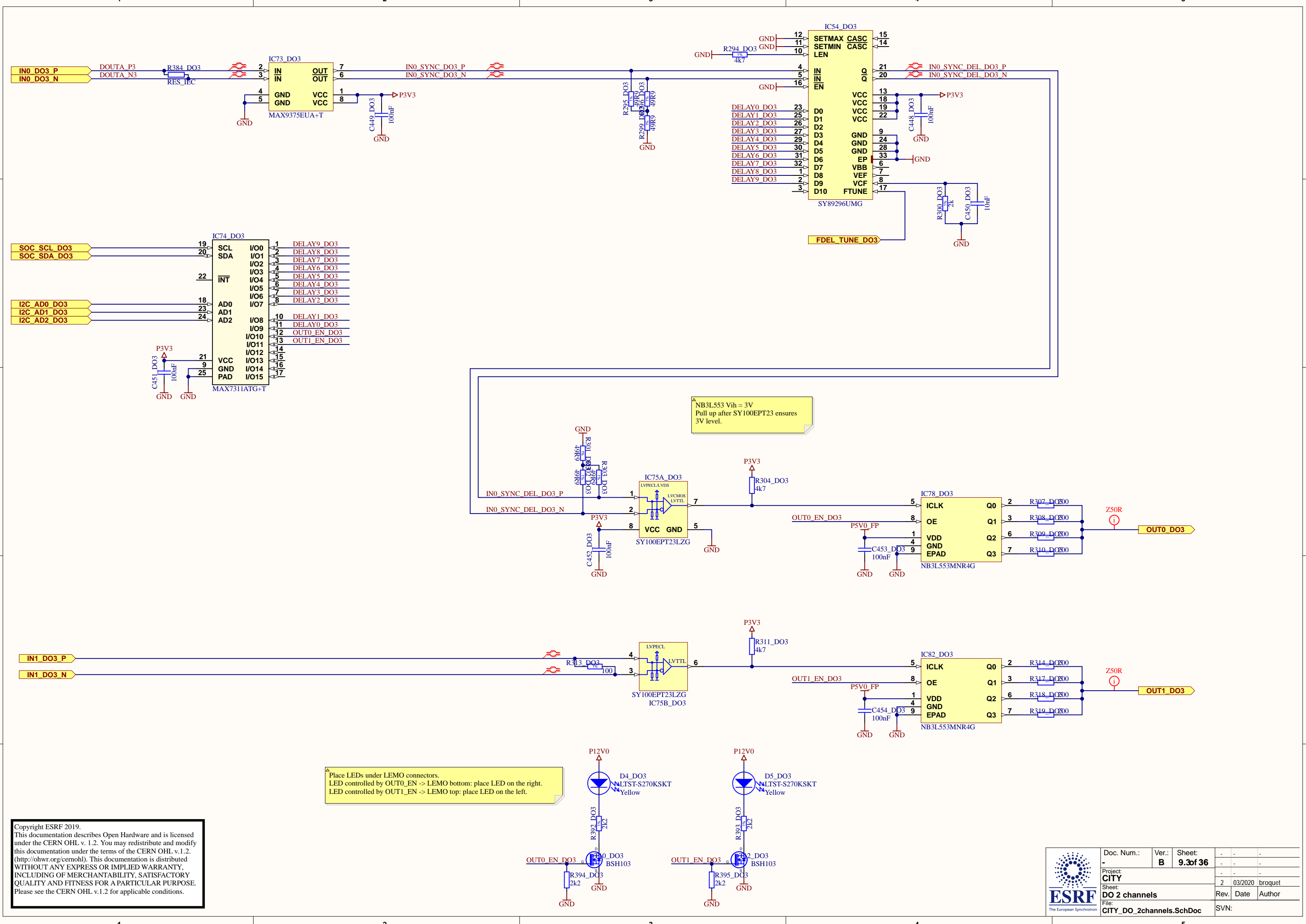
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Project: <b>CITY</b>					
Sheet: <b>DI 2 channels</b>			2	03/2020	broquet
File: <b>CITY_DI_1channel_SchDoc</b>			Rev.	Date	Author
			SVN:		






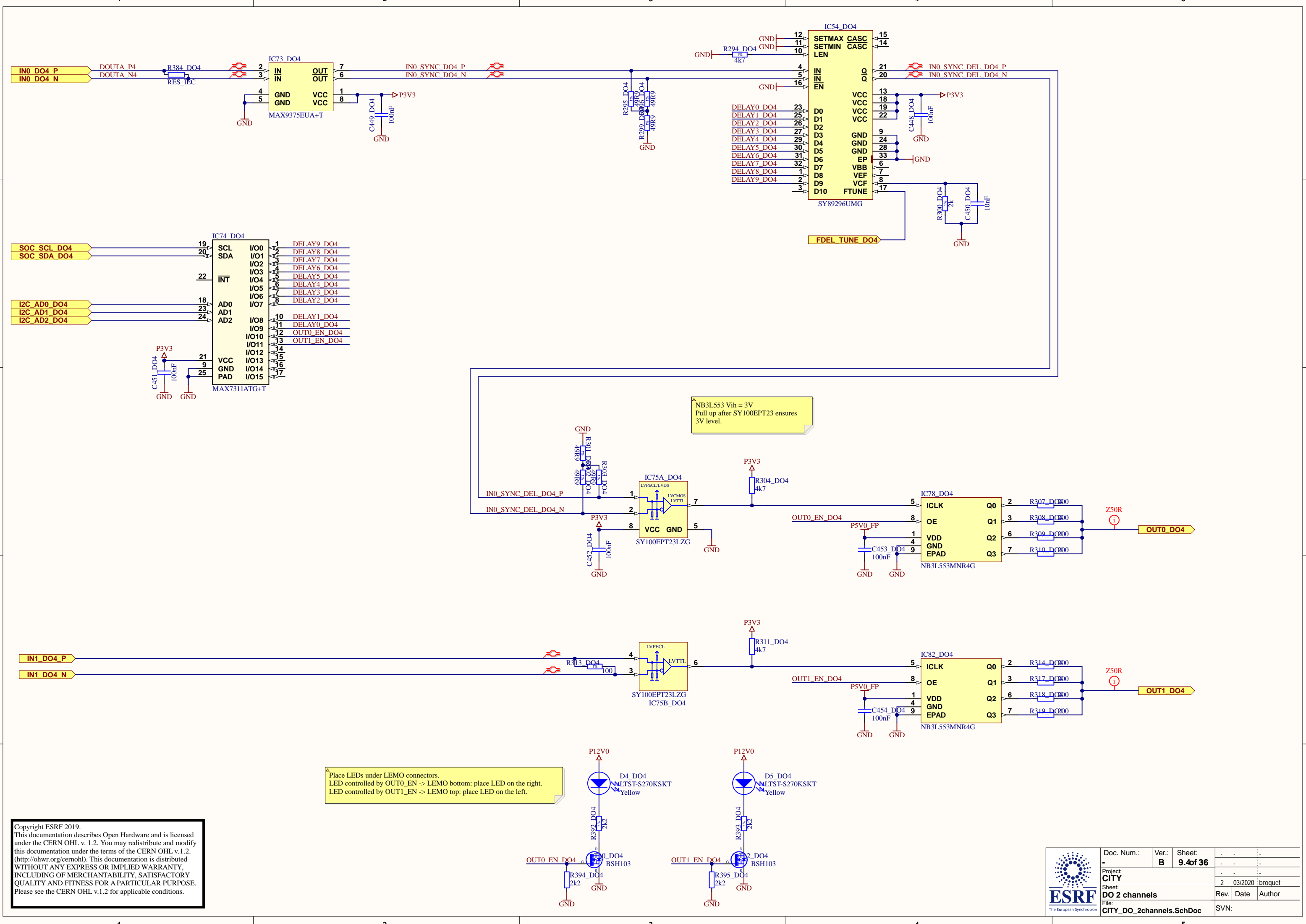
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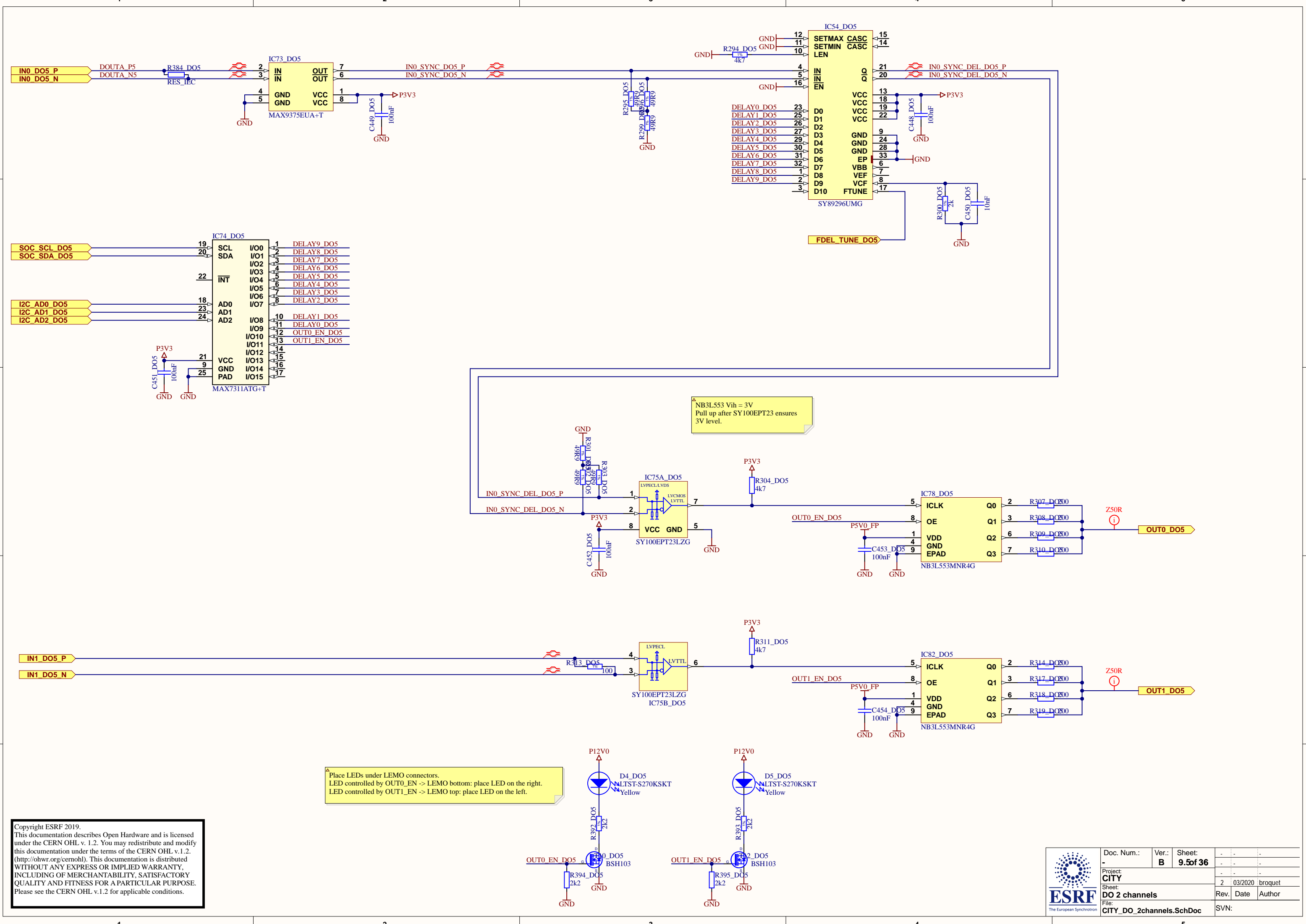


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Place LEDs under LEMO connectors.  
LED controlled by OUT0\_EN -> LEMO bottom: place LED on the right.  
LED controlled by OUT1\_EN -> LEMO top: place LED on the left.

NB3L553 Vih = 3V  
Pull up after SY100EPT23 ensures 3V level.

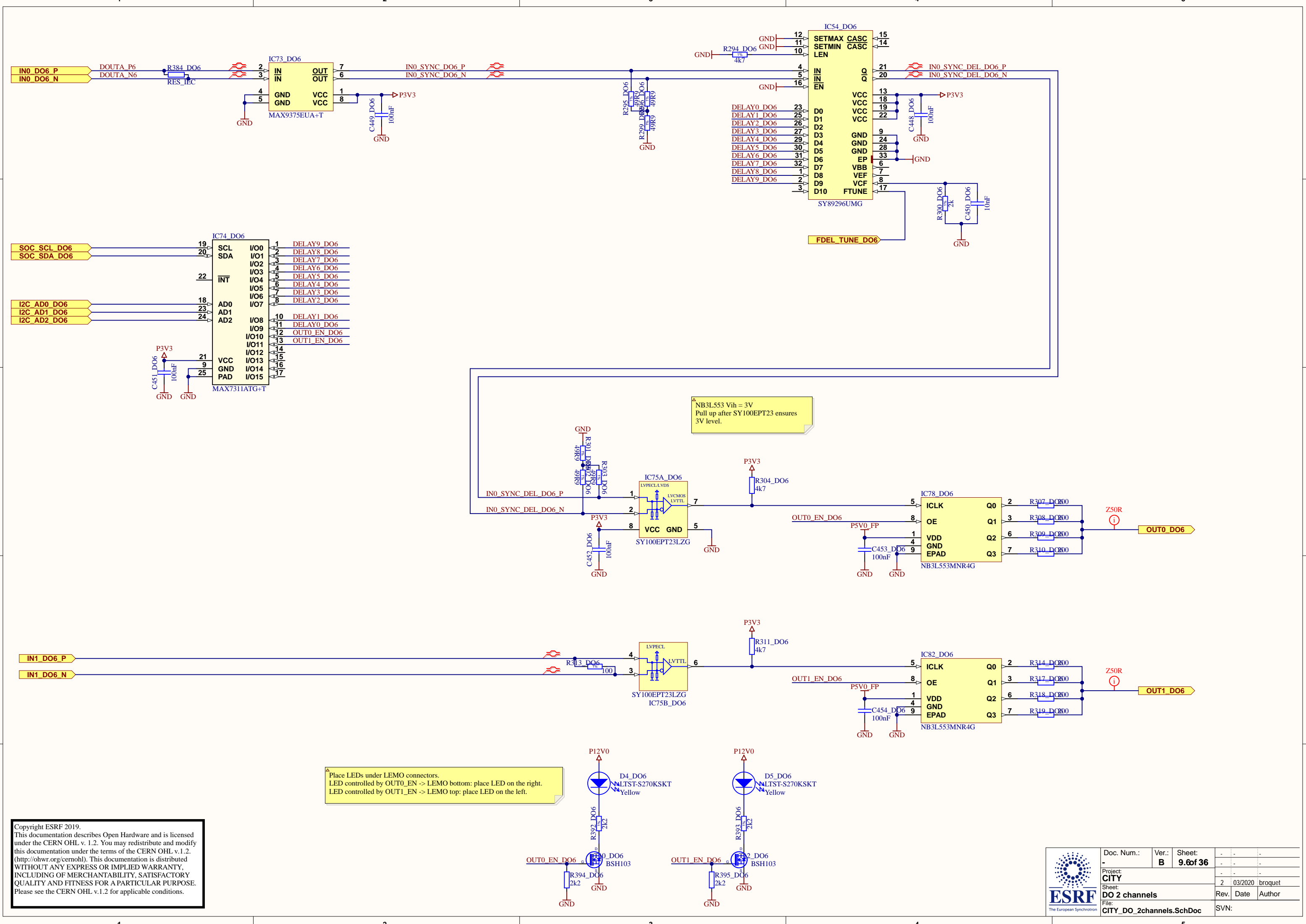
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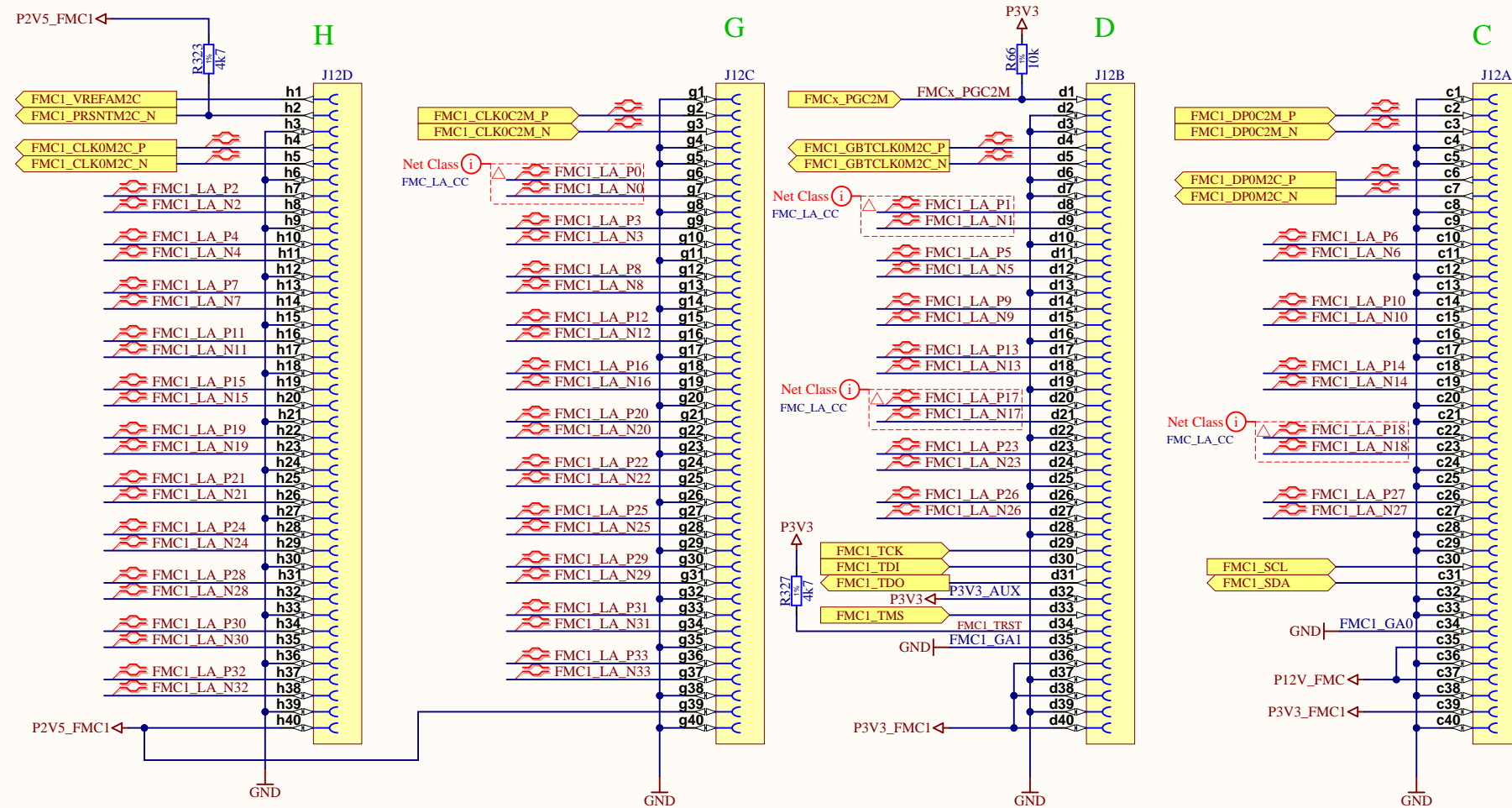
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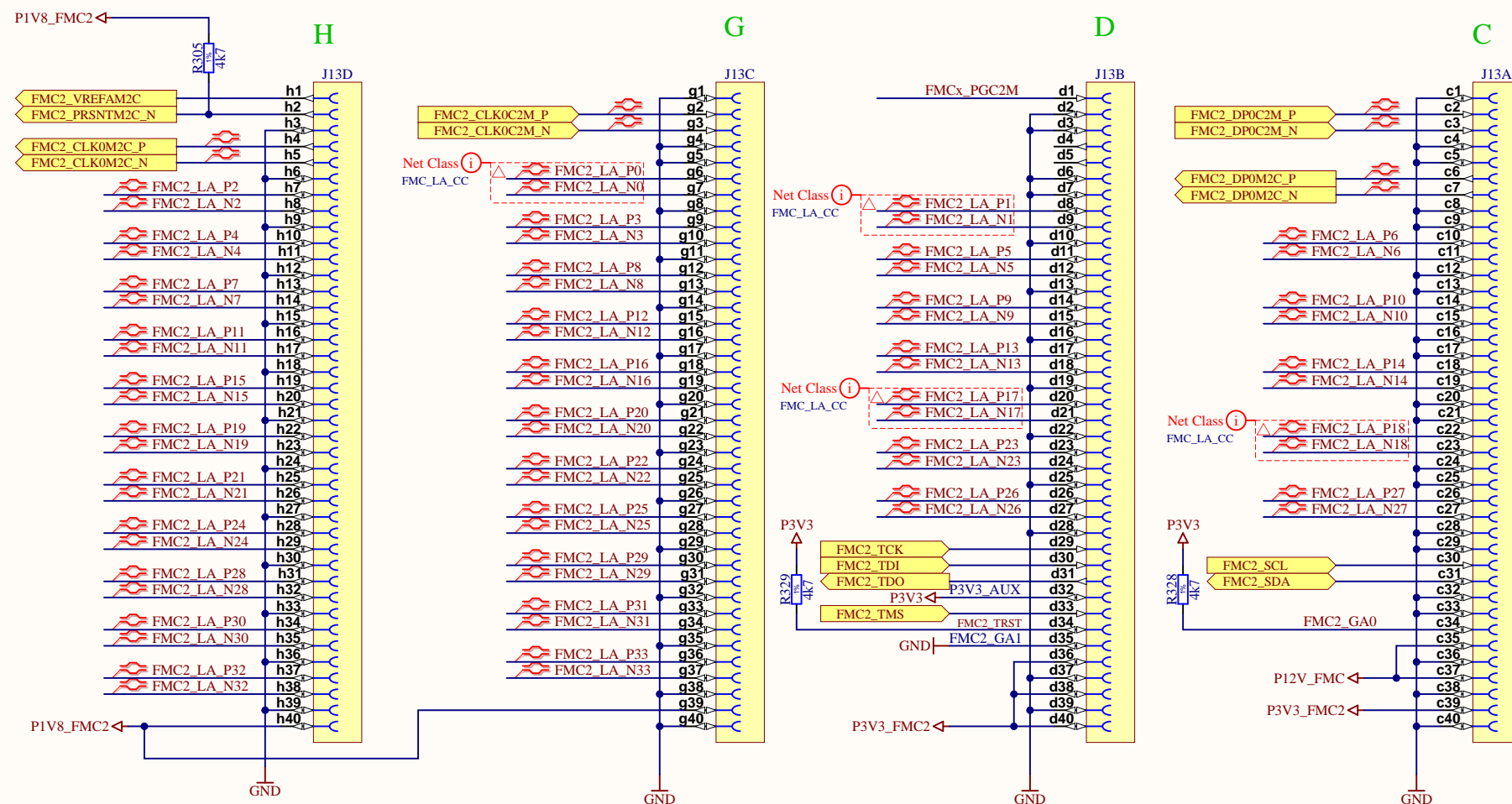
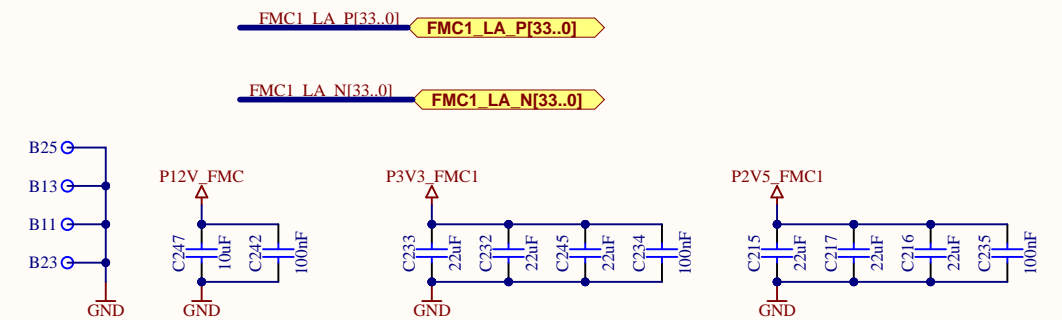
VADJ = 2.5V  
GA = '00'

ANSI/VITA 57.1:  
For all differential pairs:  
Recommendation 5.3: When signals are routed differentially each pair should provide a differential impedance of  $100\Omega \pm 10\%$

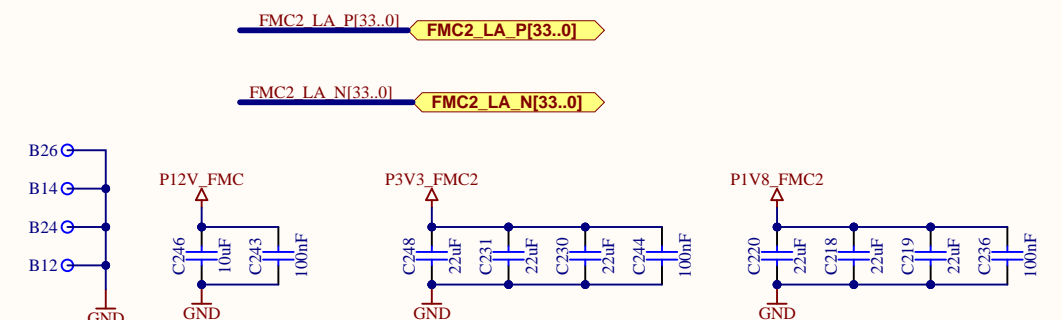
For FMCx\_CLK0M2C and FMCx\_CLK0C2M pairs:  
Rule 5.22: Clock traces shall provide a differential impedance of  $100\Omega \pm 10\%$   
Rule 5.23: The differential length mismatch on each differential clock pair shall be a maximum 11ps.

For the FMCx\_DP0 pairs:  
Rule 5.43: The differential length mismatch on each differential data pair shall 1ps.

For the FMCx\_GBTCLK0M2C pairs:  
Rule 5.48: Clock traces shall provide a differential impedance of  $100\Omega \pm 10\%$   
Rule 5.49: The differential length mismatch on each differential clock pair shall 11ps.



VADJ = 1.8V  
GA = '01'



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## A



**D**

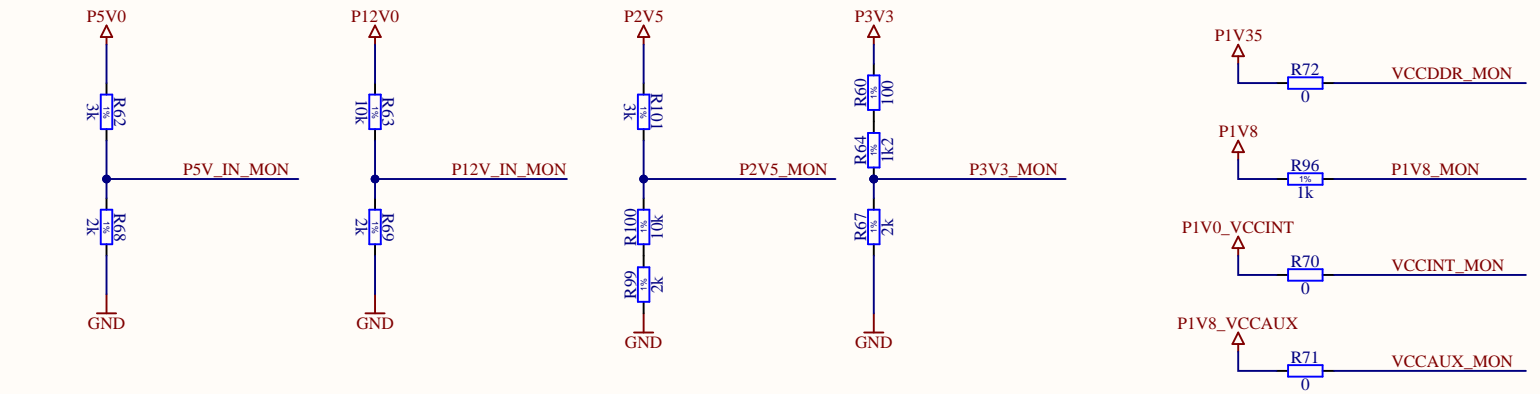
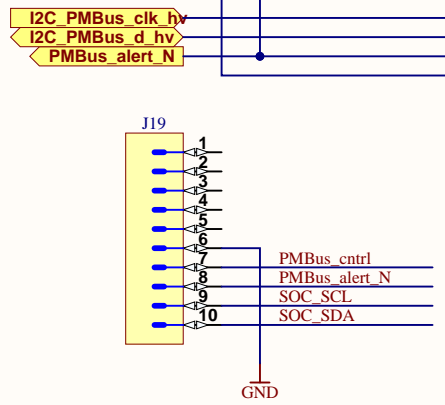
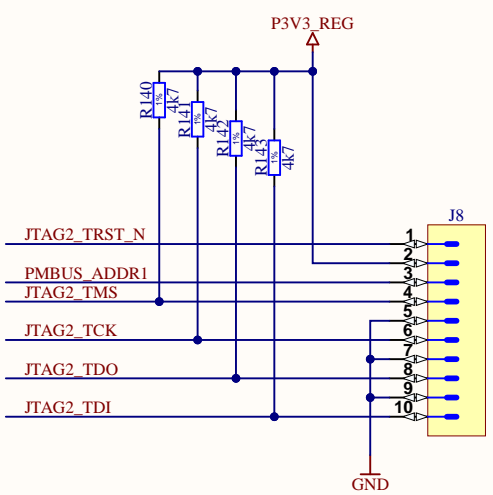
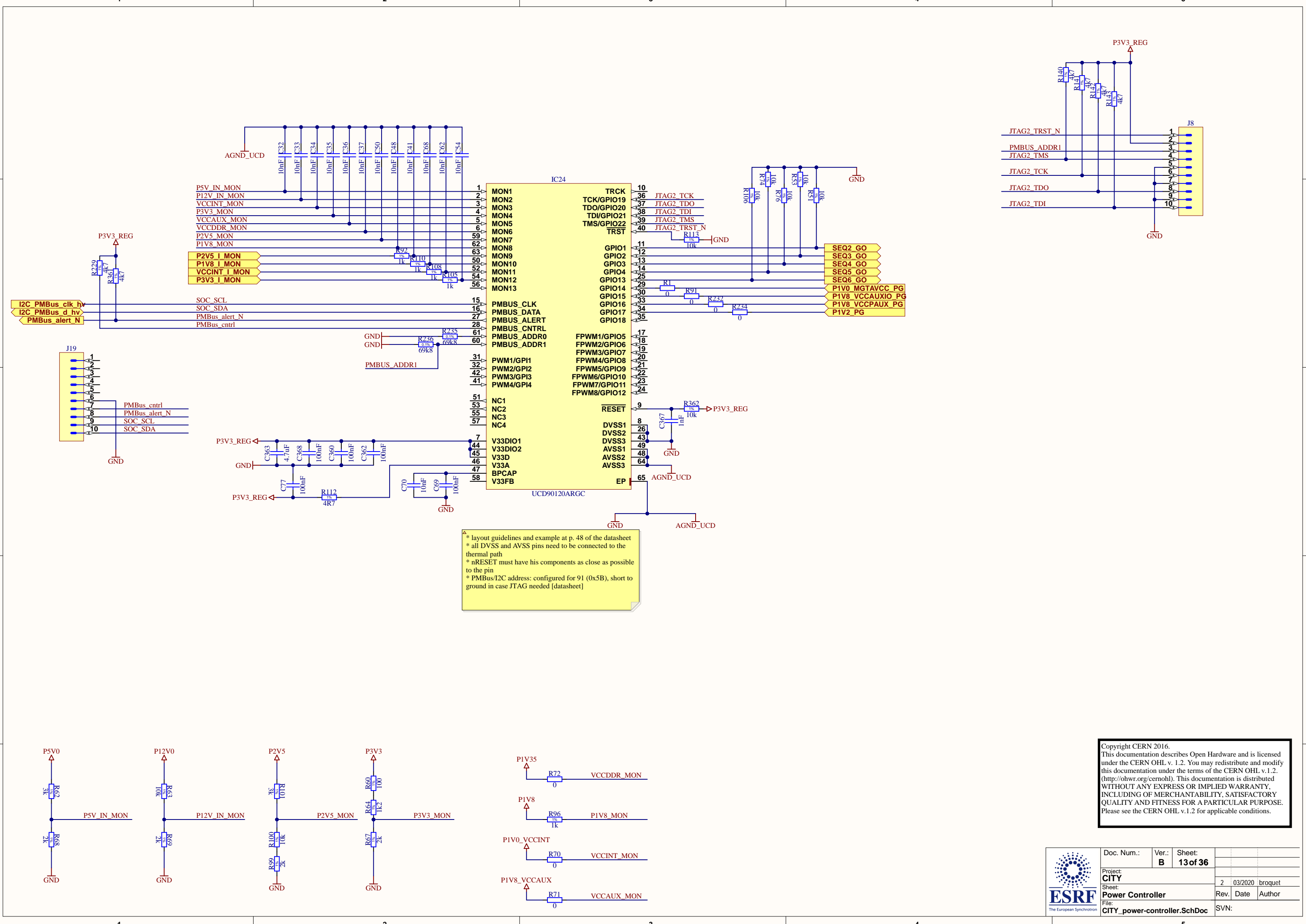


## 2








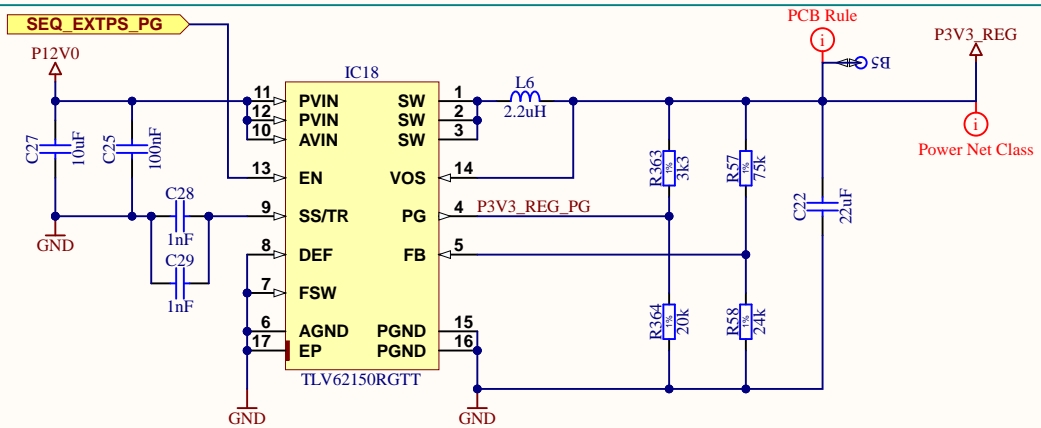


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 <b>ESRF</b> The European Synchrotron	Doc. Num.:	Ver.:	Sheet:				
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	Project:	CITY					
	Sheet:	Power Controller			2	03/2020	broquet
	File:	CITY_power-controller.SchDoc			Rev.	Date	Author
				SVN:			



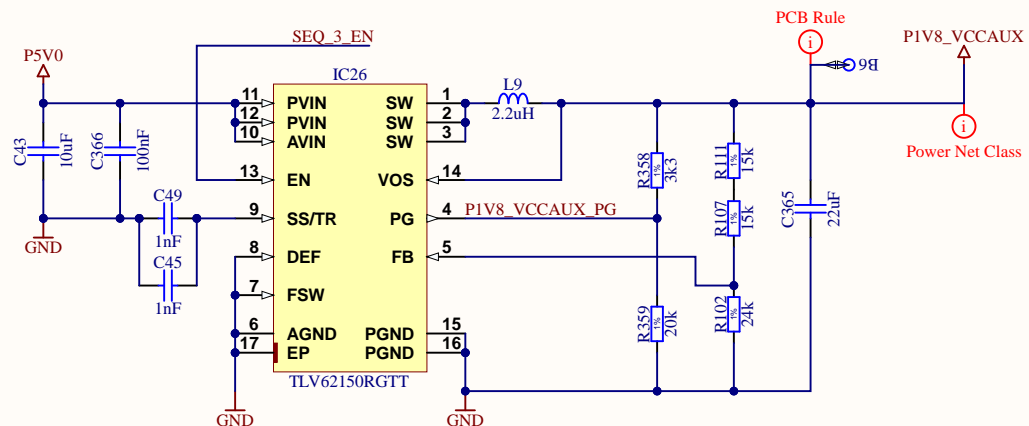




### 3.3V VREG (1A)

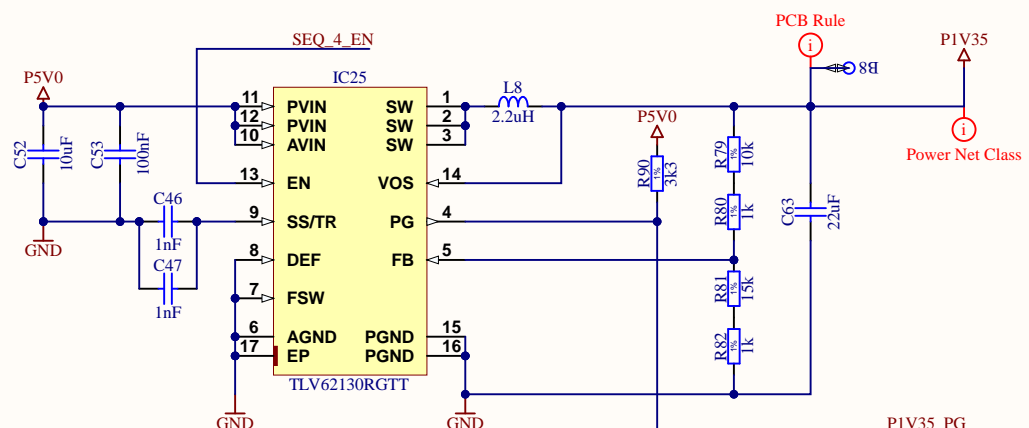
- \*fsw = 2.5 MHz
- \*layout example at datasheet p.21
- \*100nF directly across the AVIN and AGND pins
- \* Not only used for the LDOs at this page!

Fabrication Testpoint Usage [Testpoint - One Required    Multiple - Not Allowed]



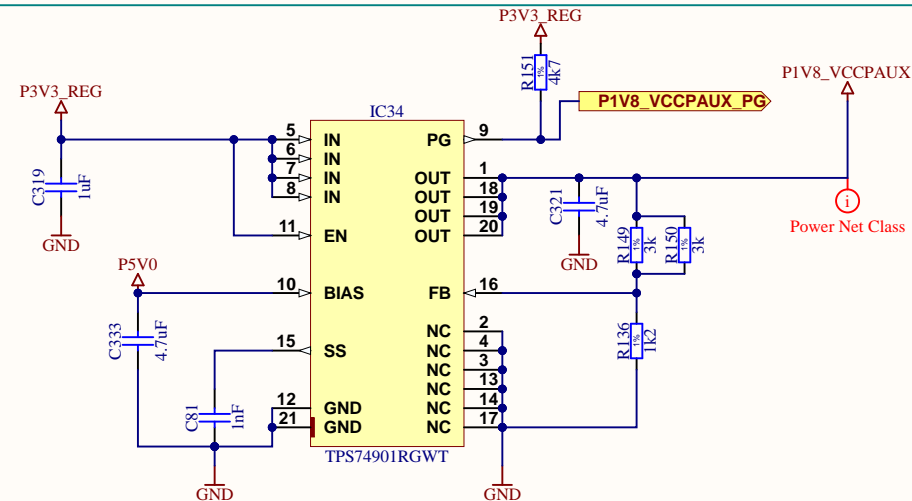
1.8V VCCAUX (800mA)

- \*fsw = 2.5 MHz
- \*layout example at datasheet p.21
- \*100nF directly across the AVIN and AGND pins



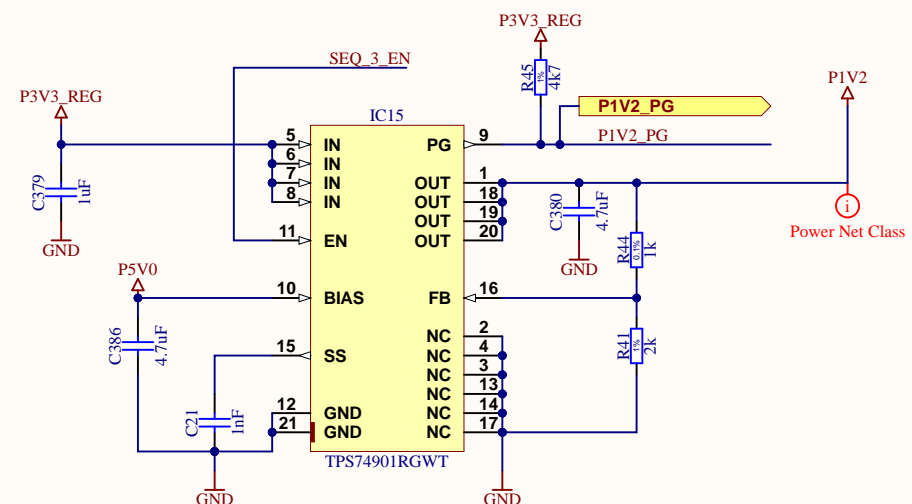
1.35V VCCDDR (1.1A)

- \*fsw = 2.5 MHz
- \*layout example at datasheet p.22
- \*100nF directly across the AVIN and AGND pins



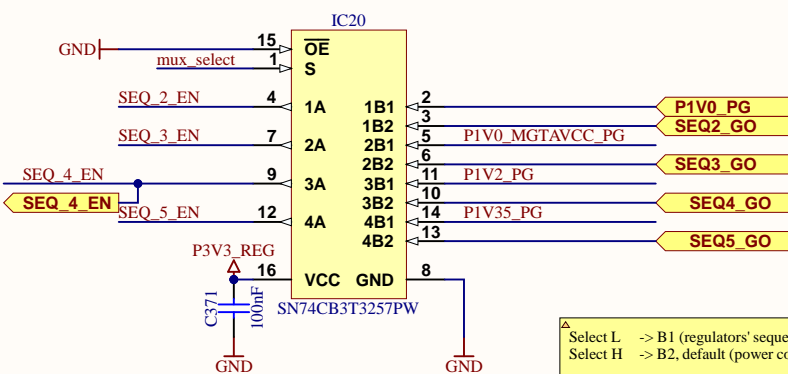
1.8V VCCPAUX (120mA linear)

\*layout example at datasheet p.20  
\*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; only 180 mW dissipation with a  $\theta_{JA}$  of 120 °C/W.

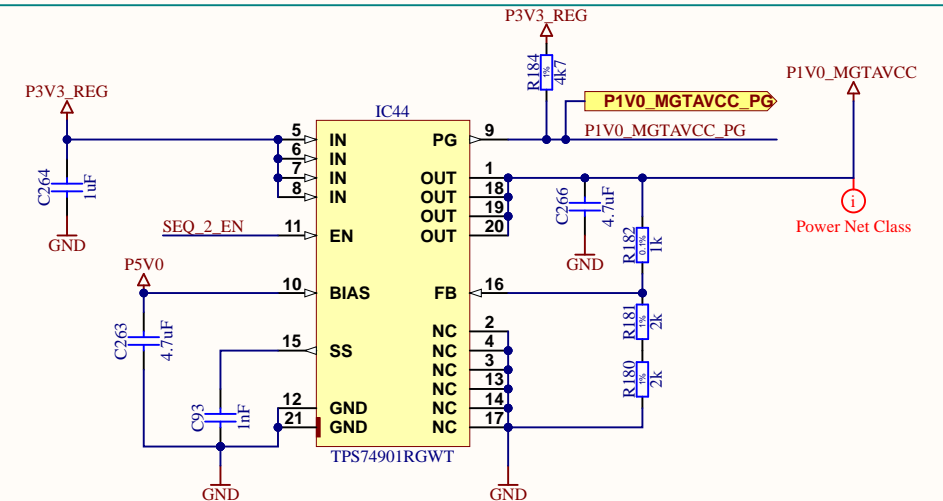
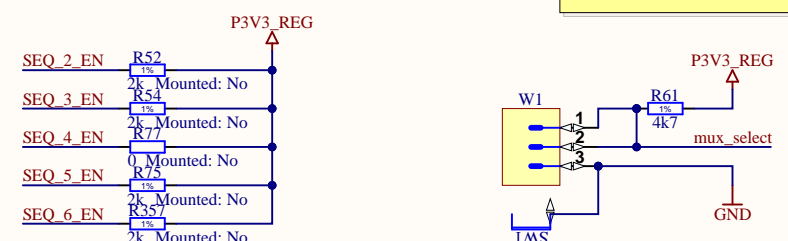


1.2V all (130mA linear)

\*layout example at datasheet p.20  
\*the IC pad must be attached to a minimum 10x10 mm amount of copper  
PCB area; 273 mW dissipation with a  $\theta_{JA}$  of 120 °C/W.

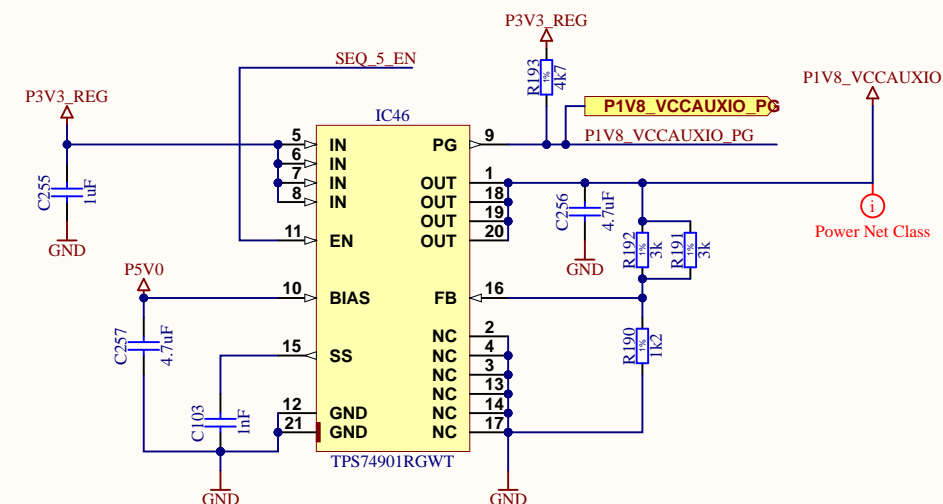


Select L -> B1 (regulators' sequence)  
 Select H -> B2, default (power controller sequence)



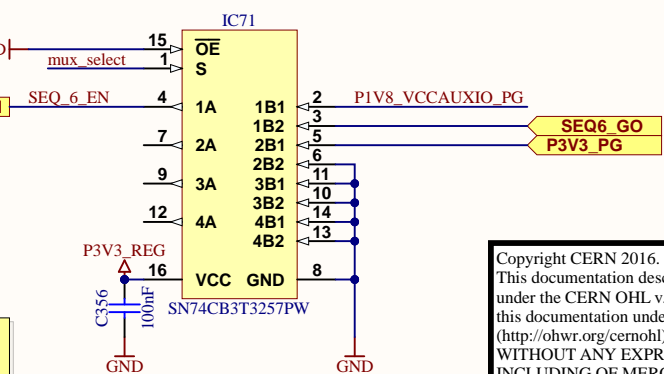
1.0V MGTAVCC (150mA linear)

\*layout example at datasheet p.20  
\*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 345 mW dissipation with a  $\theta_{JA}$  of 120 °C/W.



1.8V VCCAUX IO (130mA linear)

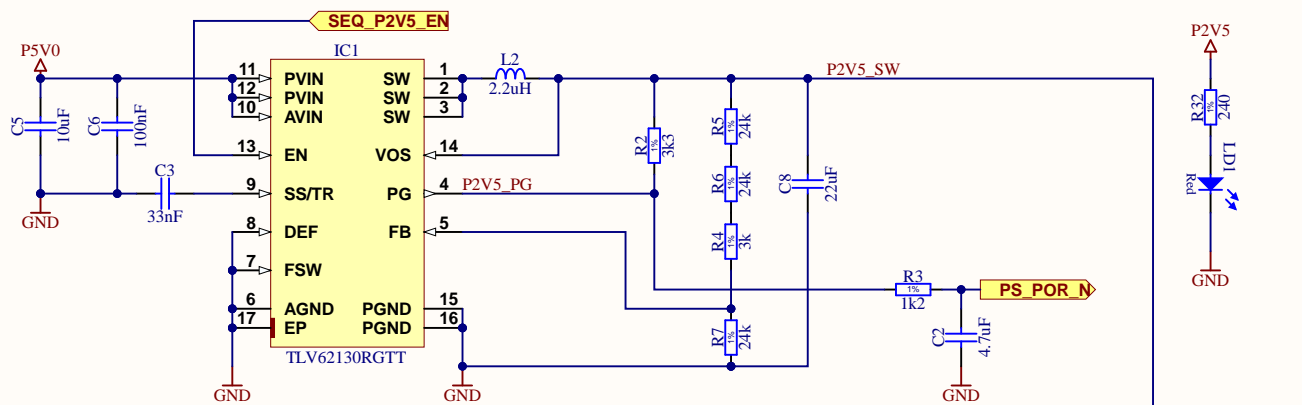
\*layout example at datasheet p.20  
\*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a  $\theta_{JA}$  of 120 °C/W.



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Project: <b>CITY</b>			2	03/2020	broquet
Sheet: <b>Supplies 2</b>			Rev.	Date	Author
File: <b>CITY_power-supplies-2 SchDoc</b>			SVN:		

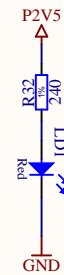


2.5V all (3A max)

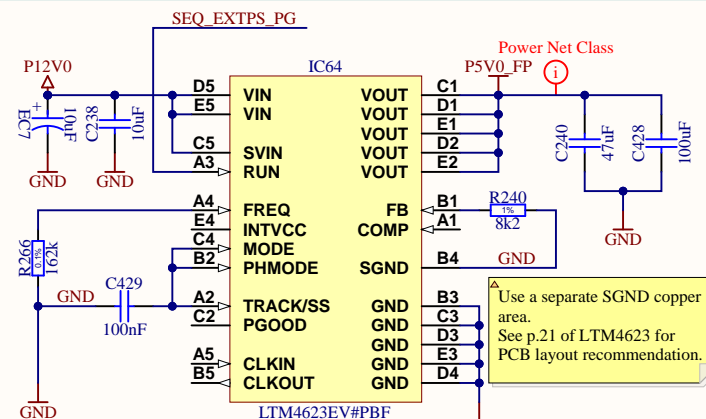
\*fsw = 2.5 MHz  
\*layout example at datasheet p.22  
\*100nF directly across the AVIN and AGND pins

RC delay (tau=21ms) to provide the required 40ms after VCCO\_0 assertion before deasserting PS\_POR\_B [DS191 p.18] to 2.31V (Vcc\*0.7).

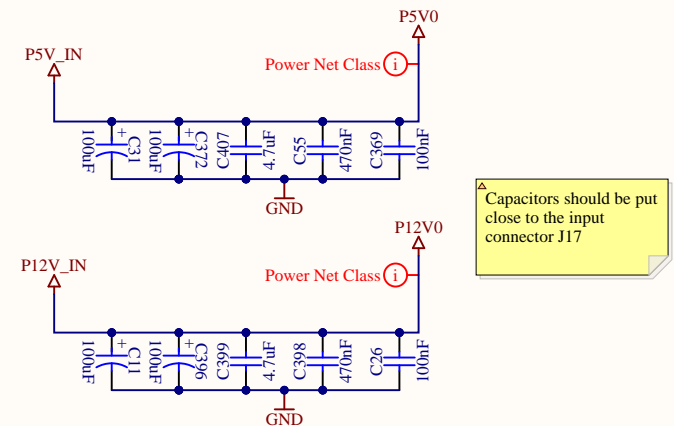
Power ON LED



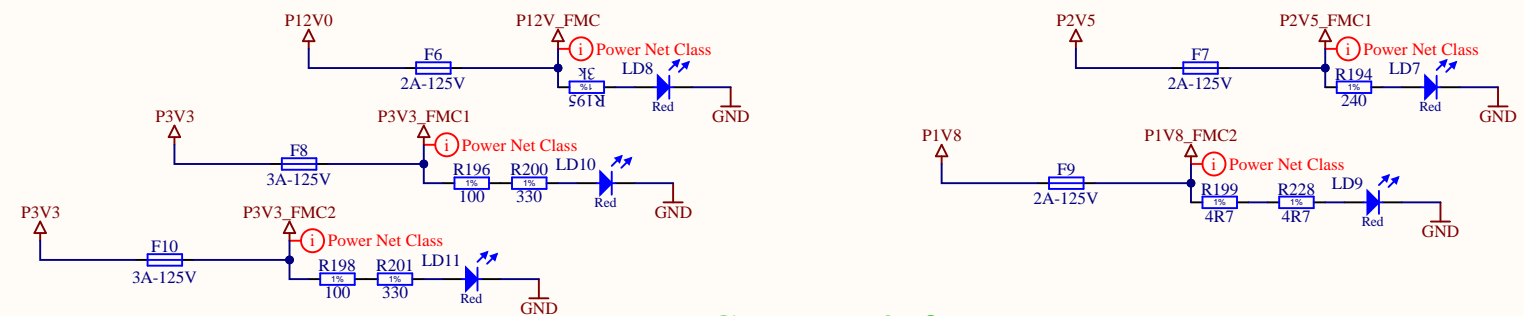
5V for Digital Output stages



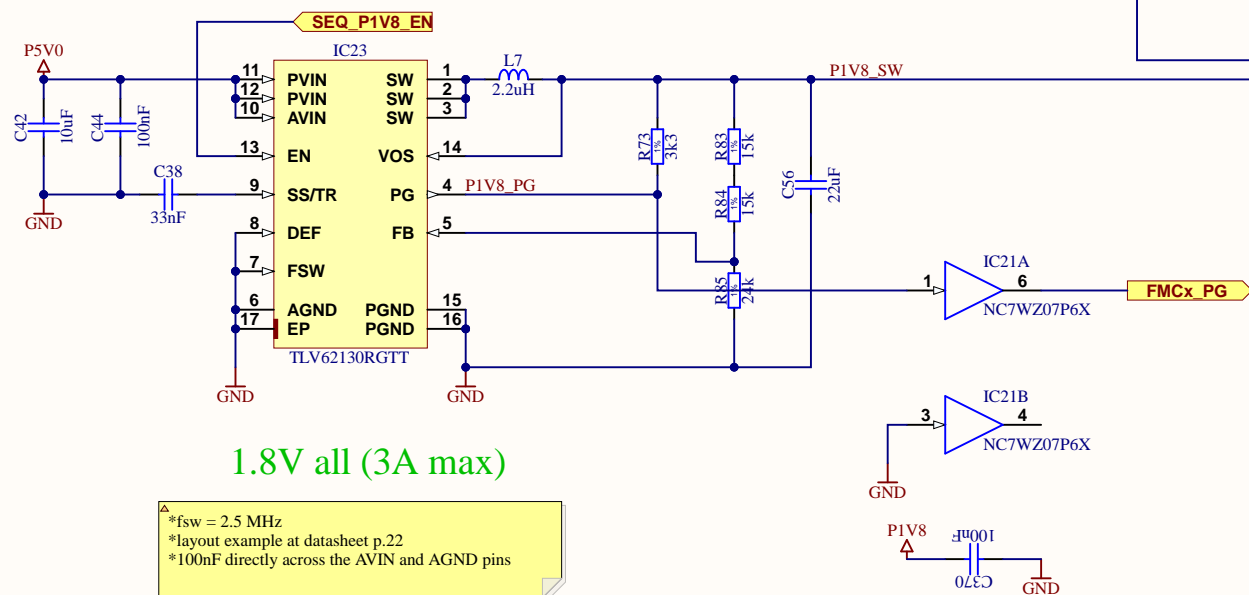
Power supply decoupling



Capacitors should be put close to the input connector J17

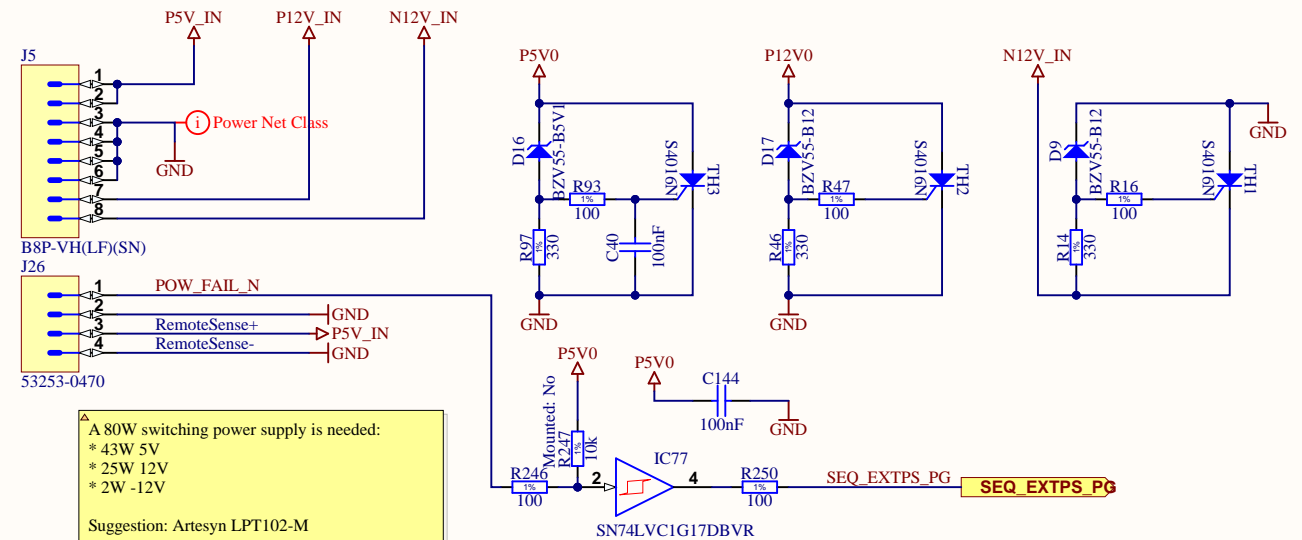
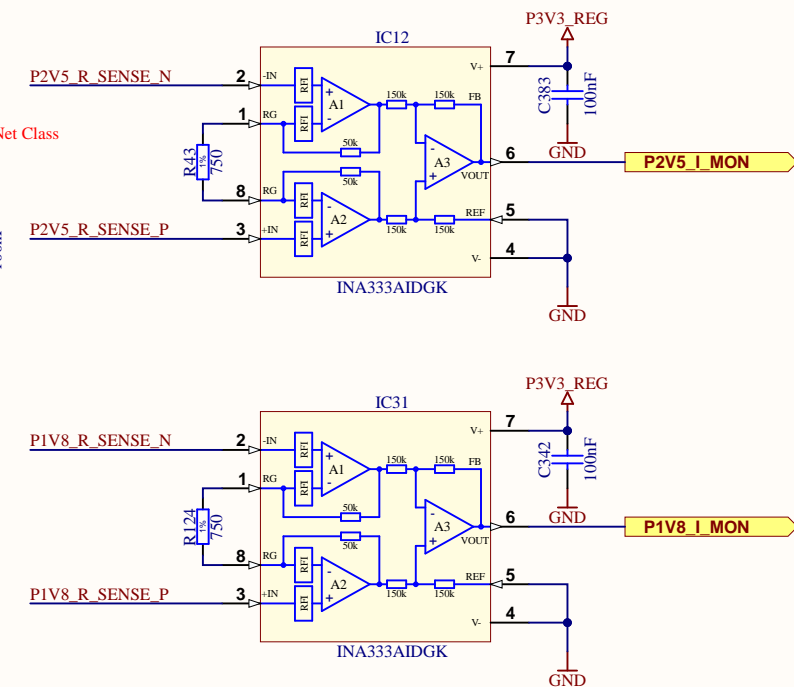
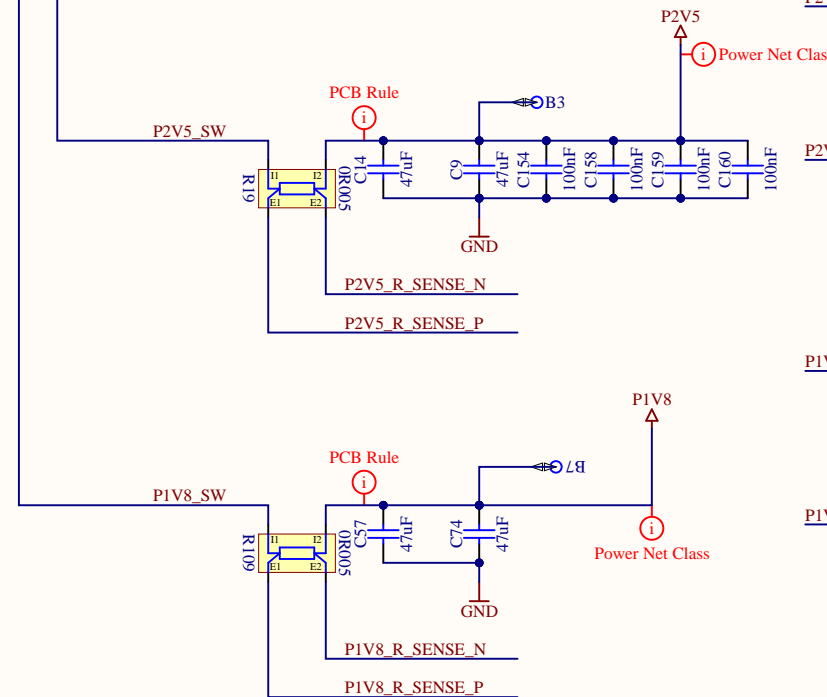
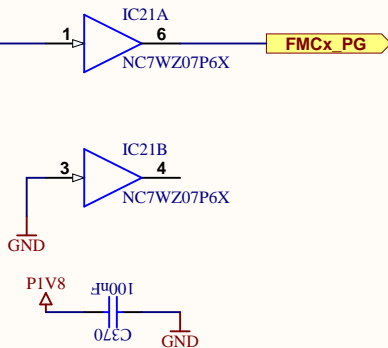


FMC power & fuses

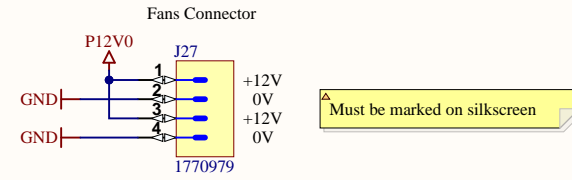


1.8V all (3A max)

\*fsw = 2.5 MHz  
\*layout example at datasheet p.22  
\*100nF directly across the AVIN and AGND pins



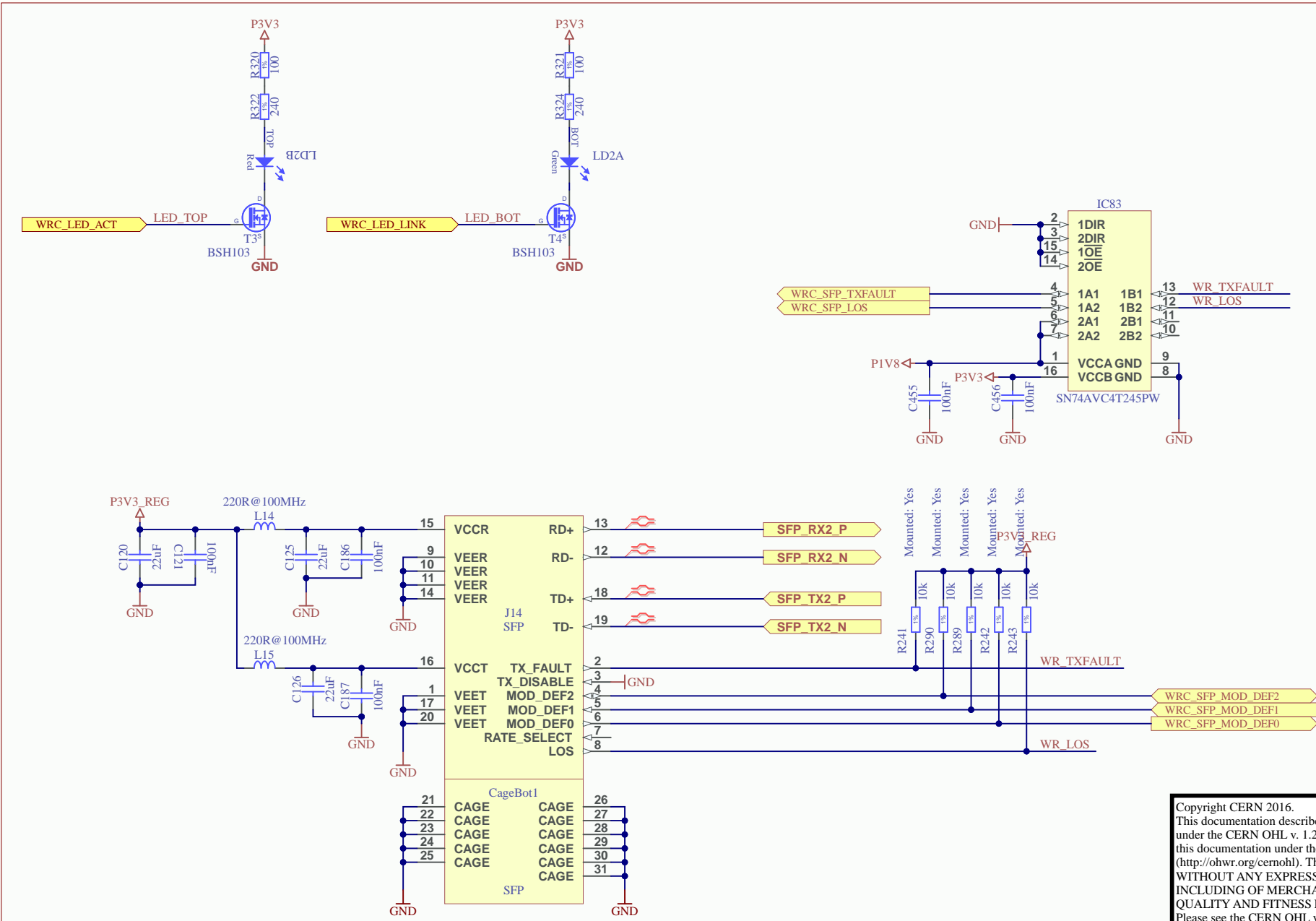
Main PCB supplies and SCR crowbar protection



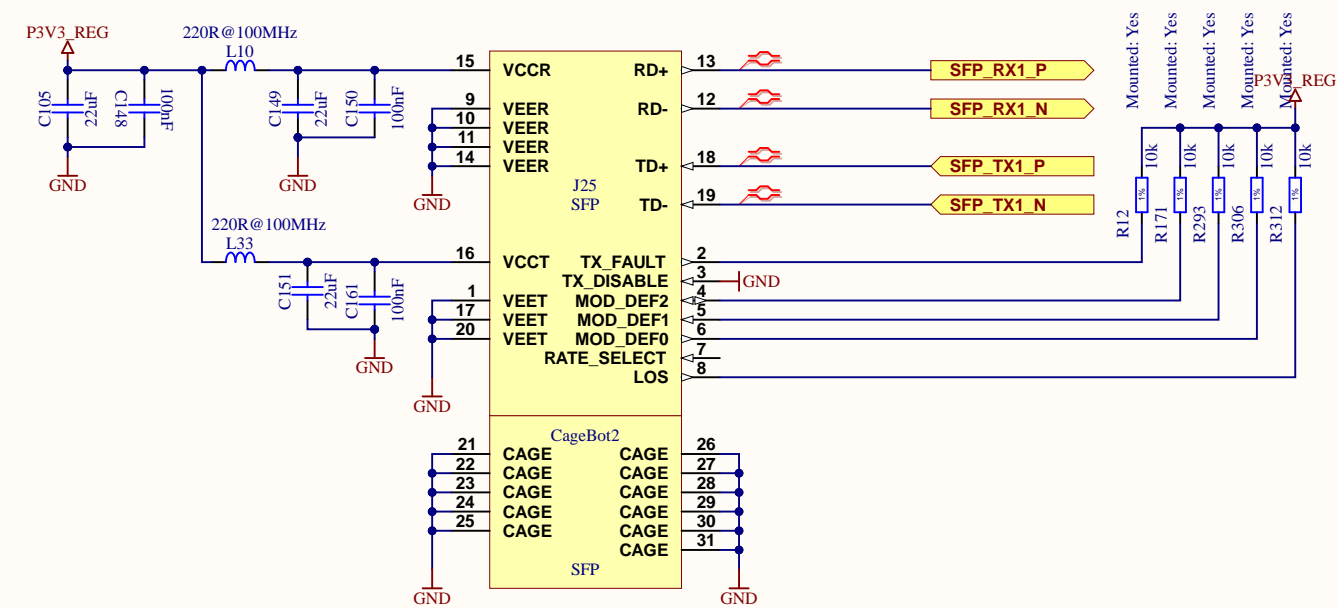
Must be marked on silkscreen

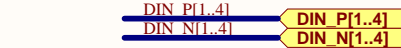
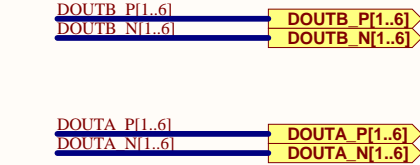
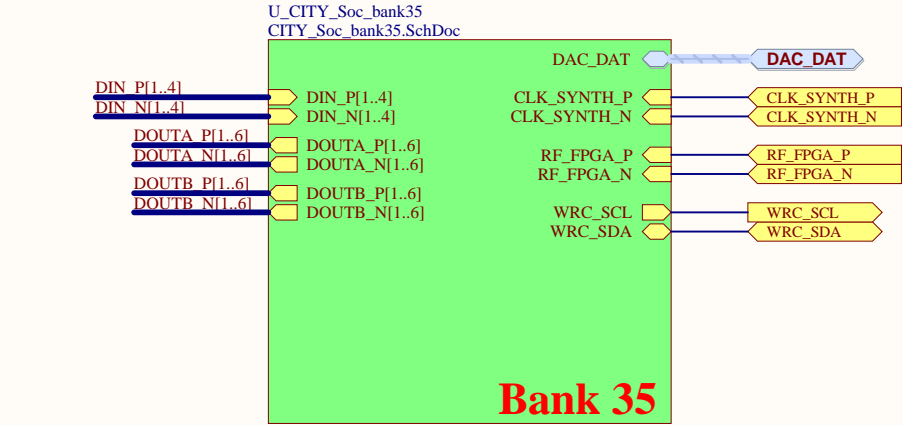
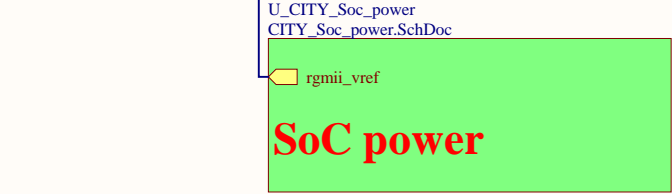
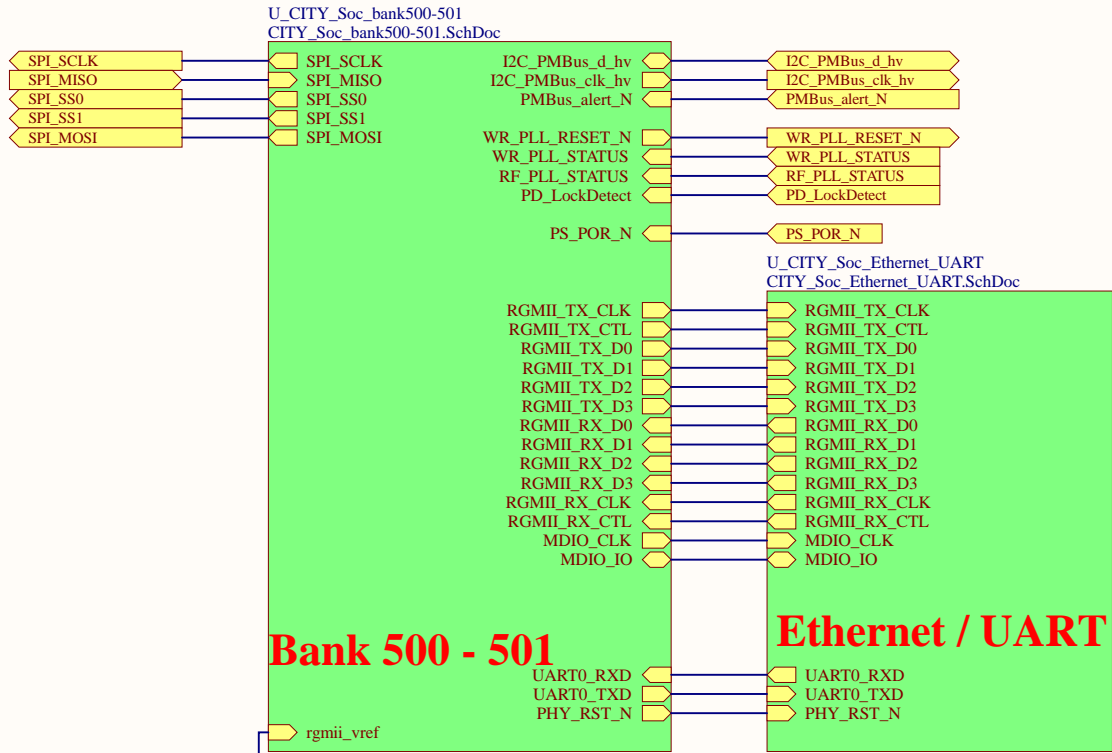
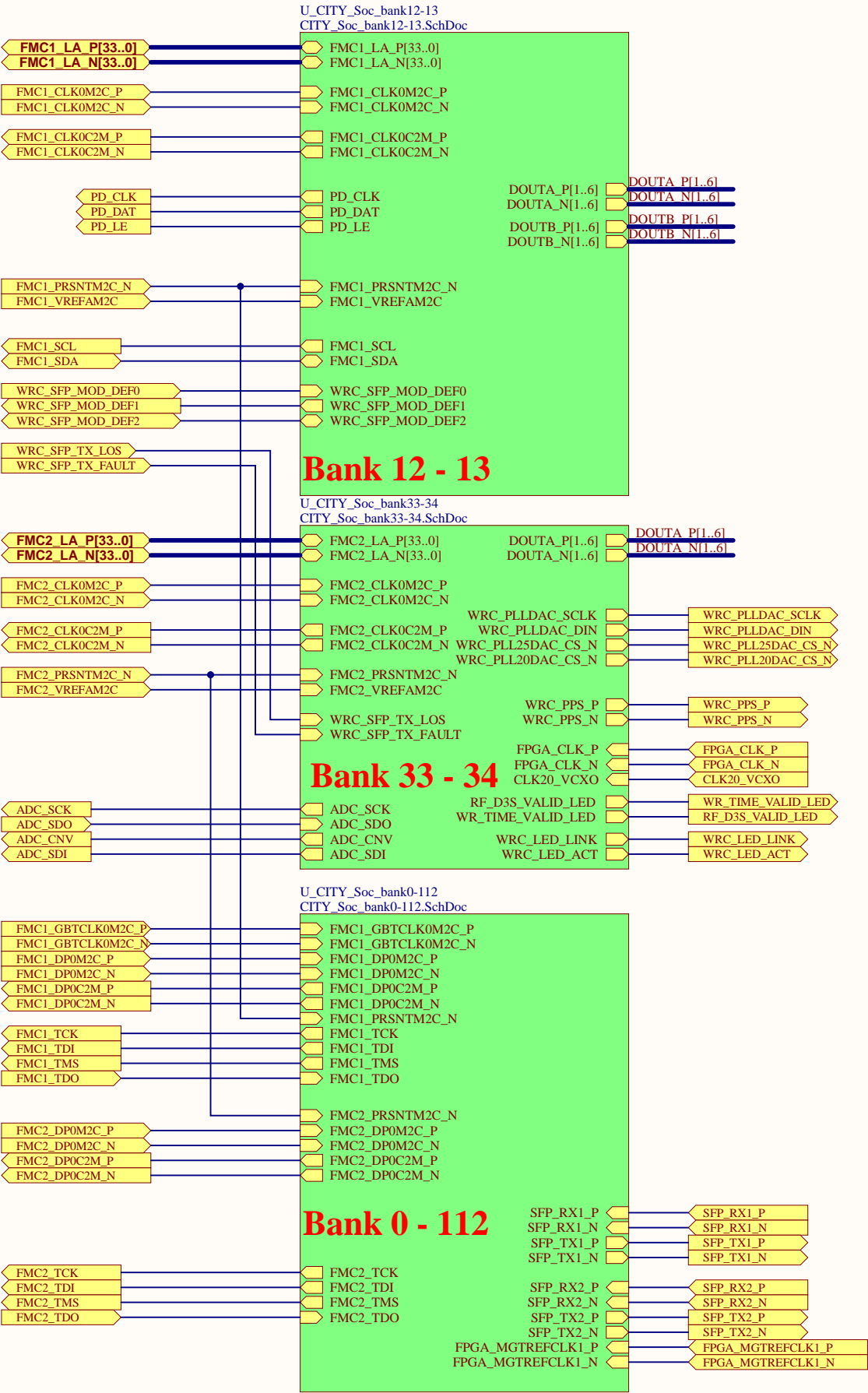
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SVN:			
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Author:			



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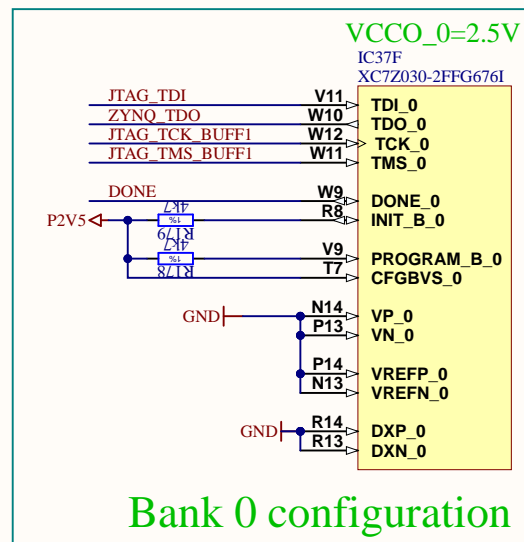
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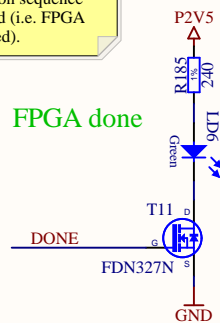
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**DDR3L**

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	Project:	CITY		2	03/2020	broquet
	Sheet:	Zynq SoC		Rev.	Date	Author
	File:	CITY_Soc_top.SchDoc		SVN:		

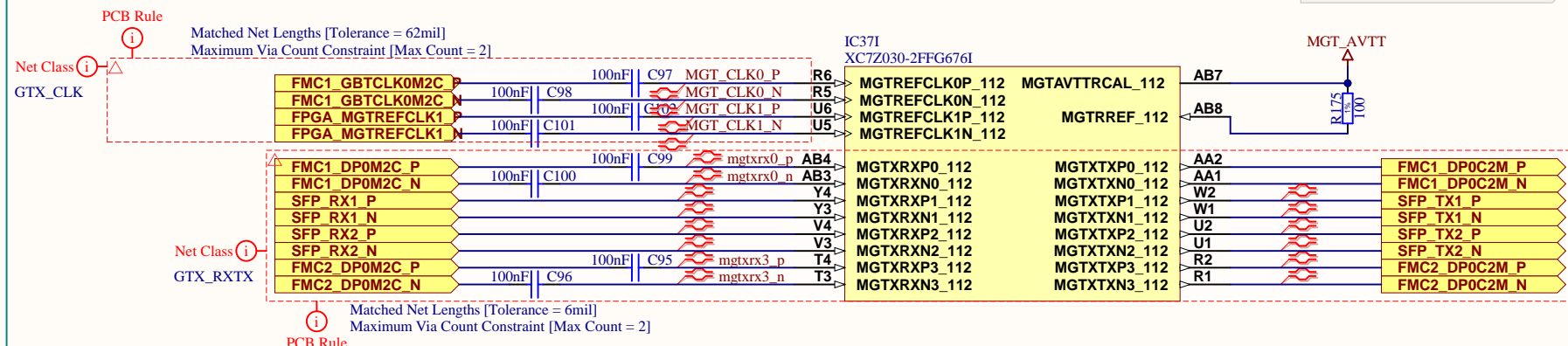




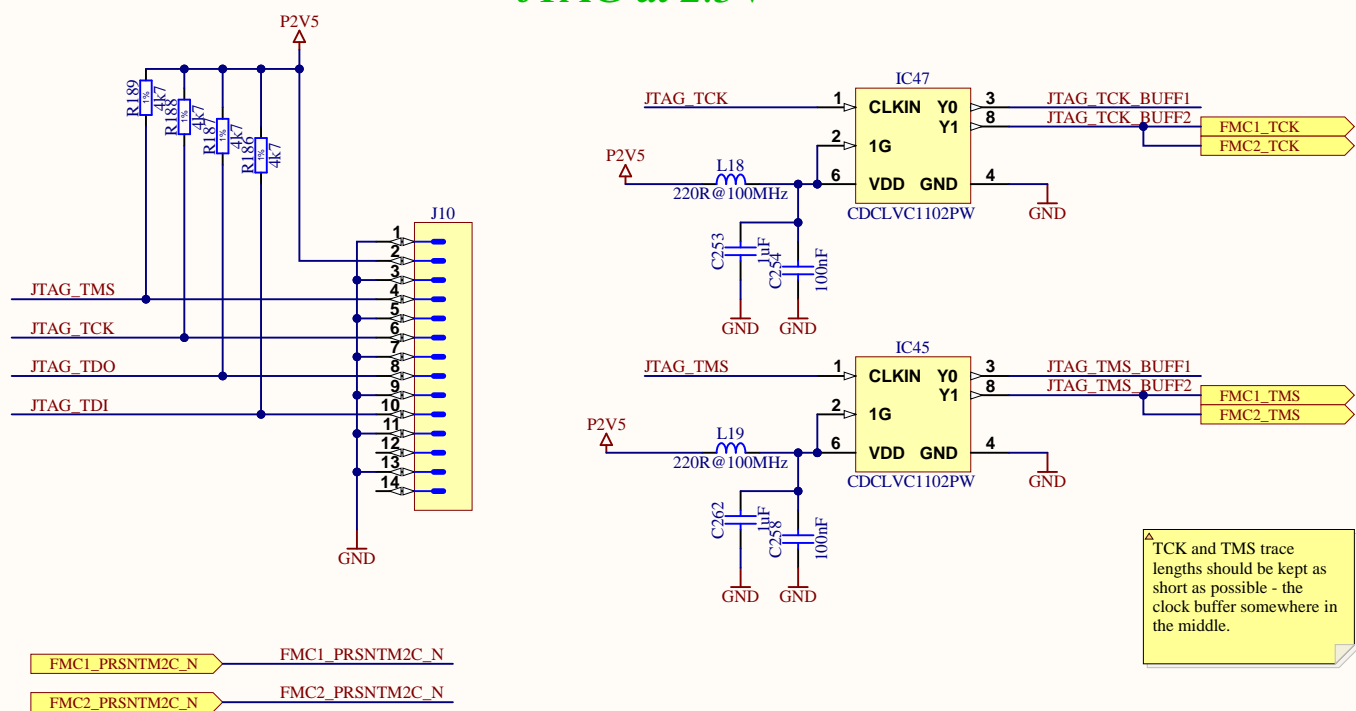
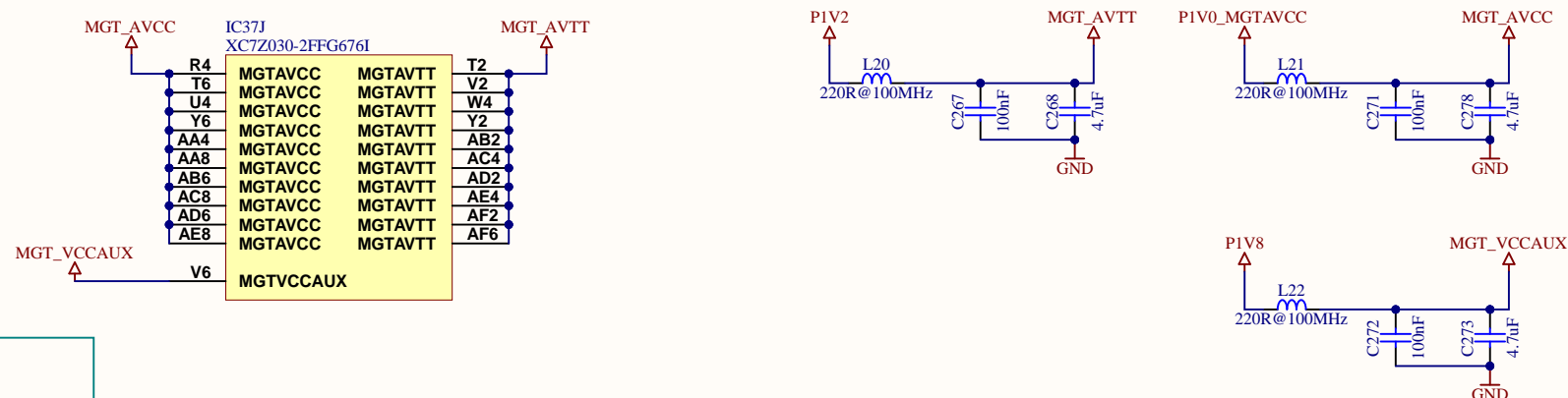
△ DONE is open-drain but has an internal 10k pull-up resistor. Kept at GND when the configuration sequence has not finished (i.e. FPGA not programmed).



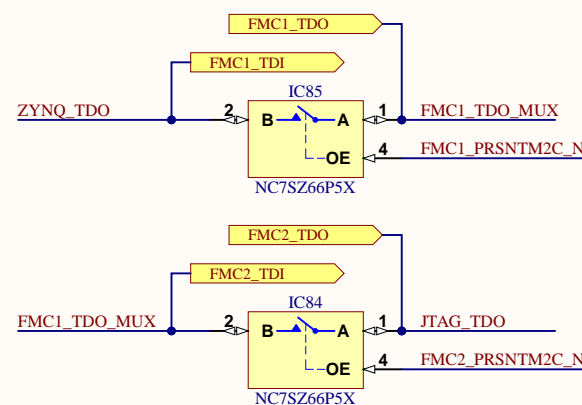
FPGA done



△ The traces from MGTAVTTRCAL\_112 and MGTRREF\_112 to the resistor should have the same length and geometry [UG476 p. 303].



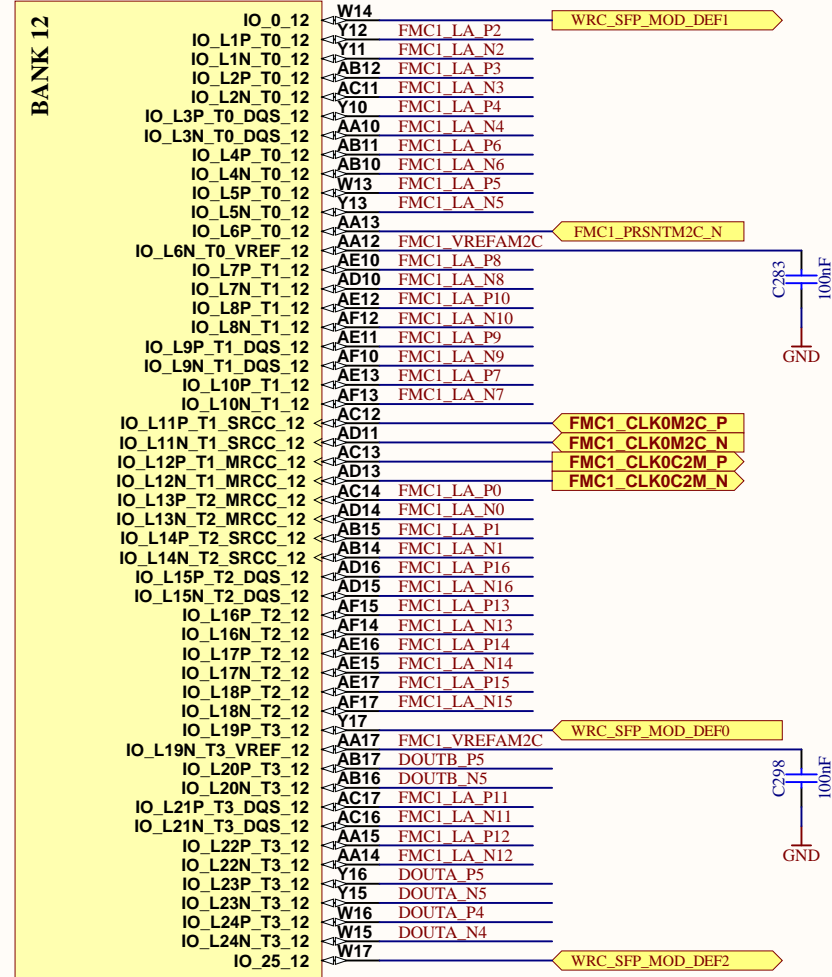
△ TCK and TMS trace lengths should be kept as short as possible - the clock buffer somewhere in the middle.



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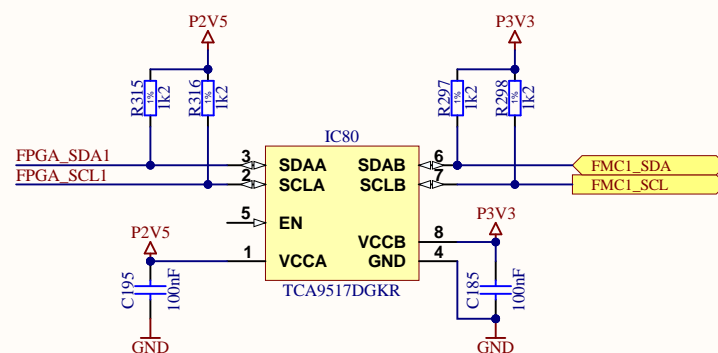
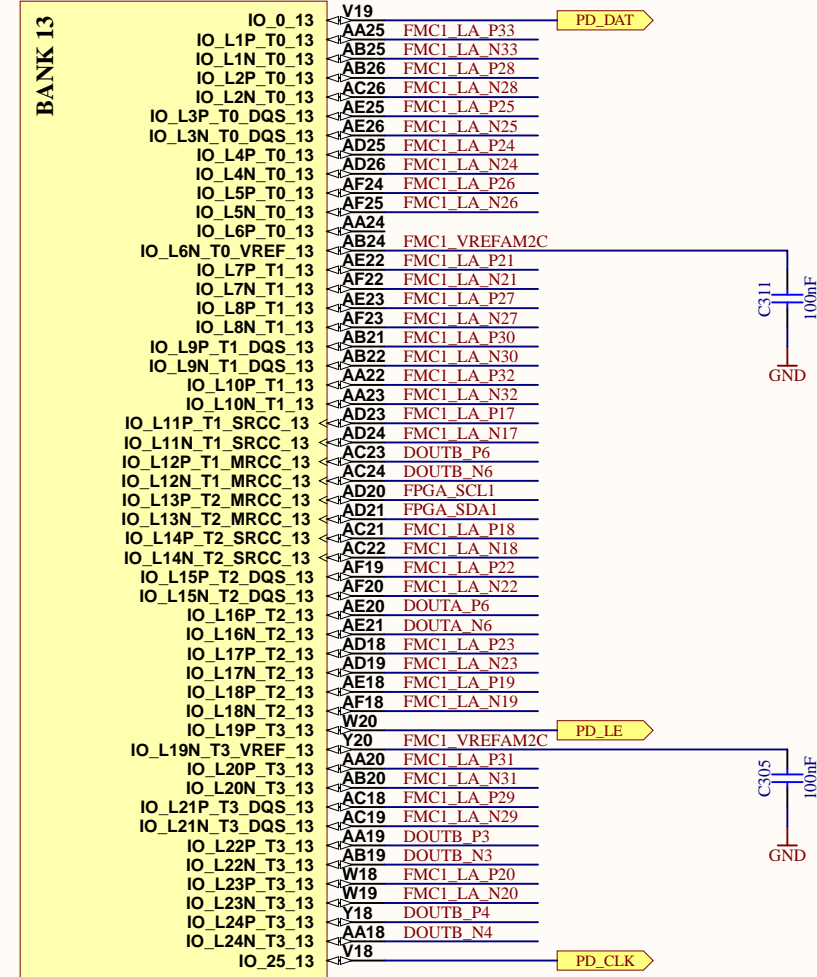
VCCO\_12=2.5V

IC37A  
XC7Z030-2FFG6761



VCCO\_13=2.5V

IC37B  
XC7Z030-2FFG6761



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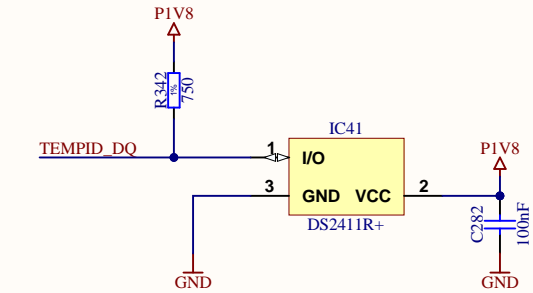


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SVN:			



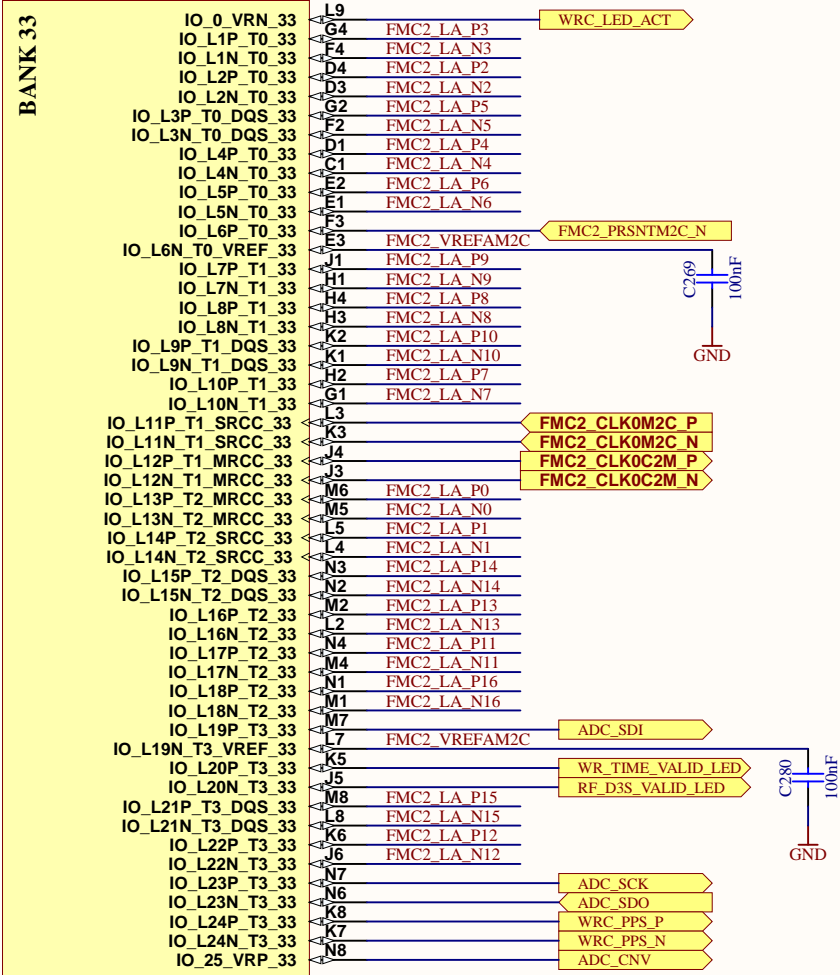
VCCO\_33=1.8V

VCCO\_34=1.8V

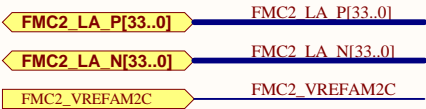
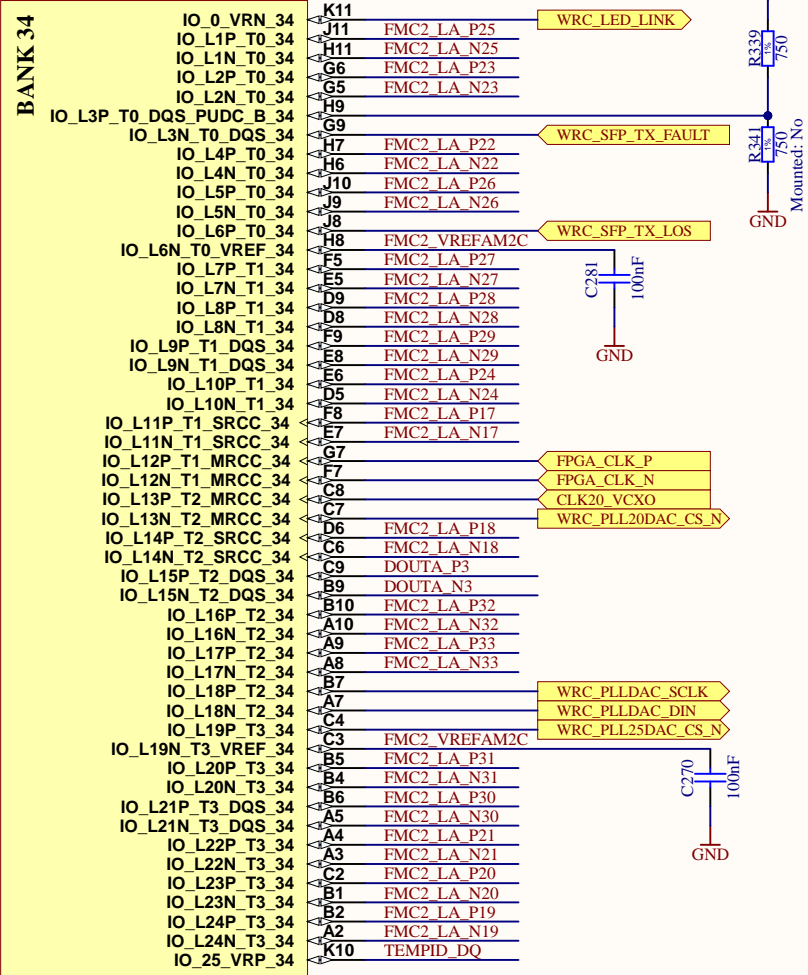


Unique 64-bit ID (Maxim 1-Wire)

IC37C  
XC7Z030-2FFG676I



IC37D  
XC7Z030-2FFG676I



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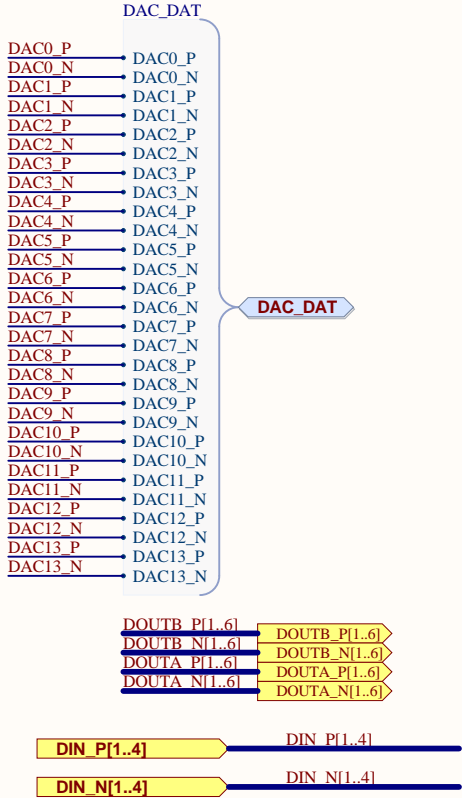
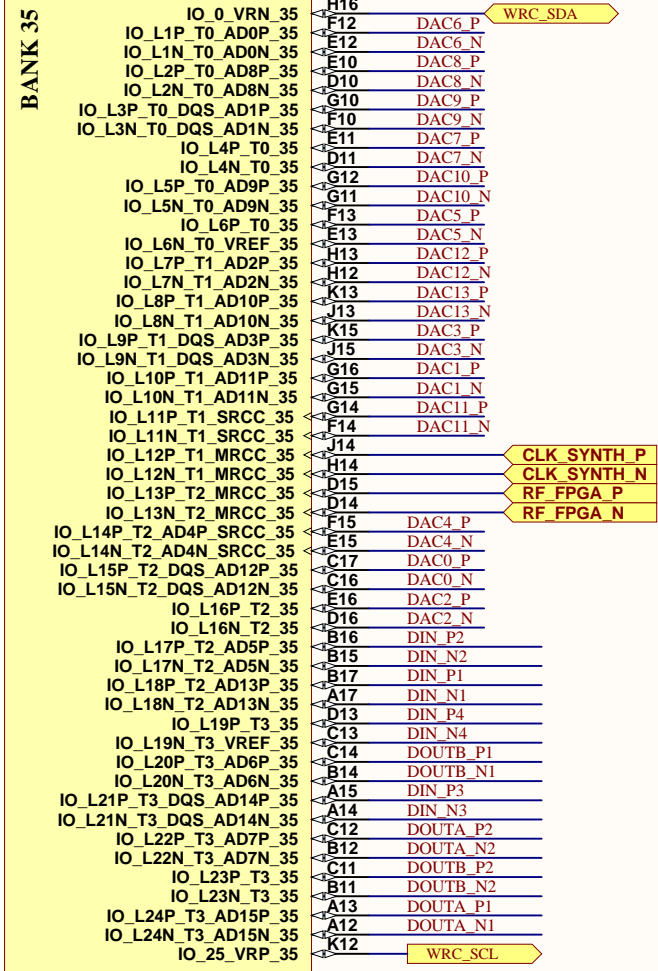


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		SVN:	

VCCO\_35=1.8V

IC37E

XC7Z030-2FFG676I



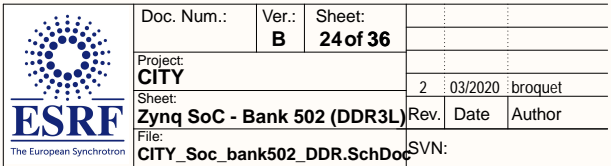
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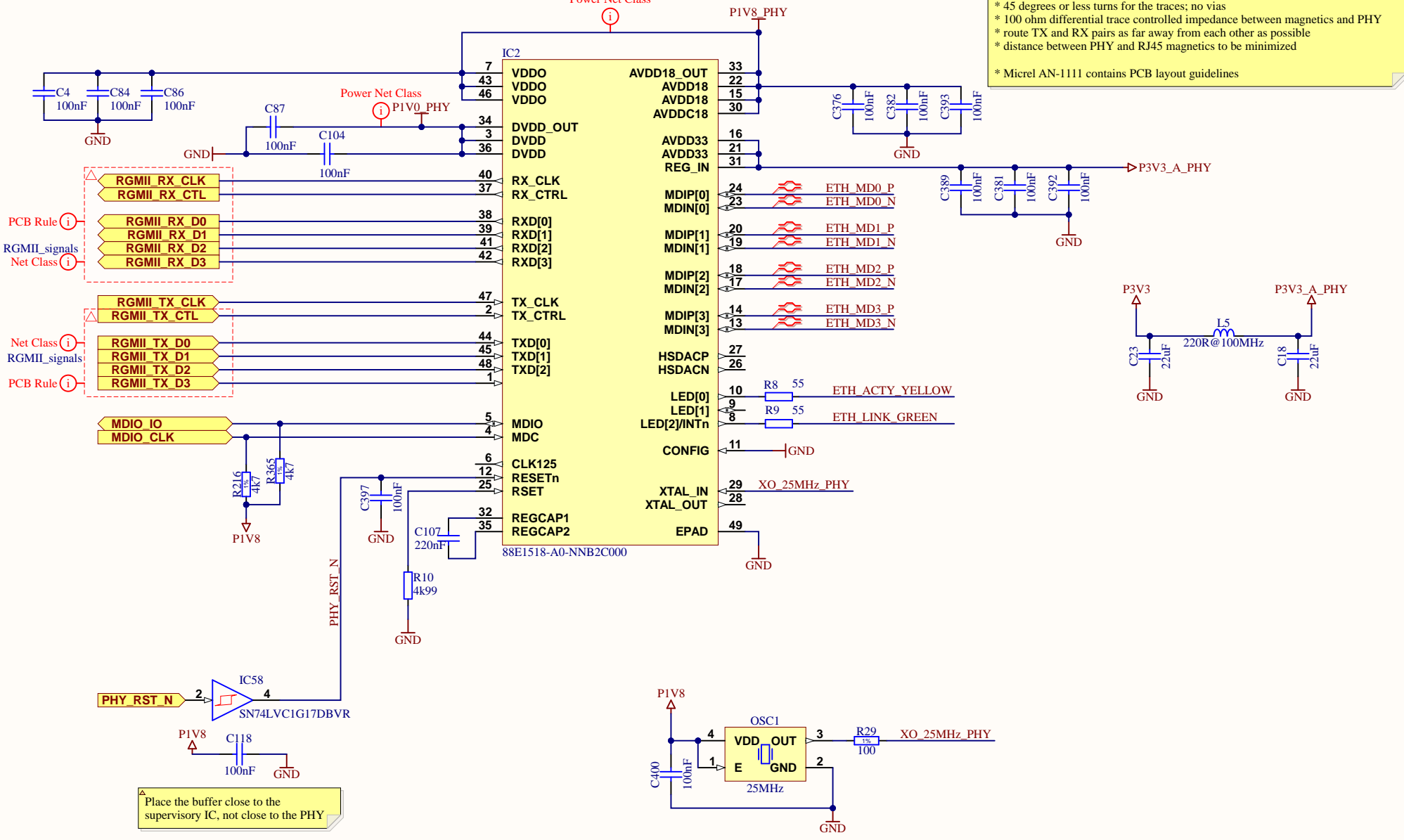
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Sheet:	Zynq SoC - Bank 35		
File:	CITY_Soc_bank35.SchDoc		
Rev.	Date	Author	
SVN:			



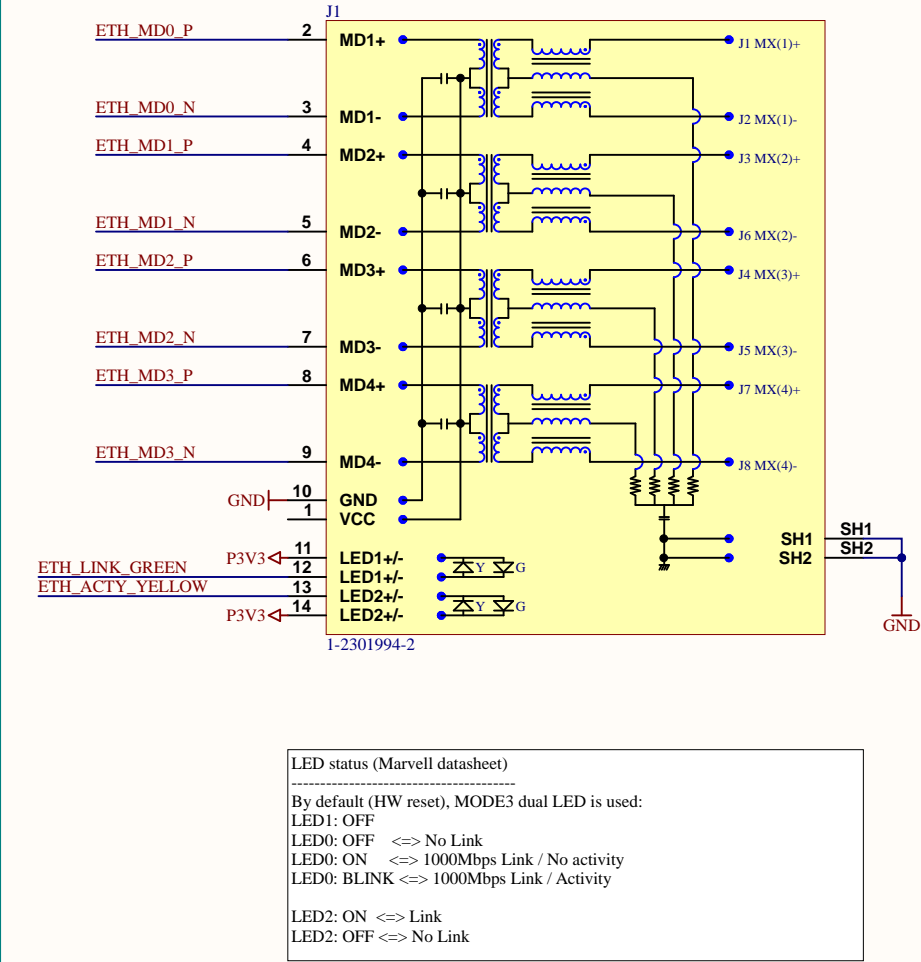




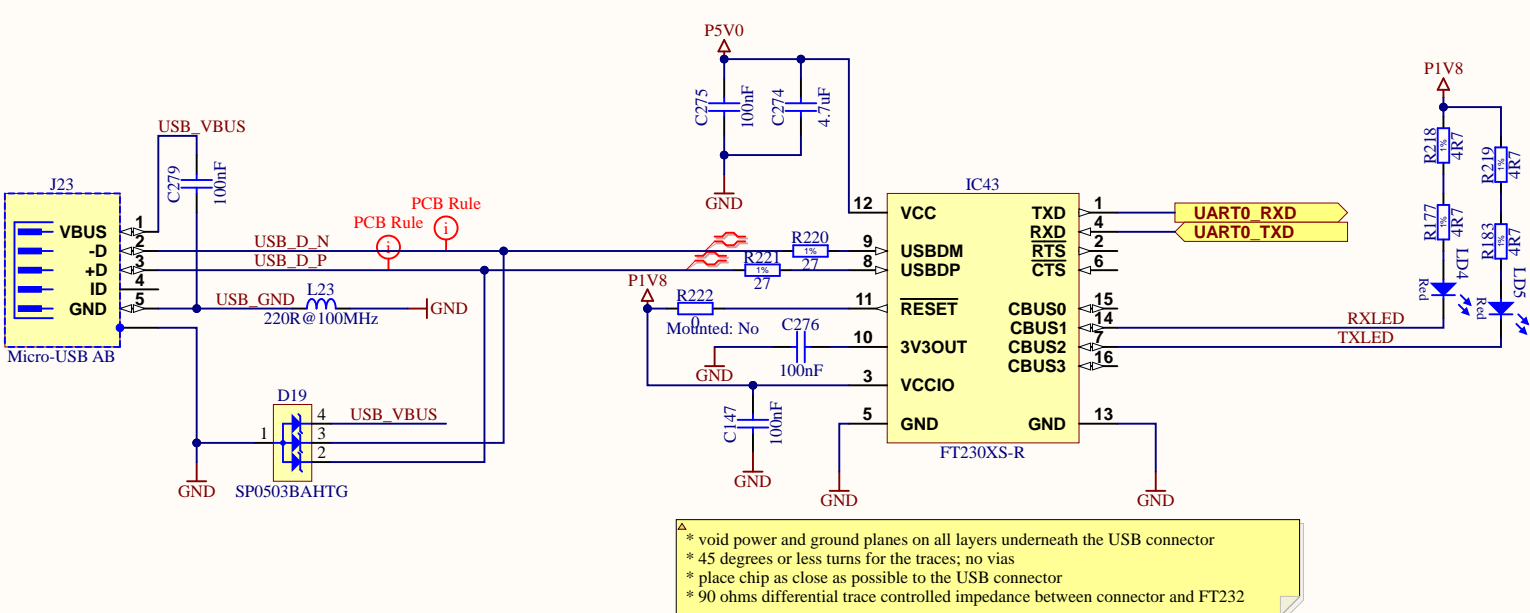
Ethernet Gigabit PHY Transceiver



Ethernet RJ45 connector



USB UART



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A

B

C

D

E

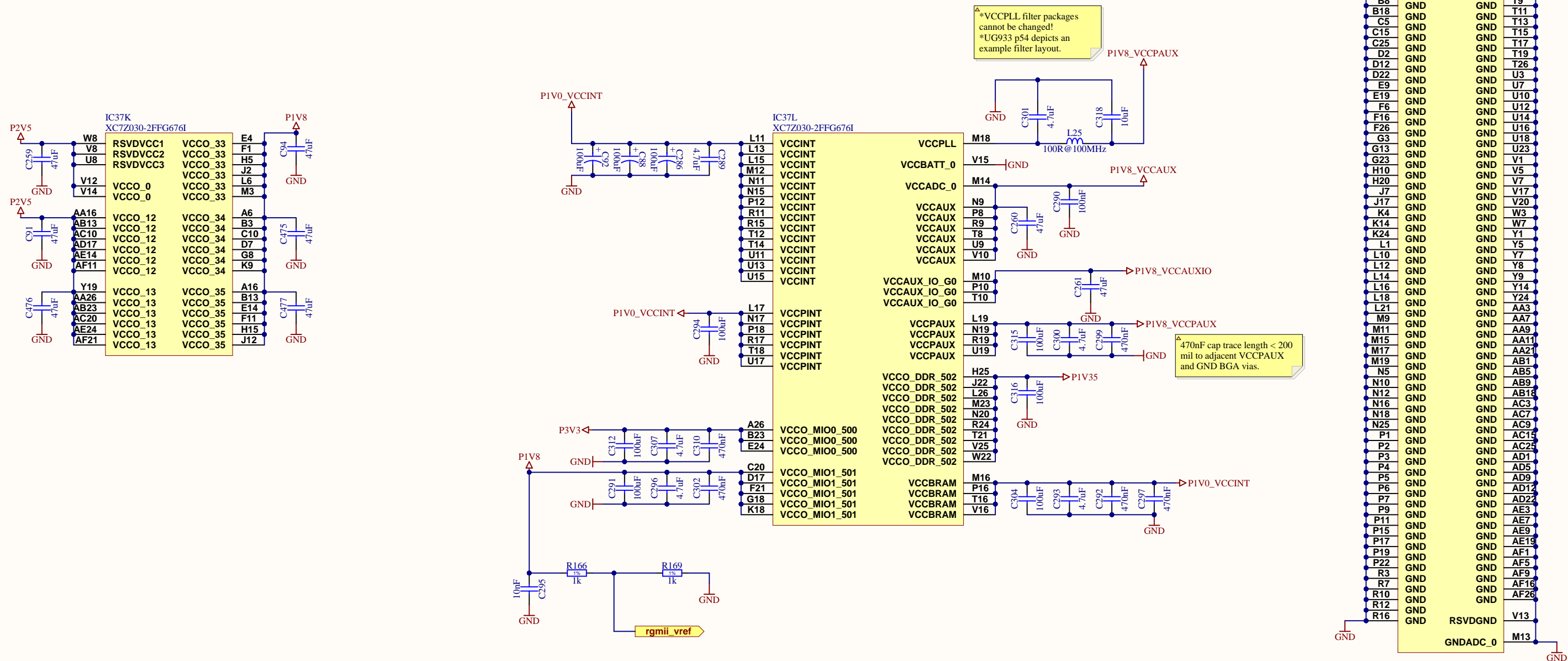
A

B

C

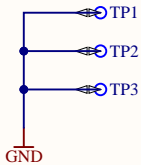
D

E

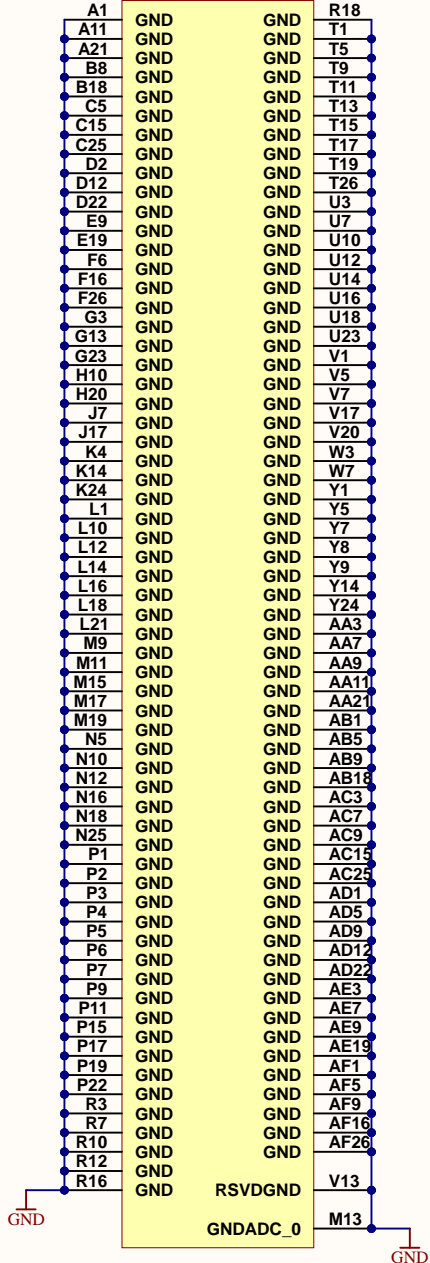


IC37N  
XC7Z030-2FFG676I

W5	NC	NC	AD7
W6	NC	NC	AD8
AA5	NC	NC	AE1
AA6	NC	NC	AE2
AC1	NC	NC	AE5
AC2	NC	NC	AE6
AC5	NC	NC	AF3
AC6	NC	NC	AF4
AD3	NC	NC	AF7
AD4	NC	NC	AF8



IC37M  
XC7Z030-2FFG676I



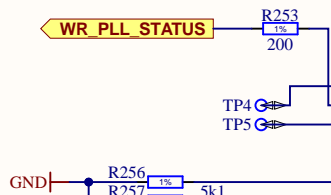
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REF: VCTXO 25MHz  
VCO: 2GHz  
Bandwidth: 10kHz  
Margin: 50Deg

WR PLL STATUS



WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
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WR PLL RESET\_N

PLL\_SCLK  
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PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
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PLL\_SDO  
WR PLL CS

WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

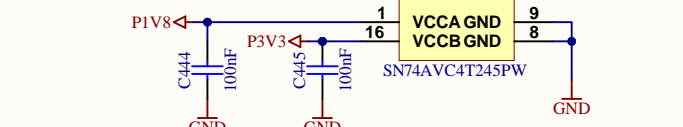
WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

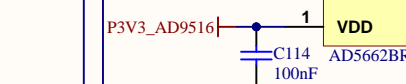
WR PLL RESET\_N

PLL\_SCLK  
PLL\_SDI  
PLL\_SDO  
WR PLL CS

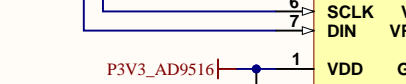
WR\_DAC\_SCLK  
WR\_DAC\_DIN  
WR\_DAC\_CS1  
WR\_DAC\_CS2



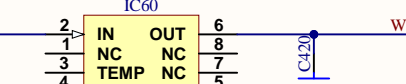
DAC\_CS1  
DAC\_SCLK  
DAC\_DIN



DAC\_CS2



DAC\_CS2



DAC\_CS2



DAC\_CS2



DAC\_CS2

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File:	WR Clocking				
	CITY_WR_clocking.SchDoc				
Rev.:	Date	Author			
SVN:					