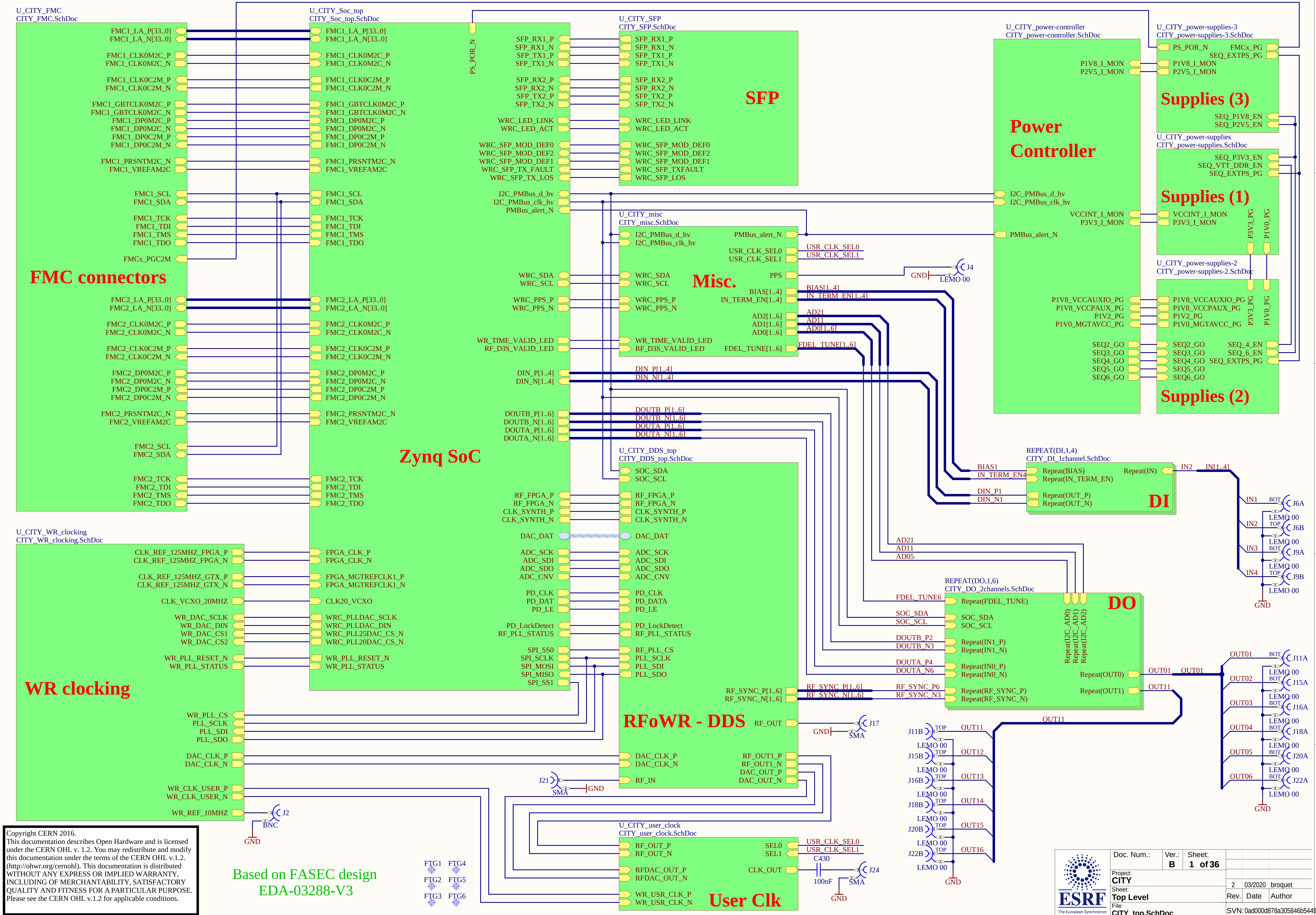
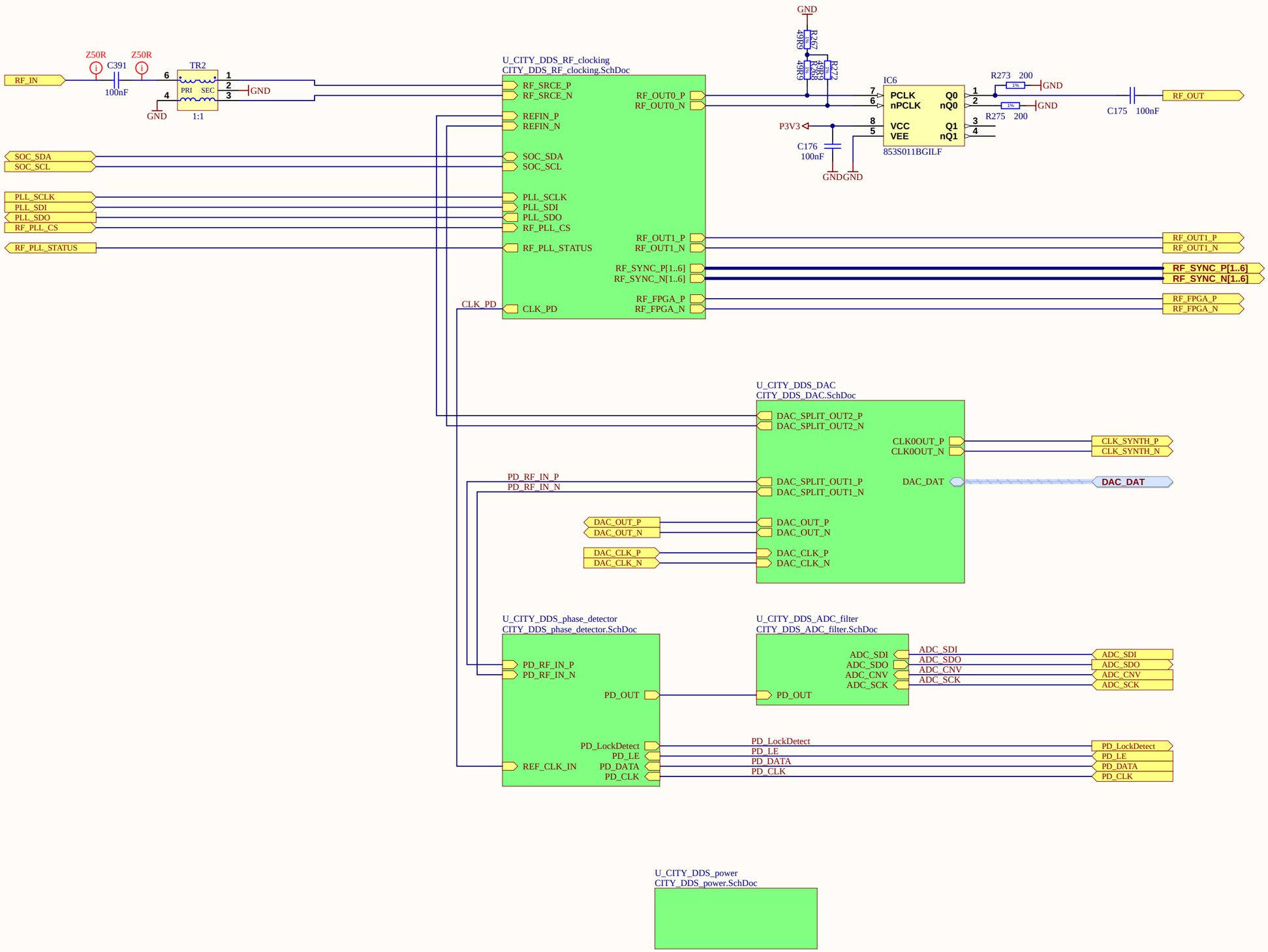


Based on FASEC design
EDA-03288-V3

Doc. Num.:	Ver.: B	Sheet: 1 of 36
Project: CITY		
Sheet: Top Level		
File: CITY_top.SchDoc		

Rev.	Date	Author
2	03/2020	broquet

SVN: 0ad000d878a305846b544933113



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Doc. Num.:	Ver.:	Sheet:
	B	2 of 36

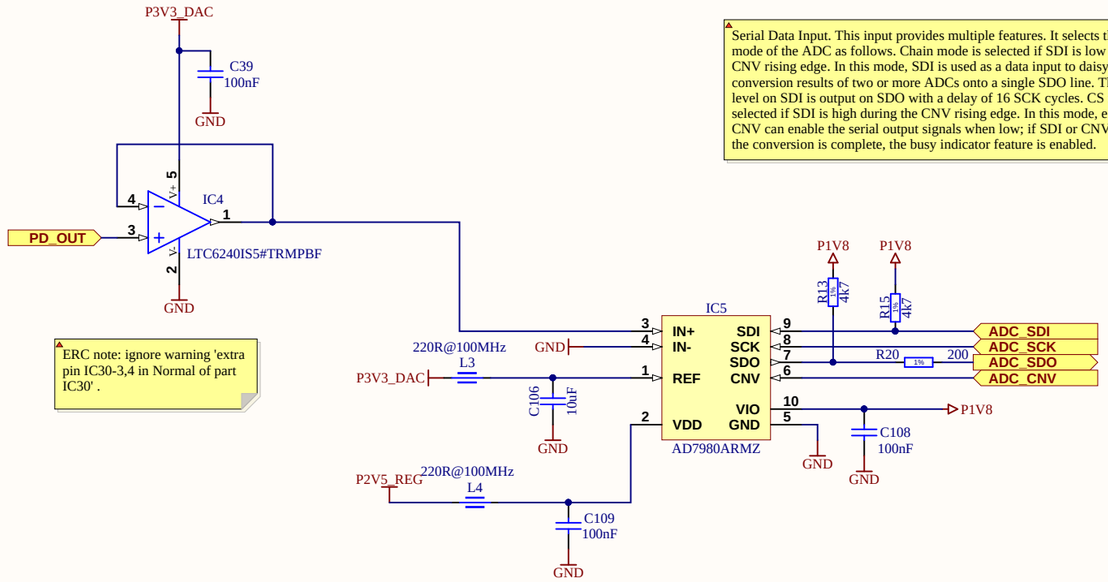
Project: **CITY**

Sheet: **DDS Top**

File: **CITY_DDS_top.SchDoc**

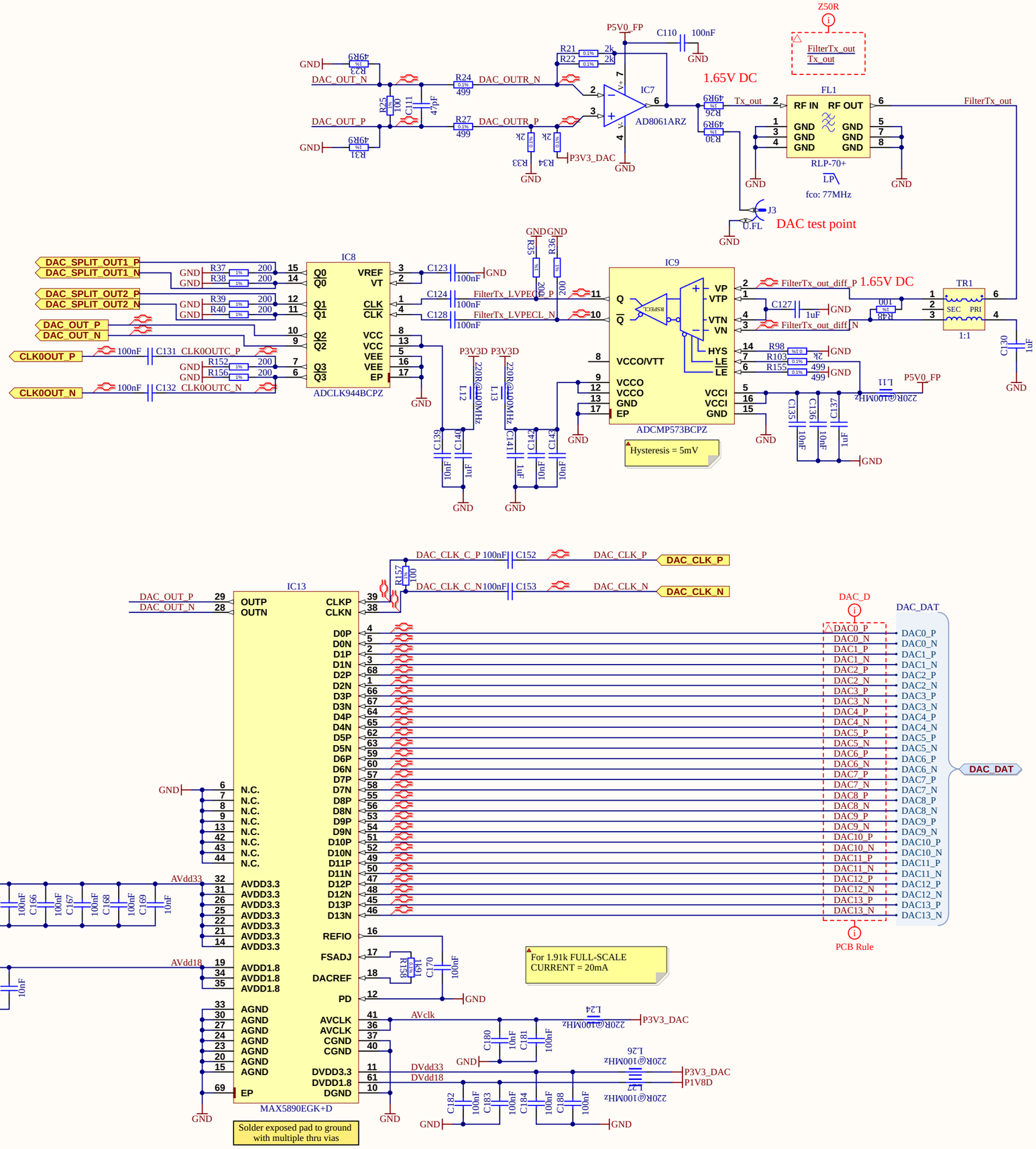
Rev.	Date	Author
2	03/2020	broquet

SVN:

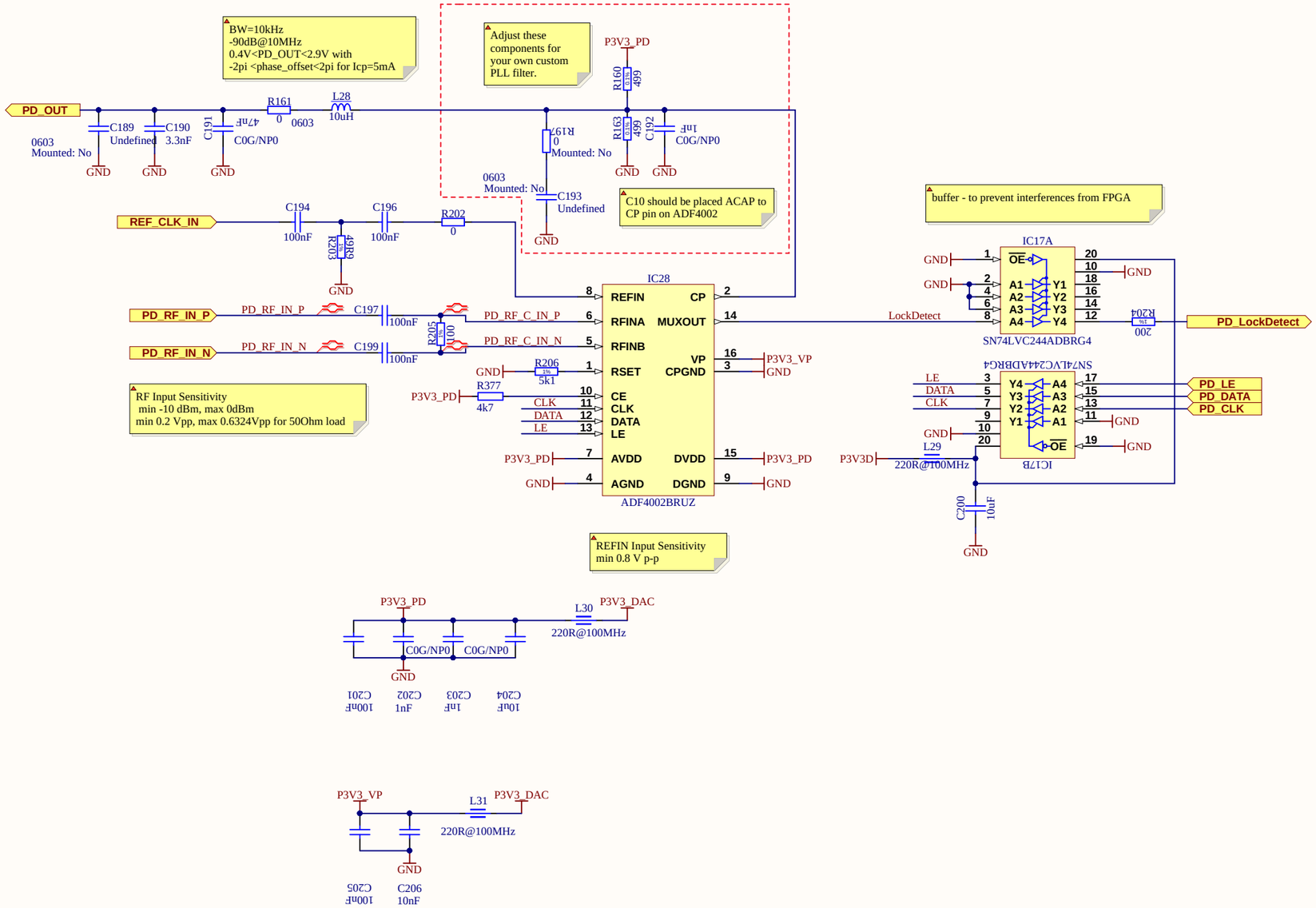


Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows. Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. CS mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low; if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.

ESRF The European Synchrotron	Doc. Num.:	Ver.: B	Sheet: 3 of 36
	Project: CITY		
	Sheet: DDS ADC	Rev. 2	Date 03/2020 Author broquet
	File: CITY_DDS_ADC_filter.SchDoc	SVN: cd3caf30cb1f52dc081901255772	

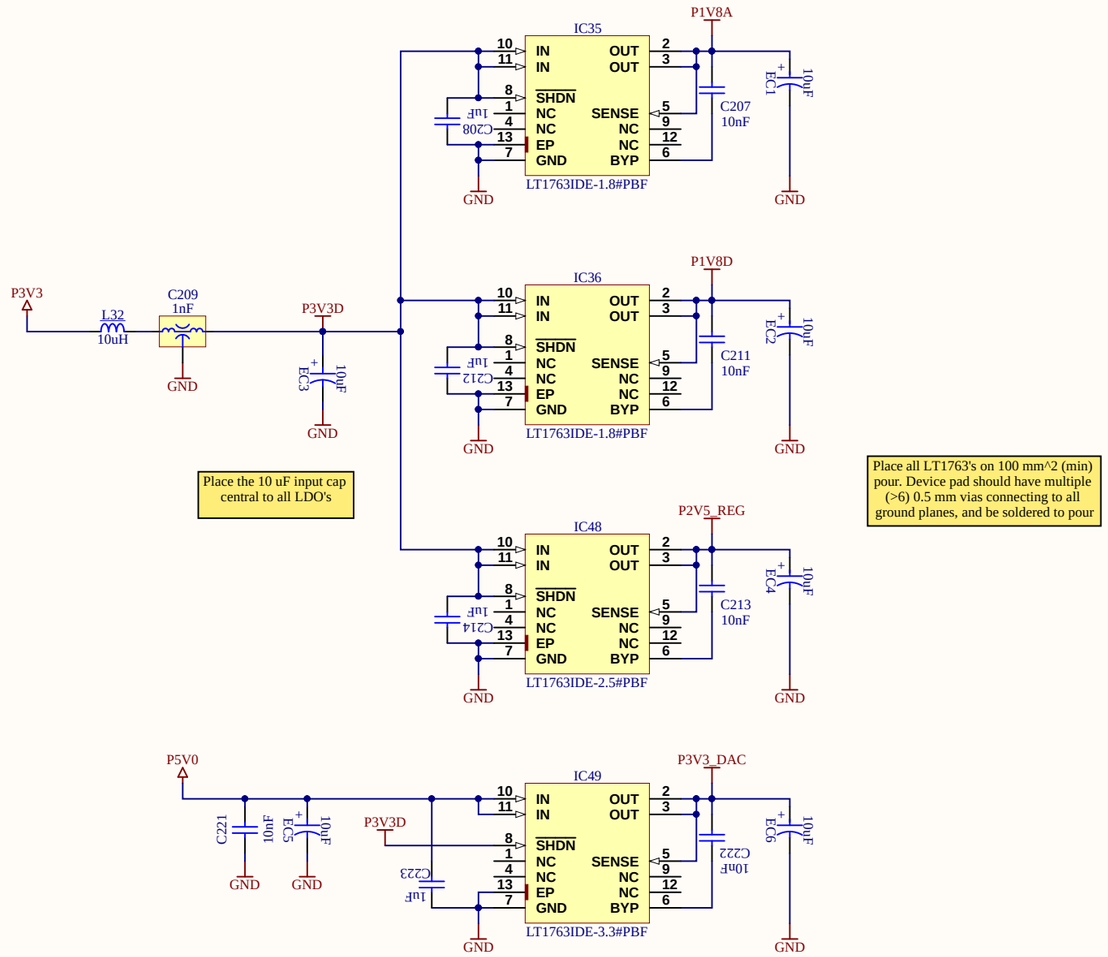


Doc. Num.:	Ver.: B	Sheet: 4 of 36	
Project: CITY			
Sheet: DDS DAC & Filter	2	03/2020	broquet
	Rev.	Date	Author
File: CITY_DDS_DAC.SchDoc	SVN: cd3caf30cb1f52dc081901255772		



ESRF The European Synchrotron	Doc. Num.:	Ver.: B	Sheet: 5 of 36
	Project: CITY		
	Sheet: DDS Phase Detector		
	File: CITY_DDS_phase_detector.SchDoc		SVN:

Rev.	Date	Author
2	03/2020	broquet



ESRF The European Synchrotron

Doc. Num.:	Ver.: B	Sheet: 6 of 36	
Project: CITY			
Sheet: DDS Power Supply Regulators			
File: CITY_DDS_power.SchDoc			

Rev.	Date	Author
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SVN:		

SOC_SCL
SOC_SDA

IC50
SOC_SCL
SOC_SDA
SCL
SDA
INT
AD0
AD1
AD2
VCC
GND
PAD
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
I/O9
I/O10
I/O11
I/O12
I/O13
I/O14
I/O15
RF_FINEDEL9
RF_FINEDEL8
RF_FINEDEL7
RF_FINEDEL6
RF_FINEDEL5
RF_FINEDEL4
RF_FINEDEL3
RF_FINEDEL2
RF_FINEDEL1
RF_FINEDEL0
GND
P3V3
C224
100nF
MAX7311ATG+T
RF_FINEDEL[0..9]

RF_SRCE_P
RF_SRCE_N
REFIN_P
REFIN_N
PLL_SCLK
RF_PLL_CS
PLL_SDI
PLL_SDO
CKSi_P
CKSi_N
C112 100nF
C113 100nF
C252 100nF
C265 100nF
C225 100nF
C226 100nF
R274 49R9
R378 100
R210 100
RF_SRCEC_P
RF_SRCEC_N
VCXO_CLK2_P
VCXO_CLK2_N
REFINC_P
REFINC_N

IC51
CLK1
CLK1B
CLK2
CLK2B
REFIN
REFINB
SCLK
CSB
SDIO
SDO
FUNCTION
STATUS
CPRSET
RSET
VS
CP
VCP
GND
OUT0
OUT0B
OUT1
OUT1B
OUT2
OUT2B
OUT3
OUT3B
OUT4
OUT4B
OUT5
OUT5B
OUT6
OUT6B
OUT7
OUT7B
RF_OUT0_P
RF_OUT0_N
RF_OUT_P
RF_OUT_N
RF_OUT3_P
RF_OUT3_N
RF_FPGA_P
RF_FPGA_N
RF_OUT0_P
RF_OUT0_N
RF_OUT1_P
RF_OUT1_N
RF_FPGA_P
RF_FPGA_N
R213 200
R214 200
R215 200
R217 200
R170 1k
R224 200
R225 5k1
R226 4k12
P3V3_RF9510
RF_PLL_STATUS
CLK_PD

RF/8
LVPECL single-ended output level.
AC coupled transmission. Capacitor in Phase Detector sheet.

Filter calculation with ADIsimCLK

352MHz target
Fvcxo: 352MHz
Fref (PFD): 44MHz
Si571 Slope tune: 33ppm/V <=> Kv = 11.628kHz/V
BW: 10kHz
Phase margin: 50deg
Charge pump current: 4.8mA
--
C1=306pF, R1=9.75k, C2=5.29nF, R2=26.5k, C3=106pF

500MHz target
Fvcxo: 500MHz
Fref: 31.25MHz
Si571 Slope tune: 33ppm/V <=> Kv = 16.5kHz/V
BW: 10kHz
Phase margin: 50deg
Charge pump current: 4.8mA
--
C1=217pF, R1=13.7k, C2=3.75nF, R2=37.3k, C3=75.6pF

AD9510BCPZ

C229 300pF
R233 9k76
C239 5.6nF
R244 26k7
C241 110pF

Adjust these components for the targeted Frequency and PLL configuration.
Use ADIsimCLK with Si571 parameters given below.

OSC6
SDA
SCL
OE
VDD
GND
VC
CLK+
CLK-
571AMB001871DG
C288 100nF
CKSi_P
CKSi_N
R245 200
R248 200

Si571 Custom part

Fcenter : 352.37MHz
Temperature stability: 20ppm
Slope tune : 33ppm/V
Minimum APR: +/- 12ppm => OK for ESRF accelerator master source variation (RF correction)
Output level : LVPECL
I2C address : 0x55

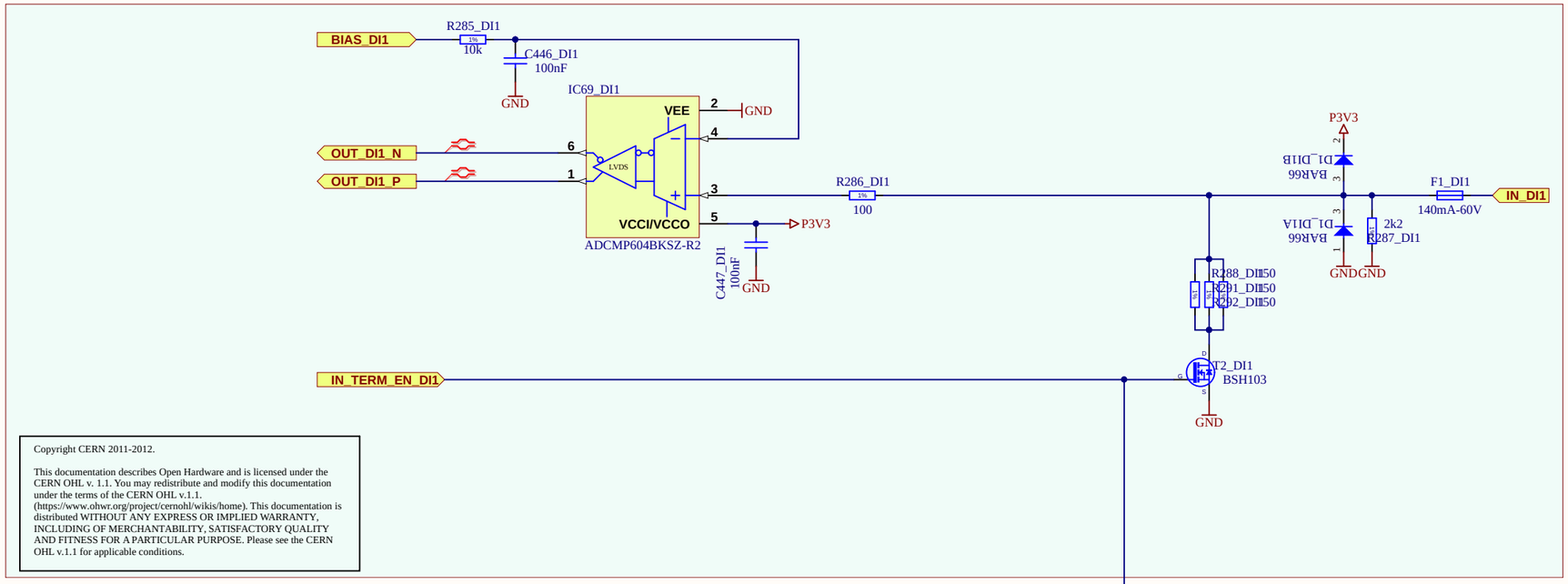
IC90
P5V0
IN
IN
SHDN
NC
NC
EP
GND
OUT
OUT
NC
NC
NC
BYP
P3V3_RFVCXO
C473 1uF
10uF EC8
C474 10nF
LT1763IDE-3.3#PBF

IC52
SETMAX
SETMIN
LEN
IN
IN
EN
VCC
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
GND
EP
VBB
VEF
VCF
FTUNE
Q
Q
CASC
CASC
RF_FINEDEL0
RF_FINEDEL1
RF_FINEDEL2
RF_FINEDEL3
RF_FINEDEL4
RF_FINEDEL5
RF_FINEDEL6
RF_FINEDEL7
RF_FINEDEL8
RF_FINEDEL9
RF_DEL_P
RF_DEL_N
R207 4k7
R211 49R9
R222 49R9
R223 49R9
C227 100nF
R227 2k
C228 10nF
SY89296UMG

IC65
CLK
nCLK
NC
VREF
VDD
VDD
VDD
GND
EP
Q0
nQ0
Q1
nQ1
Q2
nQ2
Q3
nQ3
Q4
nQ4
Q5
nQ5
RF_SYNC_P1
RF_SYNC_N1
RF_SYNC_P2
RF_SYNC_N2
RF_SYNC_P3
RF_SYNC_N3
RF_SYNC_P4
RF_SYNC_N4
RF_SYNC_P5
RF_SYNC_N5
RF_SYNC_P6
RF_SYNC_N6
R269 49R9
R270 49R9
R271 49R9
C249 100nF
C250 100nF
C251 100nF
8P34S1106NLGI
RF_SPLIT_signals
Net Class
PCB Rule
RF_SYNC_P[1..6]
RF_SYNC_N[1..6]
RF_SYNC_P[1..6]
RF_SYNC_N[1..6]

C308 100nF
C314 100nF
C317 100nF
C322 100nF
C324 100nF
C374 100nF
C375 100nF
C377 100nF
C378 100nF
C384 100nF
C385 100nF
C387 100nF
C388 100nF
C390 100nF
L34 220R@100MHz

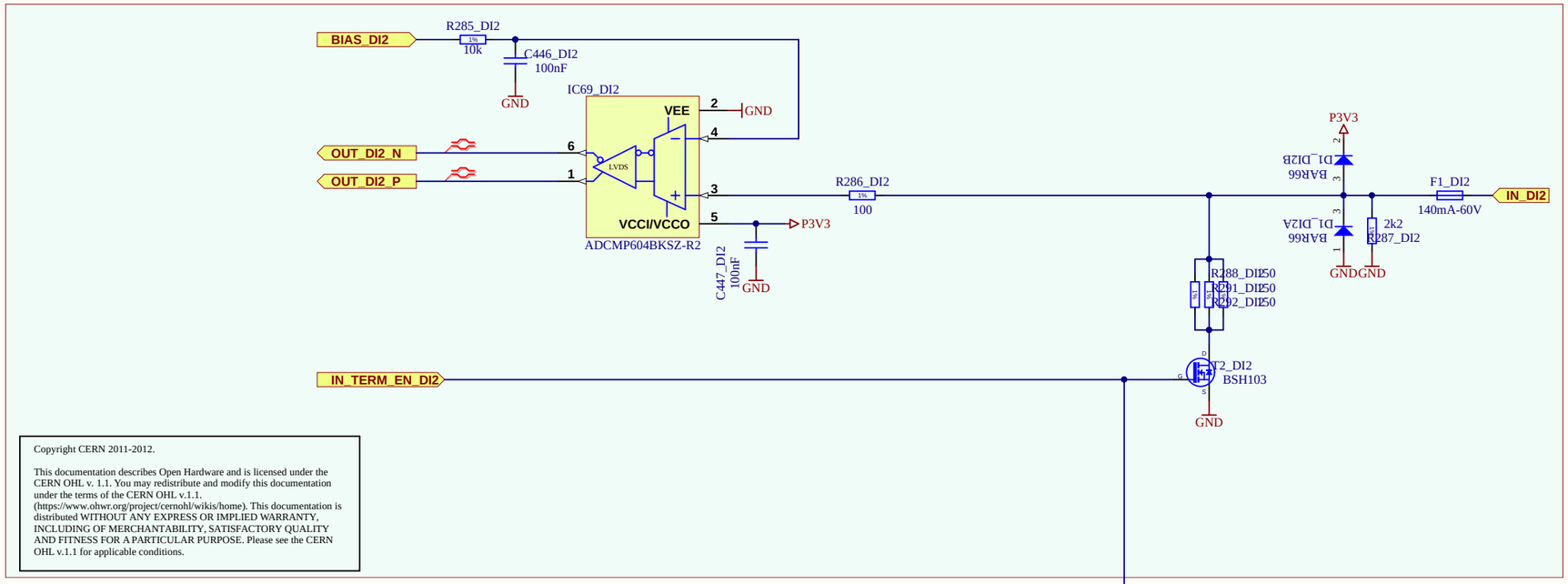
ESRF The European Synchrotron	Doc. Num.: -	Ver.: B	Sheet: 7 of 36
	Project: CITY		
	Sheet: DDS RF Clocking	Rev. 2	Date 03/2020
	File: CITY_DDS_RF_clocking.SchDoc		Author broquet
		SVN:	



Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

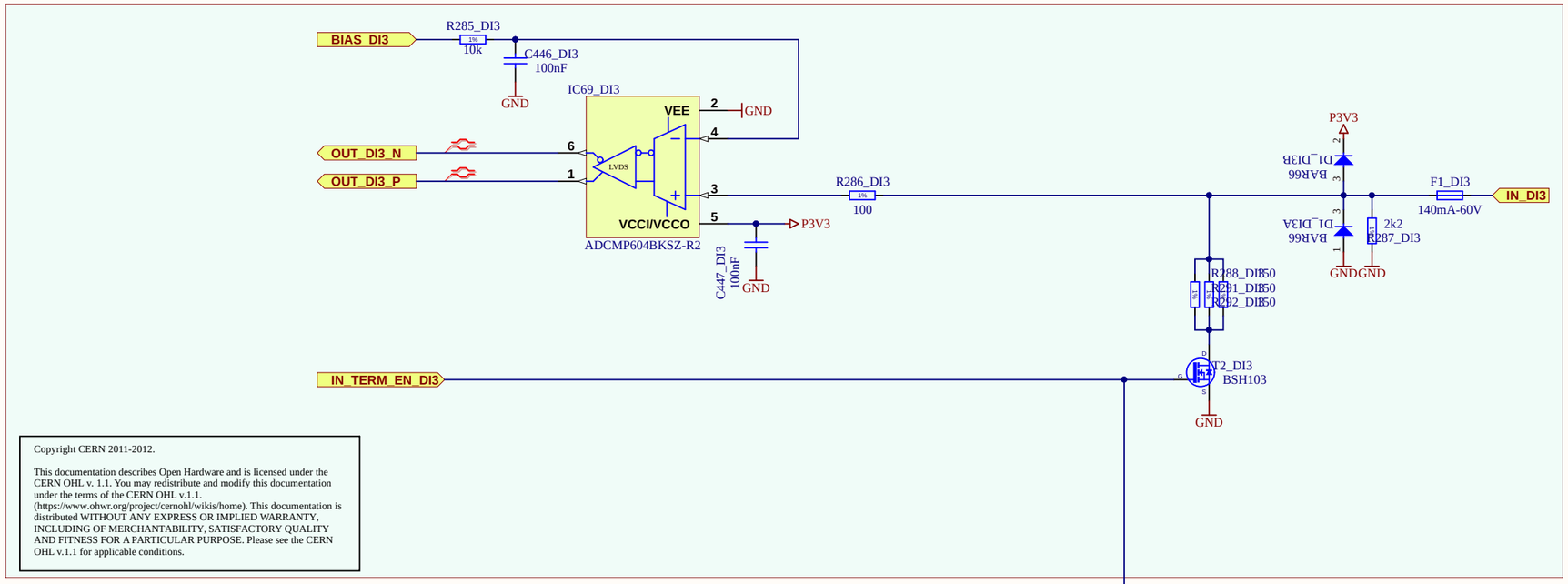
ESRF The European Synchrotron	Doc. Num.:	Ver.: B	Sheet: 8.1of 36
	Project: CITY		
	Sheet: DI 2 channels		
	File: CITY_DI_1channel.SchDoc		

Rev.	Date	Author
2	03/2020	broquet
	SVN:	



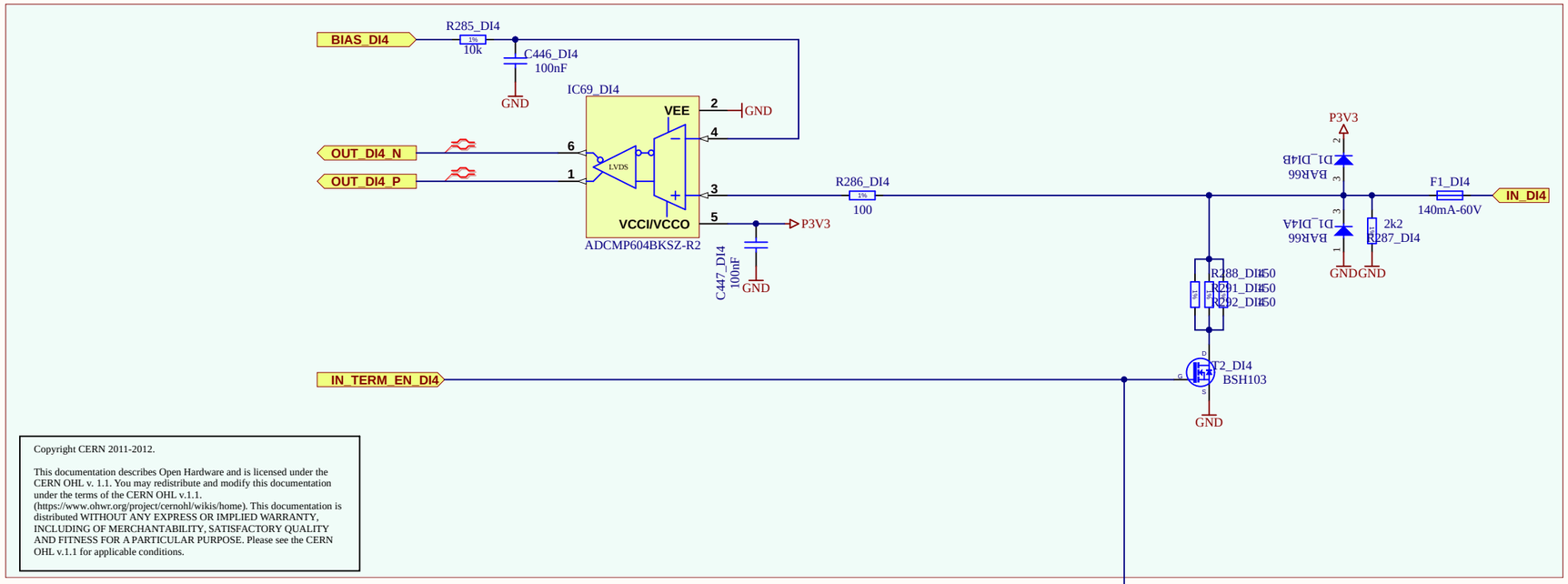
Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

ESRF The European Synchrotron	Doc. Num.:	Ver.: B	Sheet: 8.2 of 36
	Project: CITY		
	Sheet: DI 2 channels	Rev. 2	Date 03/2020 Author broquet
	File: CITY_DI_1channel.SchDoc	SVN:	



Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

ESRF The European Synchrotron	Doc. Num.:	Ver.: B	Sheet: 8.3of 36	
	Project: CITY			
	Sheet: DI 2 channels	Rev.	Date	Author
	File: CITY_DI_1channel.SchDoc	2	03/2020	broquet
		SVN:		



Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

ESRF The European Synchrotron	Doc. Num.:	Ver.: B	Sheet: 8.4of 36
	Project: CITY		
	Sheet: DI 2 channels		
	File: CITY_DI_1channel.SchDoc		

Rev.	Date	Author
2	03/2020	broquet
	SVN:	

Internal pull-down on Reset pin.

IC73_DO1
NBSG53AMNG

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

IC54_DO1
SY89296UMG

IC74_DO1
MAX7311ATG+T

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

IC75_DO1A
SY100EPT23LZG

IC78_DO1
NB3L553MNR4G

IC75_DO1B
SY100EPT23LZG

IC82_DO1
NB3L553MNR4G

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

Doc. Num.: -	Ver.: B	Sheet: 9.1 of 36	
Project: CITY			
Sheet: DO 2 channels			
File: CITY_DO_2channels.SchDoc			

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-	-	-
-	-	-
2	03/2020	broquet
Rev.	Date	Author
SVN:		

Internal pull-down on Reset pin.

IC73_DO2
NBSG53AMNG

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

IC54_DO2
SY89296UMG

IC74_DO2
MAX7311ATG+T

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

IC75_DO2A
SY100EPT23LZG

IC78_DO2
NB3L553MNR4G

IC75_DO2B
SY100EPT23LZG

IC82_DO2
NB3L553MNR4G

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

ESRF The European Synchrotron	Doc. Num.: -	Ver.: B	Sheet: 9.2 of 36
	Project: CITY		
	Sheet: DO 2 channels		
	File: CITY_DO_2channels.SchDoc		

Rev.	Date	Author
2	03/2020	broquet

SVN:

Internal pull-down on Reset pin.

IC73_DO3
NBSG53AMNG

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

IC54_DO3
SY89296UMG

IC74_DO3
MAX7311ATG+T

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

IC75_DO3A
SY100EPT23LZG

IC78_DO3
NB3L553MNR4G

IC75_DO3B
SY100EPT23LZG

IC82_DO3
NB3L553MNR4G

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

Doc. Num.: -	Ver.: B	Sheet: 9.3 of 36	
Project: CITY			
Sheet: DO 2 channels	Rev.	Date	Author
File: CITY_DO_2channels.SchDoc	2	03/2020	broquet
	SVN:		

Internal pull-down on Reset pin.

IC73_DO4
NBSG53AMNG

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

IC54_DO4
SY89296UMG

IC74_DO4
MAX7311ATG+T

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

IC75_DO4A
SY100EPT23LZG

IC78_DO4
NB3L553MNR4G

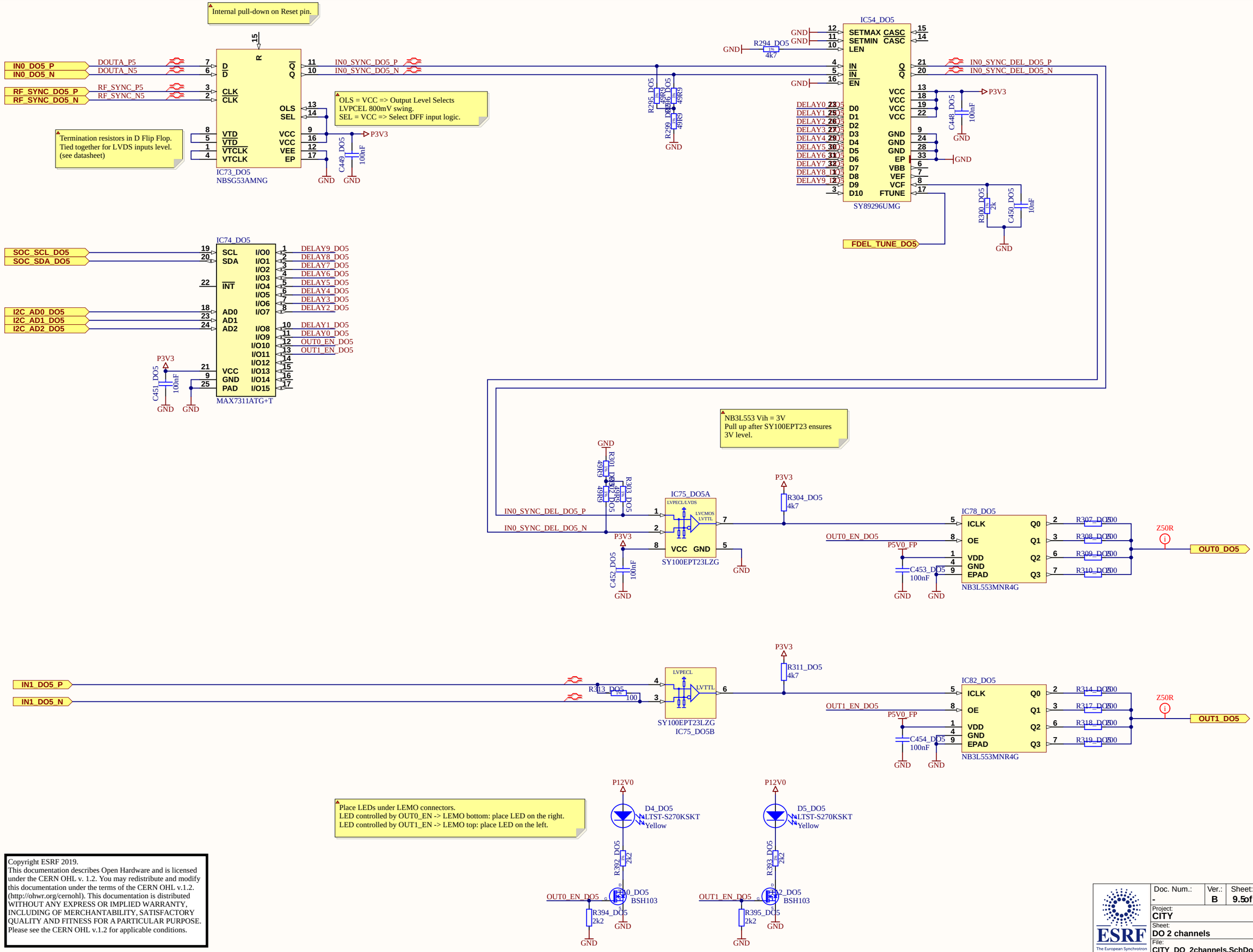
IC75_DO4B
SY100EPT23LZG

Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

ESRF The European Synchrotron	Doc. Num.: -	Ver.: B	Sheet: 9.4of 36
	Project: CITY		
	Sheet: DO 2 channels		
	File: CITY_DO_2channels.SchDoc		

Rev.	Date	Author
2	03/2020	broquet

SVN:



ESRF The European Synchrotron	Doc. Num.: -	Ver.: B	Sheet: 9.5of 36
	Project: CITY		
	Sheet: DO 2 channels		
	File: CITY_DO_2channels.SchDoc		

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-	-	-	
-	-	-	
2	03/2020	broquet	
Rev.	Date	Author	
SVN:			

Internal pull-down on Reset pin.

IC73_DO6
NBSG53AMNG

Termination resistors in D Flip Flop.
Tied together for LVDS inputs level.
(see datasheet)

OLS = VCC => Output Level Selects
LVPCEL 800mV swing.
SEL = VCC => Select DFF input logic.

IC54_DO6
SY89296UMG

IC74_DO6
MAX7311ATG+T

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures
3V level.

IC75_DO6A
SY100EPT23LZG

IC78_DO6
NB3L553MNR4G

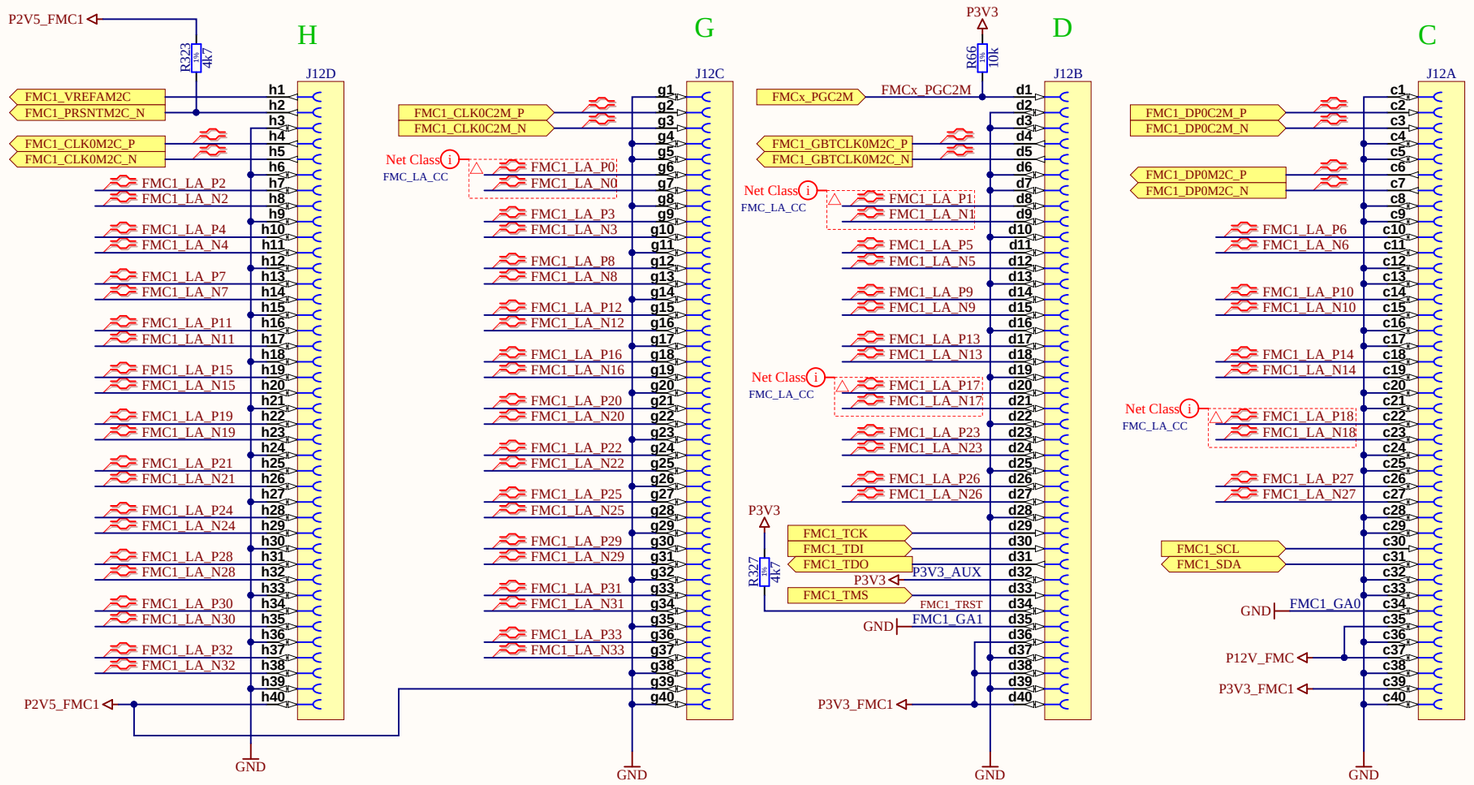
IC75_DO6B
SY100EPT23LZG

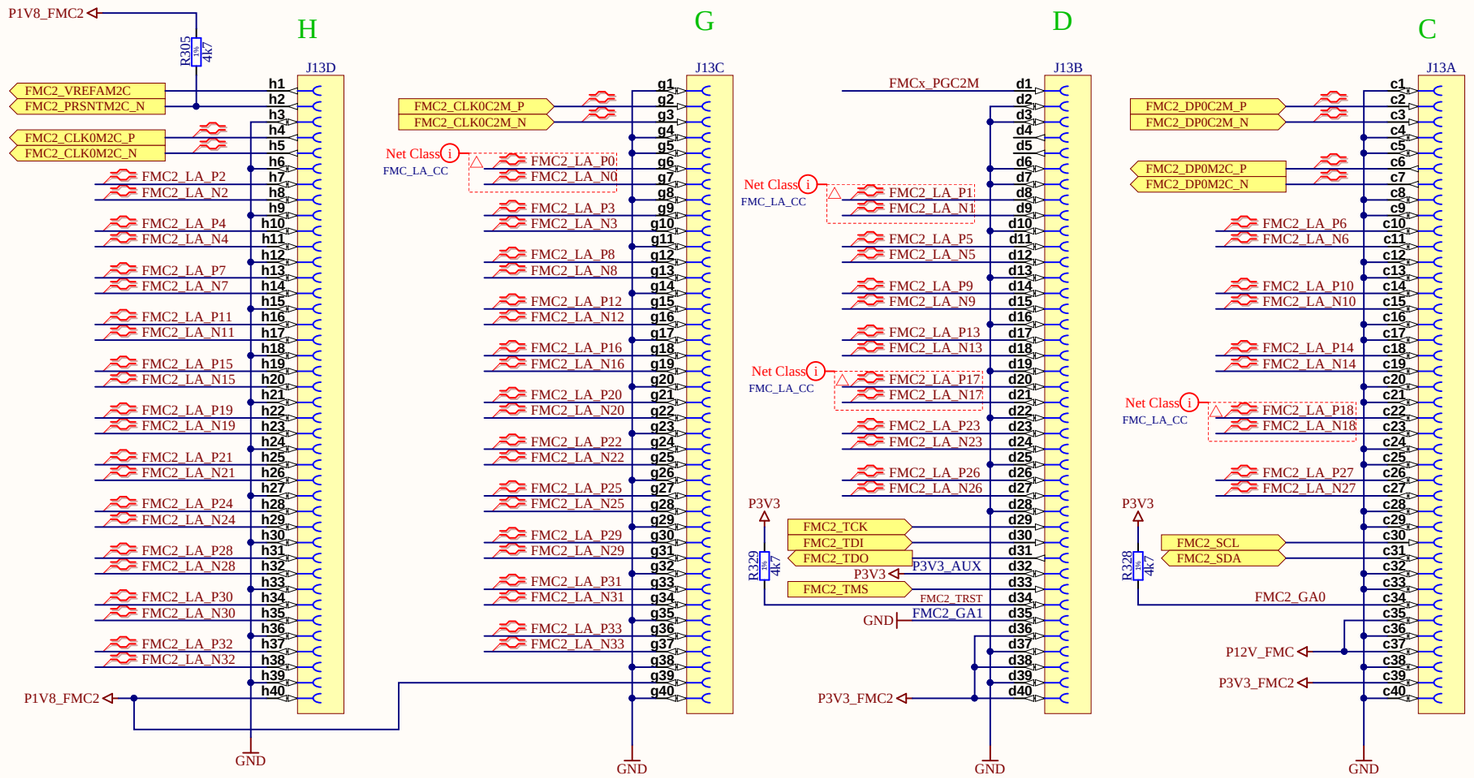
Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

ESRF The European Synchrotron	Doc. Num.: -	Ver.: B	Sheet: 9.6of 36
	Project: CITY		
	Sheet: DO 2 channels		
	File: CITY_DO_2channels.SchDoc		

Rev.	Date	Author
2	03/2020	broquet

SVN:





ESRF The European Synchrotron

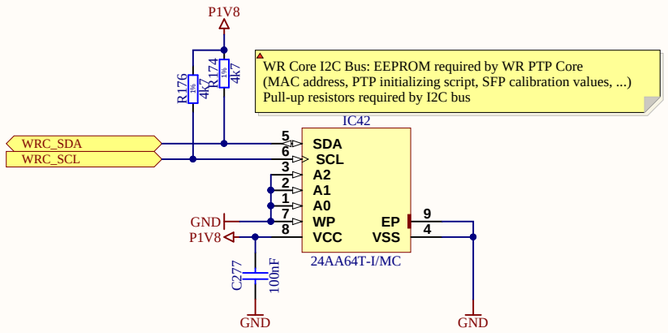
Doc. Num.:	Ver.:	Sheet:
	B	10 of 36

Project: CITY
Sheet: FMC Connectors 1 & 2
File: CITY_FMC.SchDoc

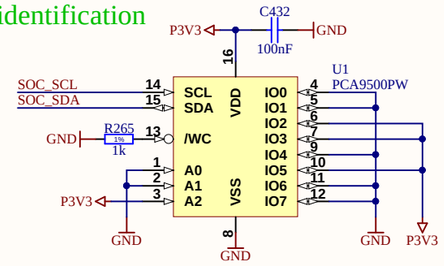
Rev.	Date	Author
2	03/2020	broquet

SVN:

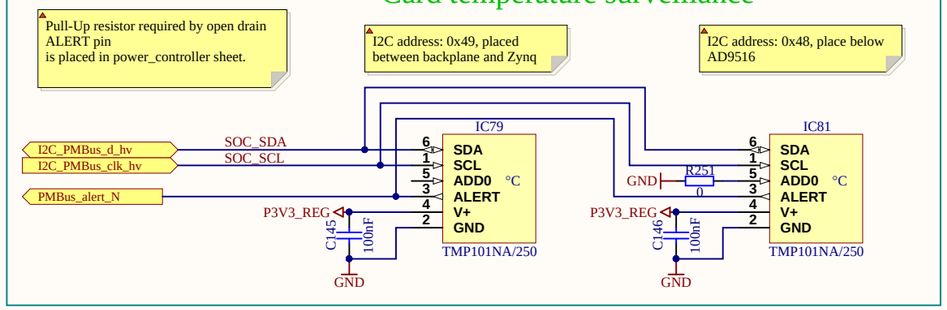
64 Kbit EEPROM (I2C @ 100 kHz max)



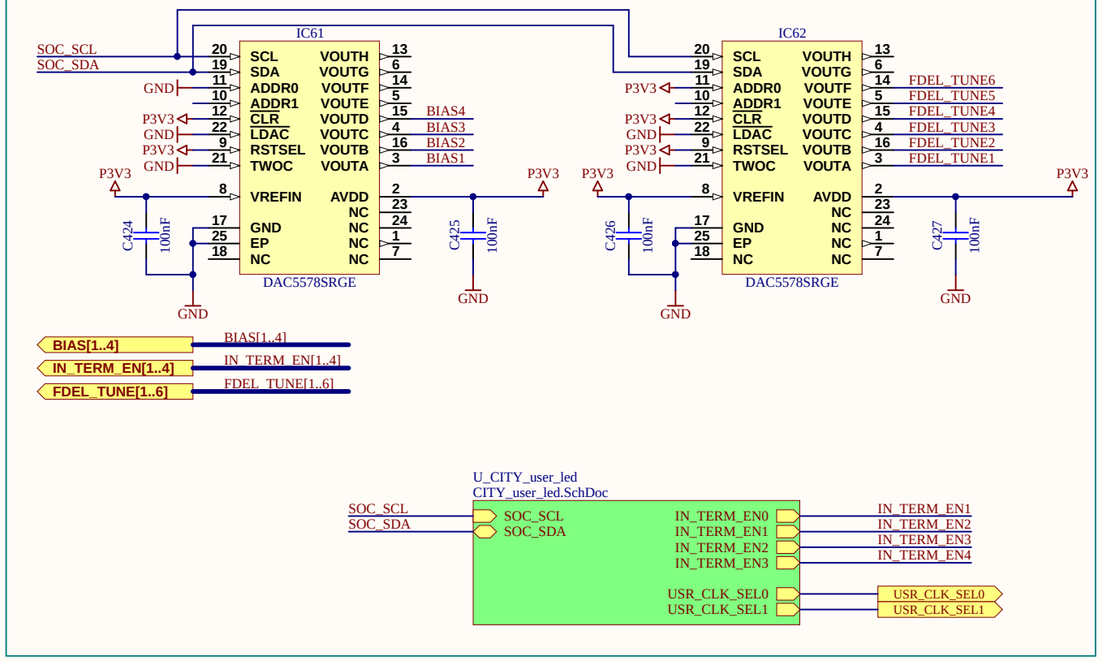
Board identification



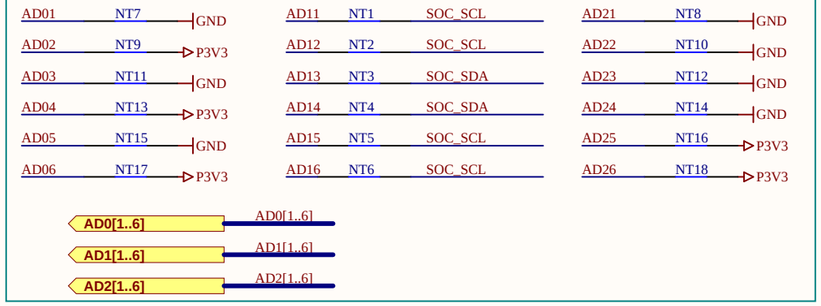
Card temperature surveillance

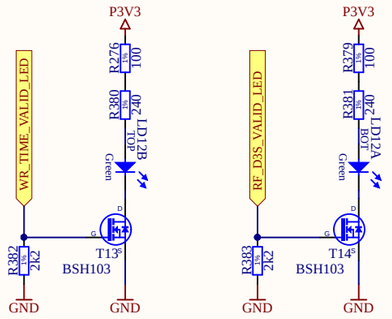


DACs for Inputs BIAS and Fine Delay Tune / User LED + GPIO

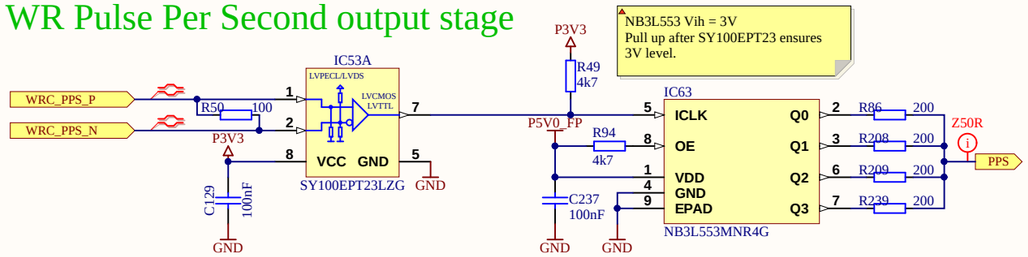


I2C address bus for DO channel IO registers





WR Pulse Per Second output stage



changelog

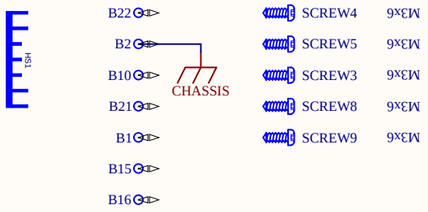
V2-0:
* several small component changes, not documented here
* power supply sequence improved
* bank 501 and all connected chips changed to 1.8V for full RGMII support
* PHY SPI wired to bank 35, in addition to existing MDIO
* UART changed to FT230X
* power controller UCD90120 GPIO rewired cause pull-downs; 2nd connecter added for use of TI adapter

V3-0:
* few small component changes, not documented here
* external patch-panel interrupt line to SoC
* i2c level converter ADUM1250 turned around cause i2c compliance problems
* D-sub 15 wiring change to follow CERN cabling convention
* TMP101 thermal sensors added

CITY V1-0:
* See the CHANGES.TXT document provided in the project

CITY V2-0:
* See CHANGES.TXT file and OHWR project issues.
* Re-routing some differential pairs

PCB mounting holes, screws & heatsink



I2C addresses

I2C addresses hex number are given in the 7bit format aligned to LSb (without R/W bit).
Example: I2C addr = 0x74 (1 1 1 0 1 0 0) --> Read access = 1 1 1 0 1 0 0 1 (0xE9)

WR Core I2C:
=========
24AA64T -> 0x50

SoC I2C (I2C PMBus):
==============
CITY_power-controller.SchDoc
UCD90120ARGC -> 0x5B

CITY_misc.SchDoc
TMP101(1) -> 0x48 (with ADD0 = 0)
TMP101(2) -> 0x49 (with ADD0 = Float)
DAC5578(1) -> 0x4C (with ADDR0 = GND, ADDR1 = float)
DAC5578(2) -> 0x4D (with ADDR0 = VCC, ADDR1 = float)
BOARD ID I/O -> 0x24 (with A0 = A1 = GND, A2 = VCC)
BOARD ID EEPROM -> 0x54 (with A0 = A1 = GND, A2 = VCC)

CITY_user_led.SchDoc
General IO control -> 0x25 (AD0 = VCC, AD1 = GND, AD2 = VCC)

DO_2channels.SchDoc (I/Os control: Finde delay, Output drivers enable)
0 -> 0x10 (AD0 = GND, AD1 = SCL, AD2 = GND)
1 -> 0x11 (AD0 = VCC, AD1 = SCL, AD2 = GND)
2 -> 0x12 (AD0 = GND, AD1 = SDA, AD2 = GND)
3 -> 0x13 (AD0 = VCC, AD1 = SDA, AD2 = GND)
4 -> 0x14 (AD0 = GND, AD1 = SCL, AD2 = VCC)
5 -> 0x15 (AD0 = VCC, AD1 = SCL, AD2 = VCC)

RF_Clocking.SchDoc
RF clock delay for outputs synchronization -> 0x16 (AD0 = GND, AD1 = SDA, AD2 = VCC)
Si571 -> 0x55 (default, fixed).

ESRF
LOGO PCB

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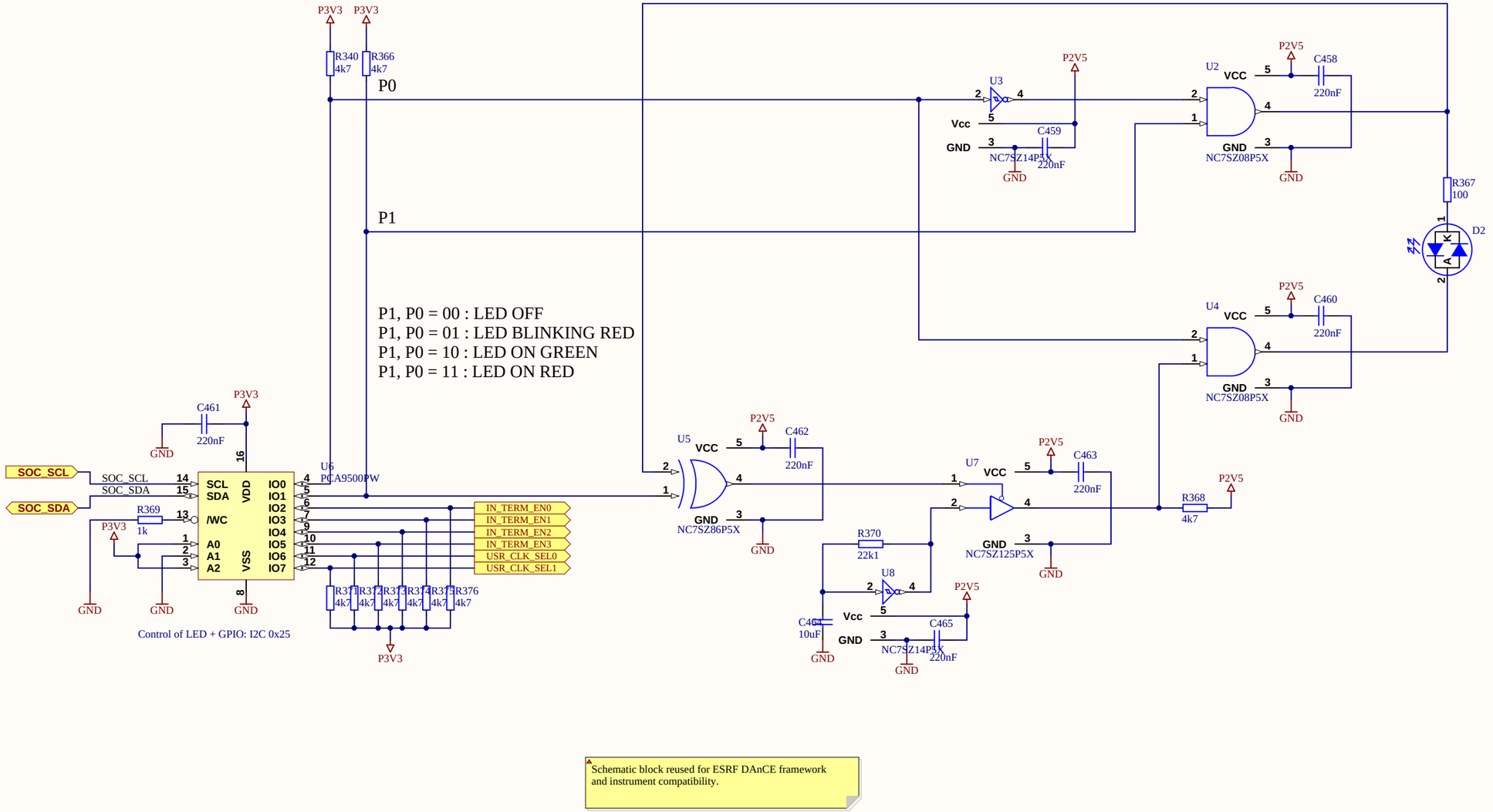
	Project: CITY			
	Sheet: Misc	Rev.	Date	Author
	File: CITY_misc.SchDoc	2	03/2020	broquet
		SVN:		



Schematic block reused for ESRF DAnCE framework and instrument compatibility.

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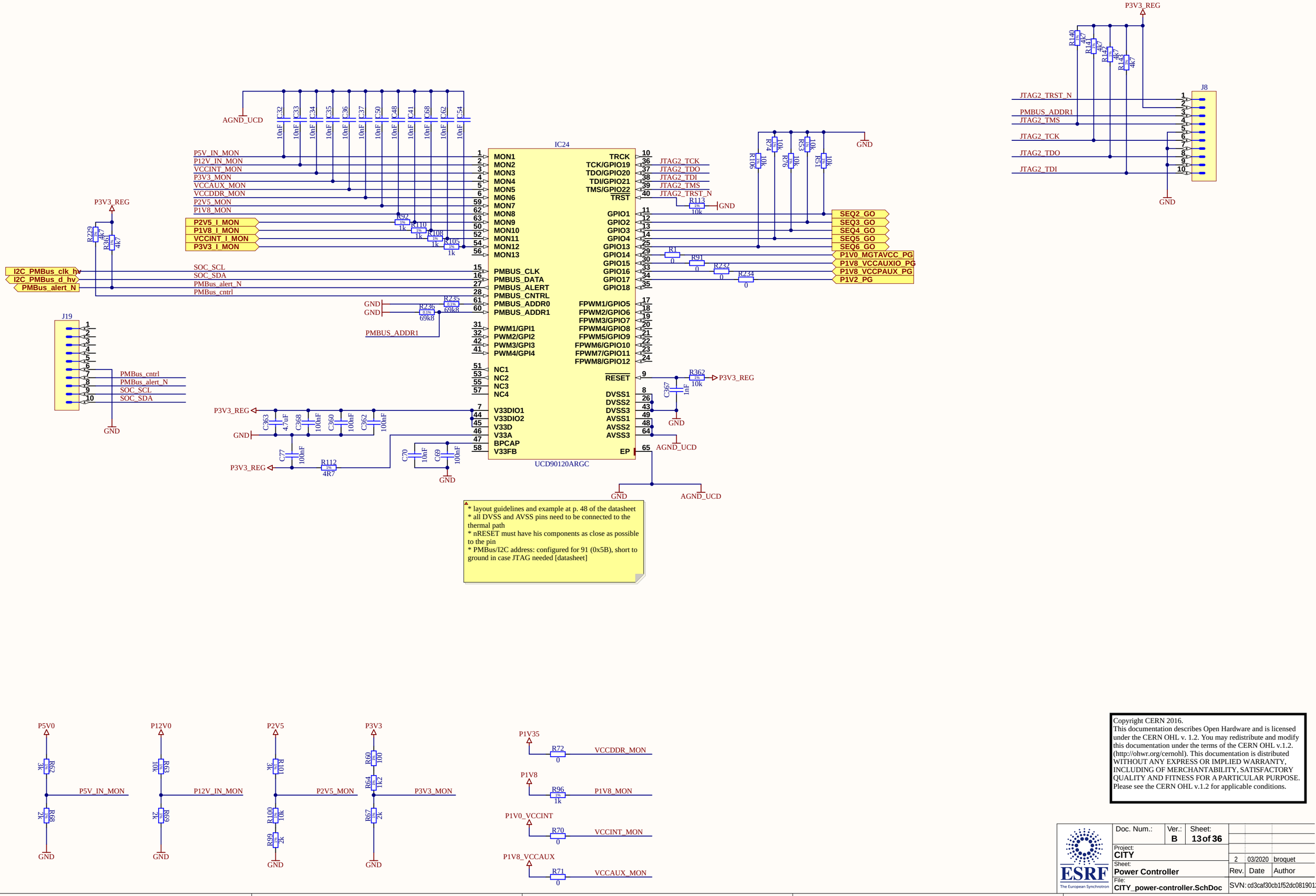
	Project: CITY		
	Sheet: User LED	Rev. 2	Date 03/2020 Author broquet
	File: CITY_user_led.SchDoc	SVN:	



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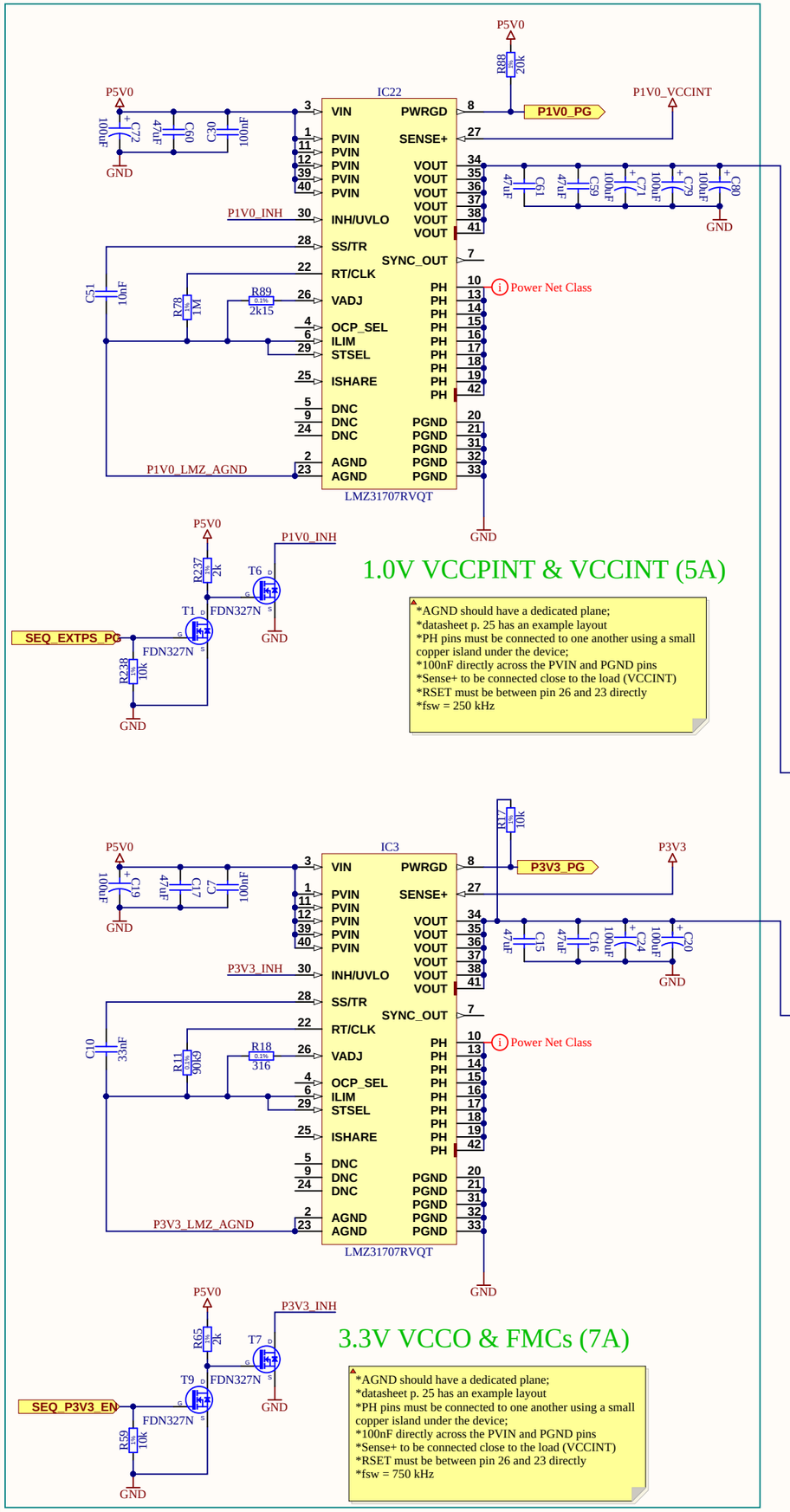
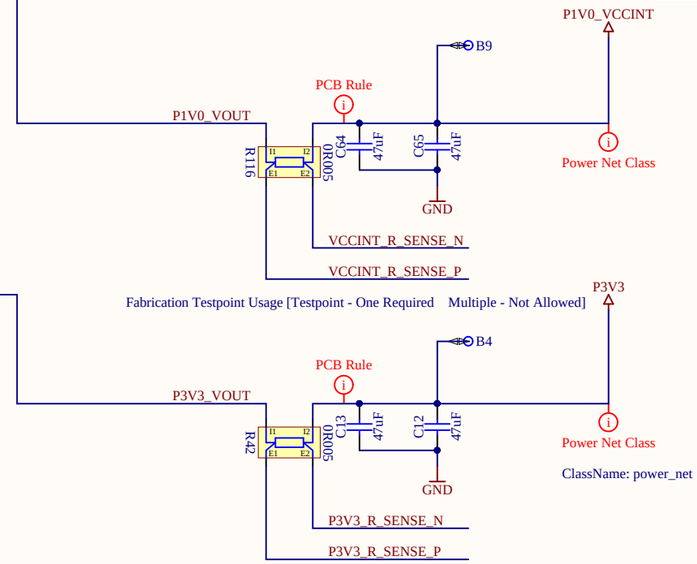
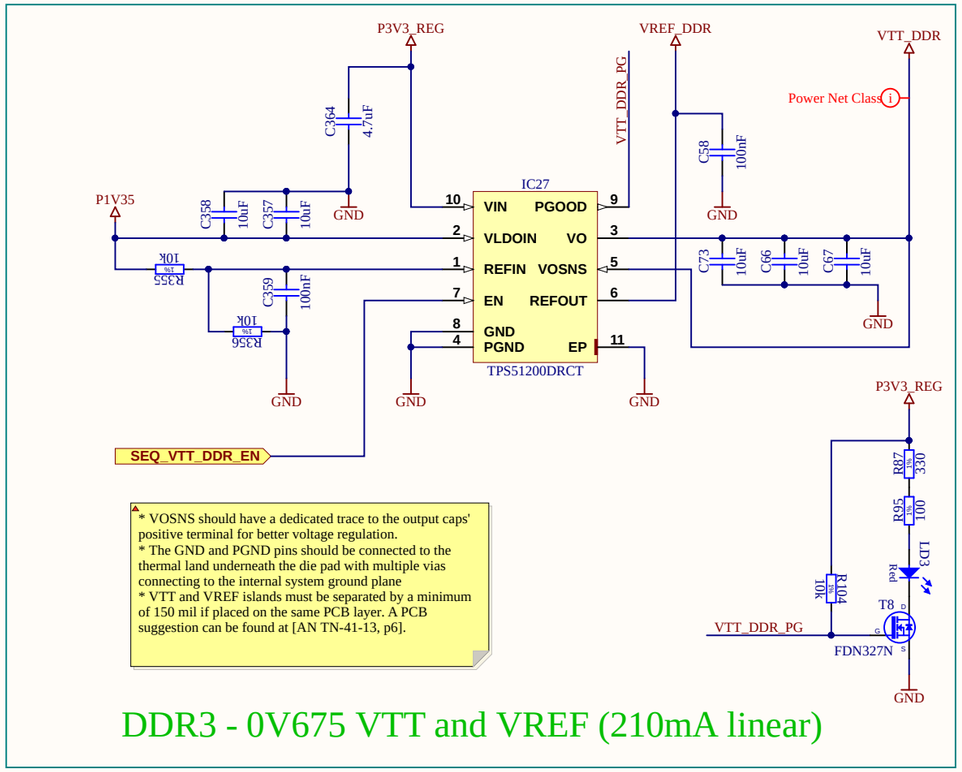
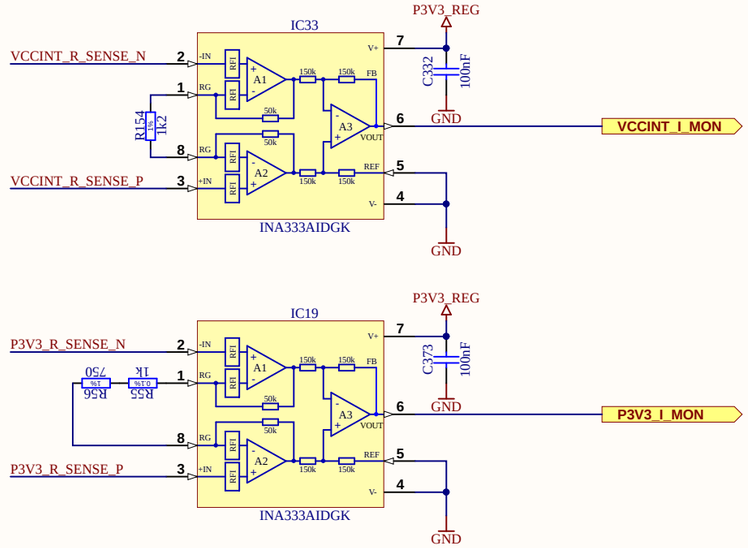
	Project: CITY		
	Sheet: Power Controller	Rev. 2	Date 03/2020 Author broquet
	File: CITY_power-controller.SchDoc	SVN: cd3caf30cb1f52dc081901255772	









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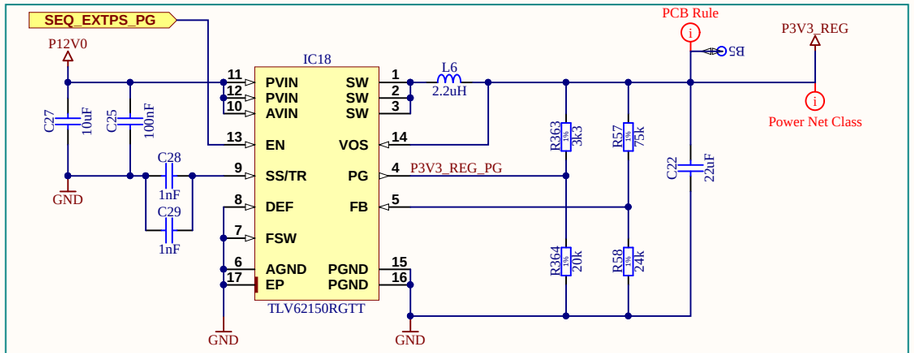
Sheet: Supplies 1			
File: CITY_power-supplies.SchDoc			

Rev.	Date	Author
2	03/2020	broquet

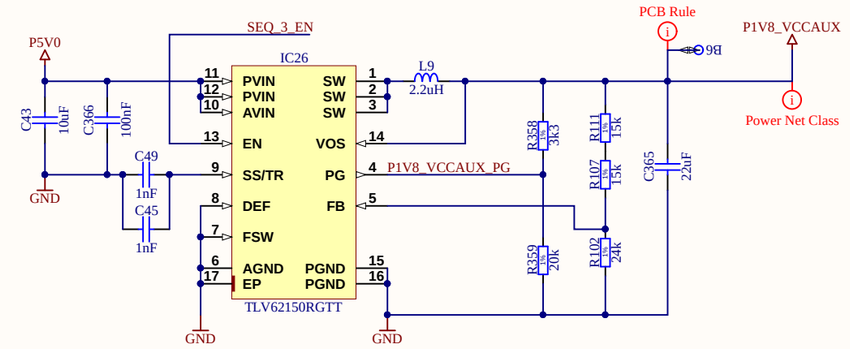
SVN: cd3caf30cb1f52dc081901255772



3.3V VREG (1A)

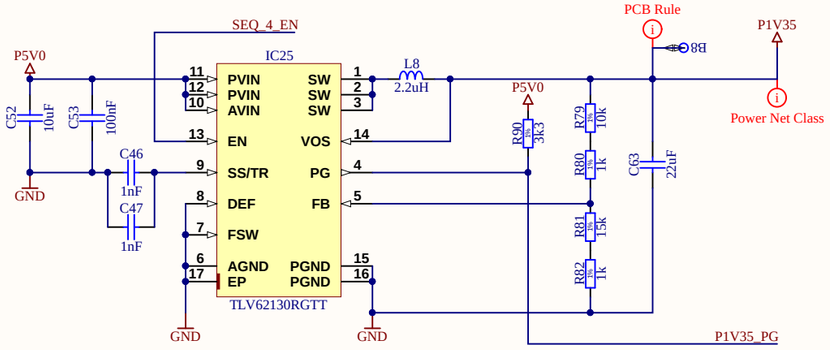
*fsw = 2.5 MHz
*layout example at datasheet p.21
*100nF directly across the AVIN and AGND pins
* Not only used for the LDOs at this page!

Fabrication Testpoint Usage [Testpoint - One Required Multiple - Not Allowed]



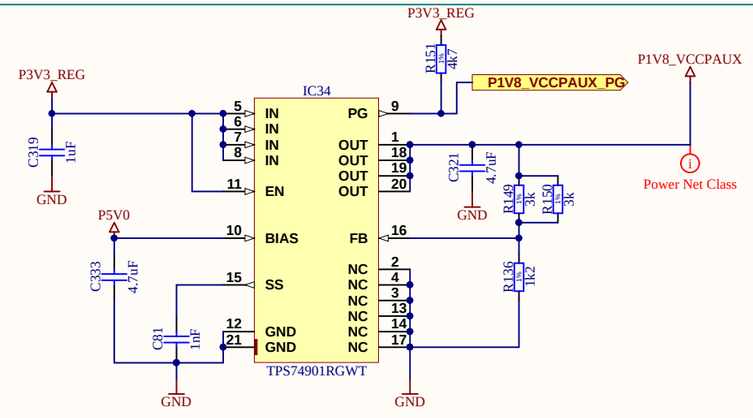
1.8V VCCAUX (800mA)

*fsw = 2.5 MHz
*layout example at datasheet p.21
*100nF directly across the AVIN and AGND pins



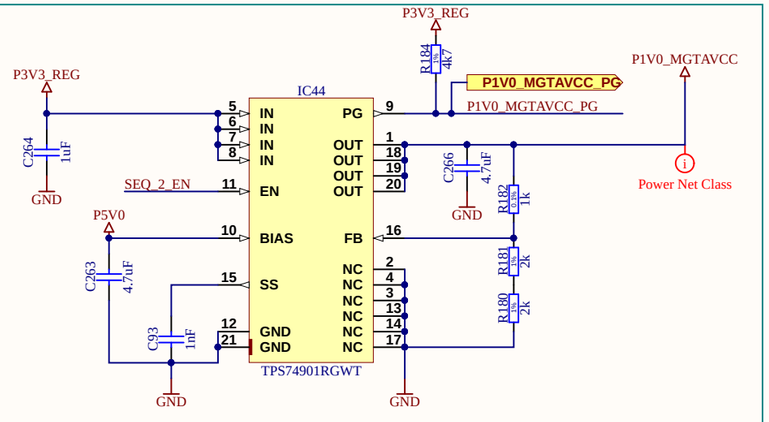
1.35V VCCDDR (1.1A)

*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins



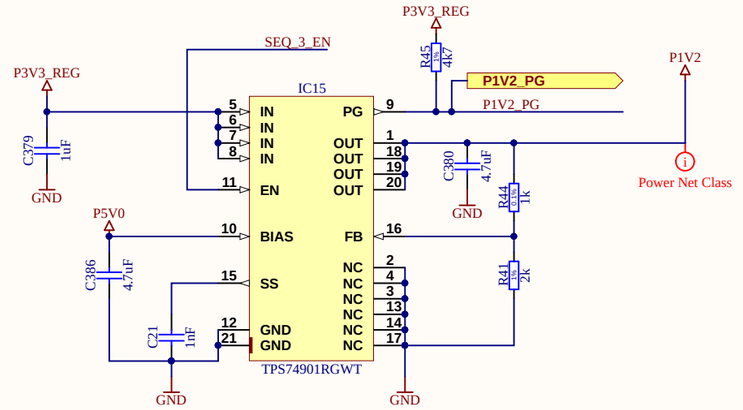
1.8V VCCPAUX (120mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; only 180 mW dissipation with a theta_JA of 120 °C/W.



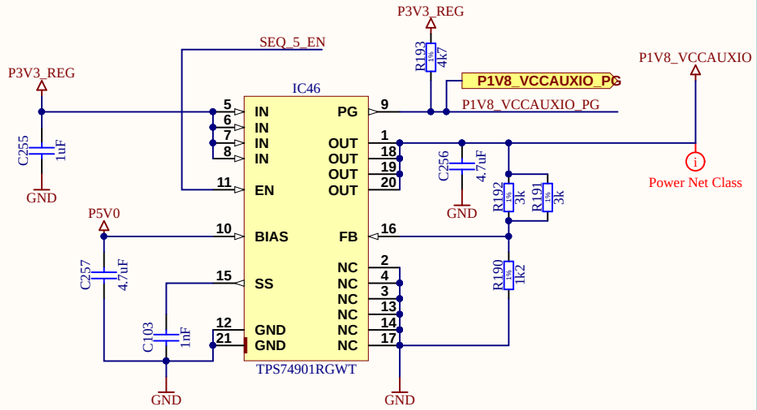
1.0V MGTAVCC (150mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 345 mW dissipation with a theta_JA of 120 °C/W.



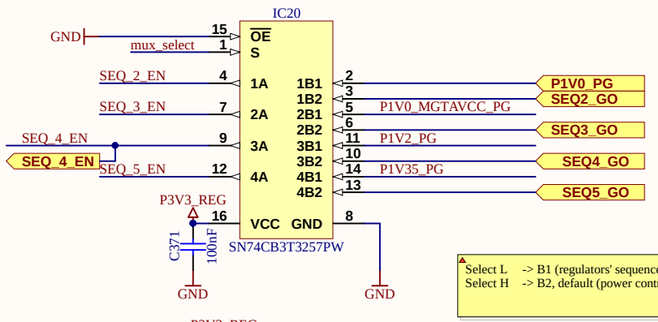
1.2V all (130mA linear)

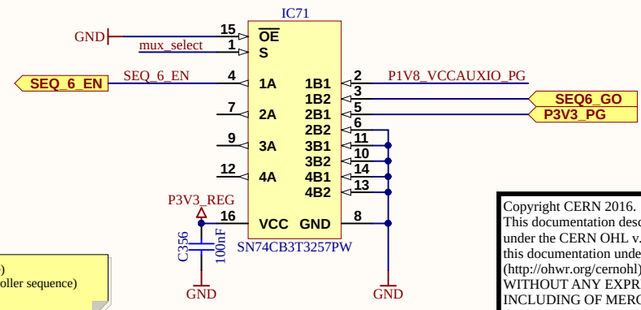
*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a theta_JA of 120 °C/W.

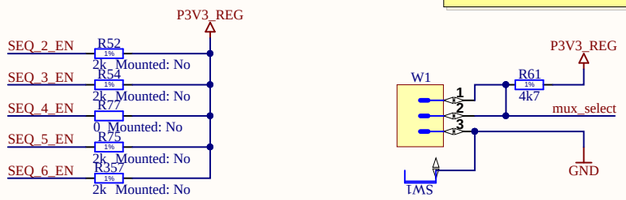


1.8V VCCAUX_IO (130mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a theta_JA of 120 °C/W.







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File: CITY_power-supplies-2.SchDoc

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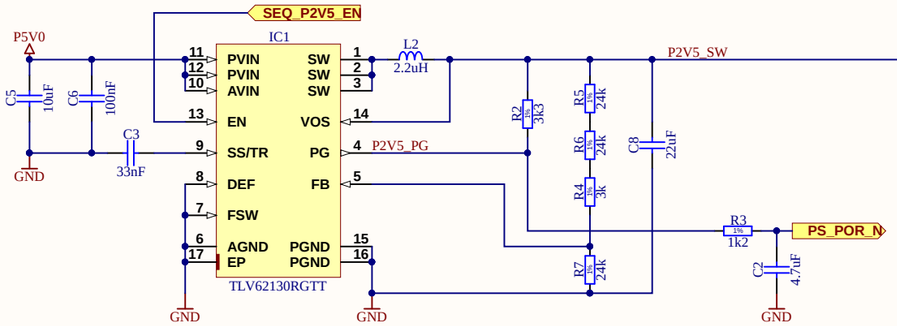
SVN: cd3caf30cb1f52dc081901255772

2.5V all (3A max)

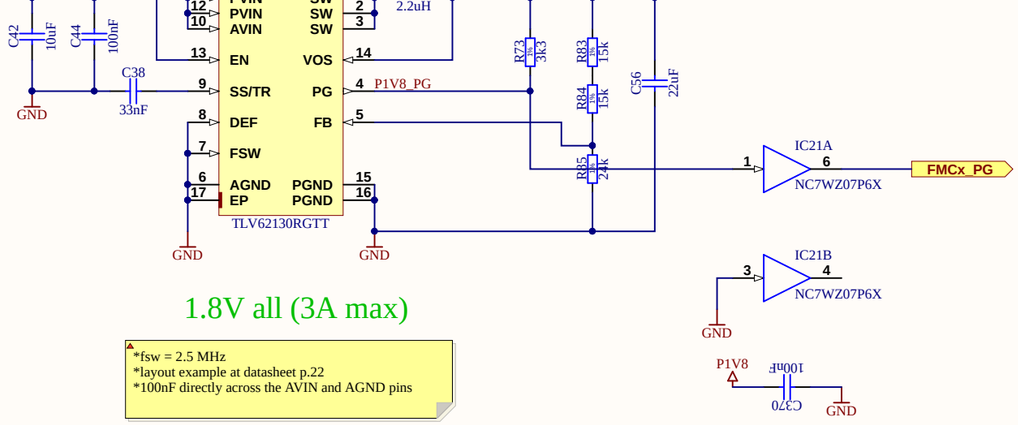


*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins

RC delay (tau=21ms) to provide the required 40ms after VCCO_0 assertion before deasserting PS_POR_B [DS191 p.18] to 2.31V (Vcc*0.7).

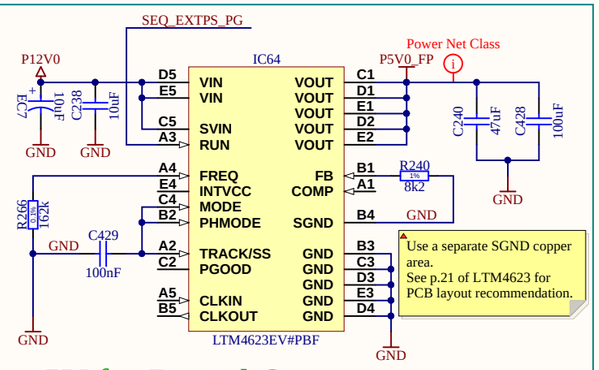
Power ON LED

1.8V all (3A max)

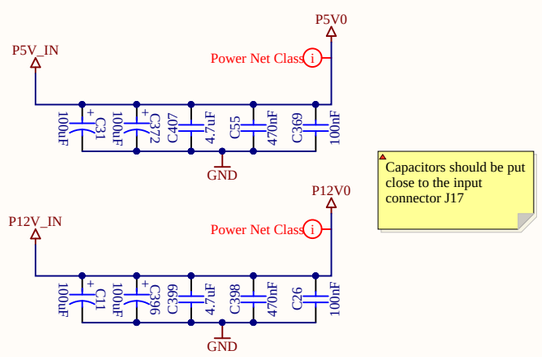


*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins

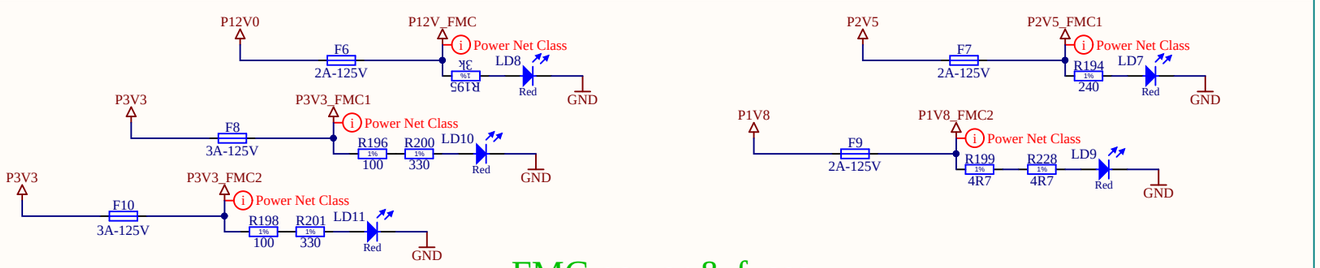
5V for Digital Output stages

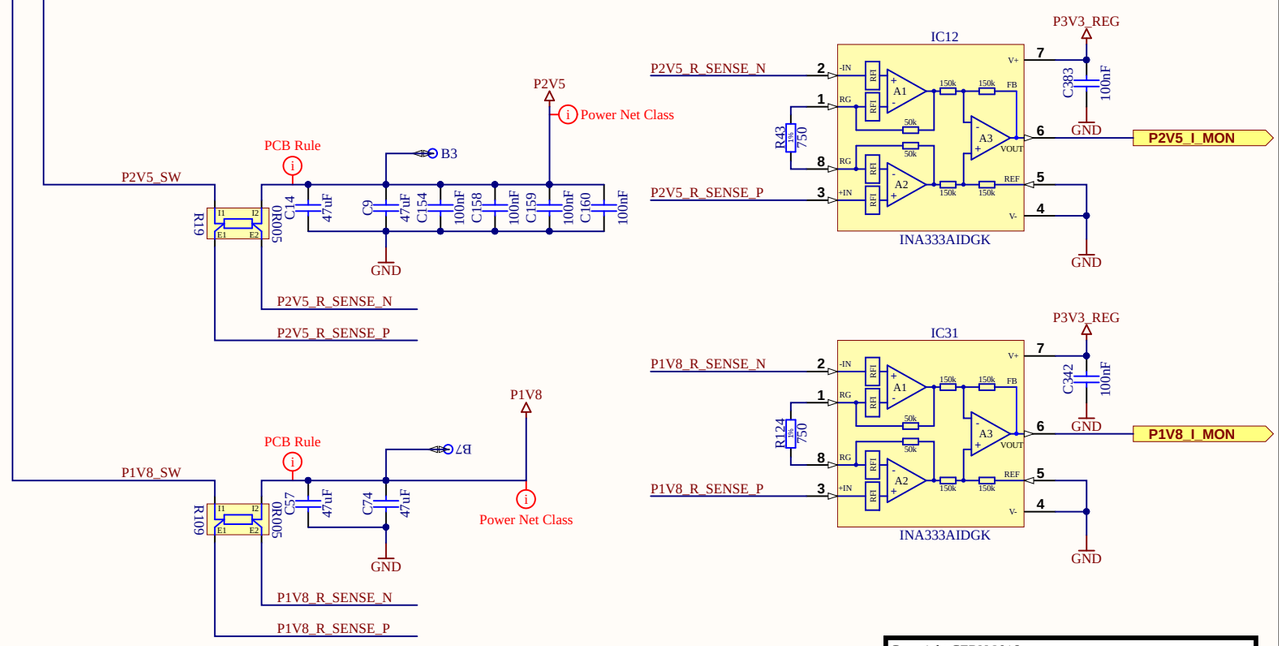


Power supply decoupling

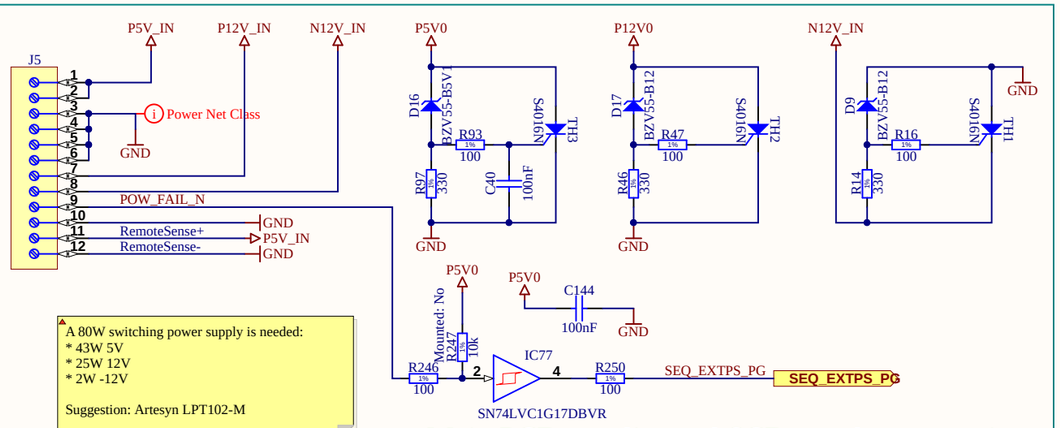


FMC power & fuses



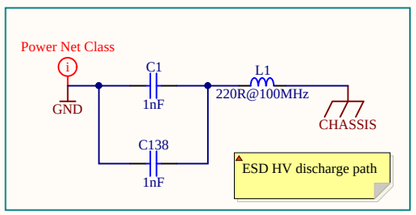


Main PCB supplies and SCR crowbar protection



A 80W switching power supply is needed:
* 43W 5V
* 25W 12V
* 2W -12V

Suggestion: Artesyn LPT102-M



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	Sheet: Supplies 3		
	File: CITY_power-supplies-3.SchDoc		

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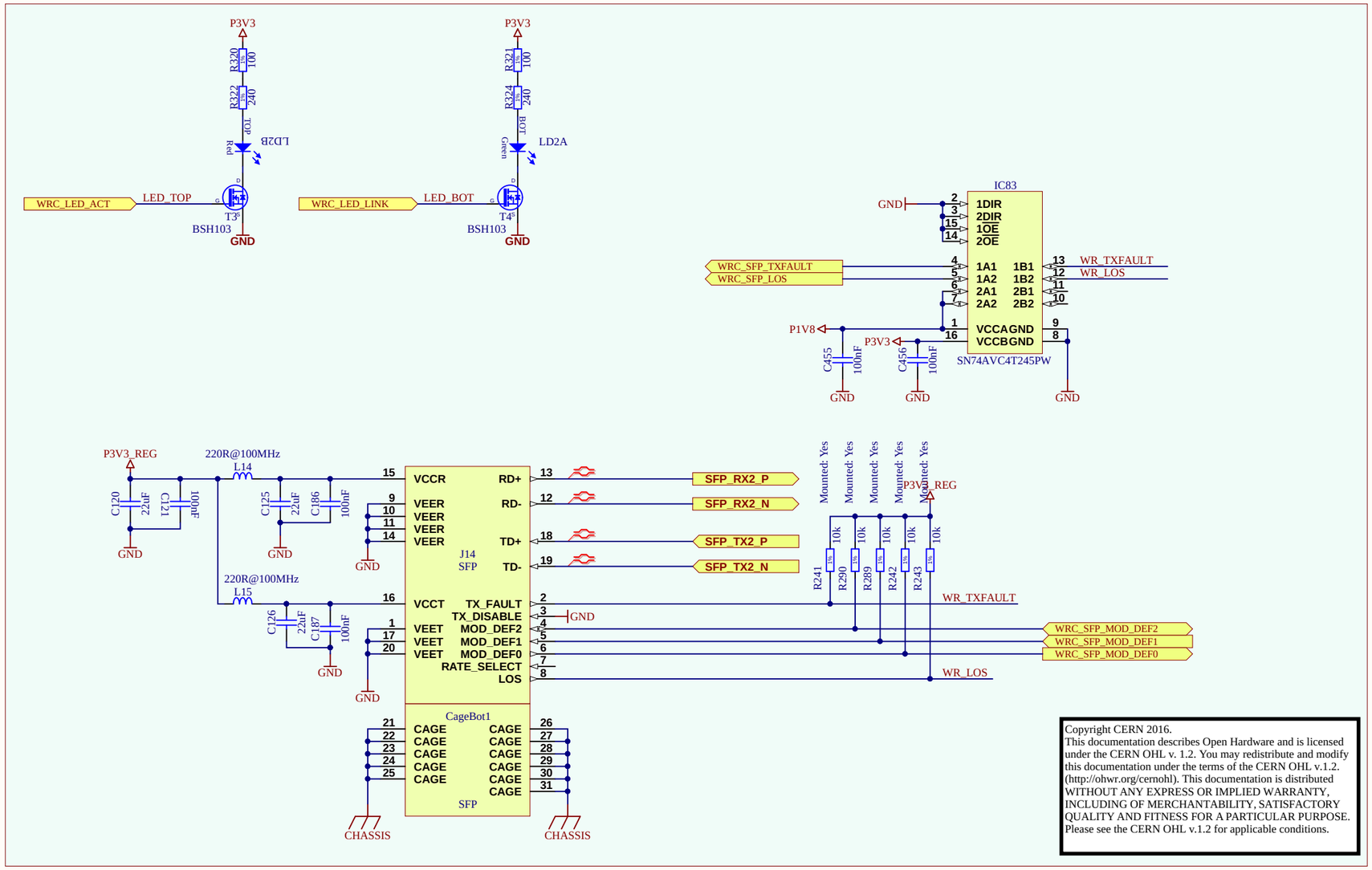
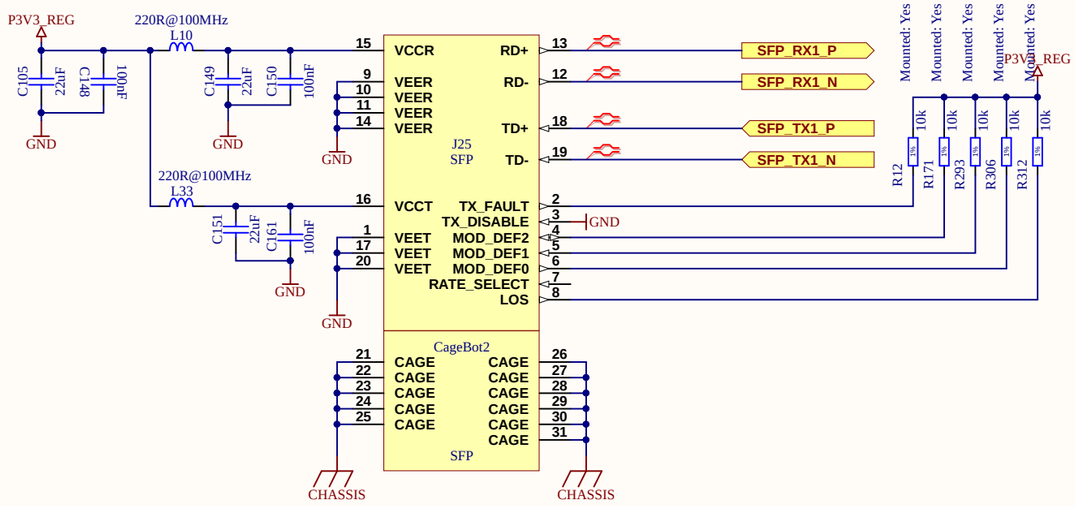
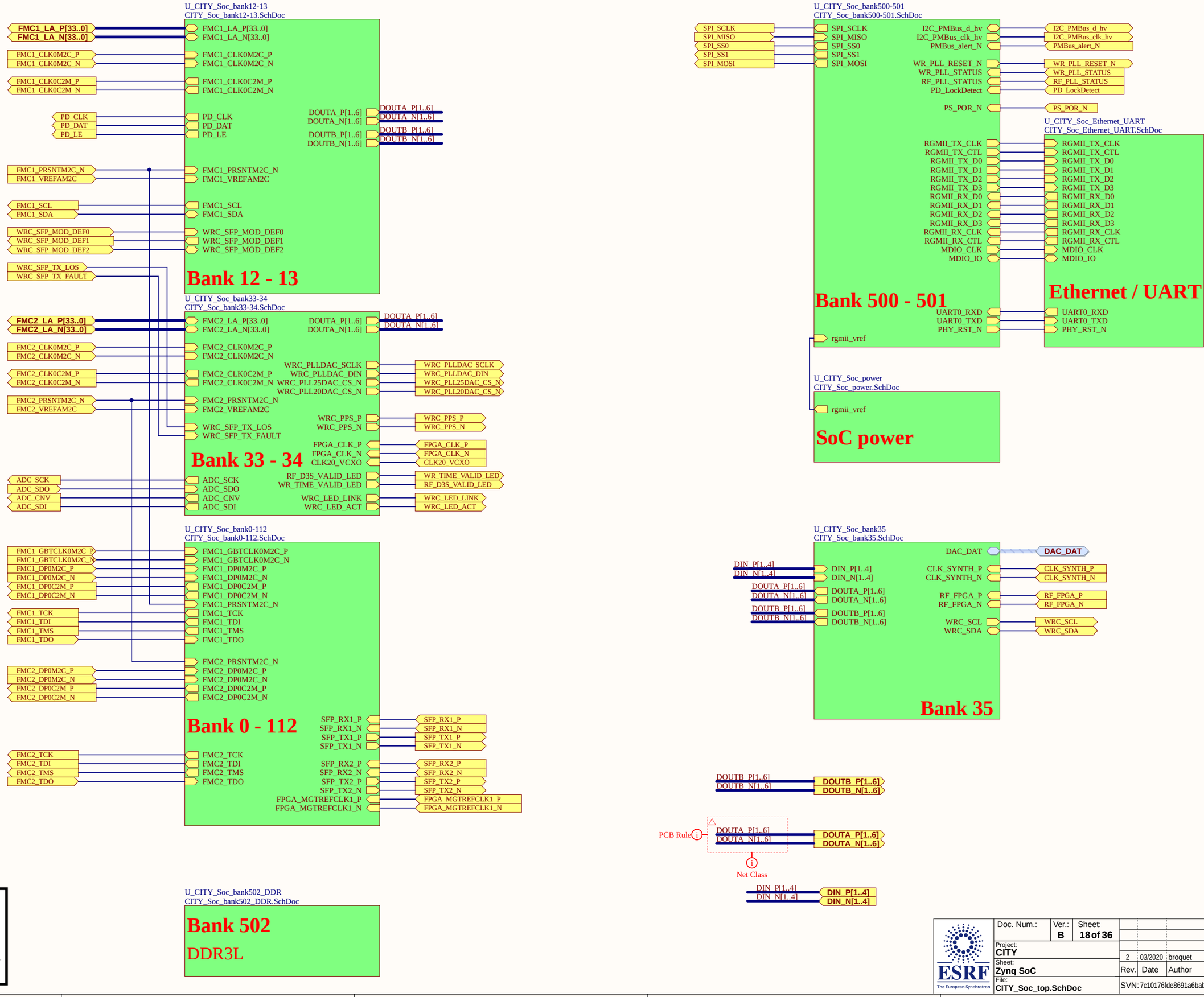
SVN:			

Based on SPEC schematics, EDA-02189-V4-0 p. 2 & 16

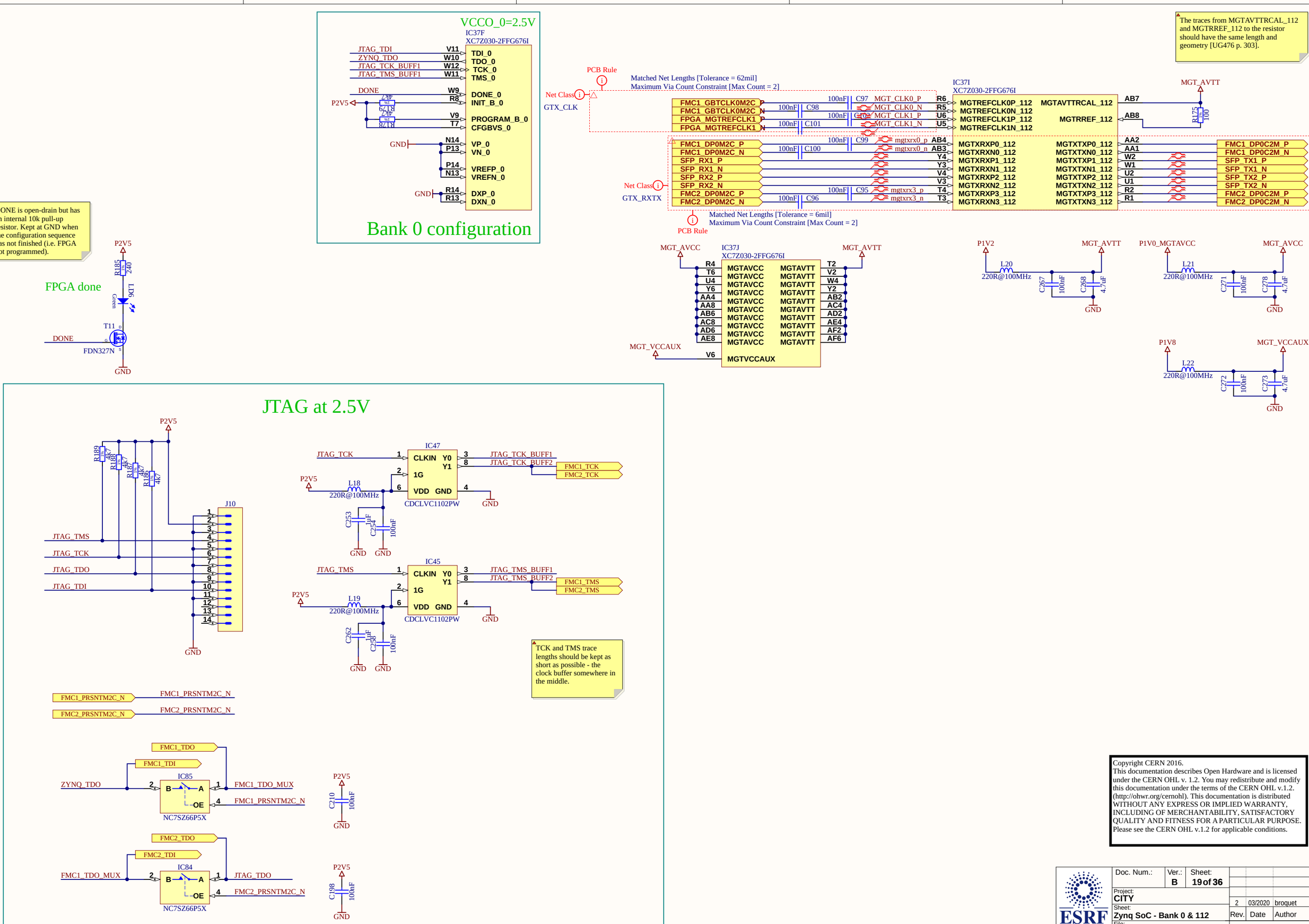




ESRF The European Synchrotron	Doc. Num.:	Ver.: B	Sheet: 17 of 36	
	Project: CITY			
	Sheet: SFP		Rev. 2	Date 03/2020 Author broquet
	File: CITY_SFP.SchDoc		SVN:	



ESRF The European Synchrotron	Doc. Num.:	Ver.: B	Sheet: 18 of 36
	Project: CITY		
	Sheet: Zynq SoC	2 / Rev.	03/2020 / Date
	File: CITY_Soc_top.SchDoc	broquet / Author	
	SVN: 7c10176fde8691a6bab03d39448		



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	Project: CITY		
	Sheet: Zynq SoC - Bank 0 & 112		
	File: CITY_Soc_bank0-112.SchDoc		

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SVN:		

VCCO_12=2.5V

IC37A
XC7Z030-2FFG676I

BANK 12

IO_0_12	W14	WRC_SFP_MOD_DEF1
IO_L1P_T0_12	Y12	FMC1_LA_P2
IO_L1N_T0_12	Y11	FMC1_LA_N2
IO_L2P_T0_12	AB12	FMC1_LA_P3
IO_L2N_T0_12	AC11	FMC1_LA_N3
IO_L3P_T0_DQS_12	Y10	FMC1_LA_P4
IO_L3N_T0_DQS_12	AA10	FMC1_LA_N4
IO_L4P_T0_12	AB11	FMC1_LA_P6
IO_L4N_T0_12	AB10	FMC1_LA_N6
IO_L5P_T0_12	W13	FMC1_LA_P5
IO_L5N_T0_12	Y13	FMC1_LA_N5
IO_L6P_T0_12	AA13	FMC1_PRSNTM2C_N
IO_L6N_T0_VREF_12	AA12	FMC1_VREFAM2C
IO_L7P_T1_12	AE10	FMC1_LA_P8
IO_L7N_T1_12	AD10	FMC1_LA_N8
IO_L8P_T1_12	AE12	FMC1_LA_P10
IO_L8N_T1_12	AF12	FMC1_LA_N10
IO_L9P_T1_DQS_12	AE11	FMC1_LA_P9
IO_L9N_T1_DQS_12	AF10	FMC1_LA_N9
IO_L10P_T1_12	AE13	FMC1_LA_P7
IO_L10N_T1_12	AF13	FMC1_LA_N7
IO_L11P_T1_SRCC_12	AC12	
IO_L11N_T1_SRCC_12	AD11	FMC1_CLK0M2C_P
IO_L12P_T1_MRCC_12	AC13	FMC1_CLK0M2C_N
IO_L12N_T1_MRCC_12	AD13	FMC1_CLK0C2M_P
IO_L13P_T2_MRCC_12	AC14	FMC1_CLK0C2M_N
IO_L13N_T2_MRCC_12	AD14	FMC1_LA_P0
IO_L14P_T2_SRCC_12	AB15	FMC1_LA_N0
IO_L14N_T2_SRCC_12	AB14	FMC1_LA_P1
IO_L15P_T2_DQS_12	AD16	FMC1_LA_N1
IO_L15N_T2_DQS_12	AD15	FMC1_LA_P16
IO_L16P_T2_12	AF15	FMC1_LA_N16
IO_L16N_T2_12	AF14	FMC1_LA_P13
IO_L17P_T2_12	AE16	FMC1_LA_N13
IO_L17N_T2_12	AE15	FMC1_LA_P14
IO_L18P_T2_12	AE17	FMC1_LA_N14
IO_L18N_T2_12	AF17	FMC1_LA_P15
IO_L19P_T3_12	Y17	FMC1_LA_N15
IO_L19N_T3_VREF_12	AA17	WRC_SFP_MOD_DEF0
IO_L20P_T3_12	AB17	FMC1_VREFAM2C
IO_L20N_T3_12	AB16	DOUTB_P5
IO_L21P_T3_DQS_12	AC17	DOUTB_N5
IO_L21N_T3_DQS_12	AC16	FMC1_LA_P11
IO_L22P_T3_12	AA15	FMC1_LA_N11
IO_L22N_T3_12	AA14	FMC1_LA_P12
IO_L23P_T3_12	Y16	FMC1_LA_N12
IO_L23N_T3_12	Y15	DOUTA_P5
IO_L24P_T3_12	W16	DOUTA_N5
IO_L24N_T3_12	W15	DOUTB_P4
IO_25_12	W17	DOUTB_N4
		WRC_SFP_MOD_DEF2

C283 100nF → GND

C298 100nF → GND

VCCO_13=2.5V

IC37B
XC7Z030-2FFG676I

BANK 13

IO_0_13	V19	PD_DAT
IO_L1P_T0_13	AA25	FMC1_LA_P33
IO_L1N_T0_13	AB25	FMC1_LA_N33
IO_L2P_T0_13	AB26	FMC1_LA_P28
IO_L2N_T0_13	AC26	FMC1_LA_N28
IO_L3P_T0_DQS_13	AE25	FMC1_LA_P25
IO_L3N_T0_DQS_13	AE26	FMC1_LA_N25
IO_L4P_T0_13	AD25	FMC1_LA_P24
IO_L4N_T0_13	AD26	FMC1_LA_N24
IO_L5P_T0_13	AF24	FMC1_LA_P26
IO_L5N_T0_13	AF25	FMC1_LA_N26
IO_L6P_T0_13	AA24	
IO_L6N_T0_VREF_13	AB24	FMC1_VREFAM2C
IO_L7P_T1_13	AE22	FMC1_LA_P21
IO_L7N_T1_13	AF22	FMC1_LA_N21
IO_L8P_T1_13	AE23	FMC1_LA_P27
IO_L8N_T1_13	AF23	FMC1_LA_N27
IO_L9P_T1_DQS_13	AB21	FMC1_LA_P30
IO_L9N_T1_DQS_13	AB22	FMC1_LA_N30
IO_L10P_T1_13	AA22	FMC1_LA_P32
IO_L10N_T1_13	AA23	FMC1_LA_N32
IO_L11P_T1_SRCC_13	AD23	FMC1_LA_P17
IO_L11N_T1_SRCC_13	AD24	FMC1_LA_N17
IO_L12P_T1_MRCC_13	AC23	DOUTB_P6
IO_L12N_T1_MRCC_13	AC24	DOUTB_N6
IO_L13P_T2_MRCC_13	AD20	FPGA_SCL1
IO_L13N_T2_MRCC_13	AD21	FPGA_SDA1
IO_L14P_T2_SRCC_13	AC21	FMC1_LA_P18
IO_L14N_T2_SRCC_13	AC22	FMC1_LA_N18
IO_L15P_T2_DQS_13	AF19	FMC1_LA_P22
IO_L15N_T2_DQS_13	AF20	FMC1_LA_N22
IO_L16P_T2_13	AE20	DOUTA_P6
IO_L16N_T2_13	AE21	DOUTA_N6
IO_L17P_T2_13	AD18	FMC1_LA_P23
IO_L17N_T2_13	AD19	FMC1_LA_N23
IO_L18P_T2_13	AE18	FMC1_LA_P19
IO_L18N_T2_13	AF18	FMC1_LA_N19
IO_L19P_T3_13	W20	PD_LE
IO_L19N_T3_VREF_13	Y20	FMC1_VREFAM2C
IO_L20P_T3_13	AA20	FMC1_LA_P31
IO_L20N_T3_13	AB20	FMC1_LA_N31
IO_L21P_T3_DQS_13	AC18	FMC1_LA_P29
IO_L21N_T3_DQS_13	AC19	FMC1_LA_N29
IO_L22P_T3_13	AA19	DOUTB_P3
IO_L22N_T3_13	AB19	DOUTB_N3
IO_L23P_T3_13	W18	FMC1_LA_P20
IO_L23N_T3_13	W19	FMC1_LA_N20
IO_L24P_T3_13	Y18	DOUTA_P4
IO_L24N_T3_13	AA18	DOUTA_N4
IO_25_13	V18	PD_CLK

C311 100nF → GND

C305 100nF → GND

DOUTA_P[1..6] → DOUTA_P[1..6]
DOUTA_N[1..6] → DOUTA_N[1..6]
DOUTB_P[1..6] → DOUTB_P[1..6]
DOUTB_N[1..6] → DOUTB_N[1..6]

FMC1_LA_P[33..0] → FMC1_LA_P[33..0]
FMC1_LA_N[33..0] → FMC1_LA_N[33..0]
FMC1_VREFAM2C → FMC1_VREFAM2C

P2V5
P3V3
R315 1k 1K2
R316 1k 1K2
R297 1k 1K2
R298 1k 1K2
IC80
FPGA_SDA1 → SDAA (3)
FPGA_SCL1 → SCLA (2)
SDAB (6) → FMC1_SDA
SCLB (7) → FMC1_SCL
EN (5)
VCCA (1)
VCCB (8)
GND (4)
TCA9517DGKR
C195 100nF → GND
C185 100nF → GND

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VCCO_33=1.8V

IC37C
XC7Z030-2FFG676I

BANK 33

IO_0_VRN_33	L9	
IO_L1P_T0_33	G4	FMC2_LA_P3
IO_L1N_T0_33	F4	FMC2_LA_N3
IO_L2P_T0_33	D4	FMC2_LA_P2
IO_L2N_T0_33	D3	FMC2_LA_N2
IO_L3P_T0_DQS_33	G2	FMC2_LA_P5
IO_L3N_T0_DQS_33	F2	FMC2_LA_N5
IO_L4P_T0_33	D1	FMC2_LA_P4
IO_L4N_T0_33	C1	FMC2_LA_N4
IO_L5P_T0_33	E2	FMC2_LA_P6
IO_L5N_T0_33	E1	FMC2_LA_N6
IO_L6P_T0_33	F3	
IO_L6N_T0_VREF_33	E3	FMC2_VREFAM2C
IO_L7P_T1_33	J1	FMC2_LA_P9
IO_L7N_T1_33	H1	FMC2_LA_N9
IO_L8P_T1_33	H4	FMC2_LA_P8
IO_L8N_T1_33	H3	FMC2_LA_N8
IO_L9P_T1_DQS_33	K2	FMC2_LA_P10
IO_L9N_T1_DQS_33	K1	FMC2_LA_N10
IO_L10P_T1_33	H2	FMC2_LA_P7
IO_L10N_T1_33	G1	FMC2_LA_N7
IO_L11P_T1_SRCC_33	L3	
IO_L11N_T1_SRCC_33	K3	
IO_L12P_T1_MRCC_33	J4	
IO_L12N_T1_MRCC_33	J3	
IO_L13P_T2_MRCC_33	M6	FMC2_LA_P0
IO_L13N_T2_MRCC_33	M5	FMC2_LA_N0
IO_L14P_T2_SRCC_33	L5	FMC2_LA_P1
IO_L14N_T2_SRCC_33	L4	FMC2_LA_N1
IO_L15P_T2_DQS_33	N3	FMC2_LA_P14
IO_L15N_T2_DQS_33	N2	FMC2_LA_N14
IO_L16P_T2_33	M2	FMC2_LA_P13
IO_L16N_T2_33	L2	FMC2_LA_N13
IO_L17P_T2_33	N4	FMC2_LA_P11
IO_L17N_T2_33	M4	FMC2_LA_N11
IO_L18P_T2_33	N1	FMC2_LA_P16
IO_L18N_T2_33	M1	FMC2_LA_N16
IO_L19P_T3_33	M7	
IO_L19N_T3_VREF_33	L7	FMC2_VREFAM2C
IO_L20P_T3_33	K5	
IO_L20N_T3_33	J5	
IO_L21P_T3_DQS_33	M8	FMC2_LA_P15
IO_L21N_T3_DQS_33	L8	FMC2_LA_N15
IO_L22P_T3_33	K6	FMC2_LA_P12
IO_L22N_T3_33	J6	FMC2_LA_N12
IO_L23P_T3_33	N7	
IO_L23N_T3_33	N6	
IO_L24P_T3_33	K8	
IO_L24N_T3_33	K7	
IO_25_VRP_33	N8	

WRC_LED_ACT
FMC2_PRSNTM2C_N
FMC2_CLK0M2C_P
FMC2_CLK0M2C_N
FMC2_CLK0C2M_P
FMC2_CLK0C2M_N
ADC_SDI
WR_TIME_VALID_LED
RF_D3S_VALID_LED
ADC_SCK
ADC_SDO
WRC_PPS_P
WRC_PPS_N
ADC_CNV

C269 100nF → GND
C280 100nF → GND

VCCO_34=1.8V

IC37D
XC7Z030-2FFG676I

BANK 34

IO_0_VRN_34	K11	
IO_L1P_T0_34	J11	FMC2_LA_P25
IO_L1N_T0_34	H11	FMC2_LA_N25
IO_L2P_T0_34	G6	FMC2_LA_P23
IO_L2N_T0_34	G5	FMC2_LA_N23
IO_L3P_T0_DQS_PUDC_B_34	H9	
IO_L3N_T0_DQS_34	G9	
IO_L4P_T0_34	H7	FMC2_LA_P22
IO_L4N_T0_34	H6	FMC2_LA_N22
IO_L5P_T0_34	J10	FMC2_LA_P26
IO_L5N_T0_34	J9	FMC2_LA_N26
IO_L6P_T0_34	J8	
IO_L6N_T0_VREF_34	H8	FMC2_VREFAM2C
IO_L7P_T1_34	F5	FMC2_LA_P27
IO_L7N_T1_34	E5	FMC2_LA_N27
IO_L8P_T1_34	D9	FMC2_LA_P28
IO_L8N_T1_34	D8	FMC2_LA_N28
IO_L9P_T1_DQS_34	F9	FMC2_LA_P29
IO_L9N_T1_DQS_34	E8	FMC2_LA_N29
IO_L10P_T1_34	E6	FMC2_LA_P24
IO_L10N_T1_34	D5	FMC2_LA_N24
IO_L11P_T1_SRCC_34	F8	FMC2_LA_P17
IO_L11N_T1_SRCC_34	E7	FMC2_LA_N17
IO_L12P_T1_MRCC_34	G7	
IO_L12N_T1_MRCC_34	F7	
IO_L13P_T2_MRCC_34	C8	
IO_L13N_T2_MRCC_34	C7	
IO_L14P_T2_SRCC_34	D6	FMC2_LA_P18
IO_L14N_T2_SRCC_34	C6	FMC2_LA_N18
IO_L15P_T2_DQS_34	C9	DOUTA_P3
IO_L15N_T2_DQS_34	B9	DOUTA_N3
IO_L16P_T2_34	B10	FMC2_LA_P32
IO_L16N_T2_34	A10	FMC2_LA_N32
IO_L17P_T2_34	A9	FMC2_LA_P33
IO_L17N_T2_34	A8	FMC2_LA_N33
IO_L18P_T2_34	B7	
IO_L18N_T2_34	A7	
IO_L19P_T3_34	C4	
IO_L19N_T3_VREF_34	C3	FMC2_VREFAM2C
IO_L20P_T3_34	B5	FMC2_LA_P31
IO_L20N_T3_34	B4	FMC2_LA_N31
IO_L21P_T3_DQS_34	B6	FMC2_LA_P30
IO_L21N_T3_DQS_34	A5	FMC2_LA_N30
IO_L22P_T3_34	A4	FMC2_LA_P21
IO_L22N_T3_34	A3	FMC2_LA_N21
IO_L23P_T3_34	C2	FMC2_LA_P20
IO_L23N_T3_34	B1	FMC2_LA_N20
IO_L24P_T3_34	B2	FMC2_LA_P19
IO_L24N_T3_34	A2	FMC2_LA_N19
IO_25_VRP_34	K10	TEMPID_DQ

WRC_LED_LINK
WRC_SFP_TX_FAULT
WRC_SFP_TX_LOS
FPGA_CLK_P
FPGA_CLK_N
CLK20_VCXO
WRC_PLL20DAC_CS_N
WRC_PLLDAC_SCLK
WRC_PLLDAC_DIN
WRC_PLL25DAC_CS_N

P1V8
R339 10k 750
R341 10k 750 Mounted: No
GND
C281 100nF → GND
C270 100nF → GND

FMC2_LA_P[33..0] → FMC2_LA_P[33..0]
FMC2_LA_N[33..0] → FMC2_LA_N[33..0]
FMC2_VREFAM2C → FMC2_VREFAM2C

DOUTA_P[1..6] → DOUTA_P[1..6]
DOUTA_N[1..6] → DOUTA_N[1..6]

P1V8
R342 10k 750
TEMPID_DQ
IC41
1 I/O
3 GND VCC 2
DS2411R+
P1V8
C282 100nF
GND
GND

Unique 64-bit ID (Maxim 1-Wire)

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VCCO_35=1.8V

IC37E
XC7Z030-2FFG676I

BANK 35

IO_0_VRN_35	H16	
IO_L1P_T0_AD0P_35	F12	DAC6_P
IO_L1N_T0_AD0N_35	E12	DAC6_N
IO_L2P_T0_AD8P_35	E10	DAC8_P
IO_L2N_T0_AD8N_35	D10	DAC8_N
IO_L3P_T0_DQS_AD1P_35	G10	DAC9_P
IO_L3N_T0_DQS_AD1N_35	F10	DAC9_N
IO_L4P_T0_35	E11	DAC7_P
IO_L4N_T0_35	D11	DAC7_N
IO_L5P_T0_AD9P_35	G12	DAC10_P
IO_L5N_T0_AD9N_35	G11	DAC10_N
IO_L6P_T0_35	F13	DAC5_P
IO_L6N_T0_VREF_35	E13	DAC5_N
IO_L7P_T1_AD2P_35	H13	DAC12_P
IO_L7N_T1_AD2N_35	H12	DAC12_N
IO_L8P_T1_AD10P_35	K13	DAC13_P
IO_L8N_T1_AD10N_35	J13	DAC13_N
IO_L9P_T1_DQS_AD3P_35	K15	DAC3_P
IO_L9N_T1_DQS_AD3N_35	J15	DAC3_N
IO_L10P_T1_AD11P_35	G16	DAC1_P
IO_L10N_T1_AD11N_35	G15	DAC1_N
IO_L11P_T1_SRCC_35	G14	DAC11_P
IO_L11N_T1_SRCC_35	F14	DAC11_N
IO_L12P_T1_MRCC_35	J14	
IO_L12N_T1_MRCC_35	H14	CLK_SYNTH_P
IO_L13P_T2_MRCC_35	D15	CLK_SYNTH_N
IO_L13N_T2_MRCC_35	D14	RF_FPGA_P
IO_L14P_T2_AD4P_SRCC_35	F15	RF_FPGA_N
IO_L14N_T2_AD4N_SRCC_35	E15	DAC4_P
IO_L15P_T2_DQS_AD12P_35	C17	DAC4_N
IO_L15N_T2_DQS_AD12N_35	C16	DAC0_P
IO_L16P_T2_35	E16	DAC0_N
IO_L16N_T2_35	D16	DAC2_P
IO_L17P_T2_AD5P_35	B16	DAC2_N
IO_L17N_T2_AD5N_35	B15	DIN_P2
IO_L18P_T2_AD13P_35	B17	DIN_N2
IO_L18N_T2_AD13N_35	A17	DIN_P1
IO_L19P_T3_35	D13	DIN_N1
IO_L19N_T3_VREF_35	C13	DIN_P4
IO_L20P_T3_AD6P_35	C14	DIN_N4
IO_L20N_T3_AD6N_35	B14	DOUTB_P1
IO_L21P_T3_DQS_AD14P_35	A15	DOUTB_N1
IO_L21N_T3_DQS_AD14N_35	A14	DIN_P3
IO_L22P_T3_AD7P_35	C12	DIN_N3
IO_L22N_T3_AD7N_35	B12	DOUTA_P2
IO_L23P_T3_35	C11	DOUTA_N2
IO_L23N_T3_35	B11	DOUTB_P2
IO_L24P_T3_AD15P_35	A13	DOUTB_N2
IO_L24N_T3_AD15N_35	A12	DOUTA_P1
IO_25_VRP_35	K12	DOUTA_N1
		WRC_SCL

WRC_SDA

DAC_DAT

DAC0_P	DAC0_P
DAC0_N	DAC0_N
DAC1_P	DAC1_P
DAC1_N	DAC1_N
DAC2_P	DAC2_P
DAC2_N	DAC2_N
DAC3_P	DAC3_P
DAC3_N	DAC3_N
DAC4_P	DAC4_P
DAC4_N	DAC4_N
DAC5_P	DAC5_P
DAC5_N	DAC5_N
DAC6_P	DAC6_P
DAC6_N	DAC6_N
DAC7_P	DAC7_P
DAC7_N	DAC7_N
DAC8_P	DAC8_P
DAC8_N	DAC8_N
DAC9_P	DAC9_P
DAC9_N	DAC9_N
DAC10_P	DAC10_P
DAC10_N	DAC10_N
DAC11_P	DAC11_P
DAC11_N	DAC11_N
DAC12_P	DAC12_P
DAC12_N	DAC12_N
DAC13_P	DAC13_P
DAC13_N	DAC13_N

DAC_DAT

DOUTB_P[1..6] → DOUTB_P[1..6]
DOUTB_N[1..6] → DOUTB_N[1..6]
DOUTA_P[1..6] → DOUTA_P[1..6]
DOUTA_N[1..6] → DOUTA_N[1..6]

DIN_P[1..4] → DIN_P[1..4]
DIN_N[1..4] → DIN_N[1..4]

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SVN:

VCCO_500=3.3V

VCCO_501=1.8V

rgmii_vref RGMII_VREF

IC37G
XC7Z030-2FFG676I

PS_CLK_500	B24	OSC_33
PS_POR_B_500	C23	PS_POR_OR_N
PS_SRST_B_501	A22	PS_SRST_OR_N
PS_MIO_VREF_501	H18	RGMII_VREF
PS_MIO1_500	E26	QSPI1_CS
PS_MIO2_500	D26	QSPI0_CS
PS_MIO3_500	E25	QSPI0_DQ0
PS_MIO4_500	D25	QSPI0_DQ1
PS_MIO5_500	F24	QSPI0_DQ2
PS_MIO6_500	C26	QSPI0_DQ3
PS_MIO7_500	F23	QSPI0_SCLK
PS_MIO8_500	E23	MIO_BANK0_VMODE
PS_MIO9_500	A24	MIO_BANK1_VMODE
PS_MIO10_500	D24	QSPI1_SCLK
PS_MIO11_500	A25	QSPI1_DQ0
PS_MIO12_500	B26	QSPI1_DQ1
PS_MIO13_500	A23	QSPI1_DQ2
PS_MIO14_500	B25	QSPI1_DQ3
PS_MIO15_500	D23	PMBus_alert_N
PS_MIO16_501	C24	WR_PLL_RESET_N
PS_MIO17_501	G21	RGMII_TX_CLK
PS_MIO18_501	G17	RGMII_TX_D0
PS_MIO19_501	G20	RGMII_TX_D1
PS_MIO20_501	G19	RGMII_TX_D2
PS_MIO21_501	H19	RGMII_TX_D3
PS_MIO22_501	F22	RGMII_TX_CTL
PS_MIO23_501	G22	RGMII_RX_CLK
PS_MIO24_501	F20	RGMII_RX_D0
PS_MIO25_501	J19	RGMII_RX_D1
PS_MIO26_501	F19	RGMII_RX_D2
PS_MIO27_501	H17	RGMII_RX_D3
PS_MIO28_501	F18	RGMII_RX_CTL
PS_MIO29_501	J18	SPI_SCLK
PS_MIO30_501	E20	SPI_MISO
PS_MIO31_501	K19	SPI_SS0
PS_MIO32_501	E21	SPI_SS1
PS_MIO33_501	K17	SPI_SS2
PS_MIO34_501	E22	SPI_MOSI
PS_MIO35_501	J16	
PS_MIO36_501	D19	WR_PLL_STATUS
PS_MIO37_501	K16	RF_PLL_STATUS
PS_MIO38_501	D20	PD_LockDetect
PS_MIO39_501	D21	I2C_PMBus_clk
PS_MIO40_501	C21	I2C_PMBus_d
PS_MIO41_501	C22	SD_CLK_VL
PS_MIO42_501	C19	SD_CMD_VL
PS_MIO43_501	F17	SD_D0_VL
PS_MIO44_501	D18	SD_D1_VL
PS_MIO45_501	E18	SD_D2_VL
PS_MIO46_501	C18	SD_D3_VL
PS_MIO47_501	E17	SD_CD_VL
PS_MIO48_501	B19	SD_WP_VL
PS_MIO49_501	B21	UART0_TXD
PS_MIO50_501	A18	UART0_RXD
PS_MIO51_501	B22	
PS_MIO52_501	B20	MDIO_CLK
PS_MIO53_501	A20	MDIO_IO

R139 330, R153 330, R349 20k, R350 20k, R348 20k, R344 20k, R345 20k

ALL QSPI 20k resistors should be placed near the middle of the QSPI0 traces while keeping their stubs as short as possible, in any case < 10 mm.

OSC3 VDD OUT E/D GND 33.333MHz
C313 100nF, R162 100 OSC_33

Boot Mode MIO strapping pins:
MIO[2] : '0' (PD) : JTAG Cascade mode
MIO[3] : '0' (PD) : no NOR boot, not on board
MIO[4-5] : see below (user selectable)
MIO[6] : '0' (PD) : PLL enabled
MIO[7-8] : '01' : Bank 0/1 at 3.3V/1.8V

MIO[4] SW1A	MIO[5] SW2A	
0	0	=> JTAG cascade
0	1	=> QUAD-SPI
1	0	=> NAND (not on board)
1	1	=> SD Card

microSD card

IC16 MAX13035EETE+
I/OVL1 I/OVL2 I/OVL3 I/OVL4 I/OVL5 CLKVL CLK_RET VL GND EP
I/OVCC1 I/OVCC2 I/OVCC3 I/OVCC4 I/OVCC5 CLKVCC VCC

SD_D0_VL SD_D1_VL SD_D2_VL SD_D3_VL SD_CMD_VL SD_CLK_VL

P1V8, P3V3, C115 100nF, C116 100nF, C117 1uF

J7: DAT2 DAT3 CMD VDD CLK VSS DAT0 DAT1 DETSW DETLEV
SD_D2 SD_D3 SD_CMD SD_CLK SD_D0 SD_D1

HSSD Net Class, PCB Rule, Mounted: No, R360 4k7, C361 100nF

R114 0, R127 4k7, SD_CD_VL, R165 0, SD_WP_VL

* PCB and package delay skew for SD_D[0:3] and SD_CMD relative to SD_CLK must be between 50–200 ps [UG933].
* SI analysis for the SD_CLK line highly suggested
* Write Protect (WP) pulldown for linux driver compatibility
* SD_CMD pull-up not required but seen in MZ & ZC706

SoC POR (PB and PG VCCO_0)

* boot strap pins are sampled
* BootROM is executed

IC38B IC38A NC7WZ07P6X, PS_POR_N, PS_POR_OR_N
R28 4k7 Mounted: No, C309 100nF, R164 4k7
C89 100nF

Short trace between supervisory IC and Zynq SoC required.

IC76 TPS3808G33DBVT (SENSE RESET MR CT VDD GND)
PB3, CHASSIS, R278 4k7, C157 1nF, C155 100nF, C156 100nF
PHY_RST_N

POR reset deassertion delay time: 20 ms
2.6 ms RC for pushbutton
threshold voltage = 3.07V

SoC SRST (PB)

* boot strap pins are not sampled
* BootROM is executed
* debug environment is not disturbed

R173 4k7, R167 4k7, R168 4k7
IC40B IC40A NC7WZ07P6X, PS_SRST_OR_N
IC39 TPS3808G33DBVT (SENSE RESET MR CT VDD GND)
PB1, R172 4k7, C285 1nF, C90 100nF, C284 100nF, C287 100nF

SRST reset deassertion delay time: 20 ms
2.6 ms RC for pushbutton
threshold voltage = 3.07V

QSPI at 3.3V

IC87 IC32 S25FL128SAGMFI001
SCK SI/IO0 SO/IO1 WP/IO2 HOLD/IO3 CS RESET/RFU RFU NC VIO/RFU VCC VSS
QSPI0_SCLK QSPI0_DQ0 QSPI0_DQ1 QSPI0_DQ2 QSPI0_DQ3 QSPI0_CS
QSPI1_SCLK QSPI1_DQ0 QSPI1_DQ1 QSPI1_DQ2 QSPI1_DQ3 QSPI1_CS
Net Class QSPI, PCB Rule
C320 100nF, C351 100nF
R148 20k MIO-4, R159 20k MIO-5, SW2, SW3

SPI bus level translator

IC89 SN74AVC4T245PW
1DIR 2DIR 1OE 2OE 1A1 1A2 2A1 2A2 1B1 1B2 2B1 2B2 VCCA GND VCCB GND
SPI_MISO
C470 100nF, C471 100nF

IC88 SN74AVC4T245PW
SPI_SCLK SPI_MOSI SPI_SS0 SPI_SS1
C468 100nF, C469 100nF

I2C PMBus level translator

Pull-up to P1V8, bank 500's vcco!
R230 4k7, R231 4k7, R249 4k7, R252 4k7
IC70 TCA9517DGKR (SDAA SDAB SCLA SCLB EN VCCA VCCB GND)
I2C_PMBus_d I2C_PMBus_clk → I2C_PMBus_d_hv I2C_PMBus_clk_hv
C133 100nF, C134 100nF

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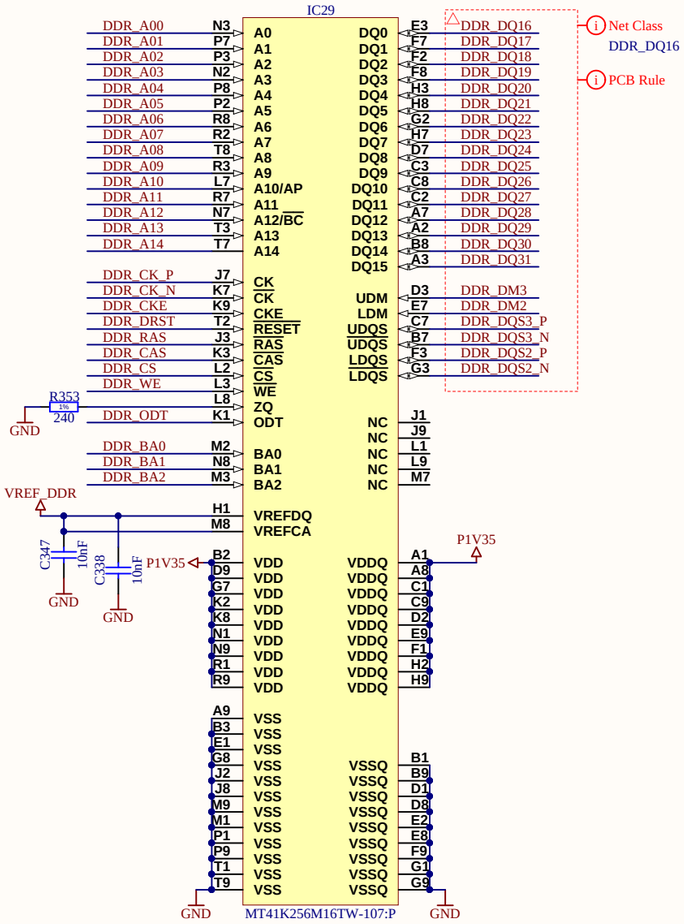
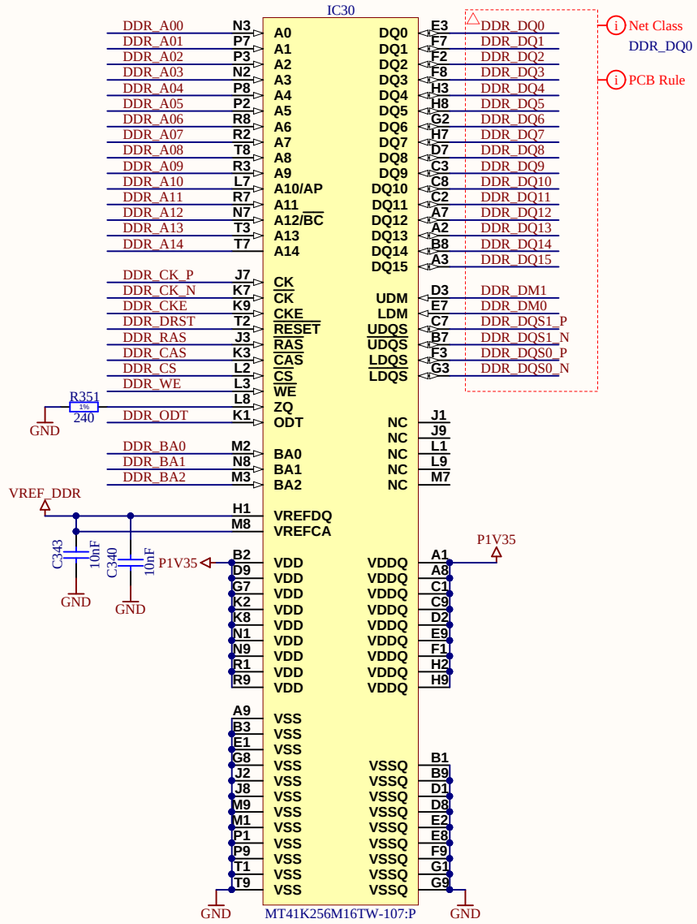
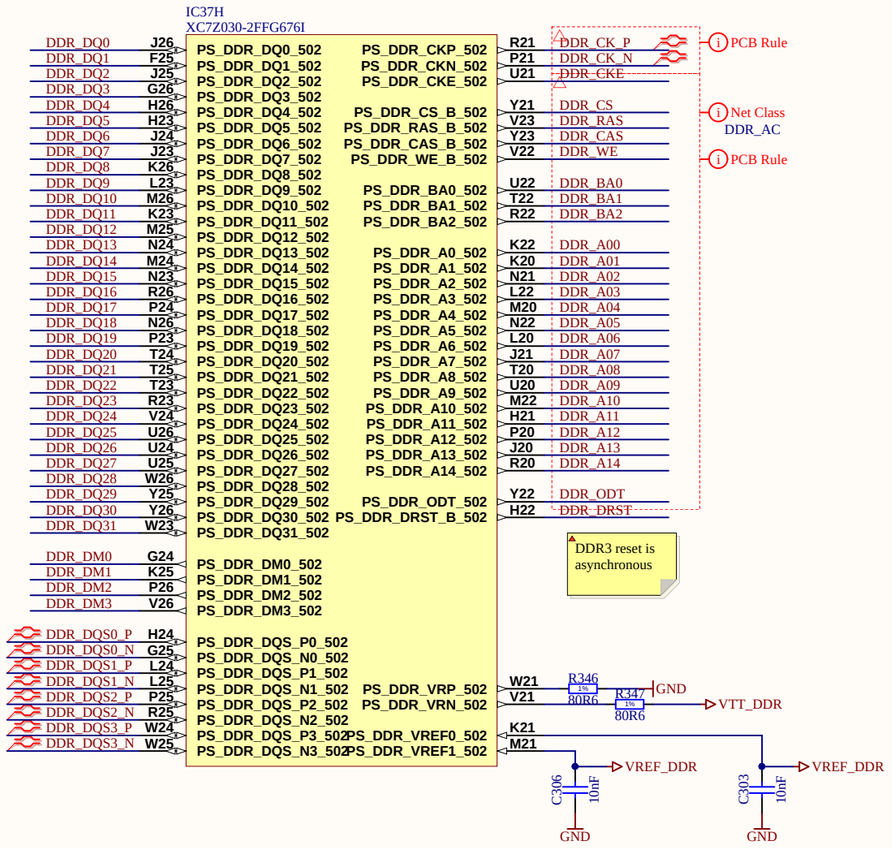
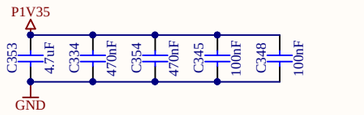


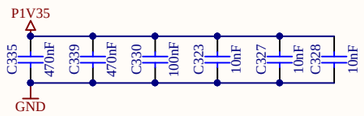




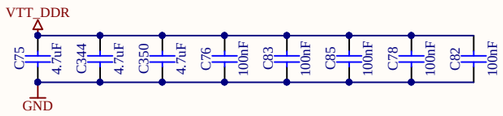
core (VSS) decoupling

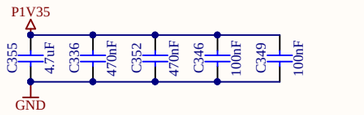


output drivers (VSSQ) decoupling

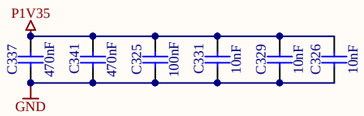


* Use separate vias for VSS and VSSQ as well as for VDD and VDDQ.
* No traces for VDD(Q) and VSS(Q), only planes; vias should have 8 mils traces [TN-46-14]
* For capacitor & terminating resistor placement, see Fig. 3, page 9 in Micrel TN-41-13 _and_ Fig. 4, page 6 in Micrel TN-46-14.
* Trace spacing constraints in Micrel TN-46-14 Table 1 (p. 8).
* VTT decoupling to be placed close to the terminated signals

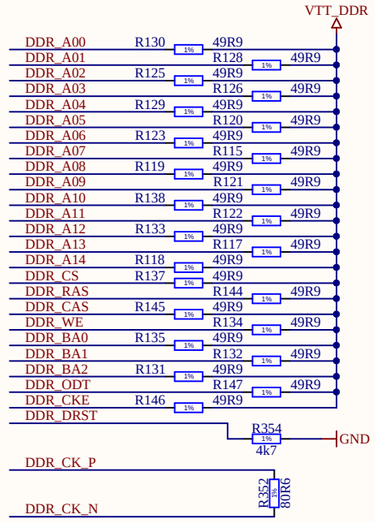




core (VSS) decoupling



output drivers (VSSQ) decoupling



* DDR3 trace lengths must include Zynq package flight time (generated in ISE using partgen -v xc7z030ffg676-2), see Documentation folder in this project.
* For DDR_AC, trace impedance should be 40 Ohms for single ended and 80 Ohms for differential signals; 50/100 Ohms is allowed if 40/80 is not achievable.
* For the DDR_DQ and DDR_DQS signals, On-Die Termination (ODT) is used and can be set to 40 or 60 Ohm (single ended) - one of these values has to be used for ALL traces.
* The two DDR3 devices should be routed and terminated in fly-by architecture, see Micrel TN-41-13 p. 20. Termination resistors should be placed past the last memory device.

Add following rules:
* 100 mil max skew between DDR_DQ and DDR_DQS
* DDR_AC hard to constrain, see [88AP510 p. 56]

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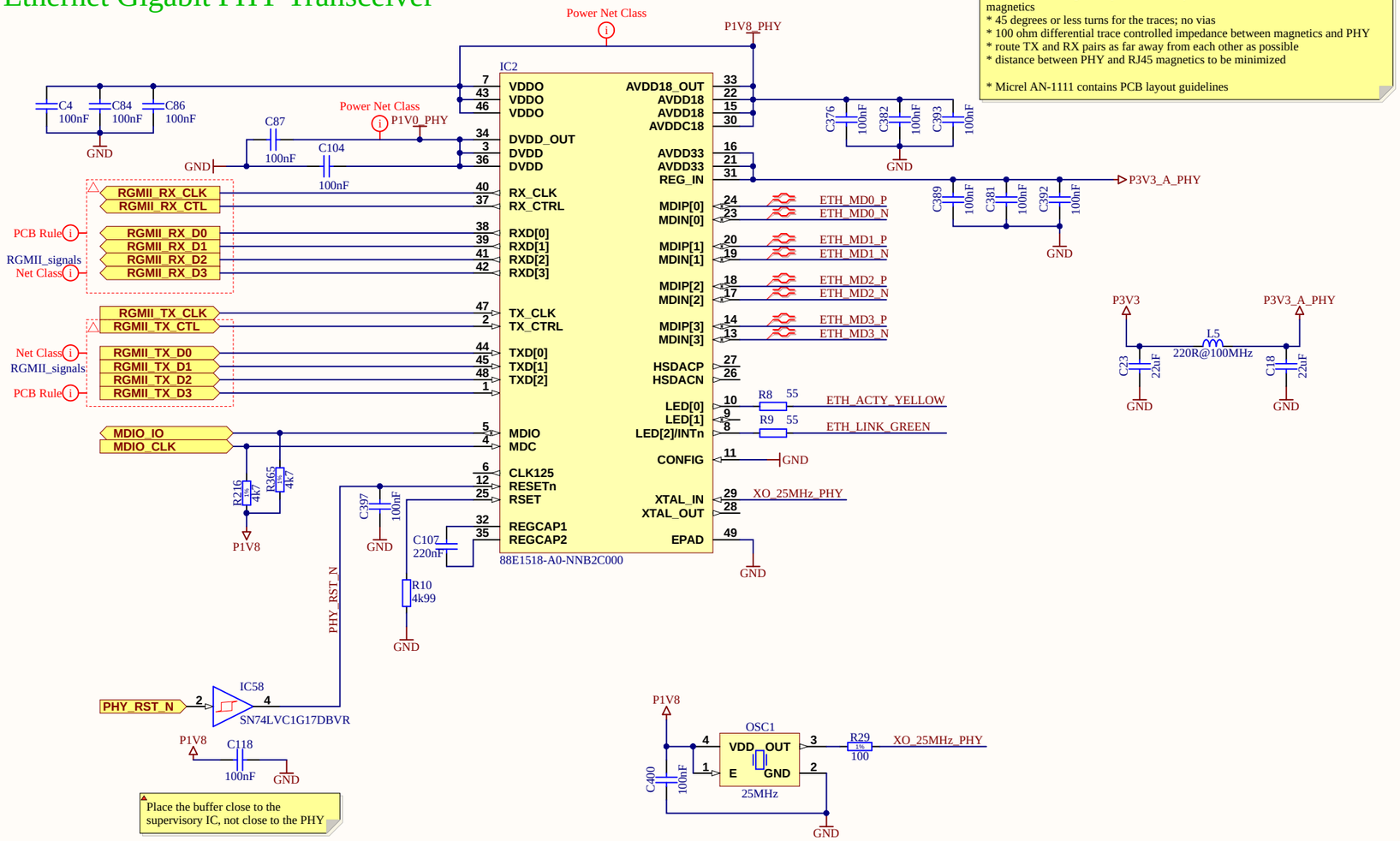
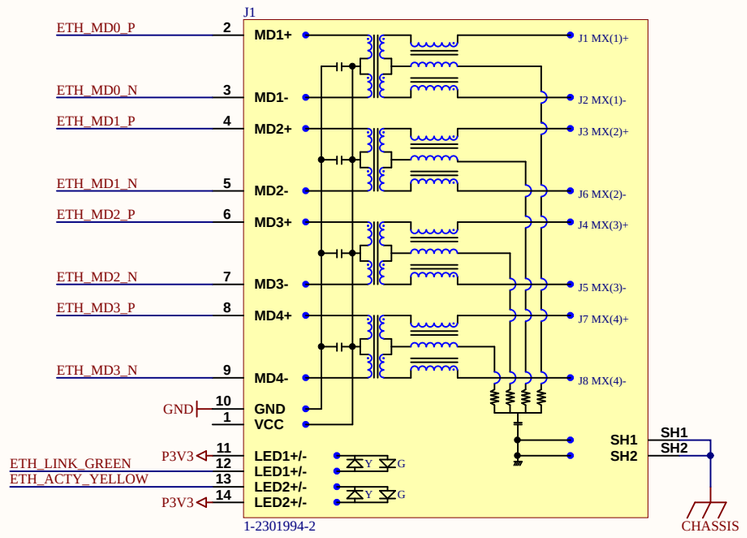
		SVN:	

Ethernet Gigabit PHY Transceiver



Ethernet RJ45 connector

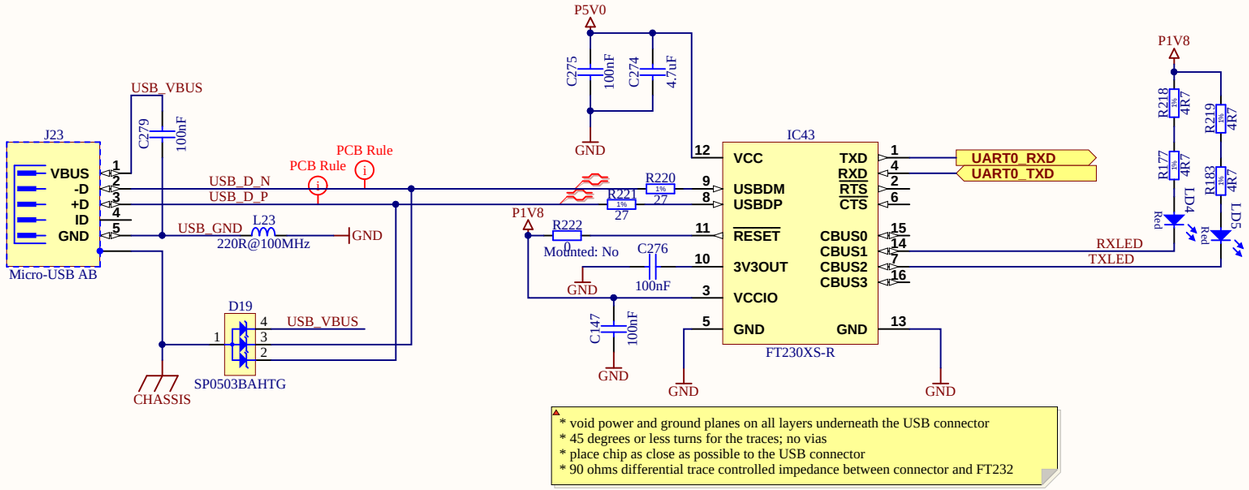


LED status (Marvell datasheet)

By default (HW reset), MODE3 dual LED is used:
LED1: OFF
LED0: OFF <=> No Link
LED0: ON <=> 1000Mbps Link / No activity
LED0: BLINK <=> 1000Mbps Link / Activity

LED2: ON <=> Link
LED2: OFF <=> No Link

USB UART



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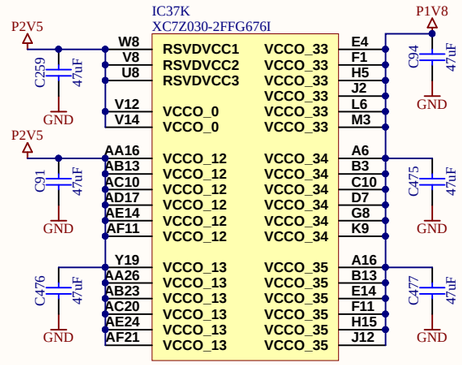
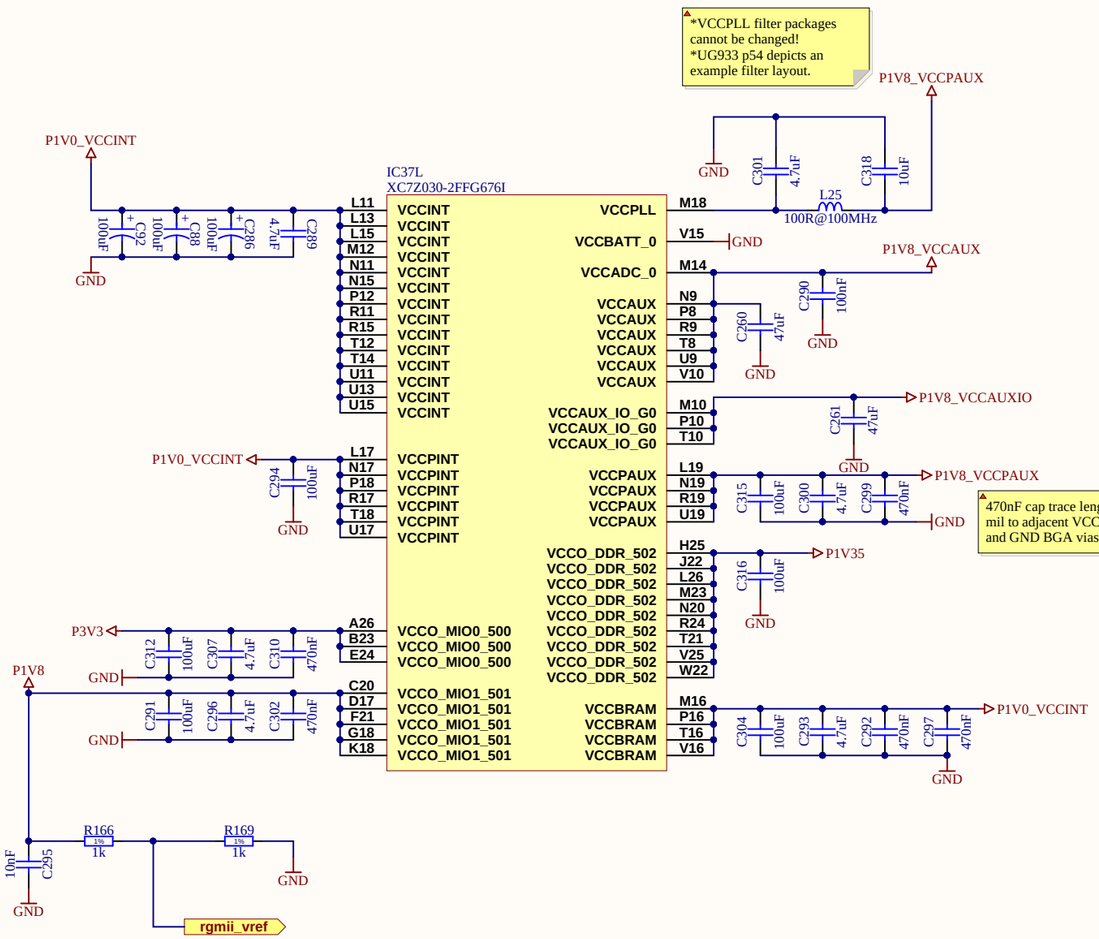
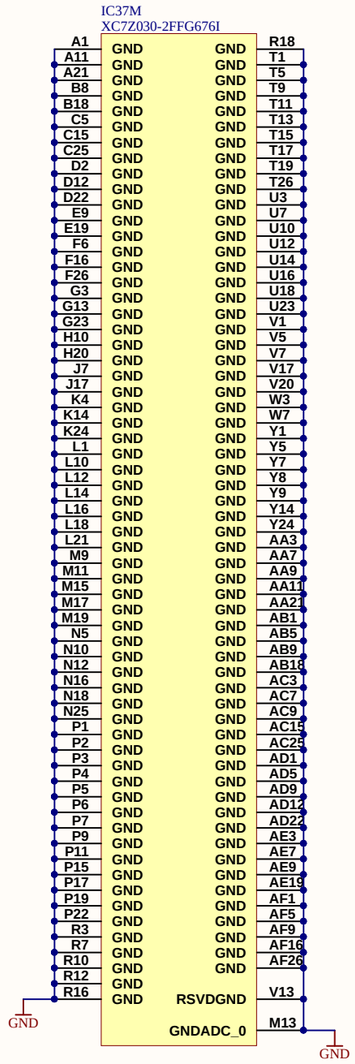
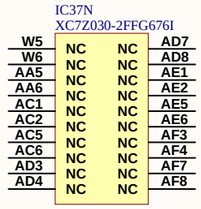
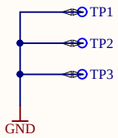








testpoints for probe, divide over the board



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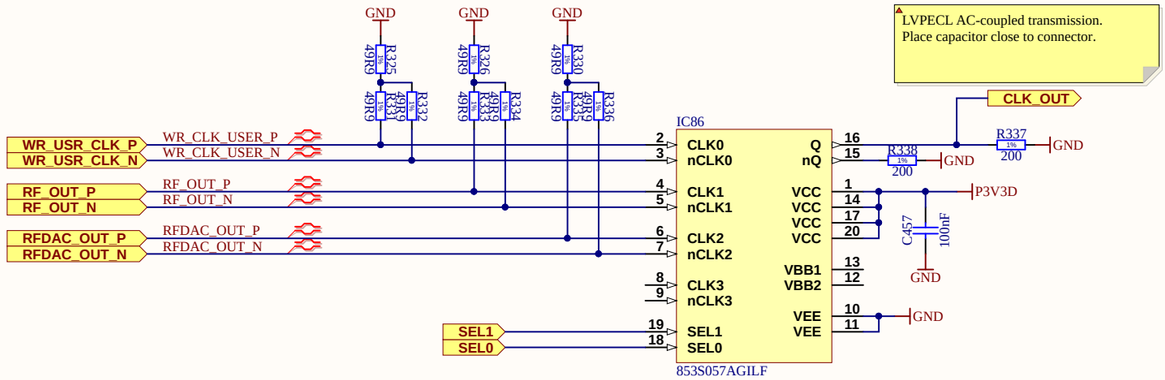
		SVN:	



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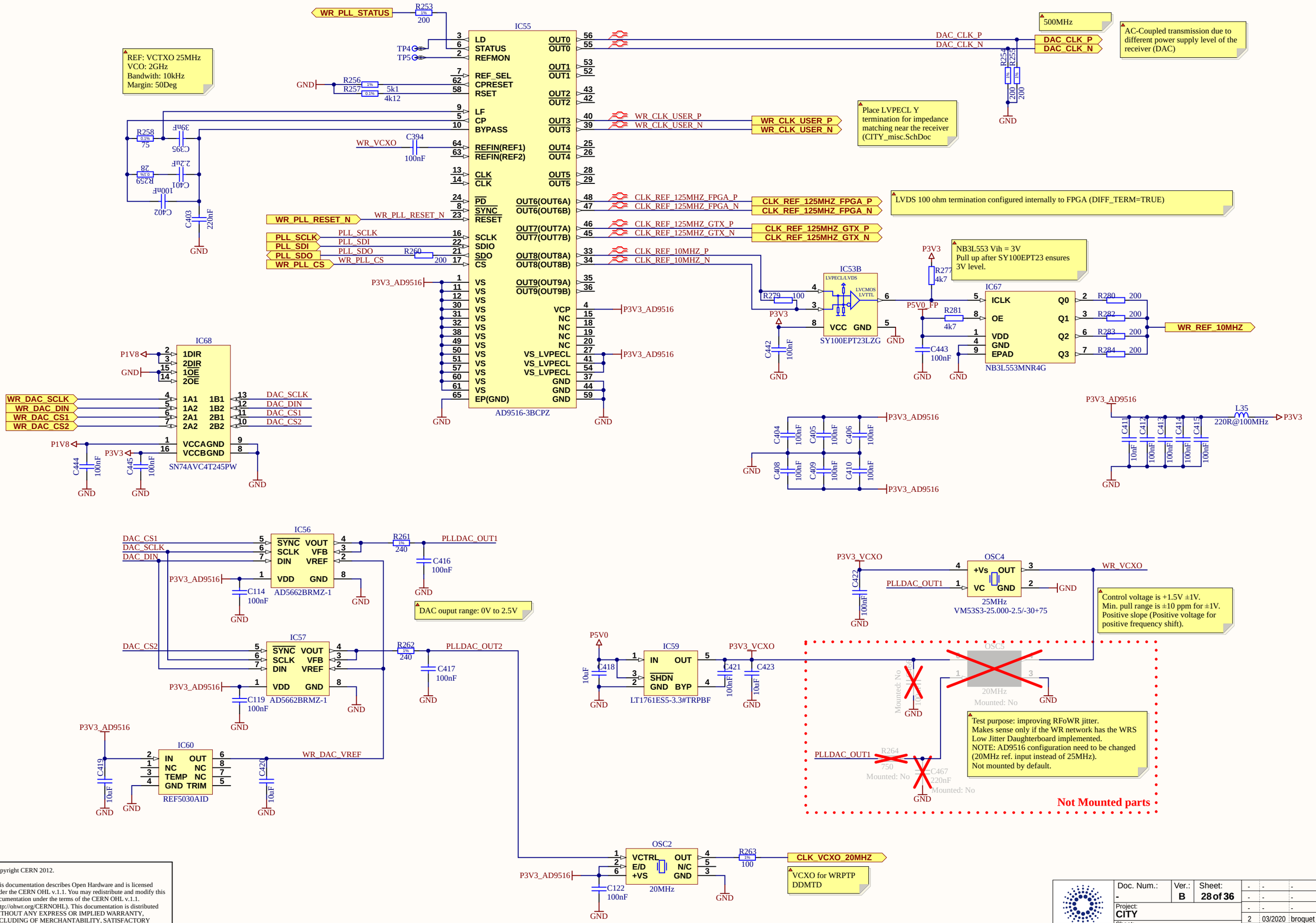

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	Sheet: WR Clocking			2 03/2020 broquet	
	File: CITY_WR_clocking.SchDoc			Rev. Date Author	SVN: