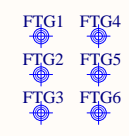



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Based on FASEC design
EDA-03288-V3



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		B	1 of 36		
	Project:	CITY		2	03/2020
	Sheet:	Top Level		Rev.	Date
	File:	CITY_top.SchDoc		Author	

SVN: 8572a12073698b3572d1447f05e

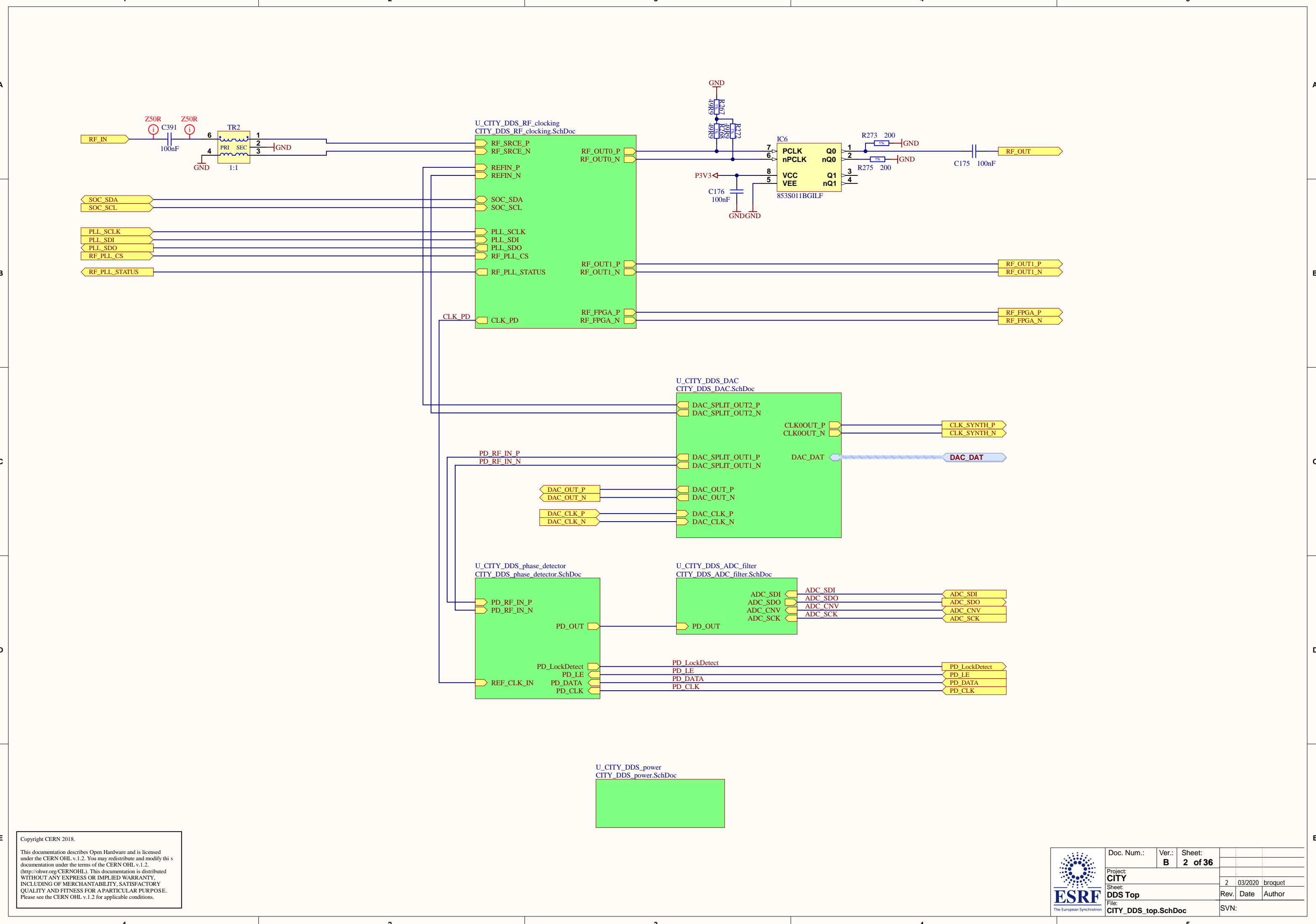
A

B

C


D

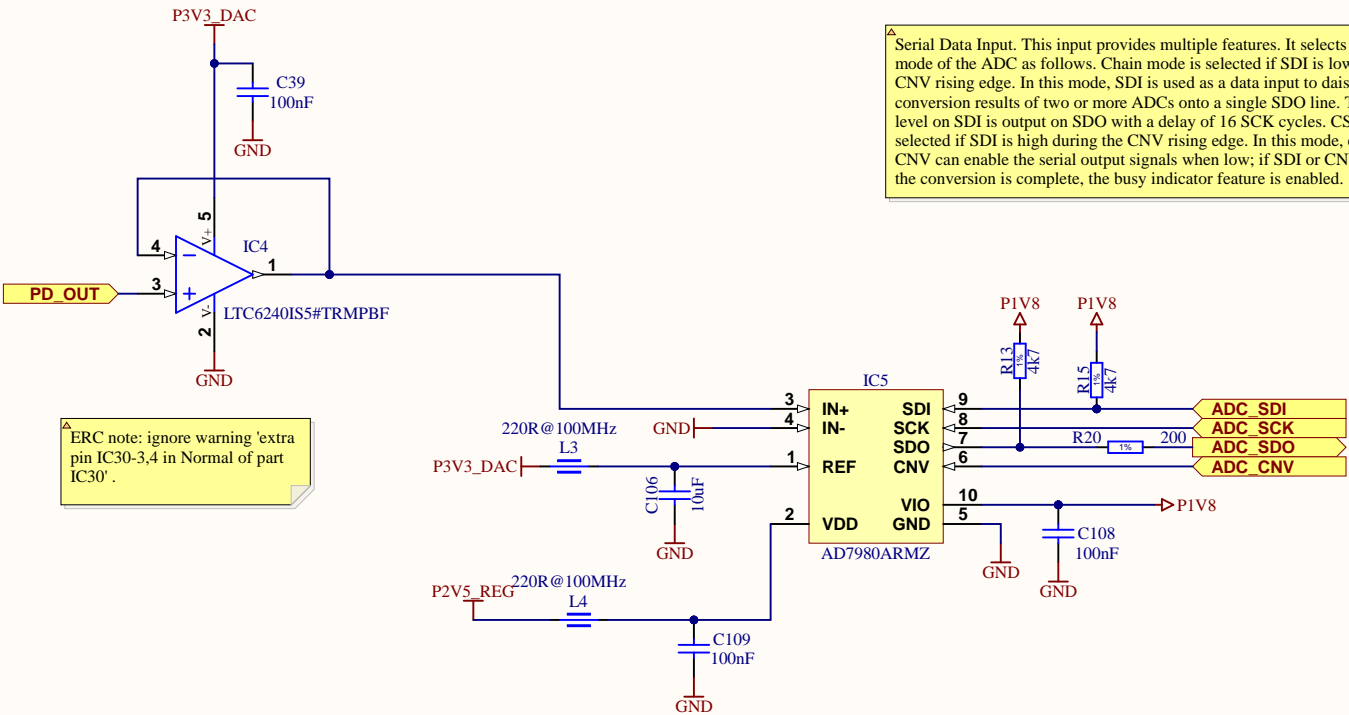
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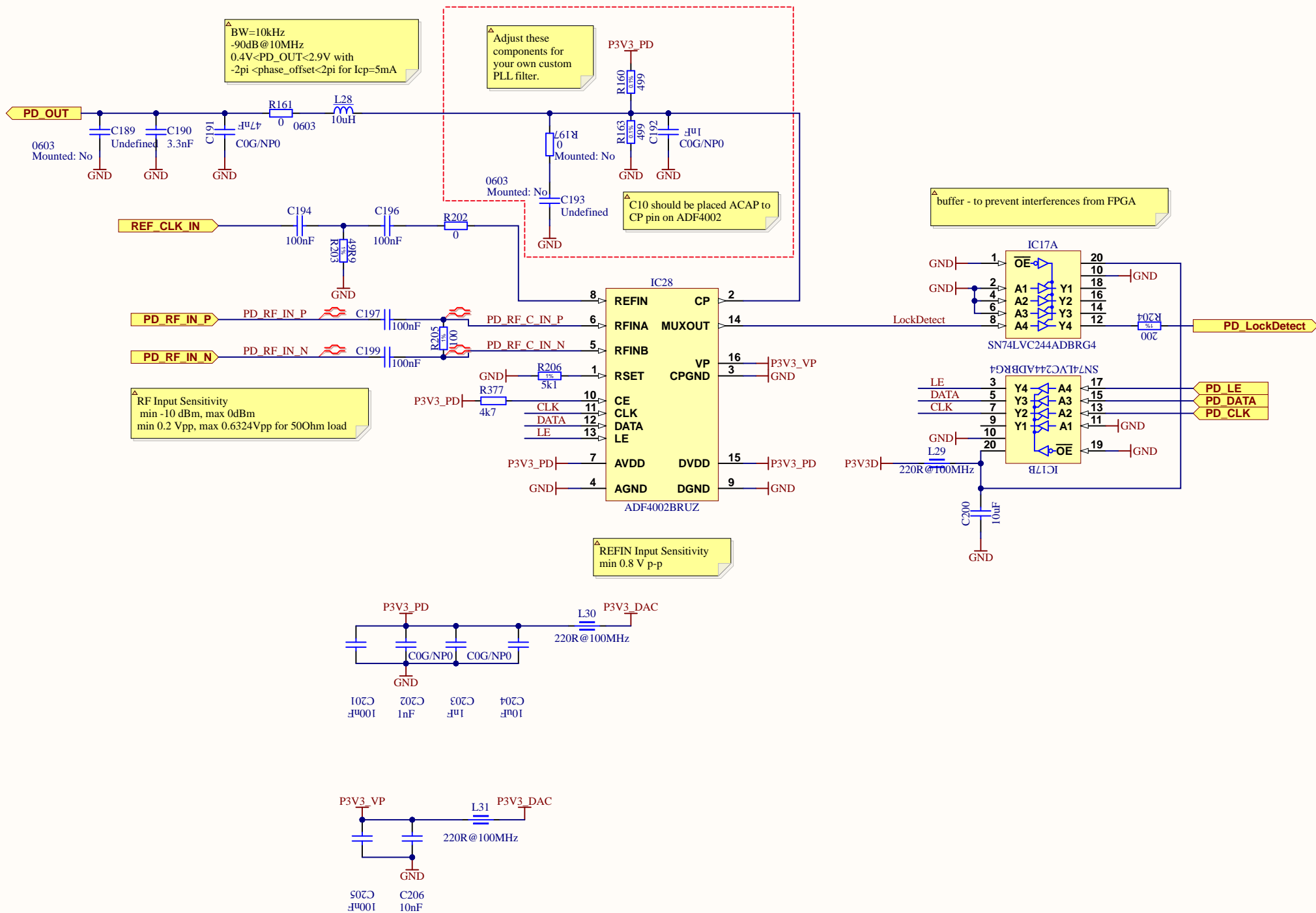


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	Project:	CITY		
	Sheet:	DDS Top		
File:	CITY_DDS_top.SchDoc	Rev.	2	03/2020
		Date	broquet	Author
		SVN:		






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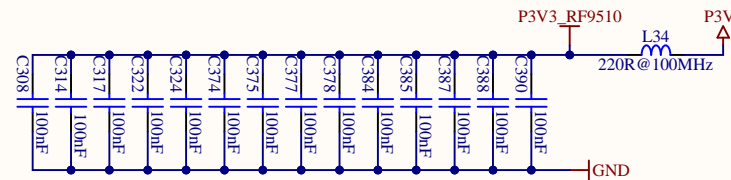
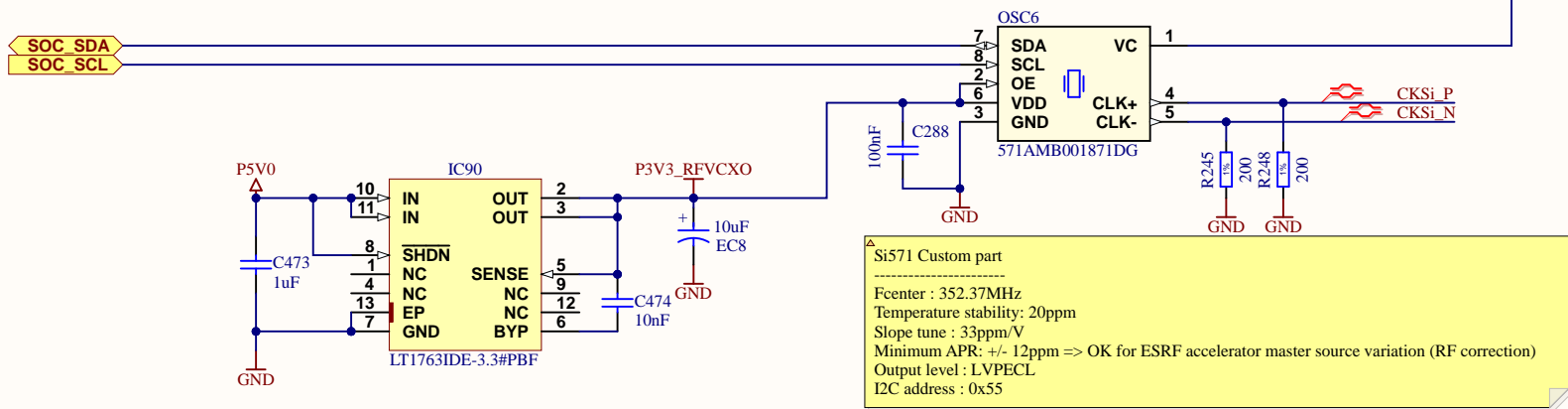
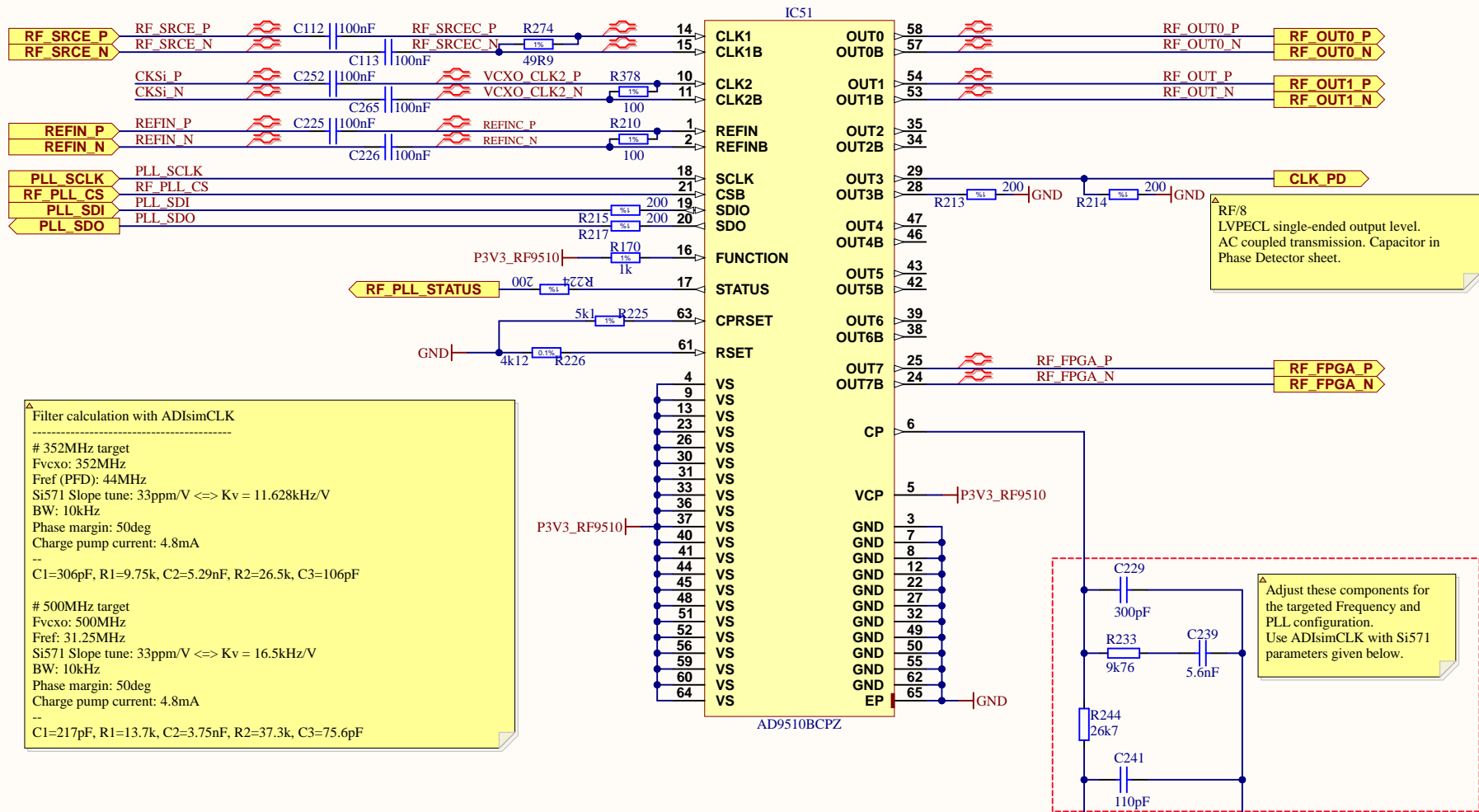
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	Doc. Num.:	Ver.:	Sheet:	
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	Project:	CITY		
	Sheet:	DDS Phase Detector		
File:	CITY_DDS_phase_detector.SchDoc	Rev.:	Date:	Author:


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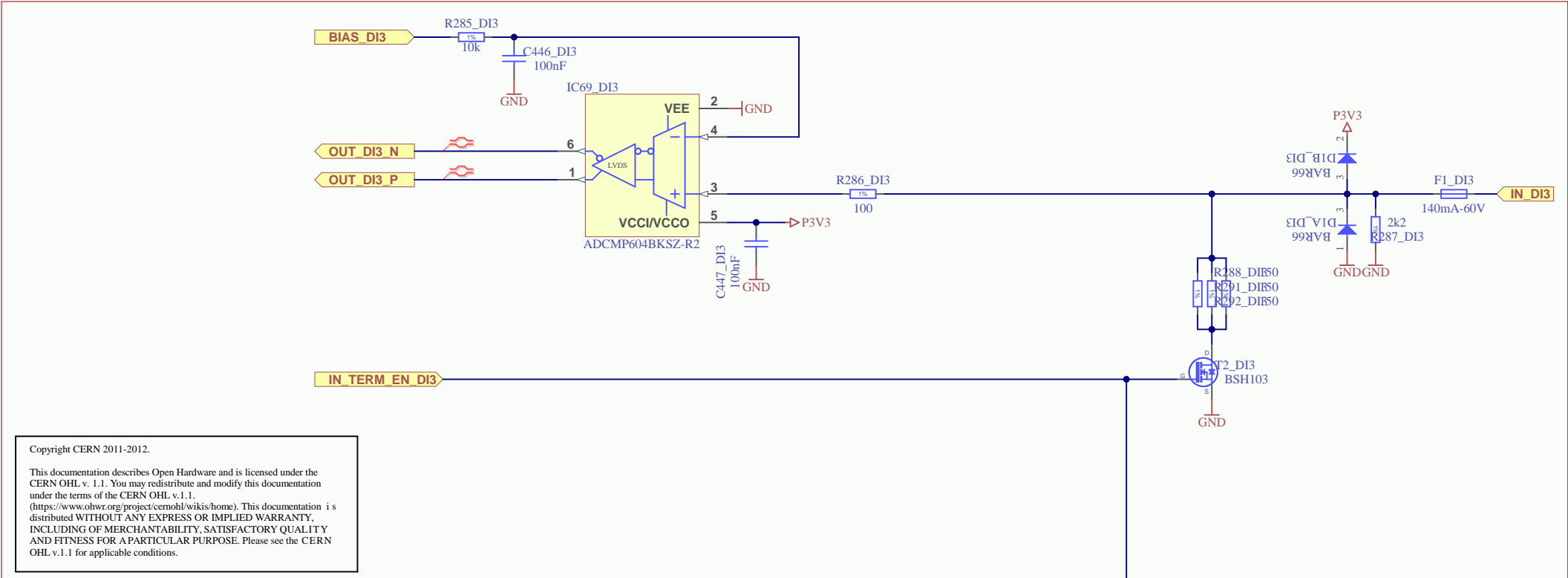
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	Doc. Num.:	Ver.:	Sheet:			
		B	6 of 36			
	Project:	CITY				
	Sheet:	DDS Power Supply Regulators				
	File:	CITY_DDS_power.SchDoc				
	Rev.	2	03/2020	broquet		
	Date					
	Author					
	SVN:					

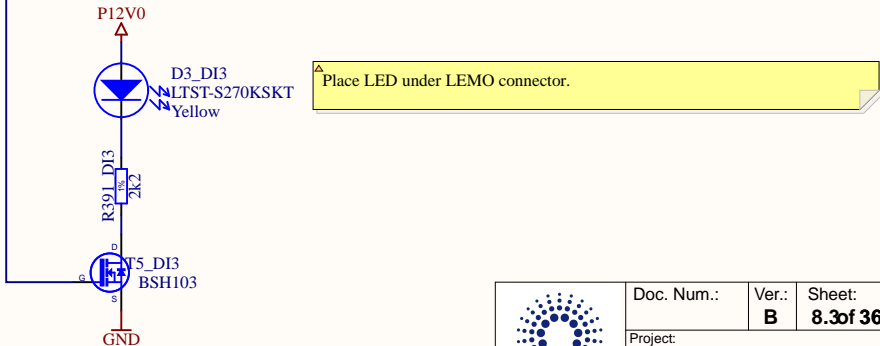


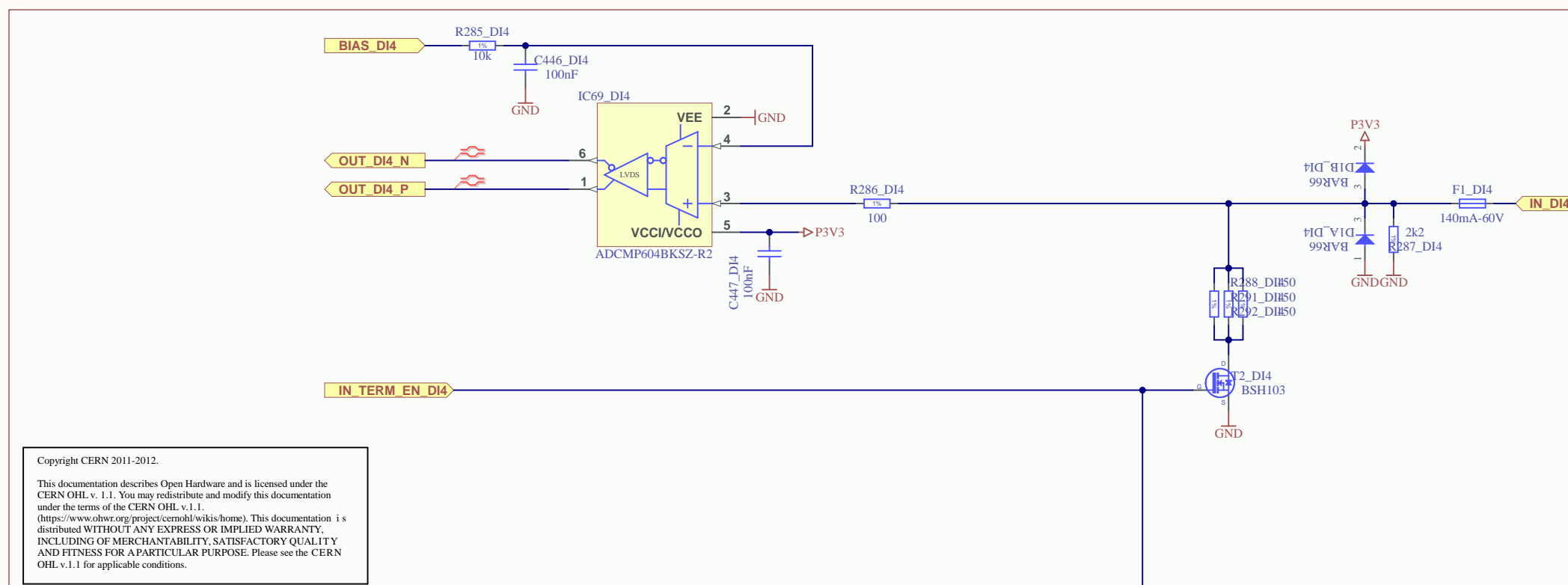
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	Doc. Num.:	Ver.:	Sheet:	-	-	-
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	Sheet:	2				
	File:	CITY_DDS_RF_clocking.SchDoc				
				Rev.	Date	Author
						broquet
				SVN:		

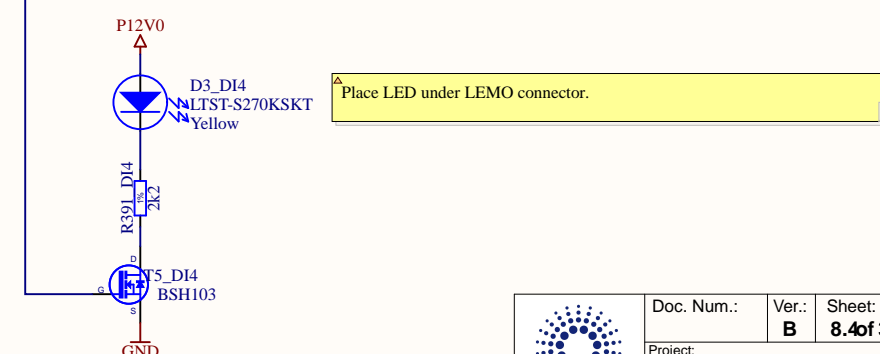


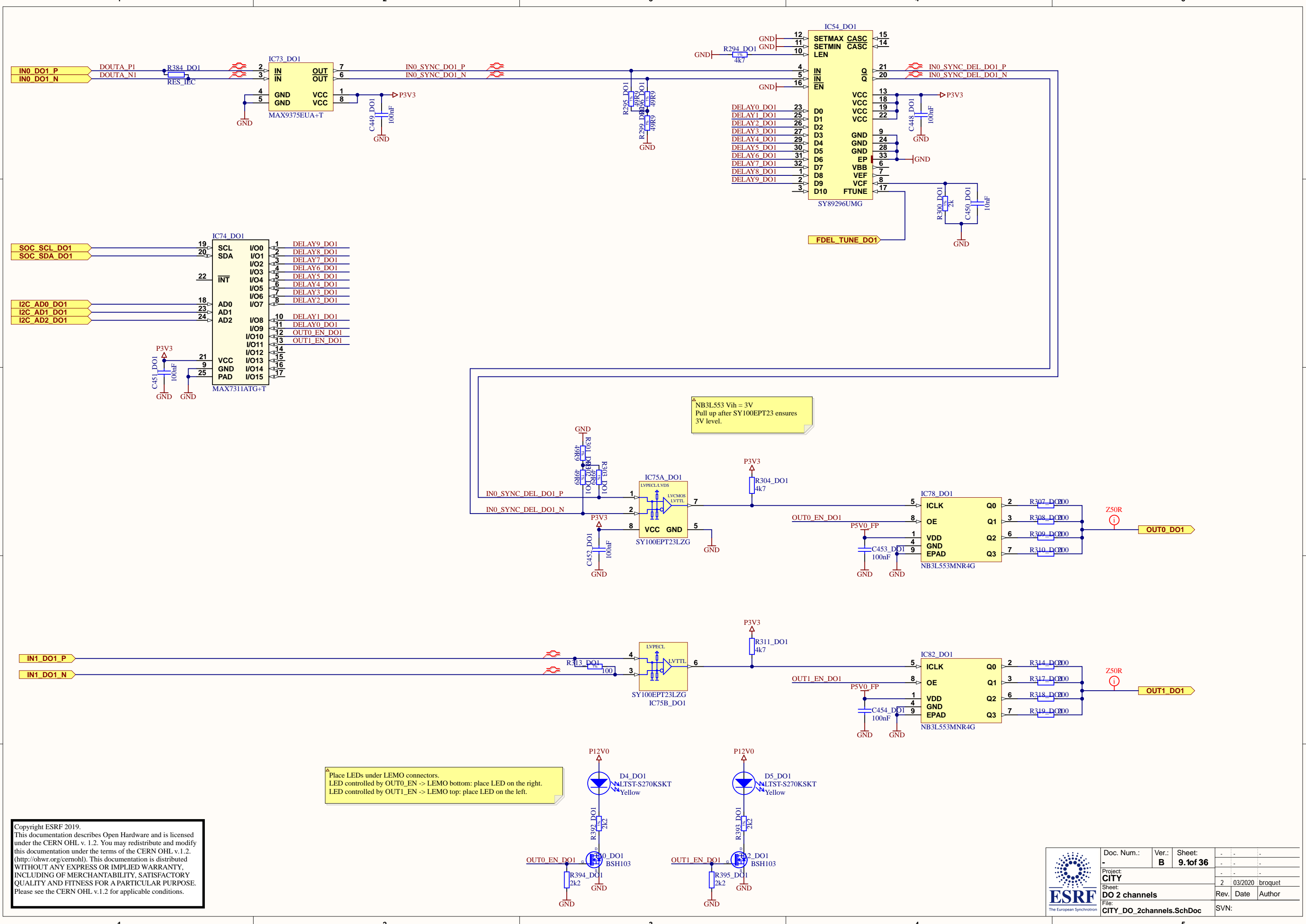
Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

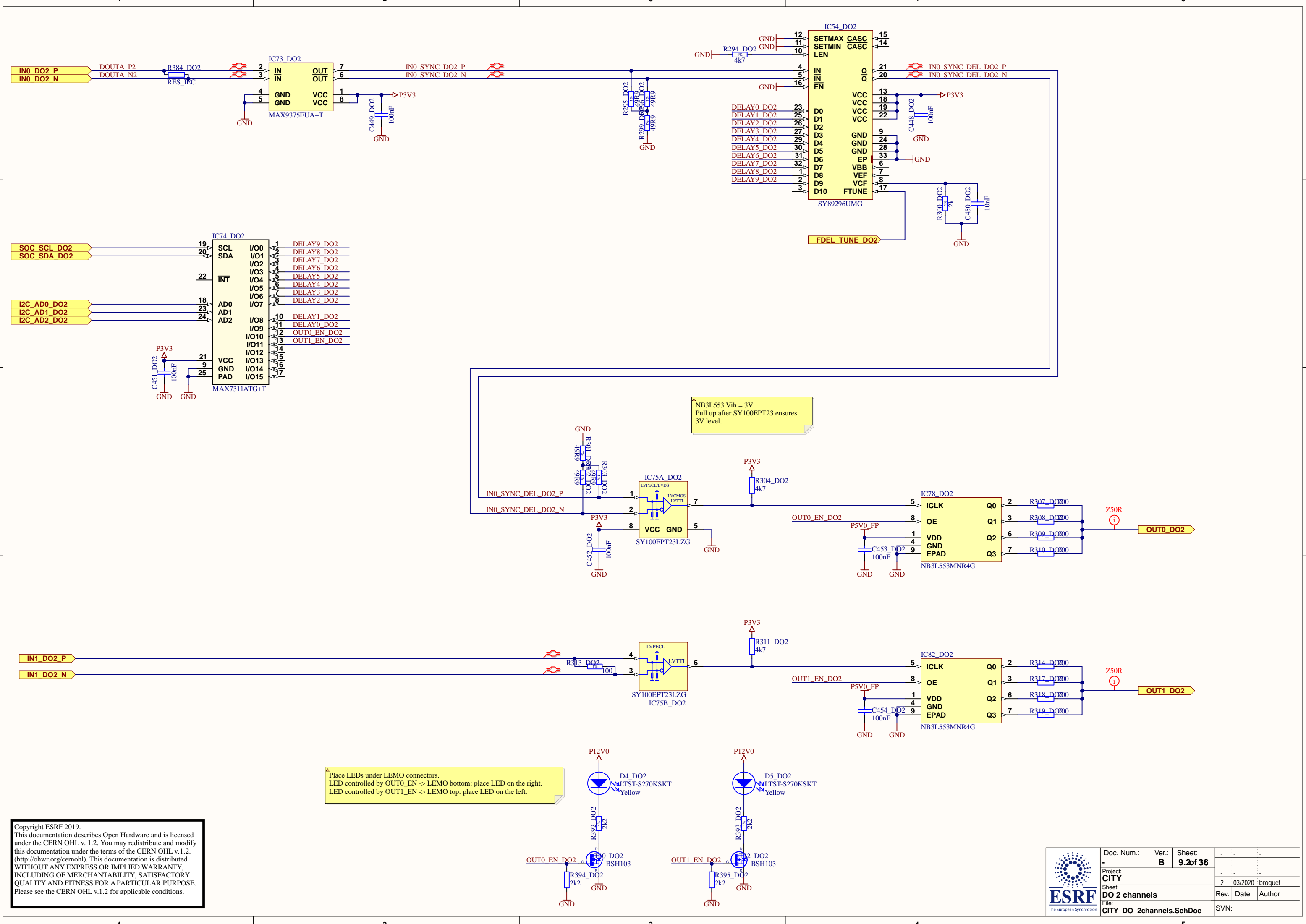





Based on FMC DIO 5ch TTL schematics, EDA-02408-V2-0

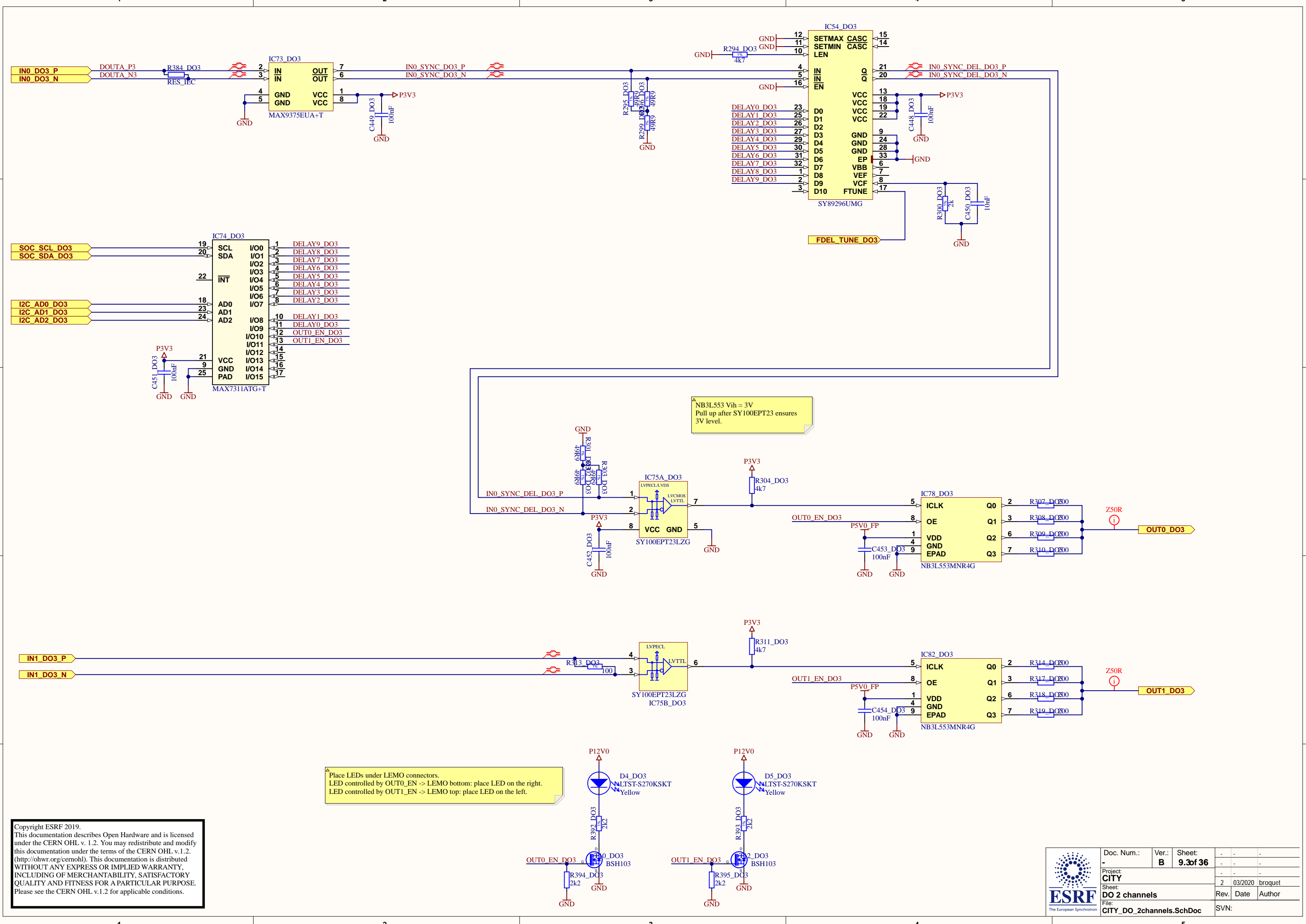







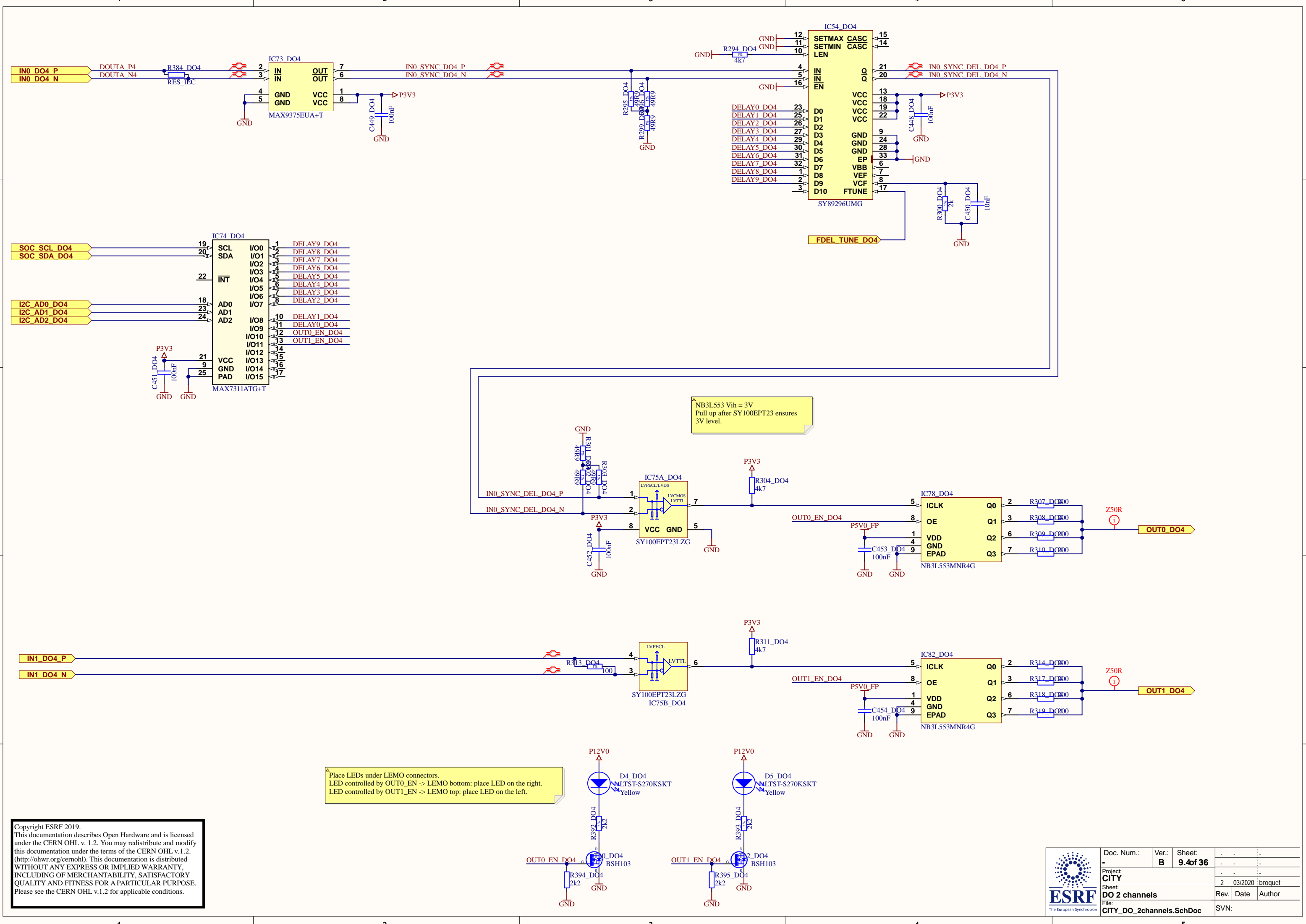
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	Doc. Num.:	Ver.:	Sheet:	-	-	-
	-	B	9.2 of 36	-	-	-
	Project:	CITY		-	-	-
	Sheet:	DO 2 channels		2	03/2020	broquet
	File:	CITY_DO_2channels.SchDoc		Rev.	Date	Author
				SVN:		



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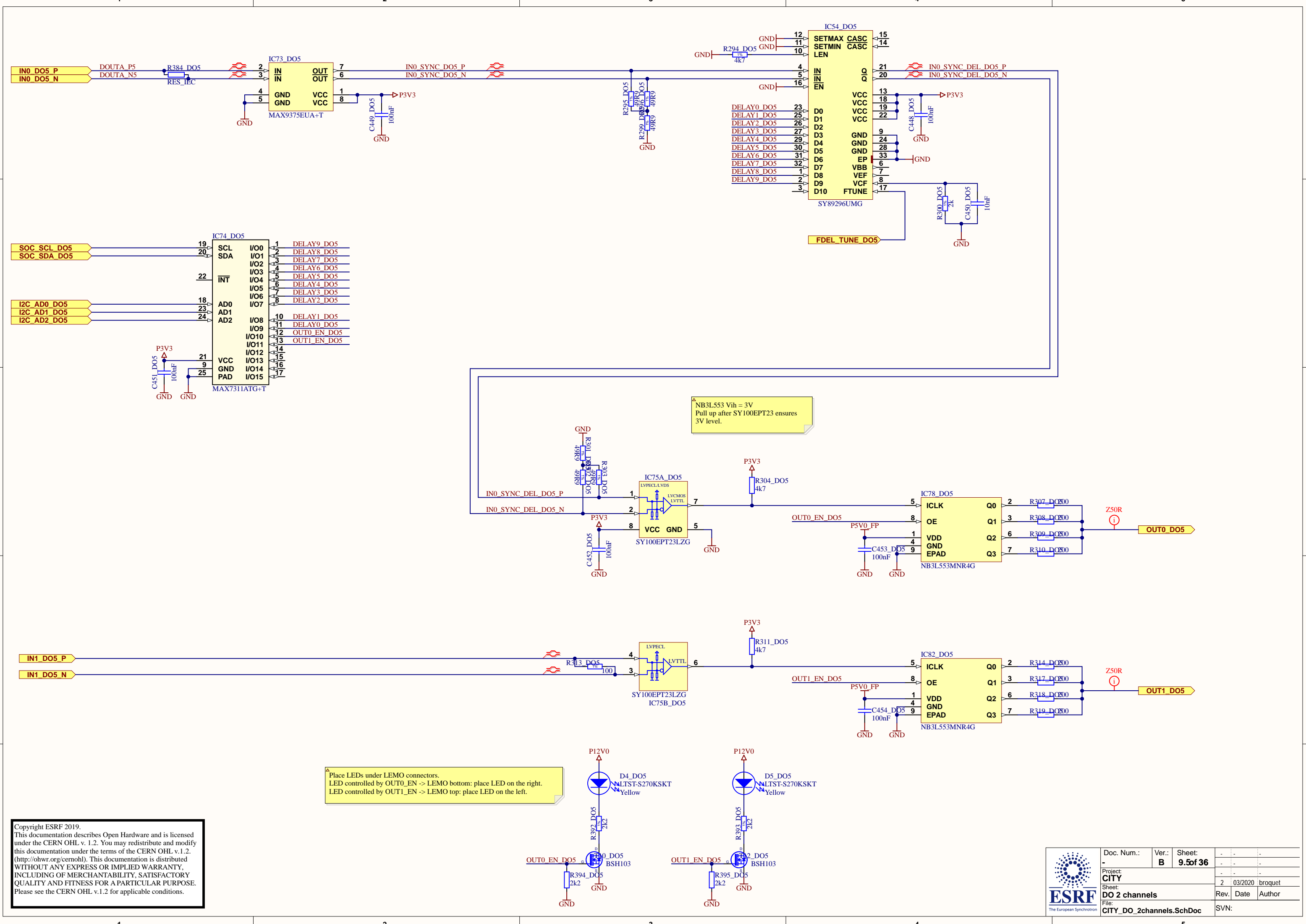
 The European Synchrotron	Doc. Num.:	Ver.:	Sheet:	-	-	-
	-	B	9.3 of 36	-	-	-
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	Sheet:	DO 2 channels				
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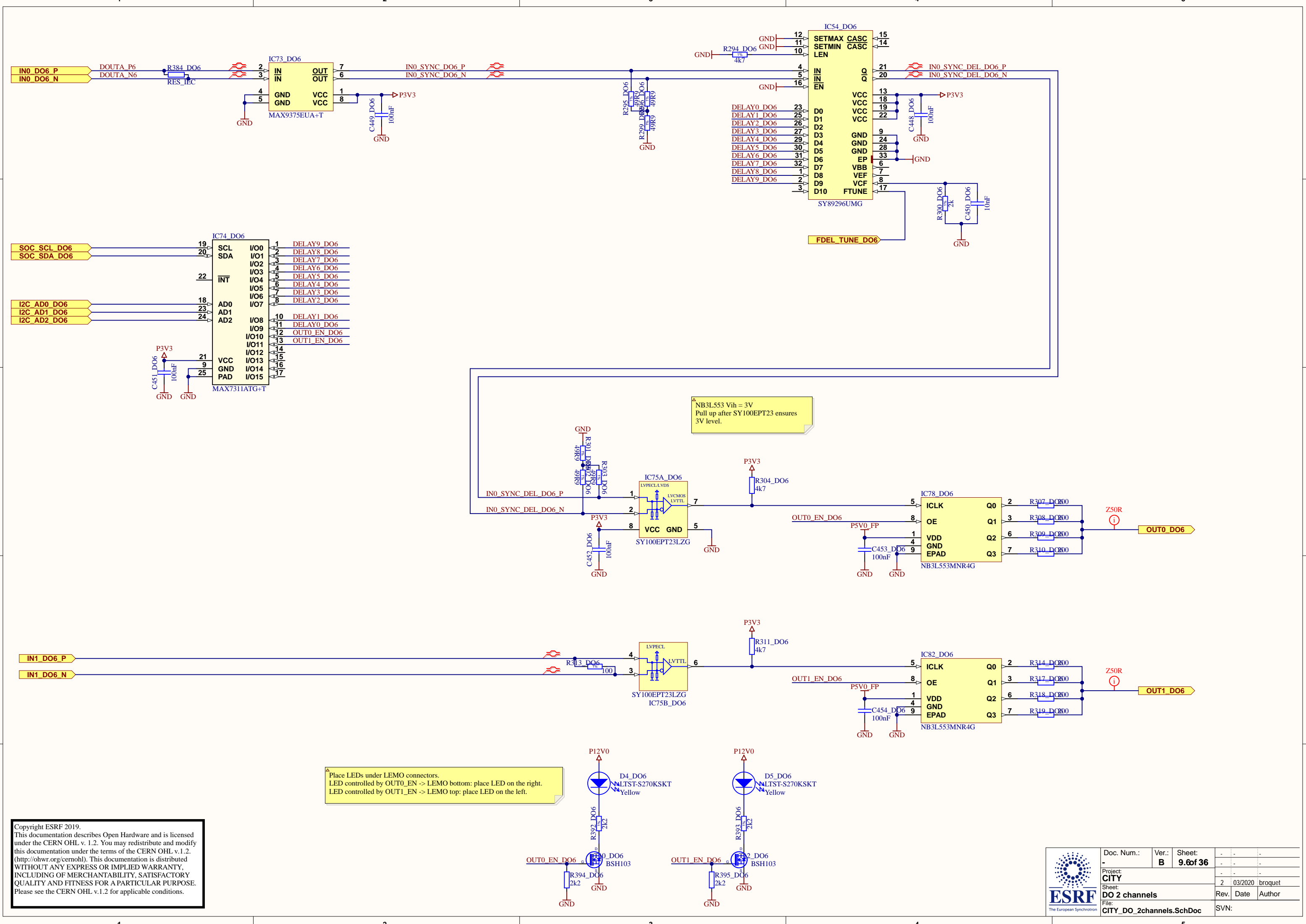
Place LEDs under LEMO connectors.
LED controlled by OUT0_EN -> LEMO bottom: place LED on the right.
LED controlled by OUT1_EN -> LEMO top: place LED on the left.

NB3L553 Vih = 3V
Pull up after SY100EPT23 ensures 3V level.




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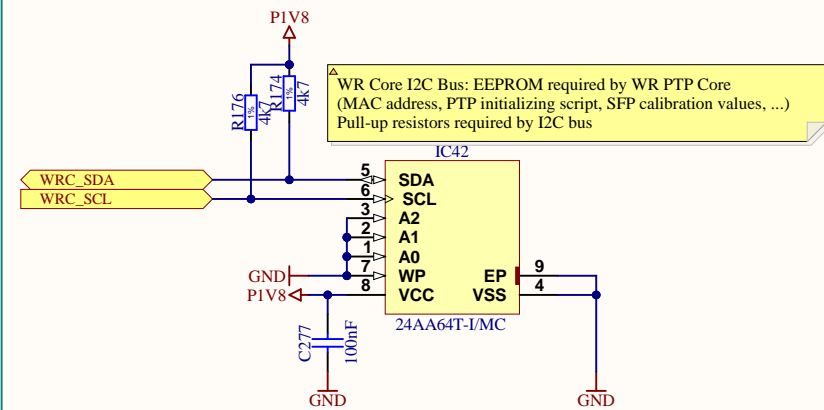
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	-	B	9.5 of 36	-	-	-
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				Rev.	Date	Author
						broquet
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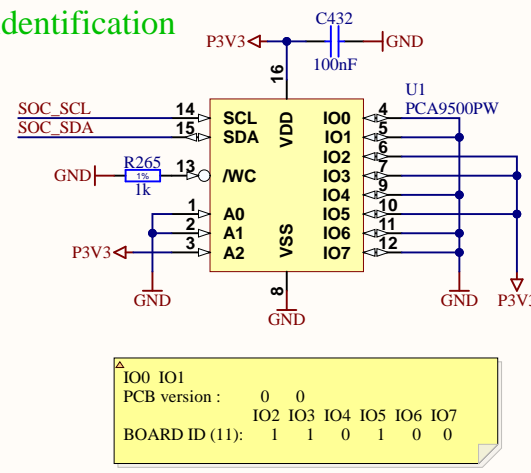
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	-	B	9.6 of 36	-	-	-
	Project:	CITY				
	Sheet:	DO 2 channels				
	File:	CITY_DO_2channels.SchDoc				
	Rev.	Date	Author	2	03/2020	broquet
	SVN:					

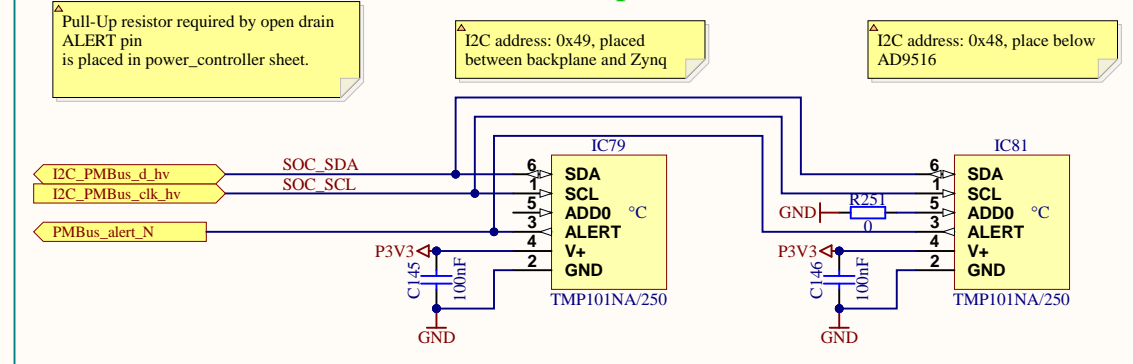
64 Kbit EEPROM (I2C @ 100 kHz max)



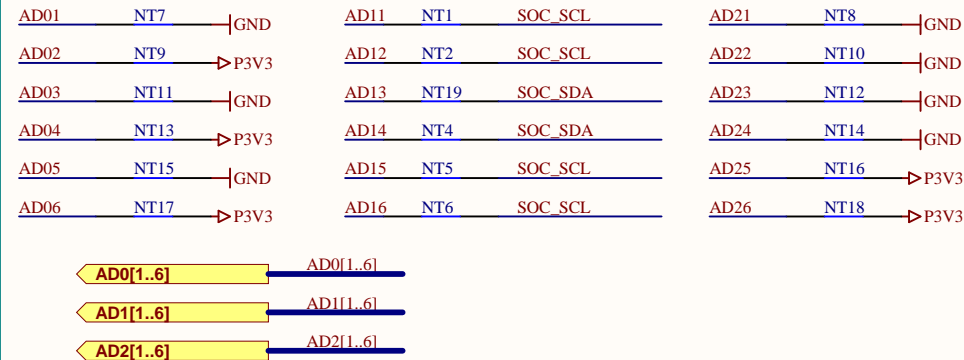
Board identification



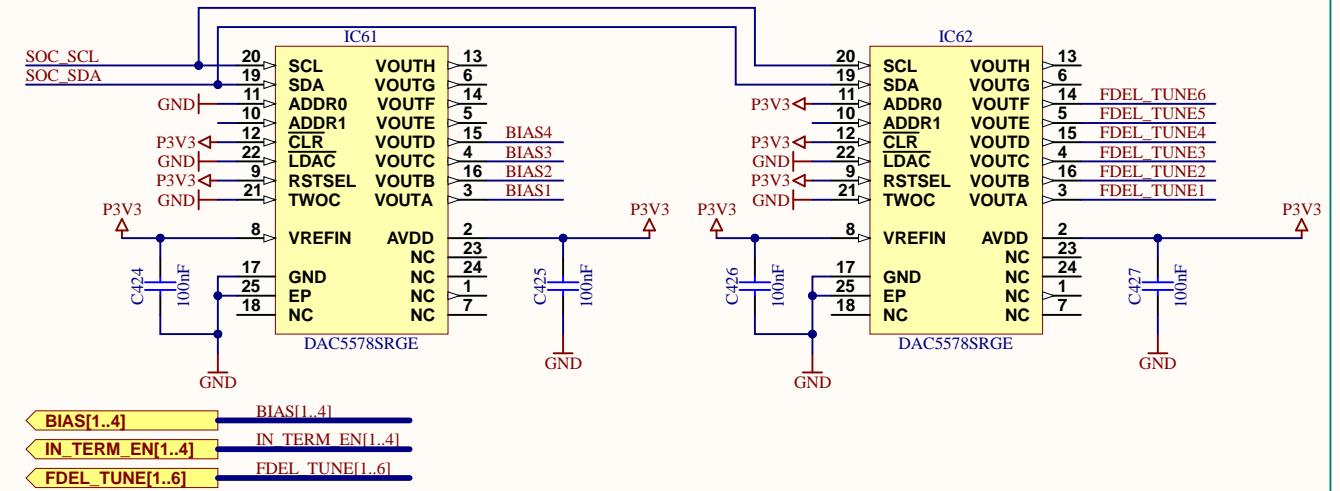
Card temperature surveillance



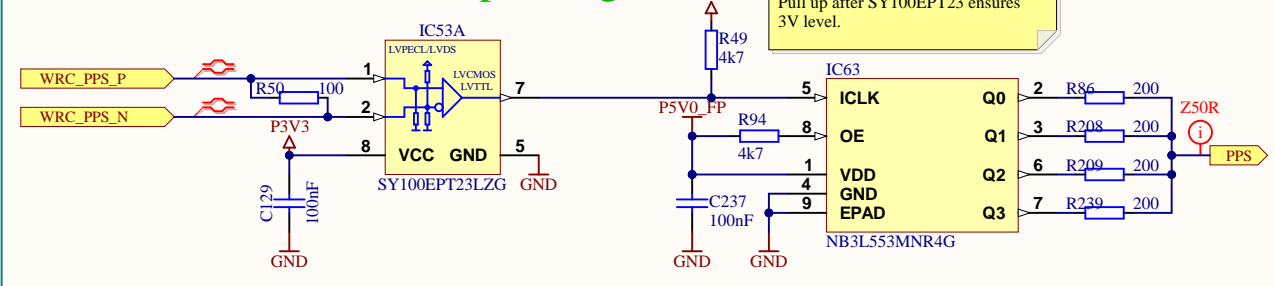
I2C address bus for DO channel IO registers



DACs for Inputs BIAS and Fine Delay Tune / User LED + GPIO



WR Pulse Per Second output stage



changelog

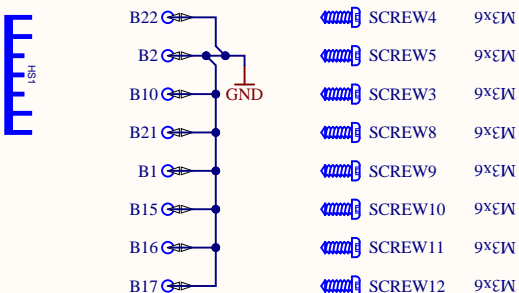
V2-0:
* several small component changes, not documented here
* power supply sequence improved
* bank 501 and all connected chips changed to 1.8V for full RGMII support
* PHY SPI wired to bank 35, in addition to existing MDIO
* UART changed to FT230X
* power controller UCD90120 GPIO rewired cause pull-downs; 2nd connector added for use of TI adapter

V3-0:
* few small component changes, not documented here
* external patch-panel interrupt line to SoC
* i2c level converter ADUM1250 turned around cause i2c compliance problems
* D-sub 15 wiring change to follow CERN cabling convention
* TMP101 thermal sensors added

CITY V1-0:
* See the CHANGES.TXT document provided in the project

CITY V2-0:
* See CHANGES.TXT file and OHWR project issues.
* Re-routing some differential pairs

PCB mounting holes, screws & heatsink



I2C addresses
I2C addresses hex number are given in the 7bit format aligned to LSb (without R/W bit).
Example: I2C addr = 0x74 (1 1 0 1 0 0) -> Read access = 1 1 0 1 0 0 1 (0xE9)

WR Core I2C:
24AA64T -> 0x50


SoC I2C (I2C PMBus):
CITY_power-controller.SchDoc
UCD90120ARGC -> 0x5B

CITY_misc.SchDoc
TMP101(1) -> 0x48 (with ADD0 = 0)
TMP101(2) -> 0x49 (with ADD0 = Float)
DAC5578(1) -> 0x4C (with ADDR0 = GND, ADDR1 = float)
DAC5578(2) -> 0x4D (with ADDR0 = VCC, ADDR1 = float)
BOARD ID I/O -> 0x24 (with A0 = A1 = GND, A2 = VCC)
BOARD ID EEPROM -> 0x54 (with A0 = A1 = GND, A2 = VCC)

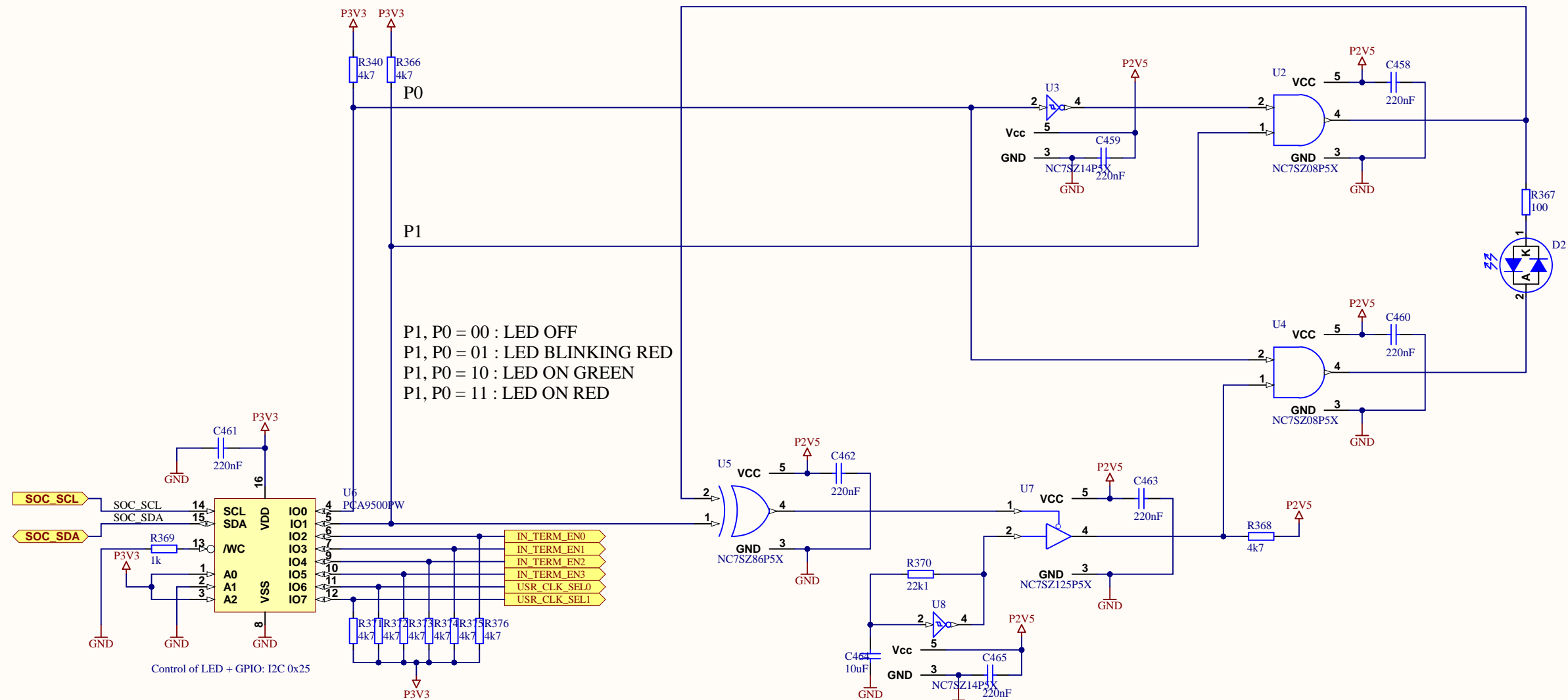
CITY_user_led.SchDoc
General IO control -> 0x25 (AD0 = VCC, AD1 = GND, AD2 = VCC)

DO_2channels.SchDoc (I/Os control: Finde delay, Output drivers enable)
0 -> 0x10 (AD0 = GND, AD1 = SCL, AD2 = GND)
1 -> 0x11 (AD0 = VCC, AD1 = SCL, AD2 = GND)
2 -> 0x12 (AD0 = GND, AD1 = SDA, AD2 = GND)
3 -> 0x13 (AD0 = VCC, AD1 = SDA, AD2 = GND)
4 -> 0x14 (AD0 = GND, AD1 = SCL, AD2 = VCC)
5 -> 0x15 (AD0 = VCC, AD1 = SCL, AD2 = VCC)

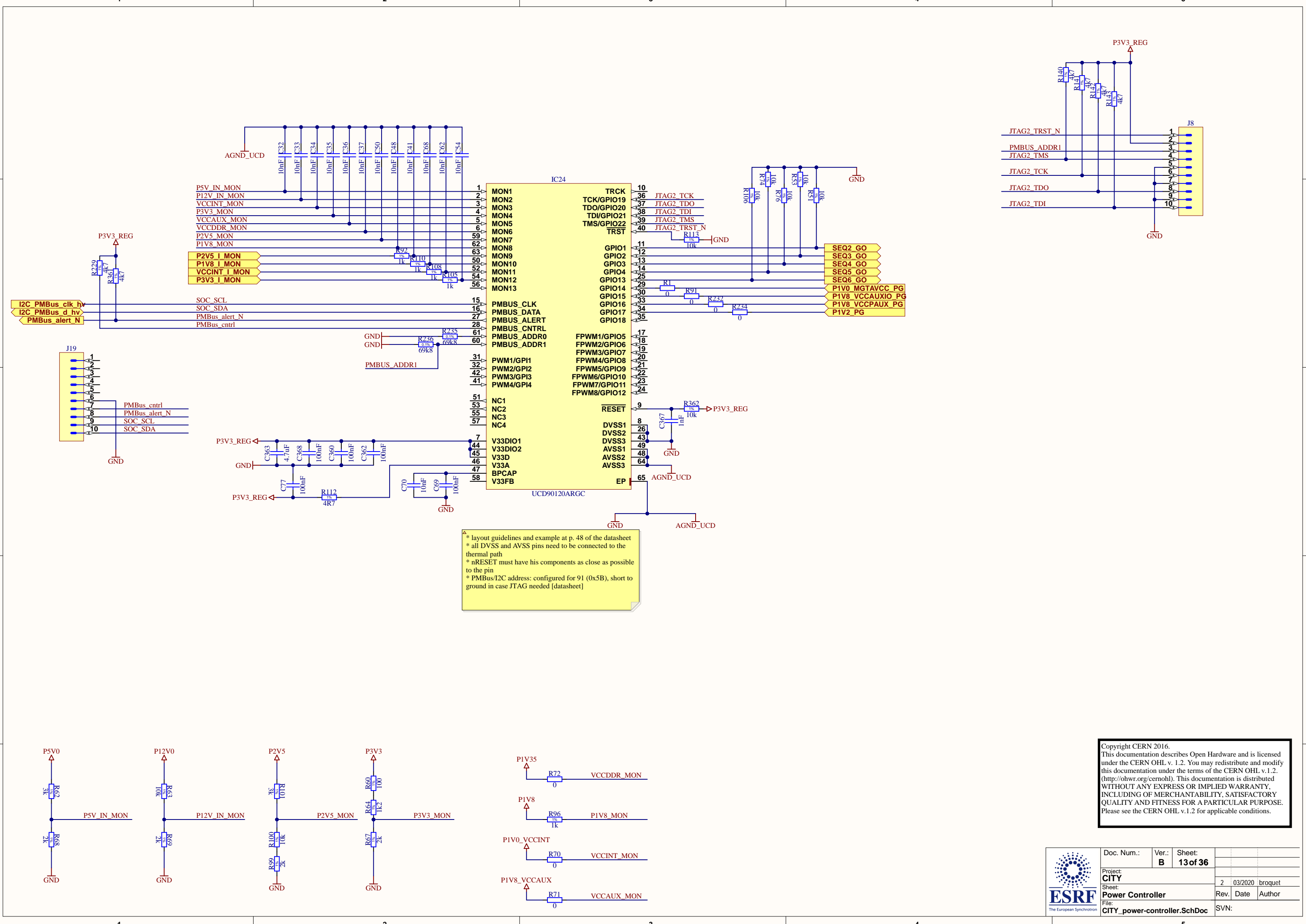
RF_Clocking.SchDoc
RF clock delay for outputs synchronization -> 0x16 (AD0 = GND, AD1 = SDA, AD2 = VCC)
Si571 -> 0x55 (default, fixed).

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	Sheet:	Misc		
	File:	CITY_misc.SchDoc		
	2	03/2020	broquet	
	Rev.	Date	Author	
				SVN:

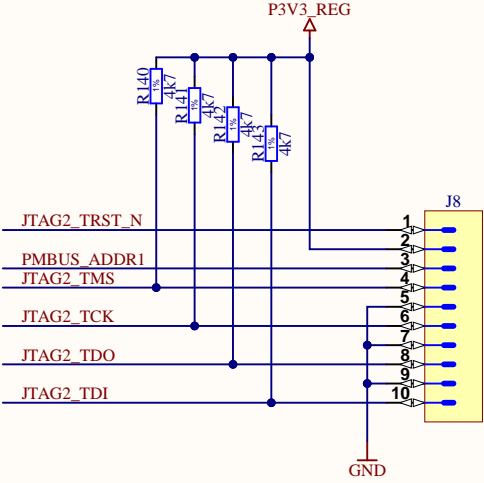
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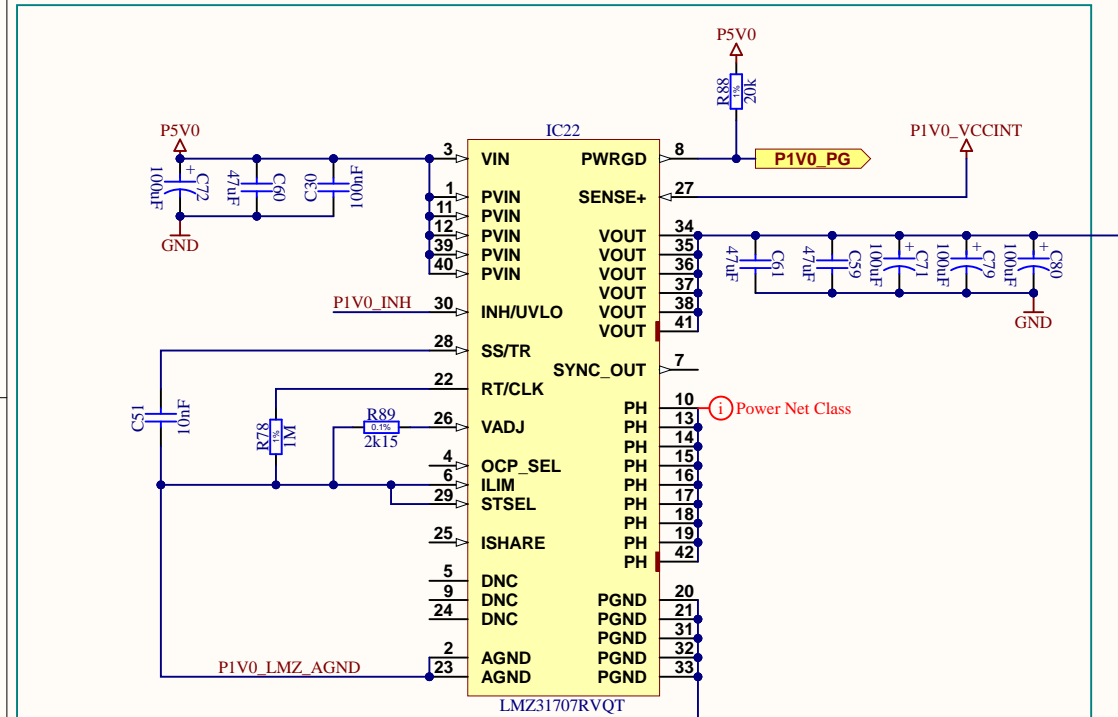


* layout guidelines and example at p. 48 of the datasheet
* all DVSS and AVSS pins need to be connected to the thermal path
* nRESET must have his components as close as possible to the pin
* PMBus/I2C address: configured for 91 (0x5B), short to ground in case JTAG needed [datasheet]



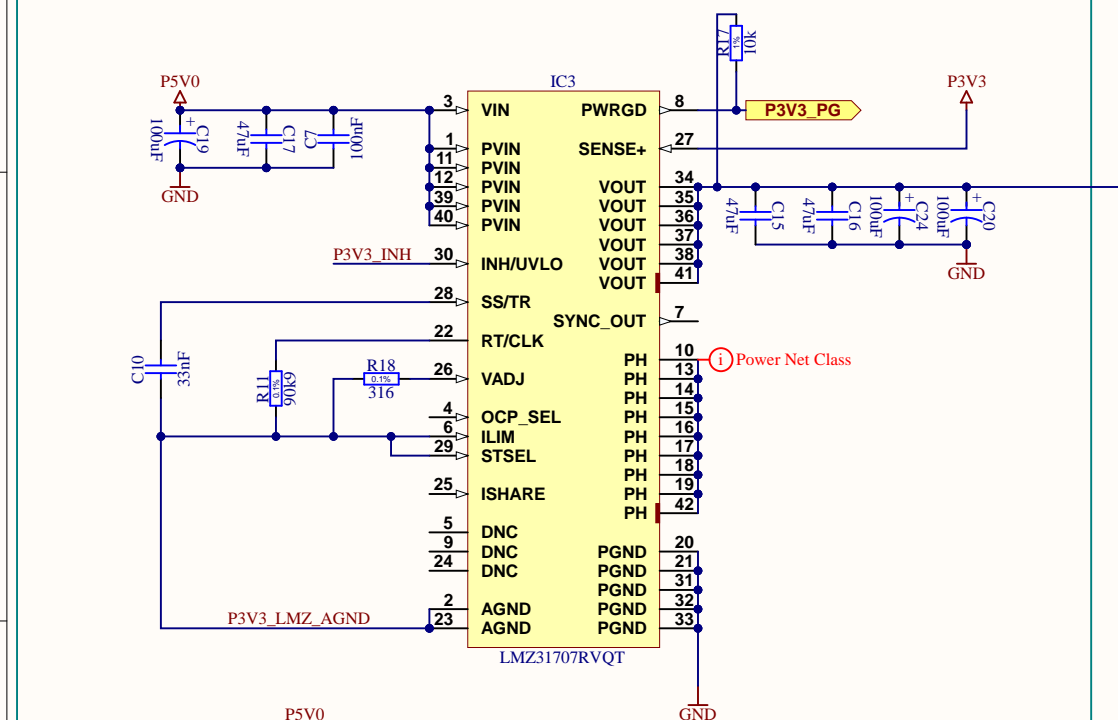
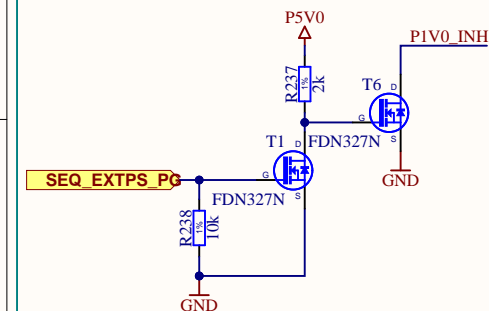
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 ESRF The European Synchrotron	Doc. Num.:	Ver.:	Sheet:			
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	Project:					
	CITY					
	Sheet:					
	Power Controller			2	03/2020	broquet
	File:			Rev.	Date	Author
	CITY_power-controller.SchDoc			SVN:		



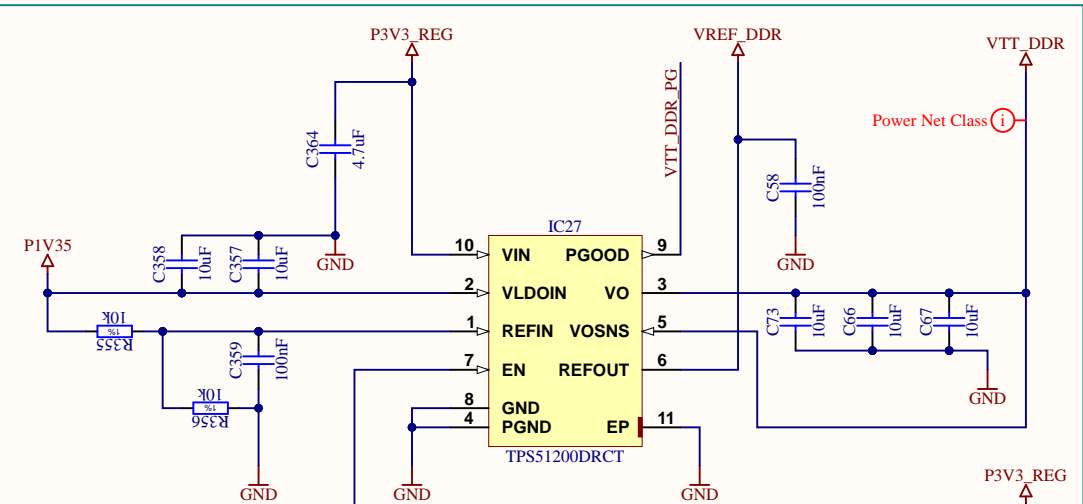
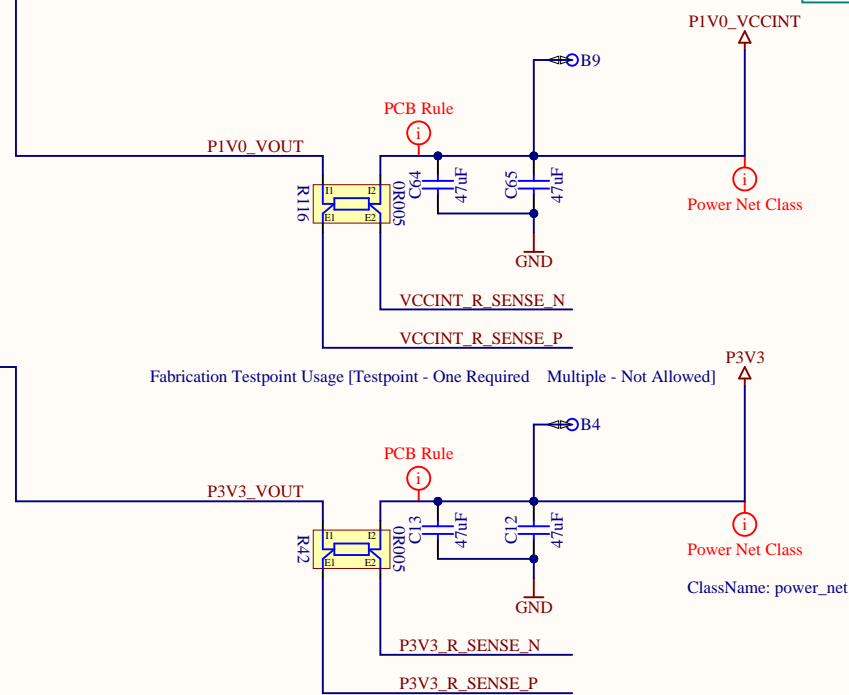
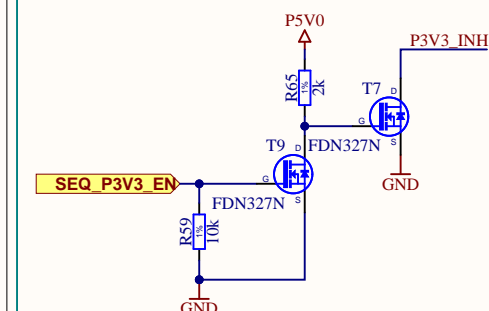
1.0V VCCPINT & VCCINT (5A)

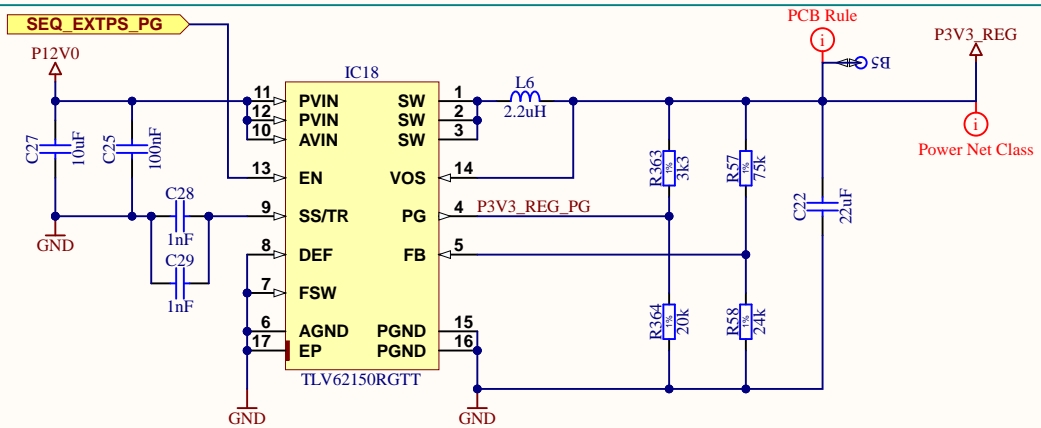
*AGND should have a dedicated plane;
 *datasheet p. 25 has an example layout
 *PH pins must be connected to one another using a small copper island under the device;
 *100nF directly across the PVIN and PGND pins
 *Sense+ to be connected close to the load (VCCINT)
 *RSET must be between pin 26 and 23 directly
 *fsw = 250 kHz



3.3V VCCO & FMCs (7A)

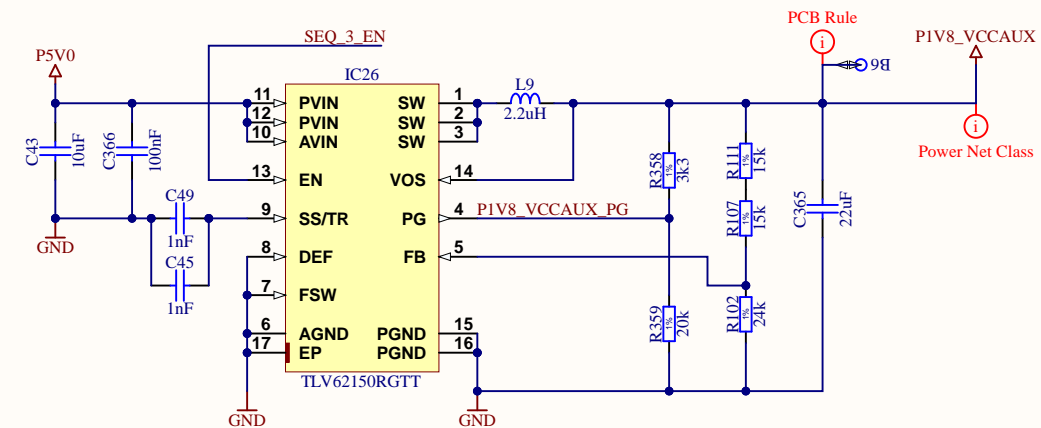
*AGND should have a dedicated plane;
 *datasheet p. 25 has an example layout
 *PH pins must be connected to one another using a small copper island under the device;
 *100nF directly across the PVIN and PGND pins
 *Sense+ to be connected close to the load (VCCINT)
 *RSET must be between pin 26 and 23 directly
 *fsw = 750 kHz





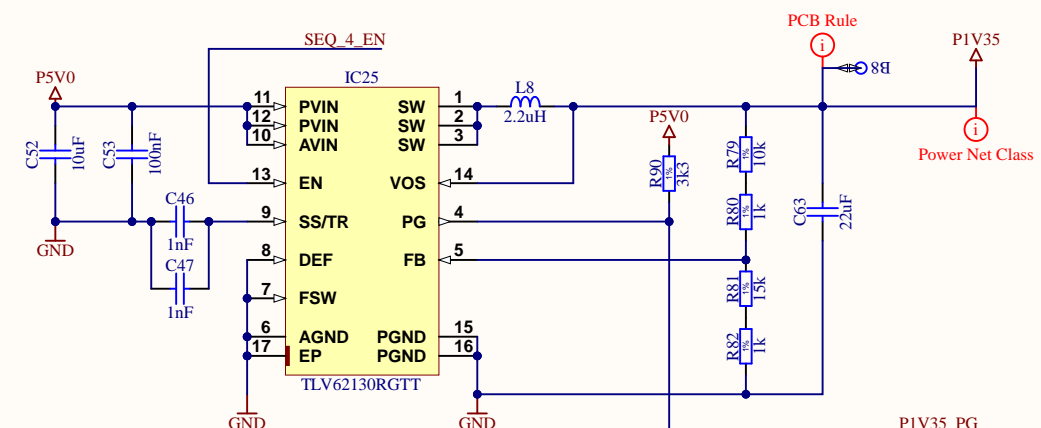
3.3V VREG (1A)

- *fsw = 2.5 MHz
- *layout example at datasheet p.21
- *100nF directly across the AVIN and AGND pins
- * Not only used for the LDOs at this page!



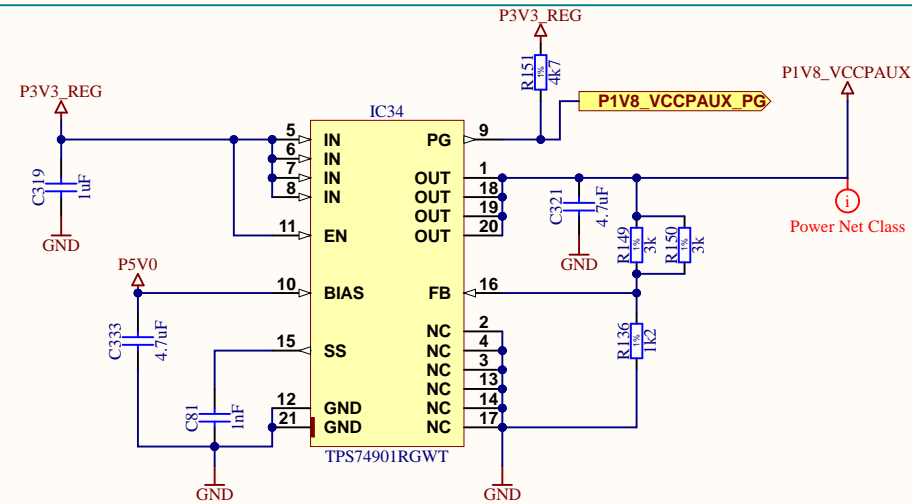
1.8V VCCAUX (800mA)

- *fsw = 2.5 MHz
- *layout example at datasheet p.21
- *100nF directly across the AVIN and AGND pins



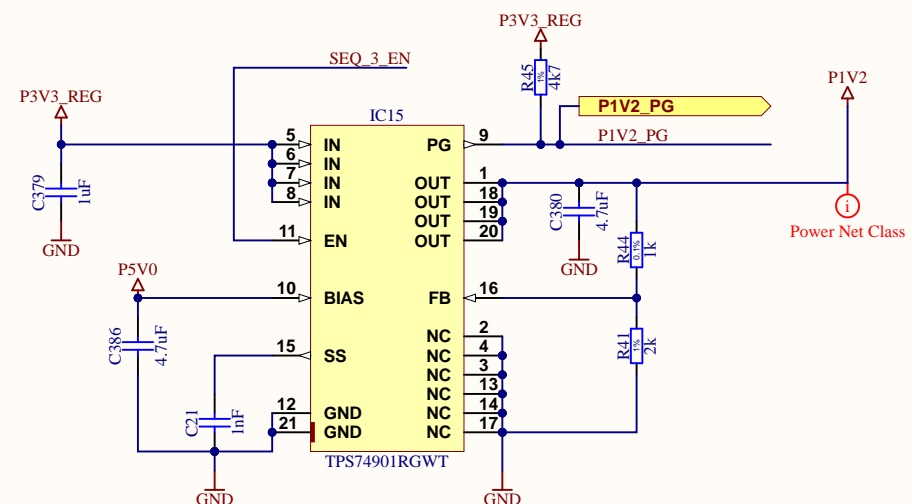
1.35V VCCDDR (1.1A)

- *fsw = 2.5 MHz
- *layout example at datasheet p.22
- *100nF directly across the AVIN and AGND pins



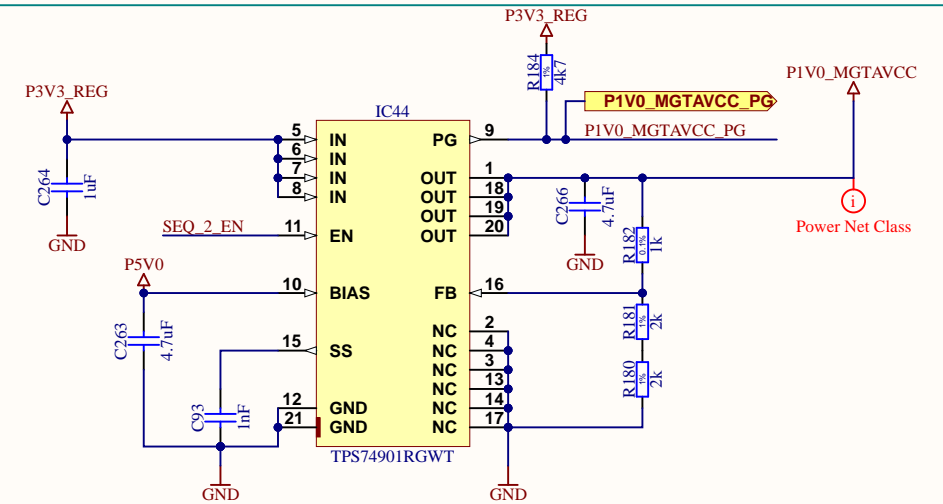
1.8V VCCPAUX (120mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; only 180 mW dissipation with a θ_{JA} of 120 °C/W.



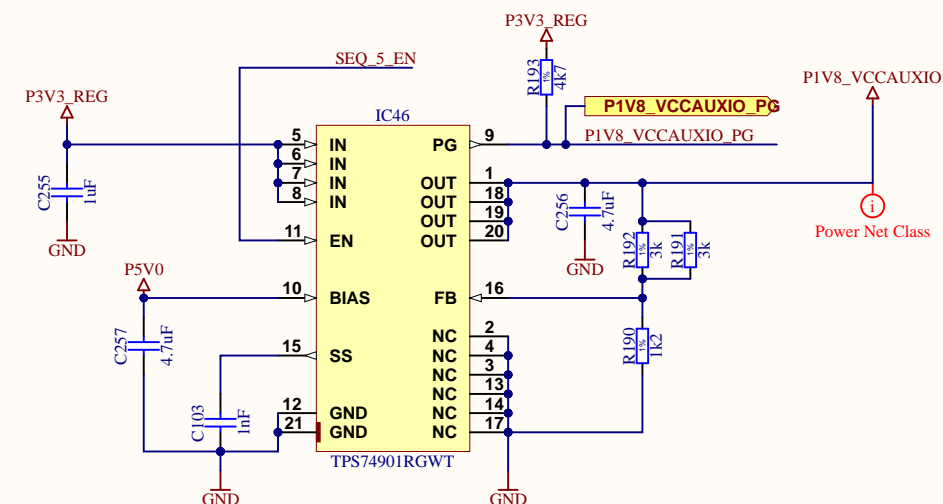
1.2V all (130mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a θ_{JA} of 120 °C/W.



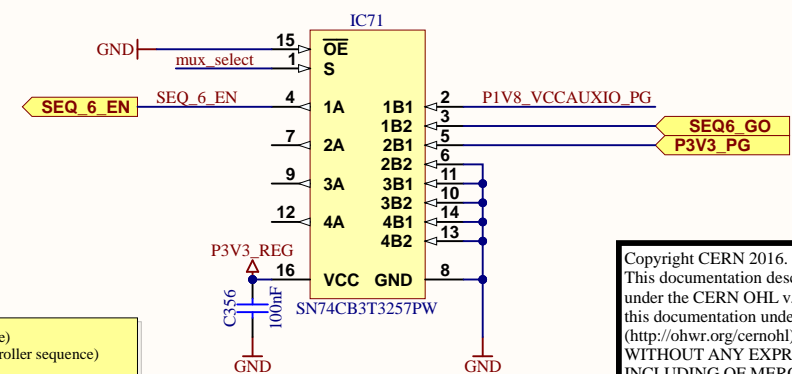
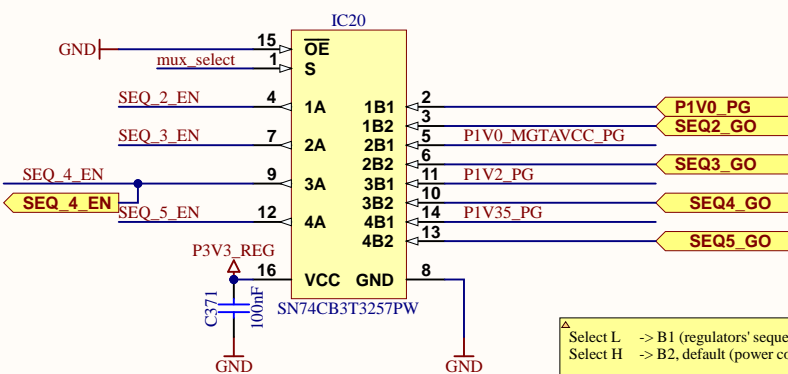
1.0V MGTAVCC (150mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 345 mW dissipation with a θ_{JA} of 120 °C/W.

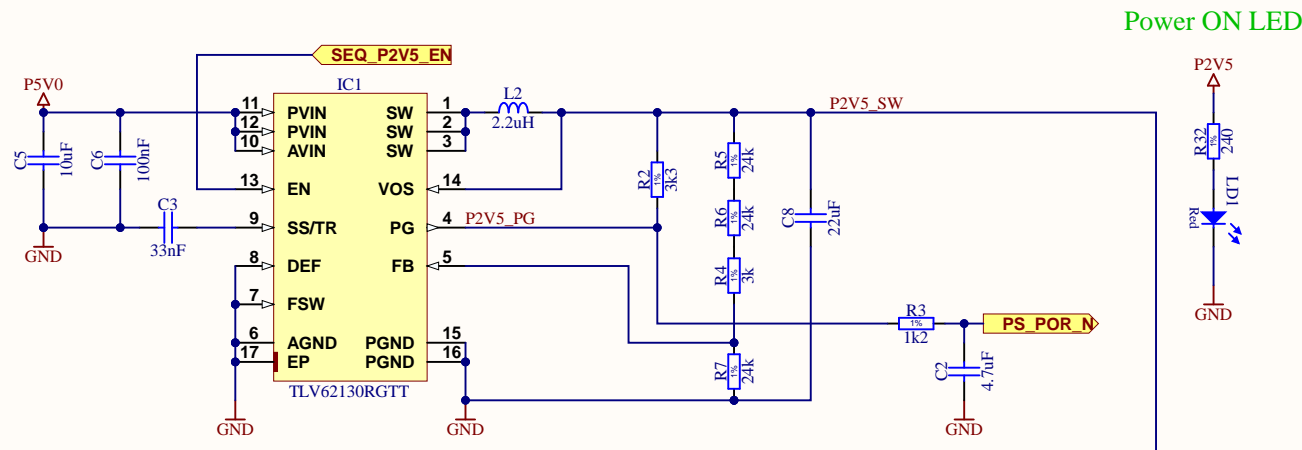


1.8V VCCAUX_IO (130mA linear)

*layout example at datasheet p.20
*the IC pad must be attached to a minimum 10x10 mm amount of copper PCB area; 273 mW dissipation with a theta_JA of 120 °C/W.



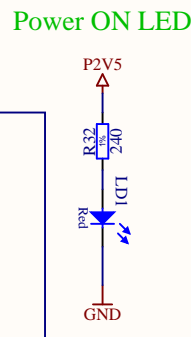
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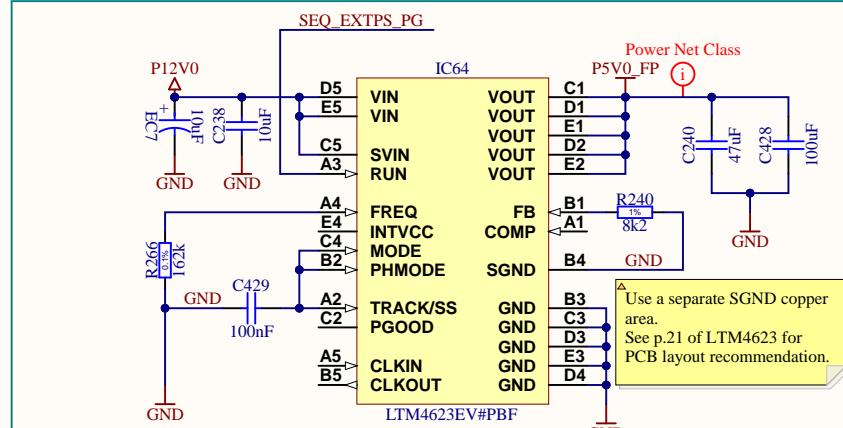
2.5V all (3A max)

*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins

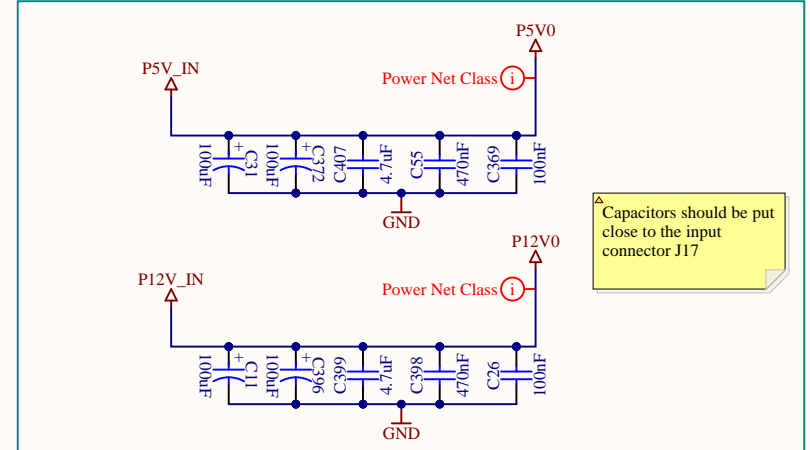
RC delay (tau=21ms) to provide the required 40ms after VCCO_0 assertion before deasserting PS_POR_B [DS191 p.18] to 2.31V (Vcc*0.7).



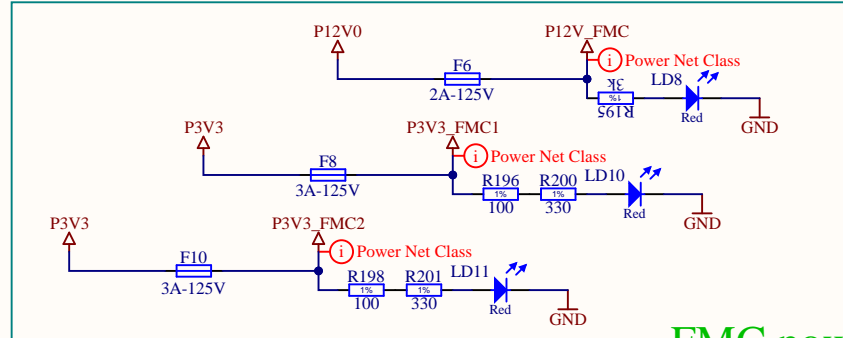
Power ON LED



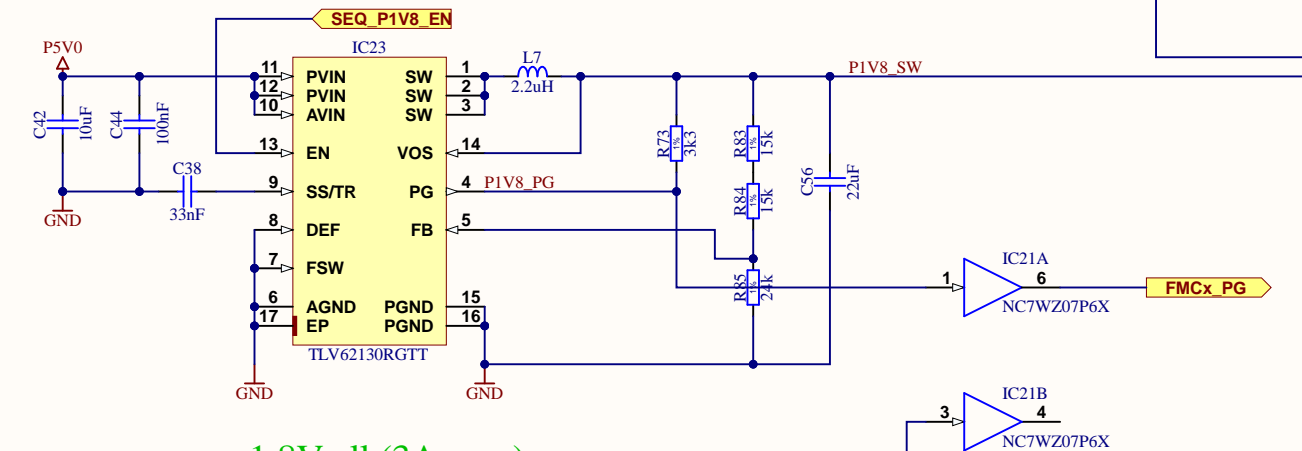
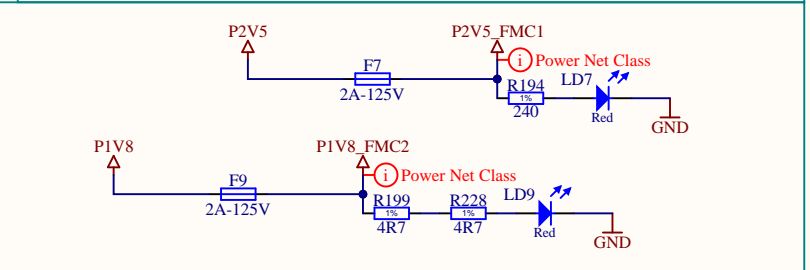
5V for Digital Output stages



Power supply decoupling

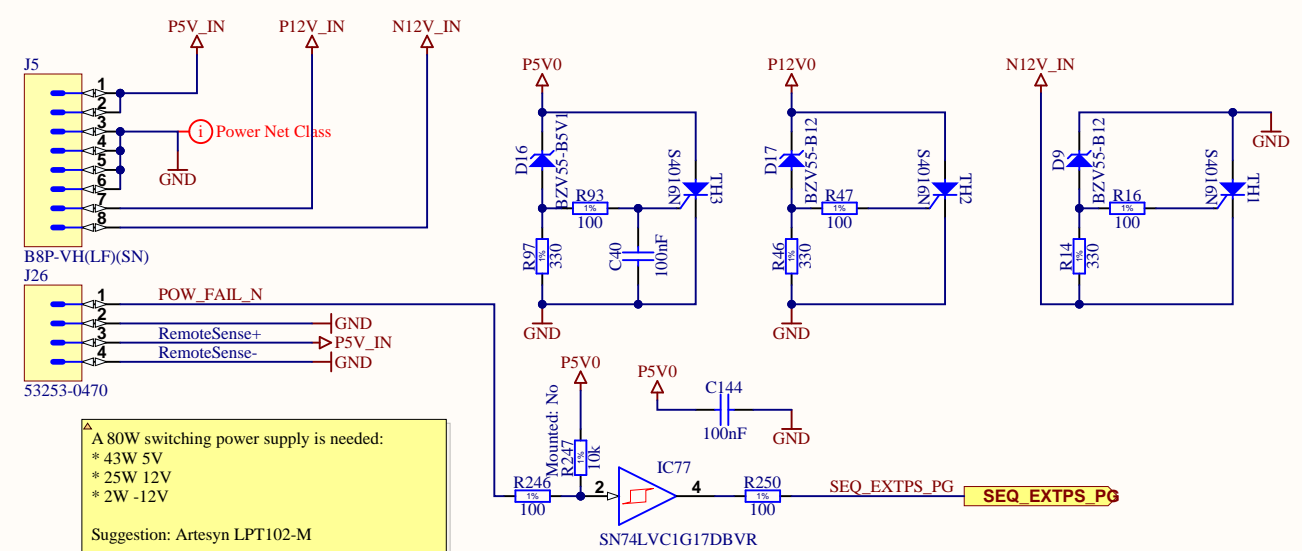
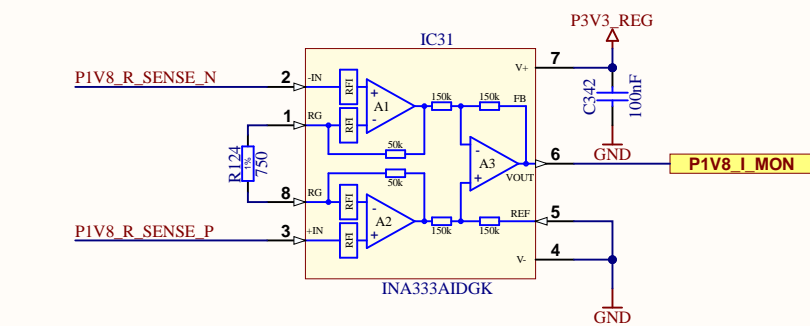
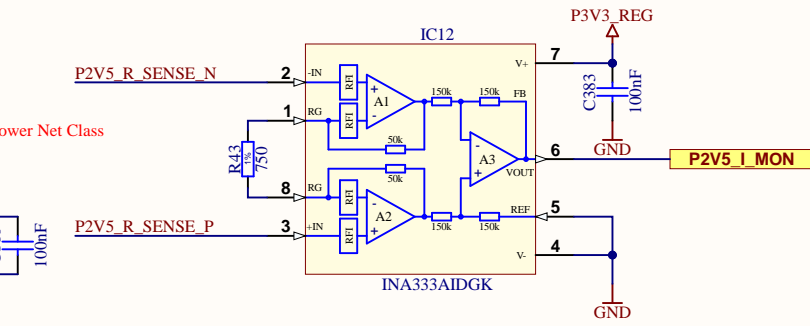
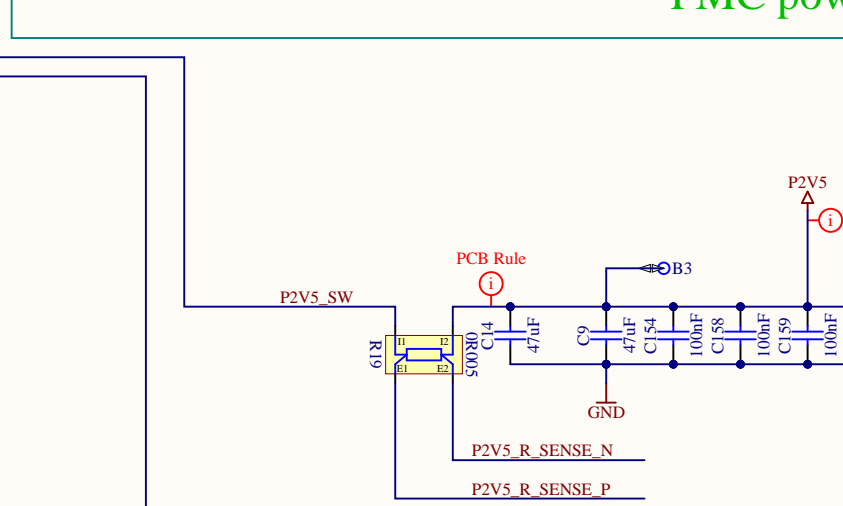
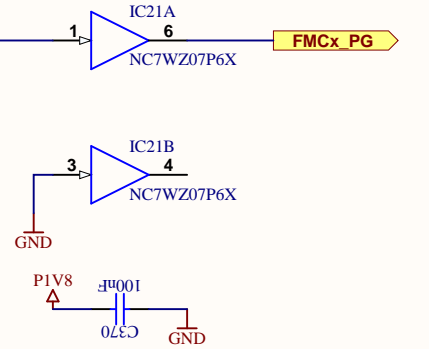


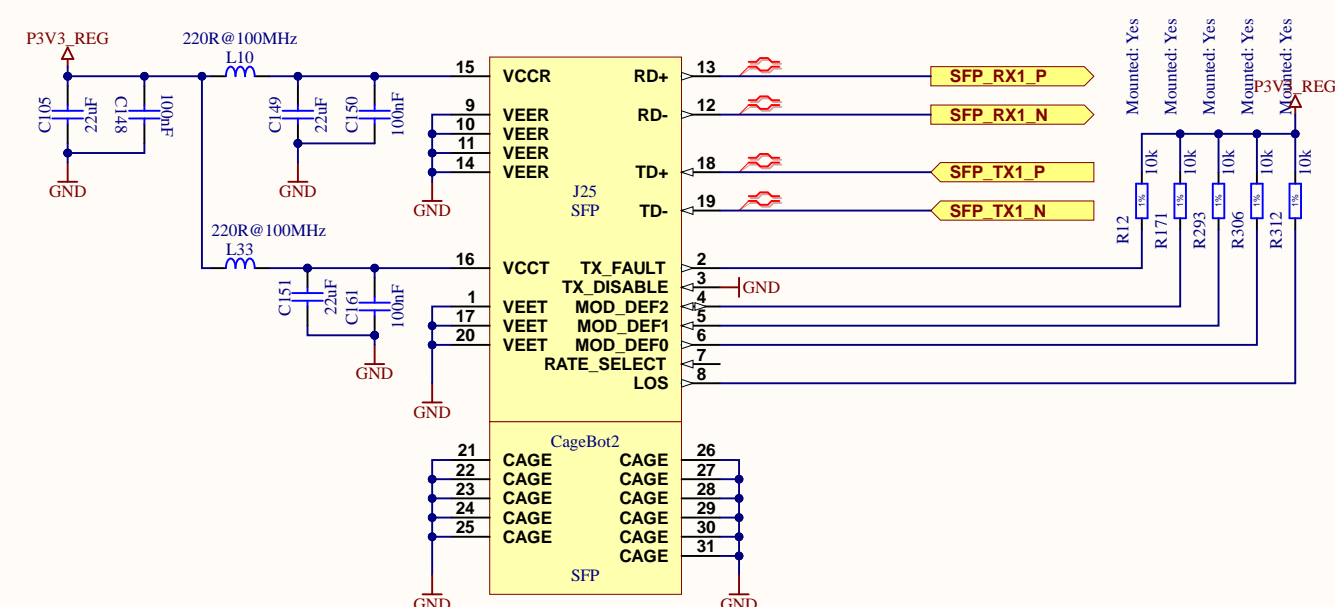
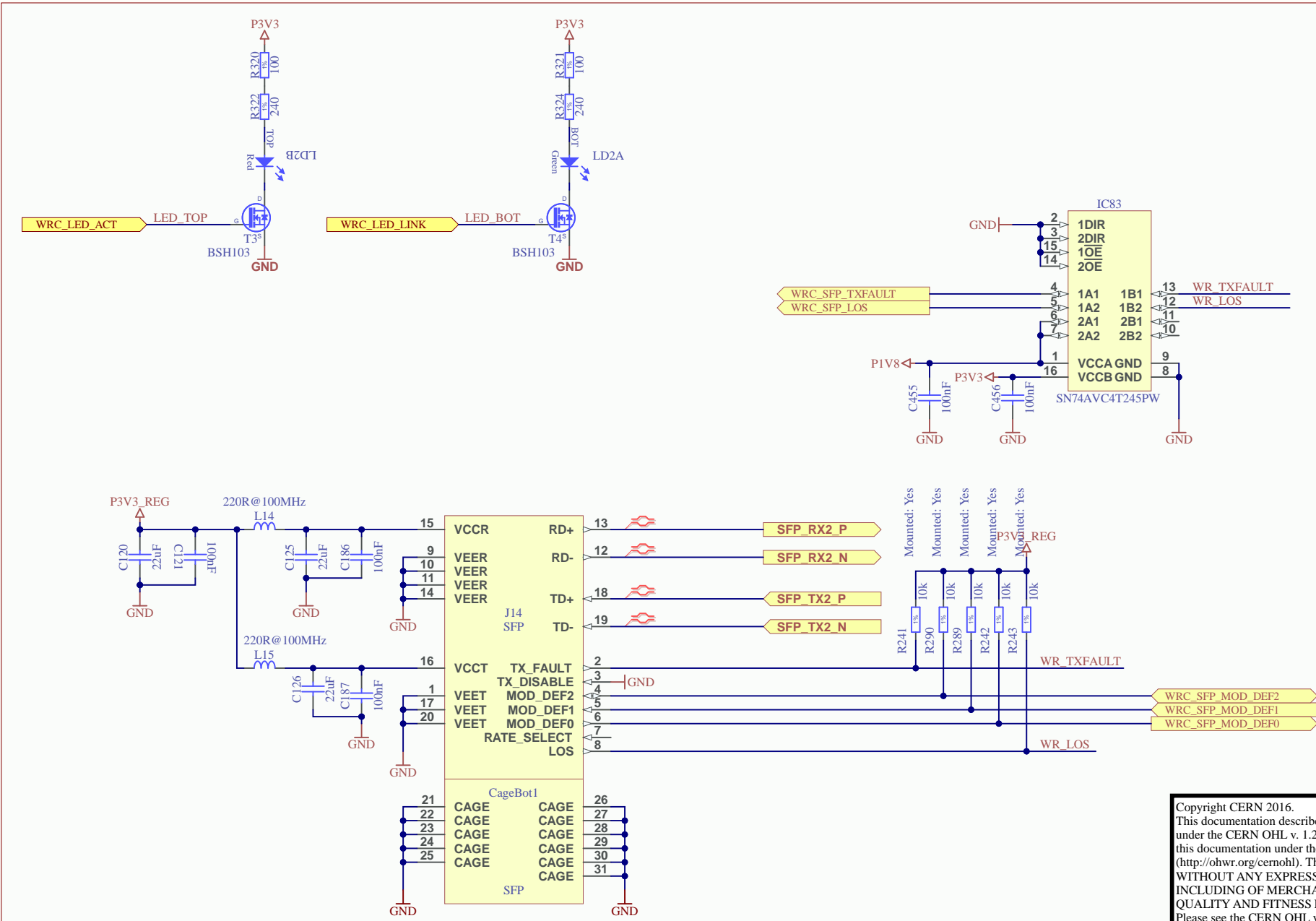
FMC power & fuses

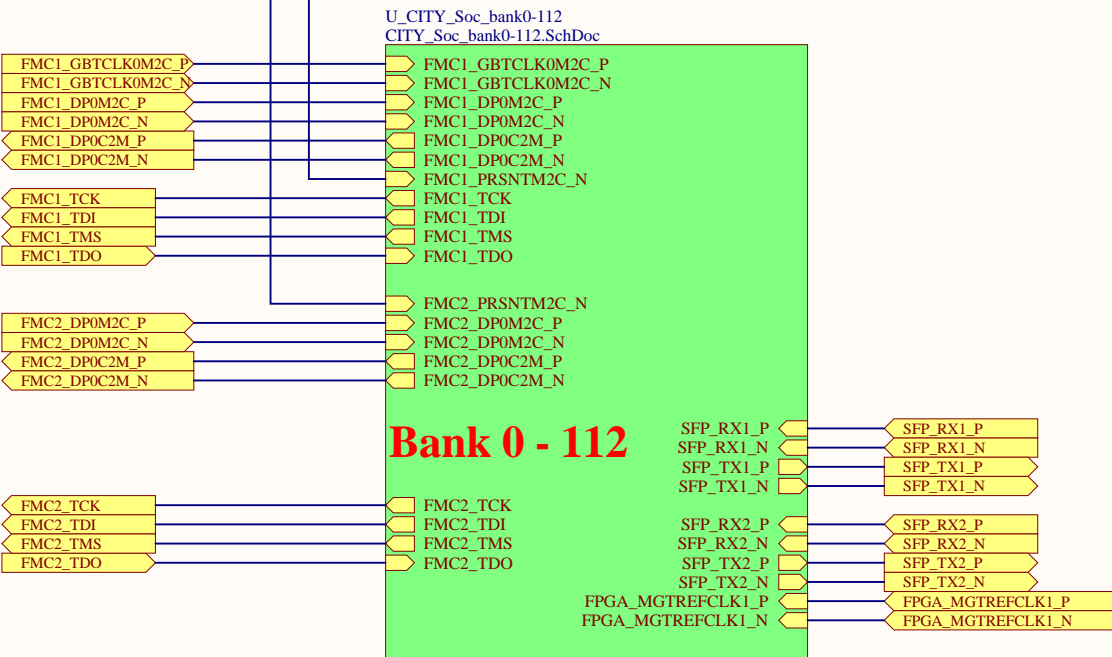
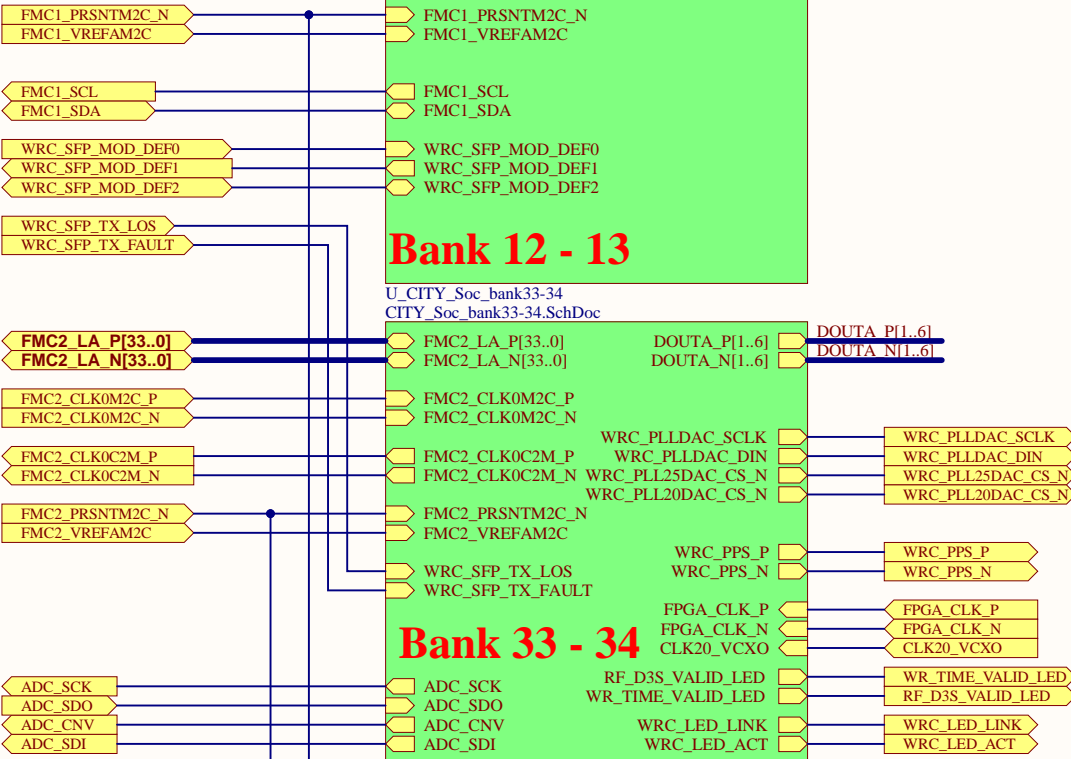
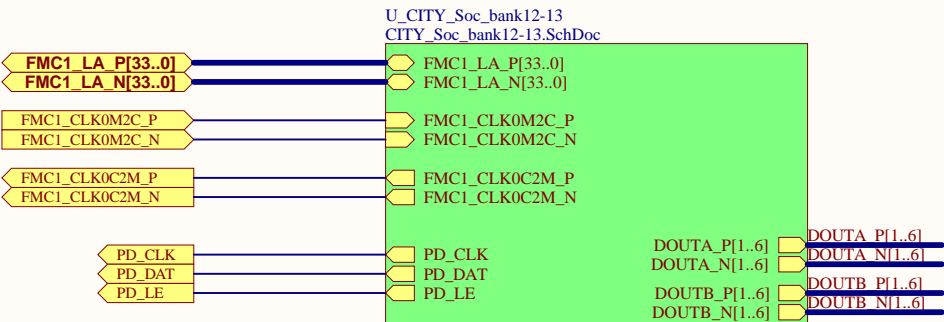


1.8V all (3A max)

*fsw = 2.5 MHz
*layout example at datasheet p.22
*100nF directly across the AVIN and AGND pins

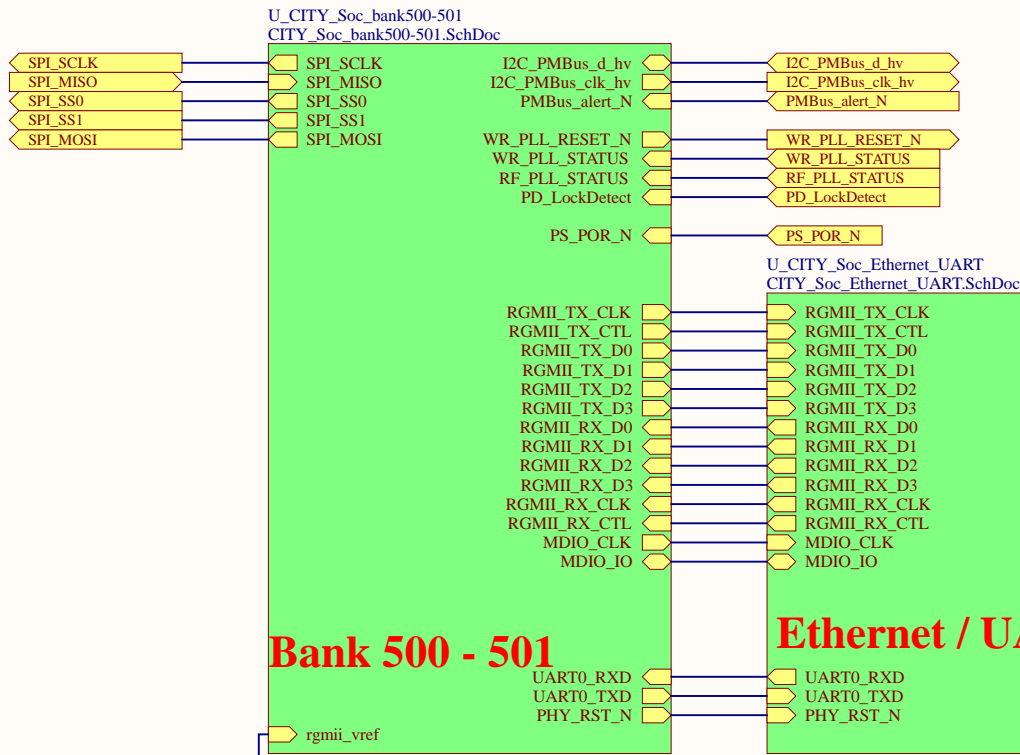






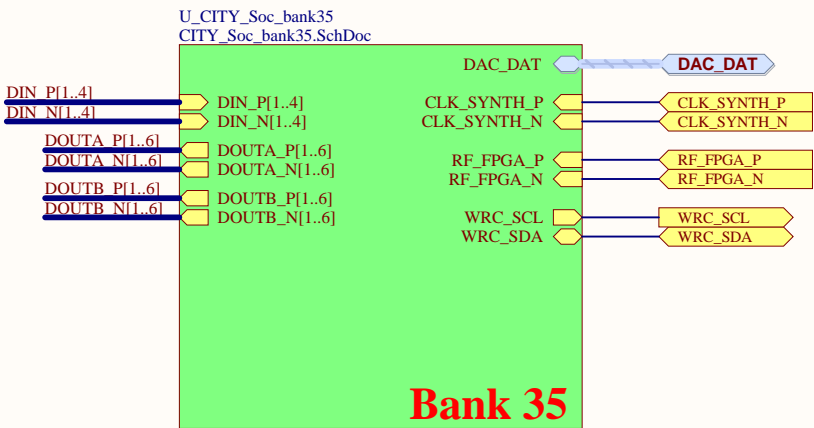
U_CITY_Soc_bank502_DDR
CITY_Soc_bank502_DDR.SchDoc

Bank 502
DDR3L



U_CITY_Soc_power
CITY_Soc_power.SchDoc

SoC power




DOUTB_P[1..6]
DOUTB_N[1..6]

DOUTA_P[1..6]
DOUTA_N[1..6]

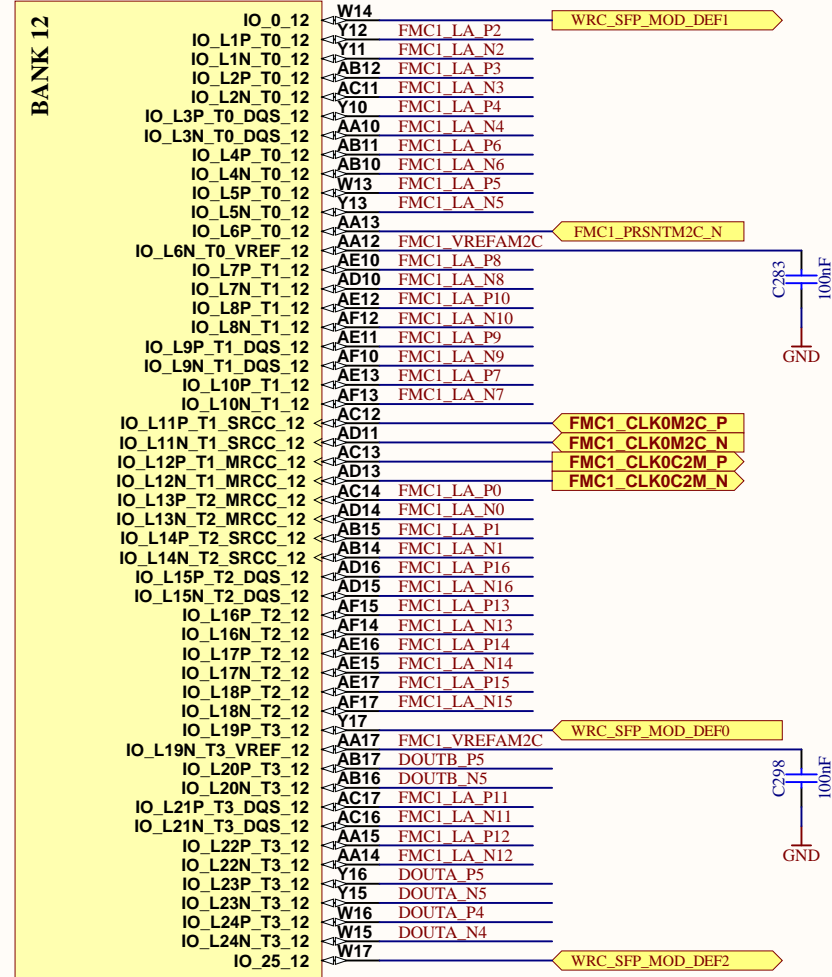
DIN_P[1..4]
DIN_N[1..4]

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 ESRF The European Synchrotron	Doc. Num.:	Ver.:	Sheet:			
		B	18 of 36			
	Project:					
	CITY					
	Sheet:			2	03/2020	broquet
	Zynq SoC			Rev.	Date	Author
	File:			SVN:		
	CITY_Soc_top.SchDoc					

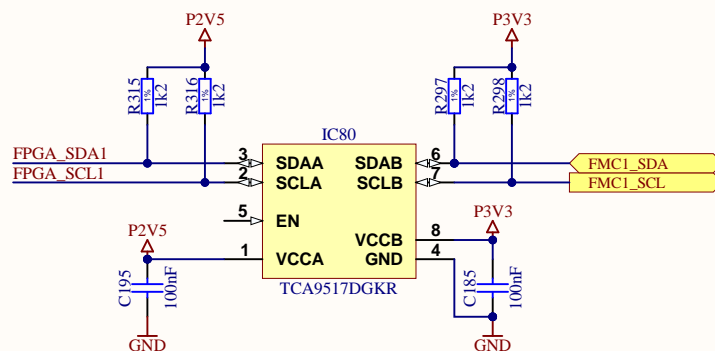
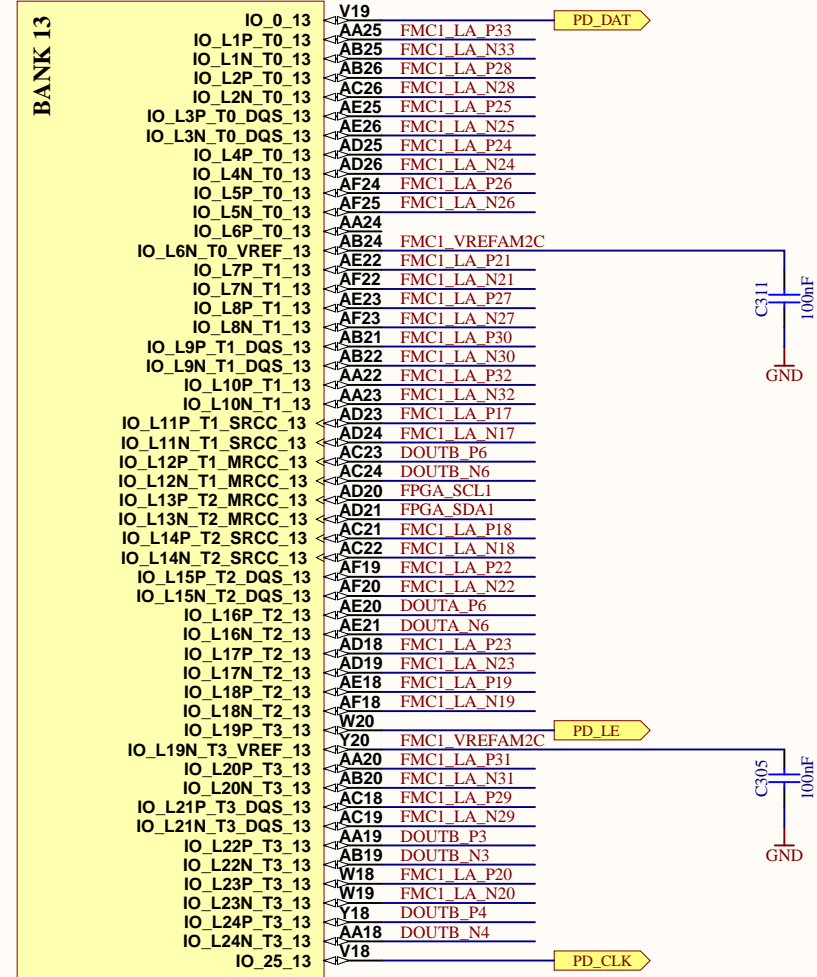
VCCO_12=2.5V

IC37A
XC7Z030-2FFG6761




VCCO_13=2.5V

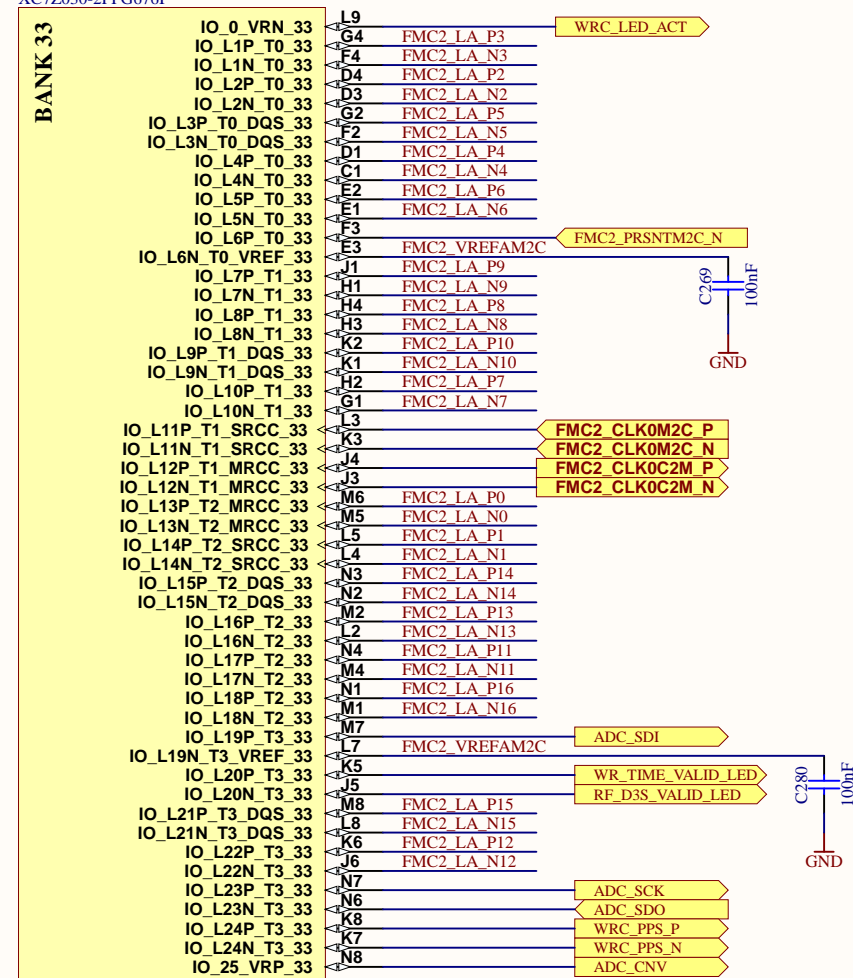
IC37B
XC7Z030-2FFG6761



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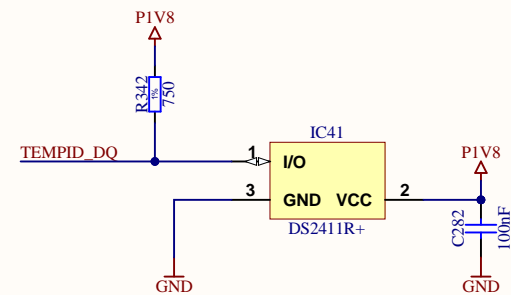
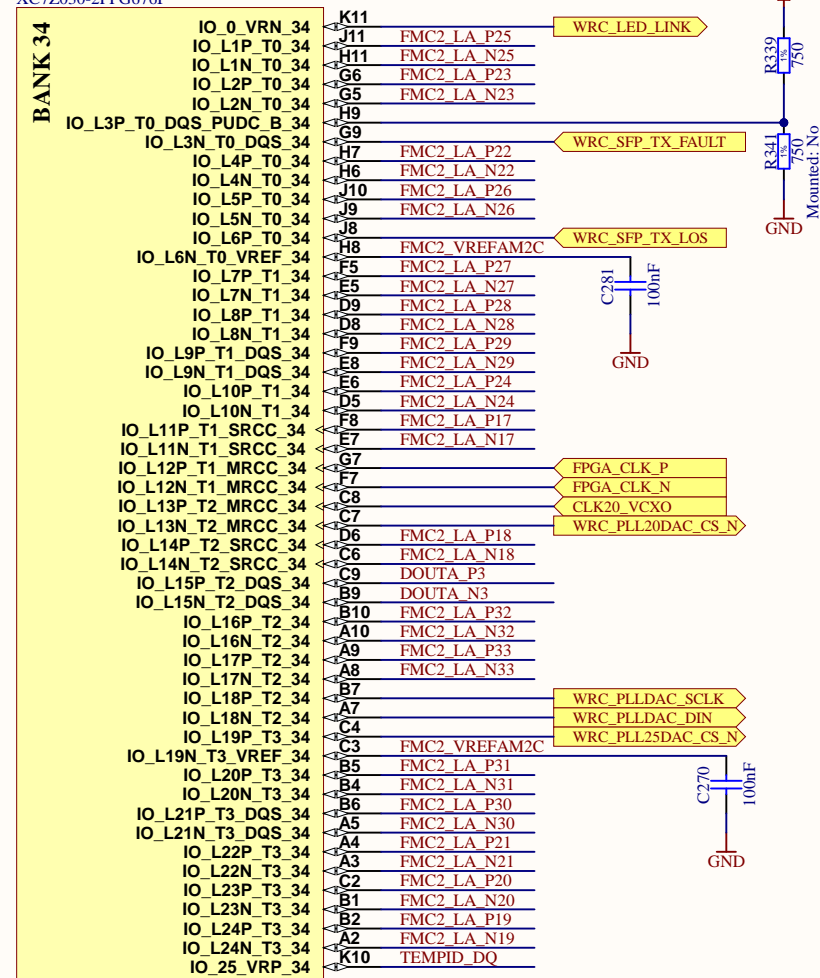
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		B	20 of 36	
	Project:	CITY		
	Sheet:	2	03/2020	broquet
	File:	CITY_Soc_bank12-13.SchDoc		
	Rev.	Date	Author	SVN:

VCCO_33=1.8V

IC37C
XC7Z030-2FFG676I

VCCO_34=1.8V

IC37D
XC7Z030-2FFG676I



Unique 64-bit ID (Maxim 1-Wire)

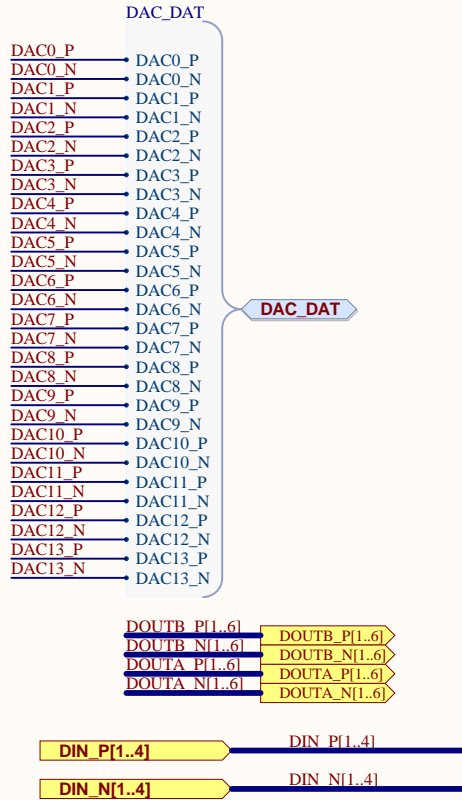
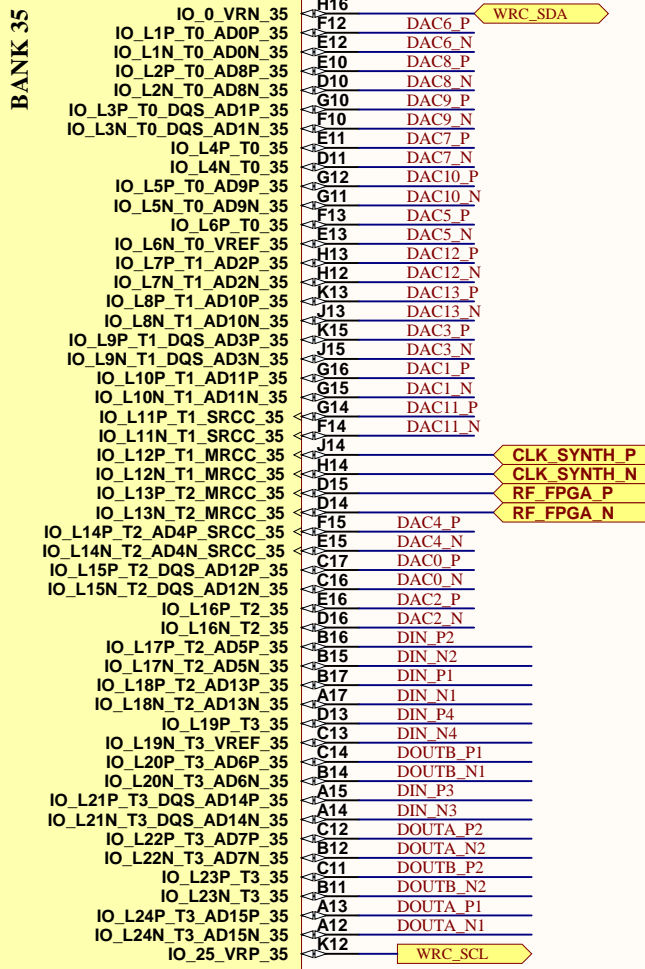


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VCCO_35=1.8V

IC37E

XC7Z030-2FFG676I

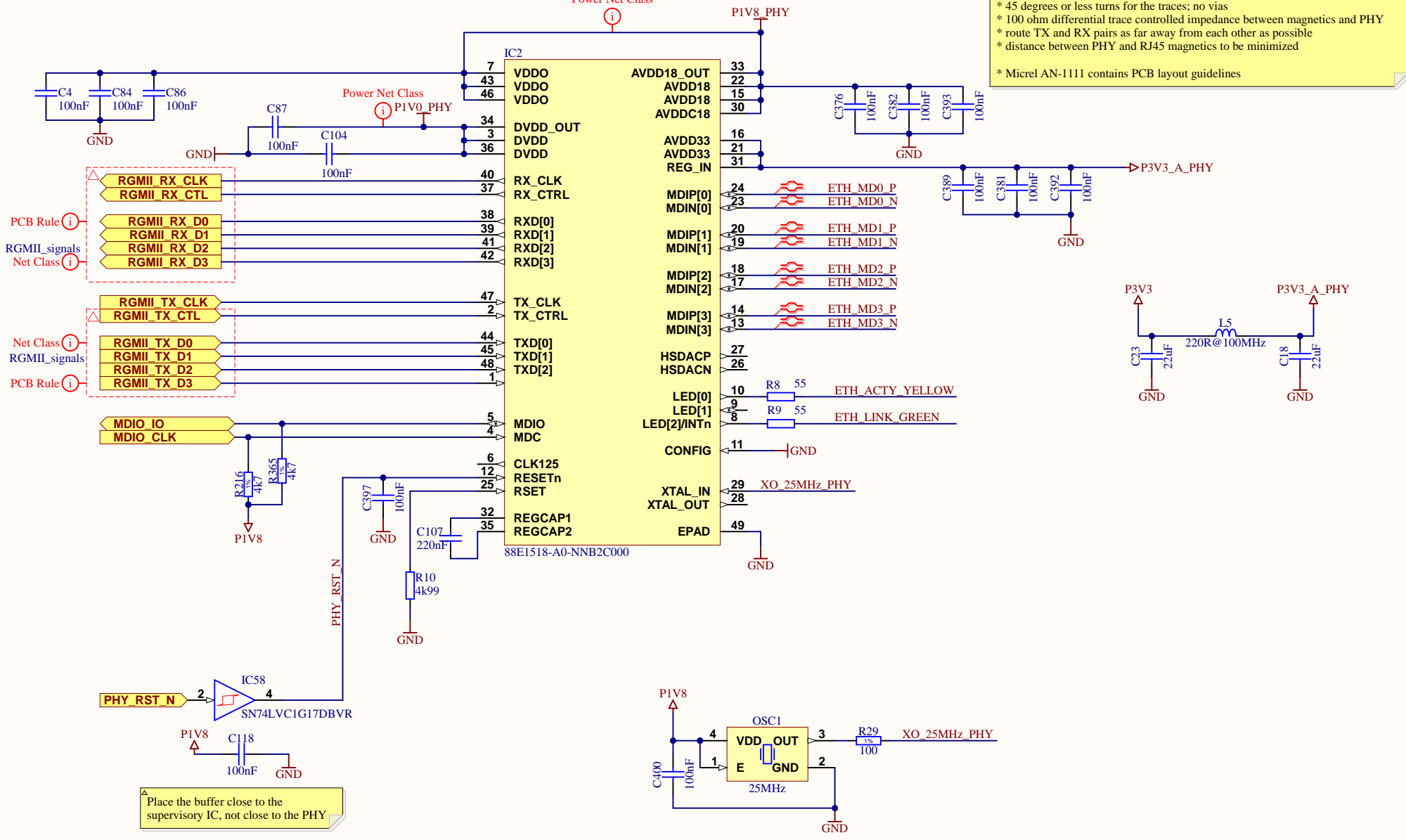


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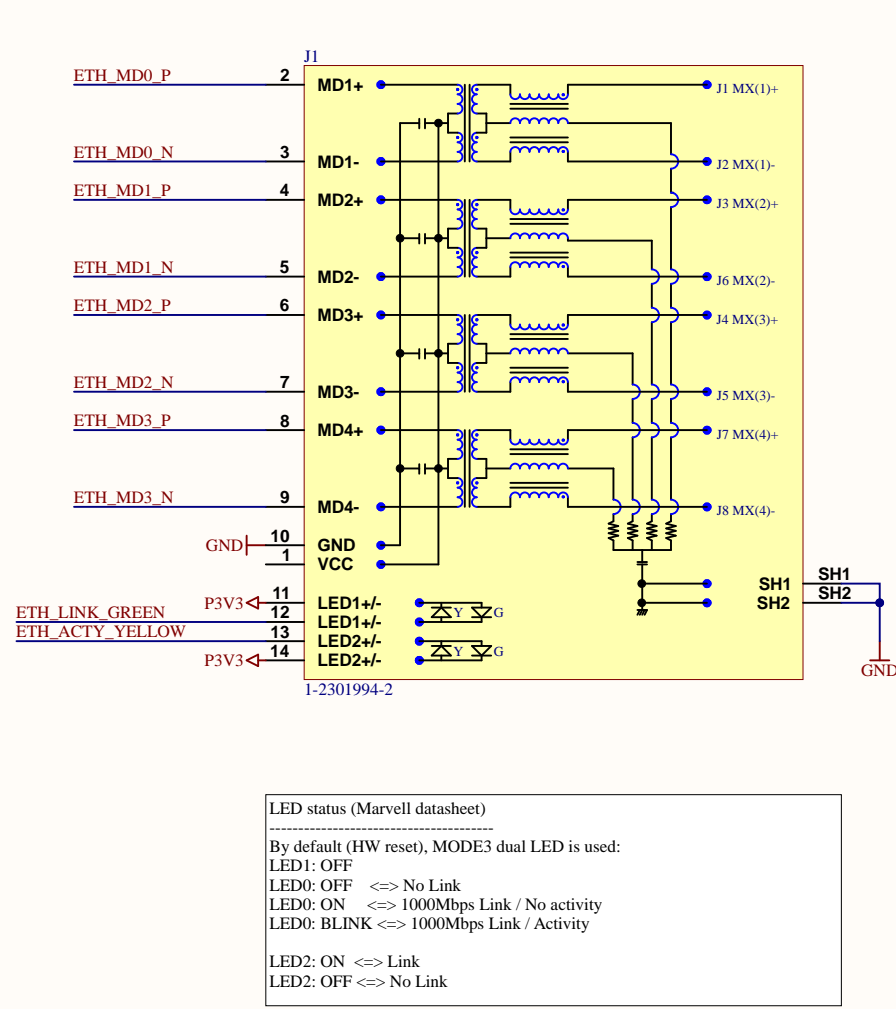


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	B	22 of 36	
Project:	CITY		
Sheet:	2	03/2020	broquet
File:	Zynq SoC - Bank 35	Rev.	Date
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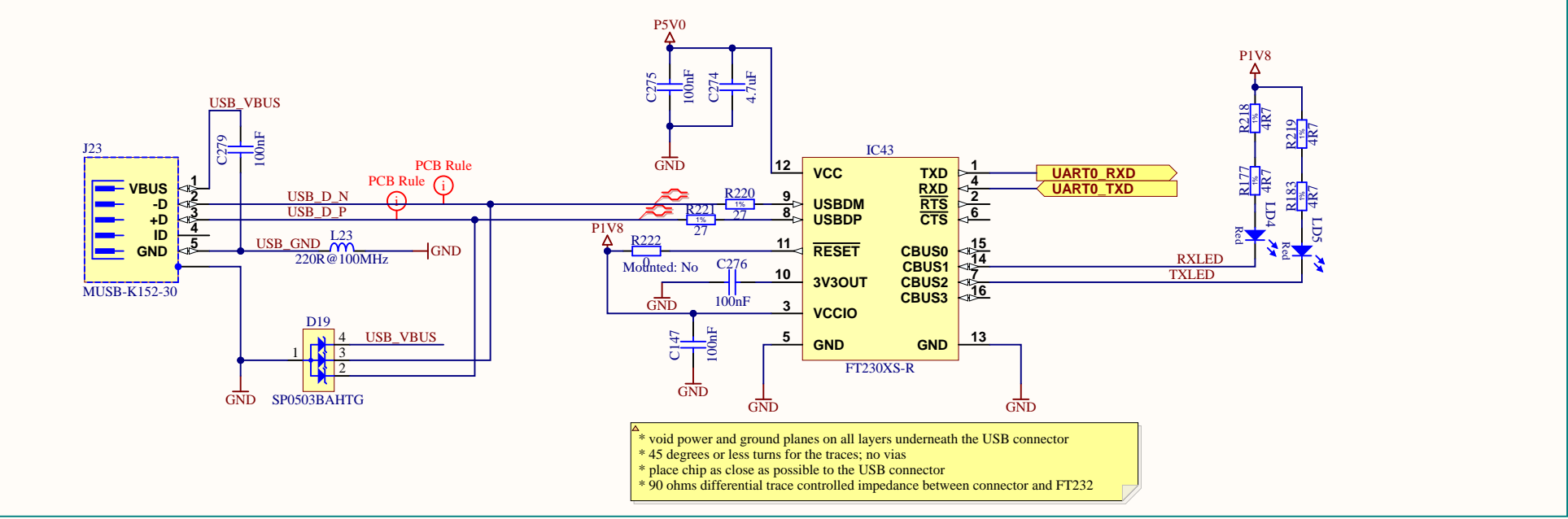
Ethernet Gigabit PHY Transceiver



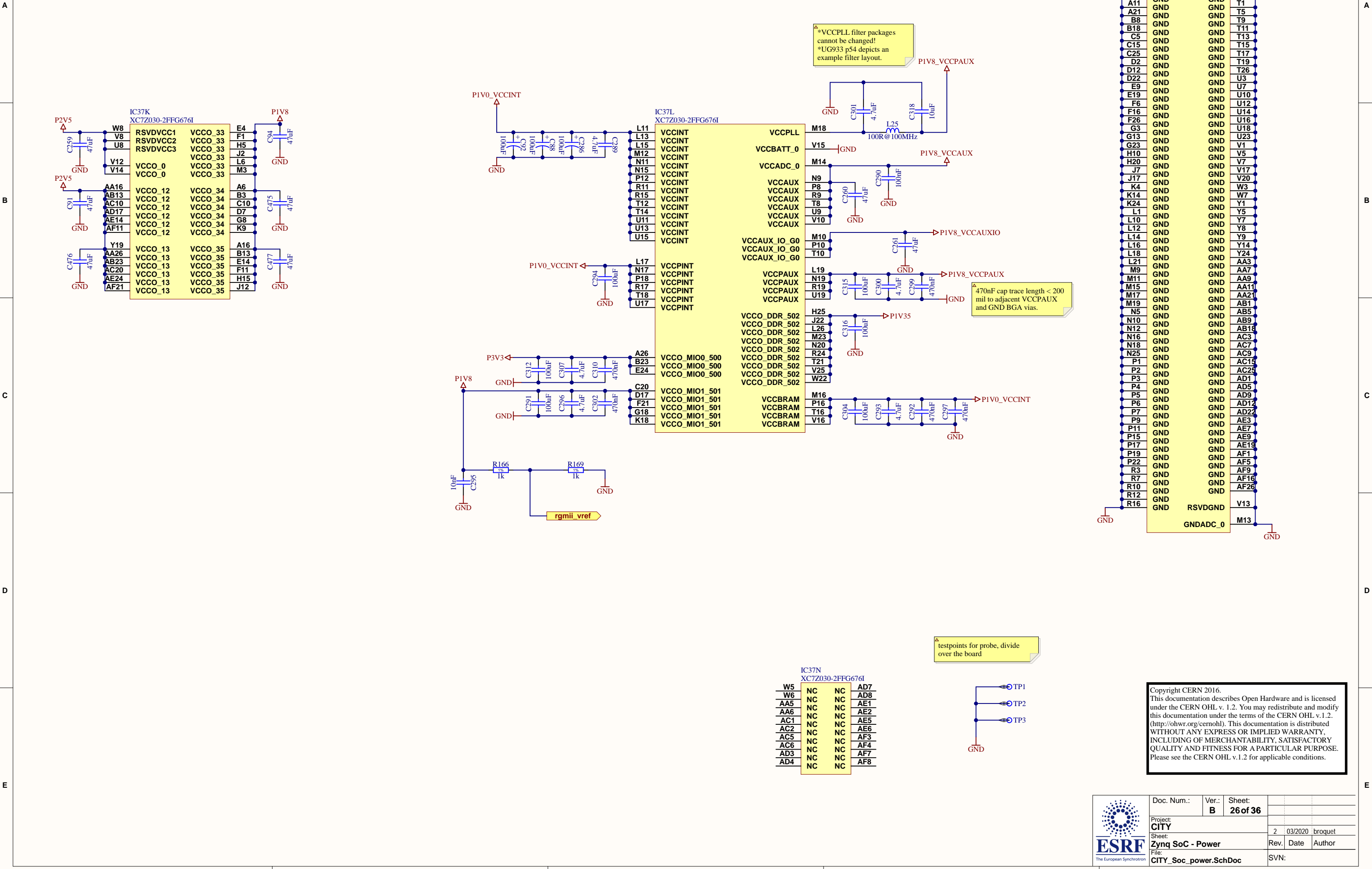
Ethernet RJ45 connector

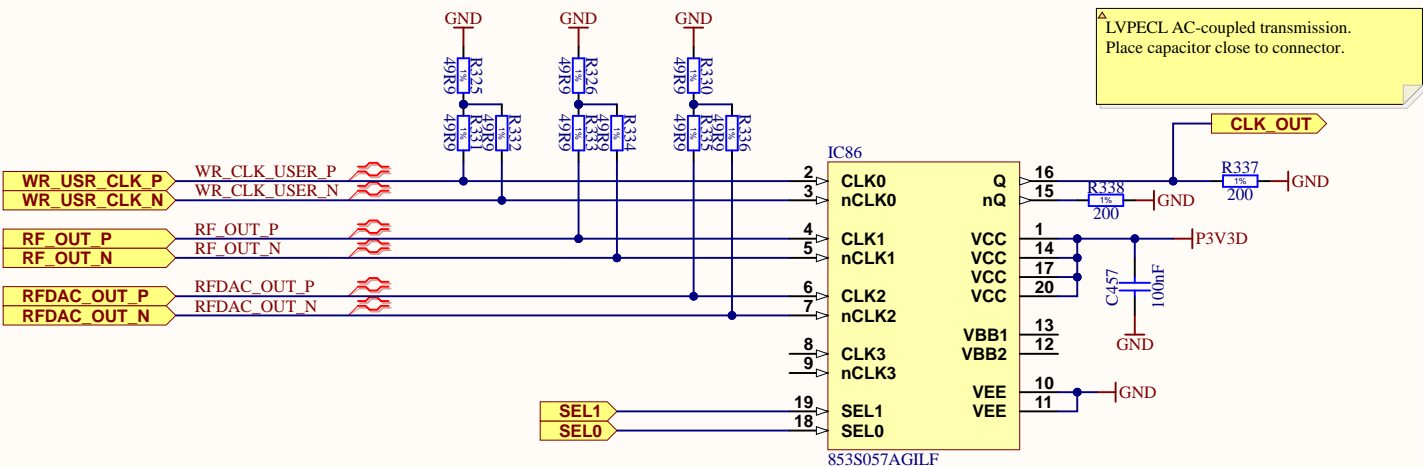


USB UART




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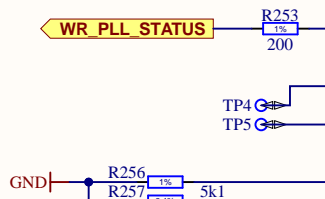


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	Doc. Num.:	Ver.:	Sheet:			
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	Project:	CITY		2	03/2020	broquet
	Sheet:	User Clock		Rev.	Date	Author
File:		CITY_user_clock.SchDoc		SVN:		

REF: VCTXO 25MHz
VCO: 2GHz
Bandwidth: 10kHz
Margin: 50Deg

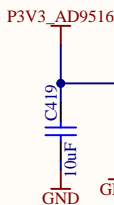
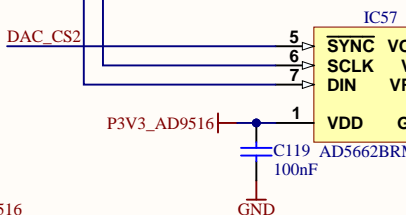
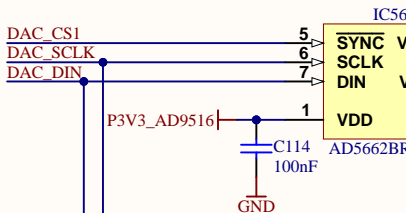
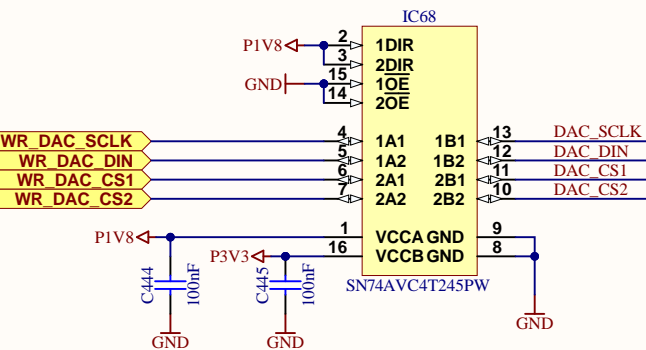
WR PLL STATUS



WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

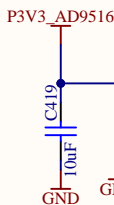
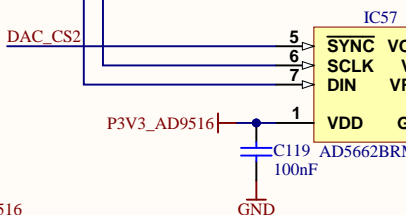
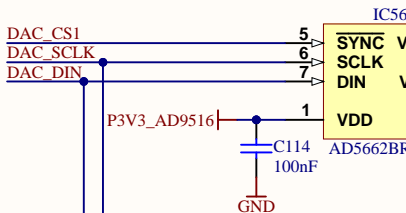
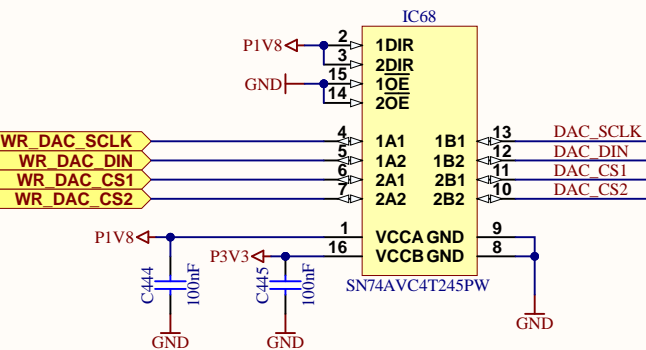
P3V3_AD9516



WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

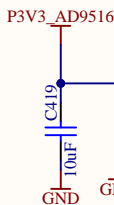
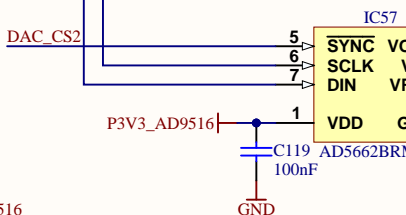
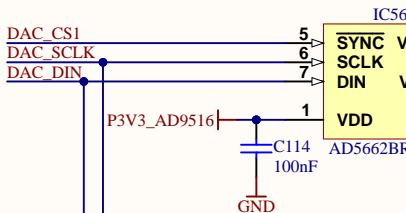
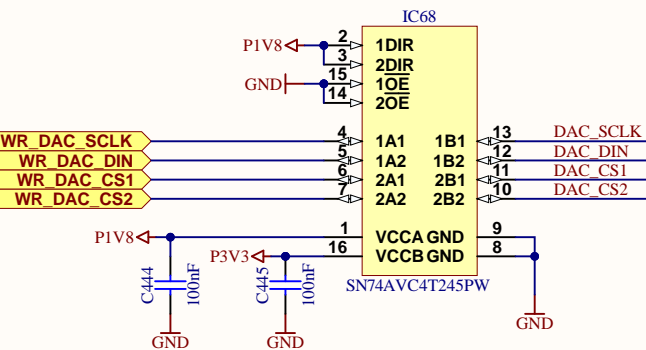
P3V3_AD9516



WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

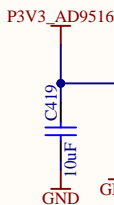
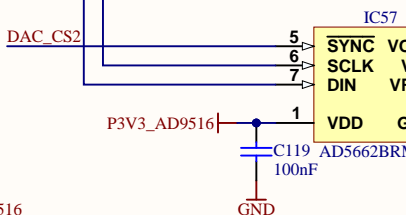
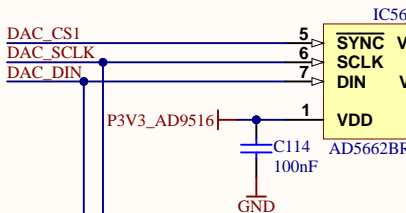
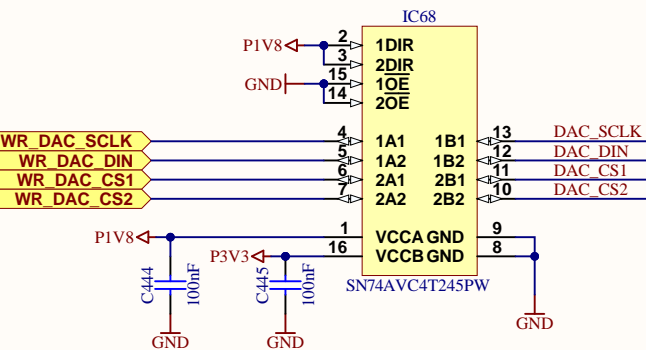
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WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

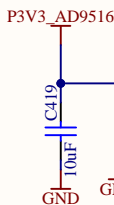
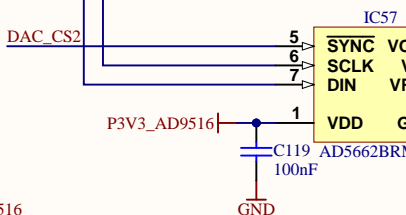
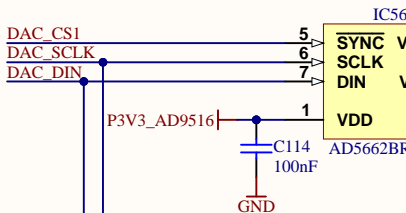
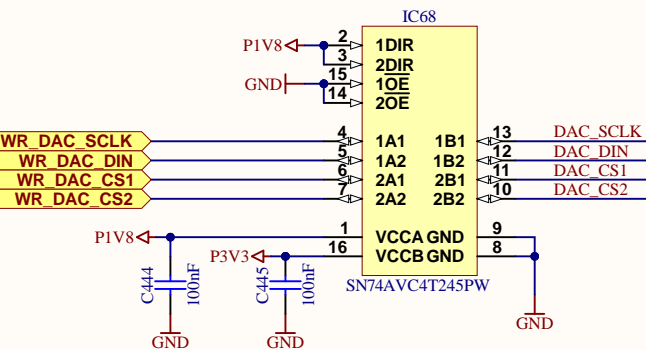
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WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

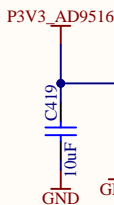
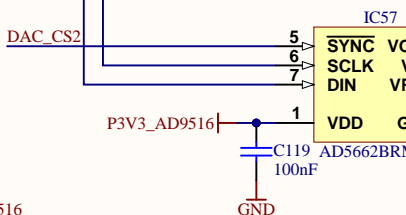
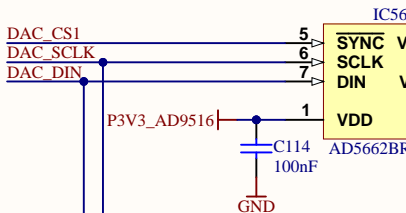
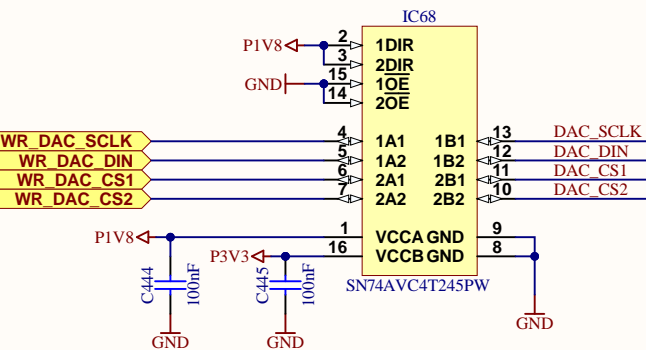
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WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

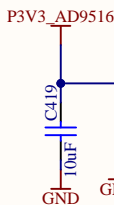
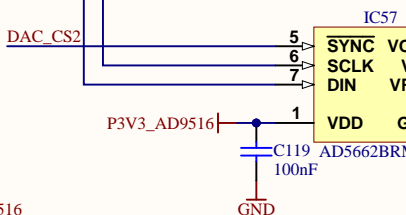
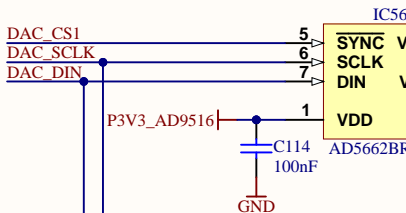
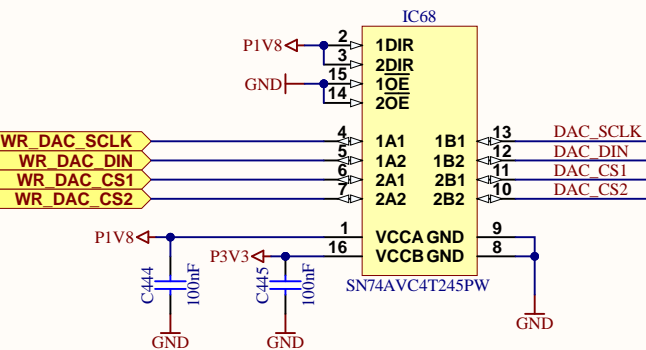
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WR PLL RESET_N

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PLL_SDI
PLL_SDO
WR PLL_CS

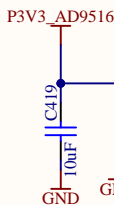
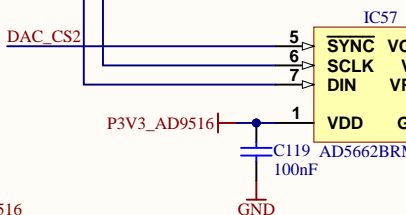
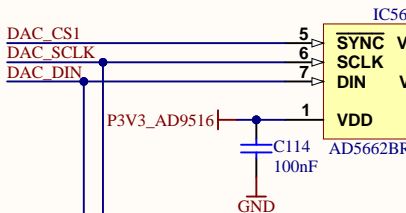
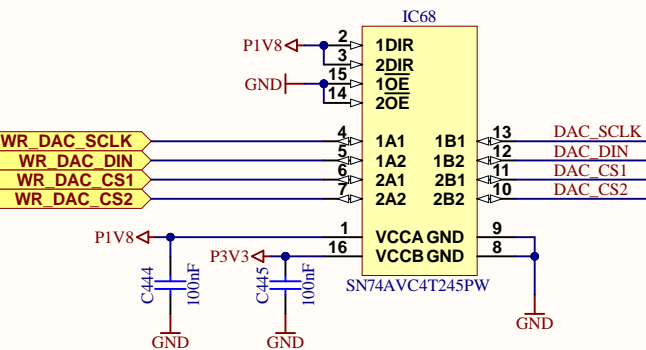
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WR PLL RESET_N

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PLL_SDI
PLL_SDO
WR PLL_CS

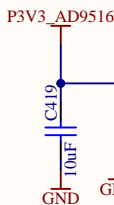
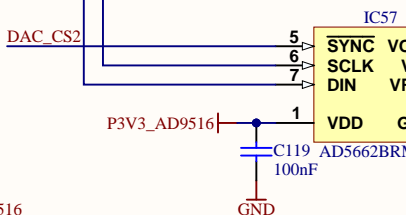
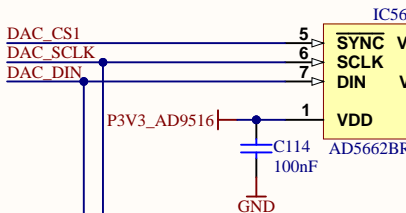
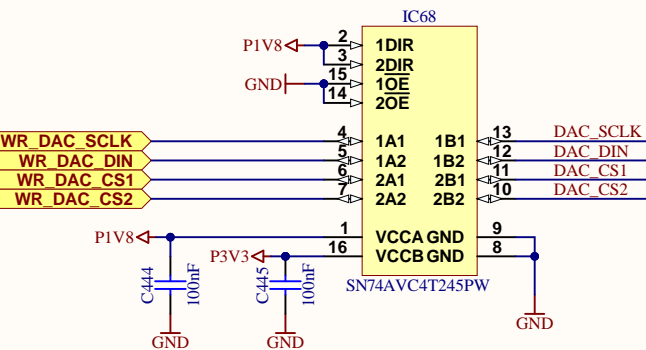
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WR PLL RESET_N

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PLL_SDI
PLL_SDO
WR PLL_CS

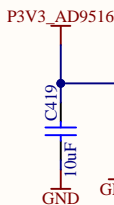
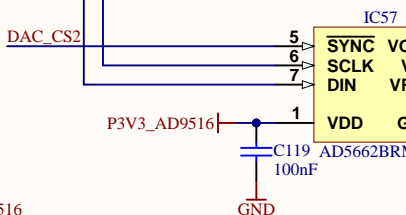
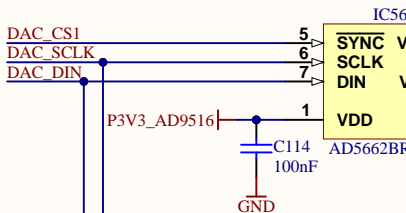
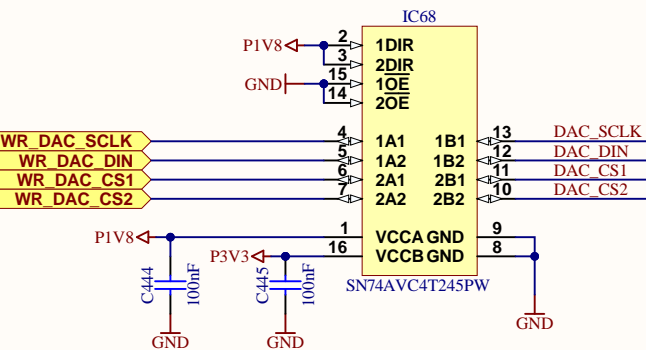
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PLL_SDI
PLL_SDO
WR PLL_CS

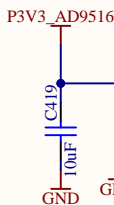
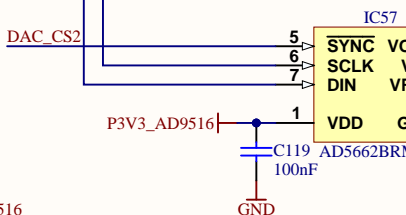
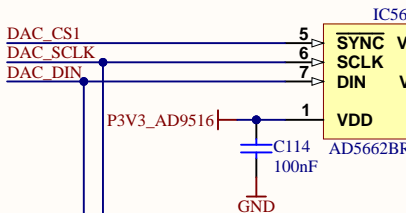
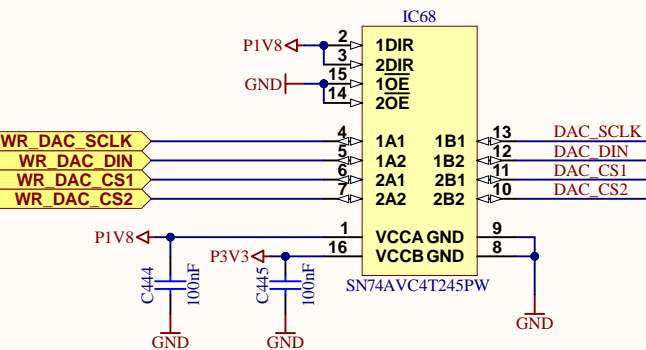
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WR PLL RESET_N

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PLL_SDO
WR PLL_CS

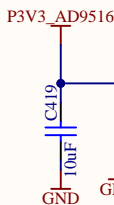
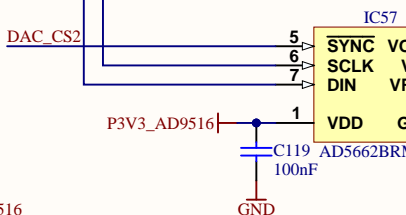
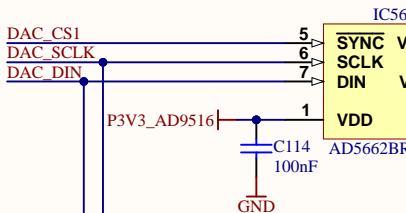
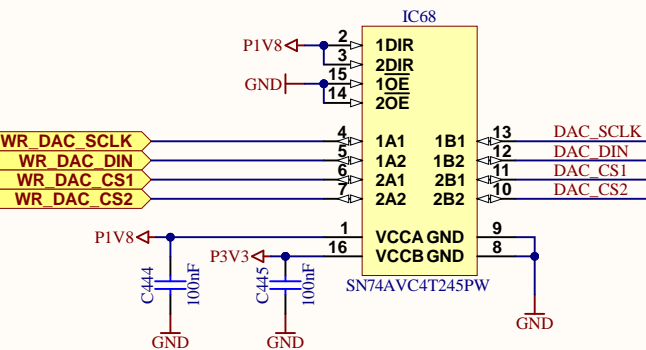
P3V3_AD9516



WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

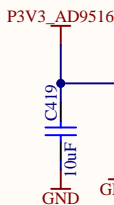
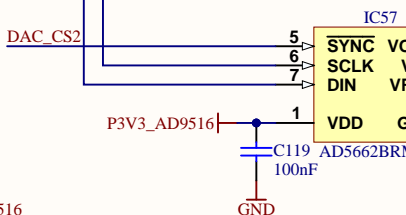
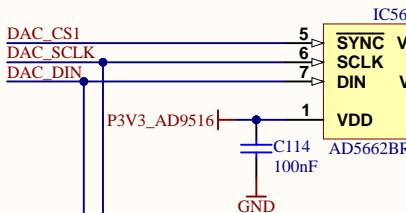
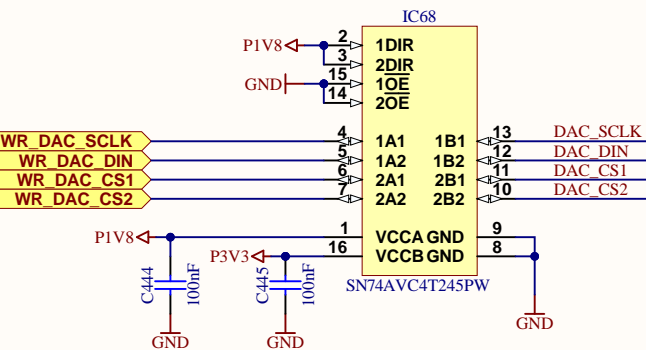
P3V3_AD9516



WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

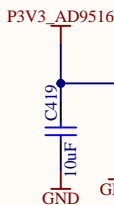
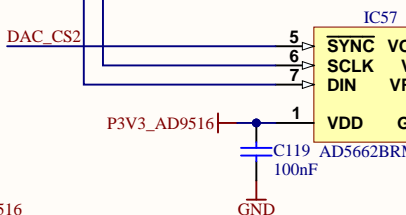
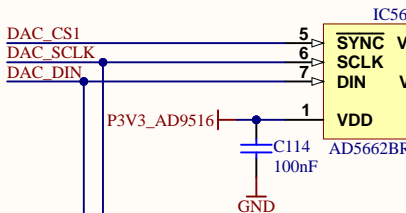
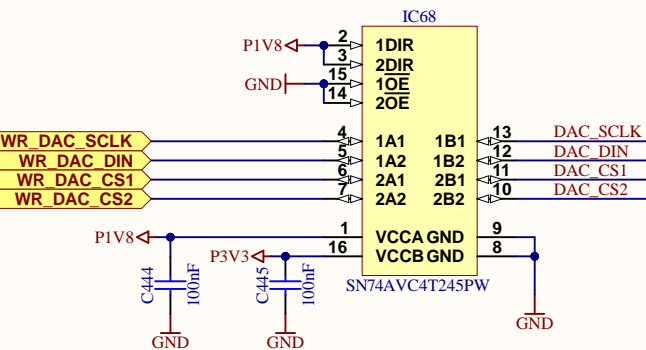
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WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

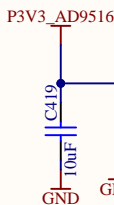
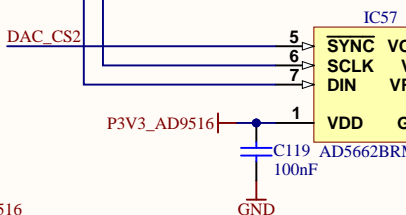
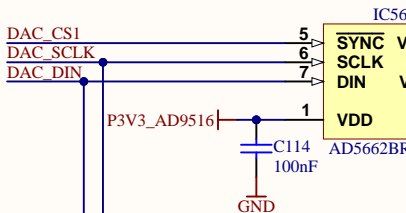
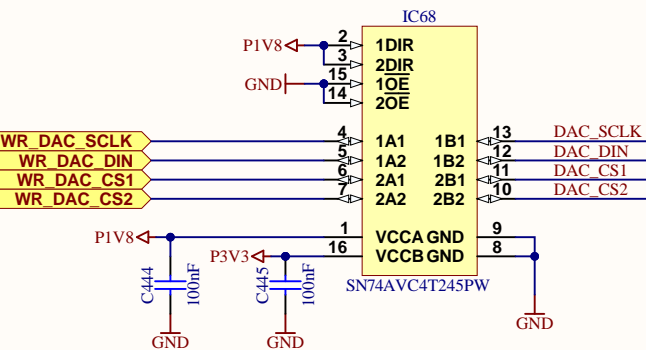
P3V3_AD9516



WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

P3V3_AD9516



WR PLL RESET_N

PLL_SCLK
PLL_SDI
PLL_SDO
WR PLL_CS

P3V3_AD9516

