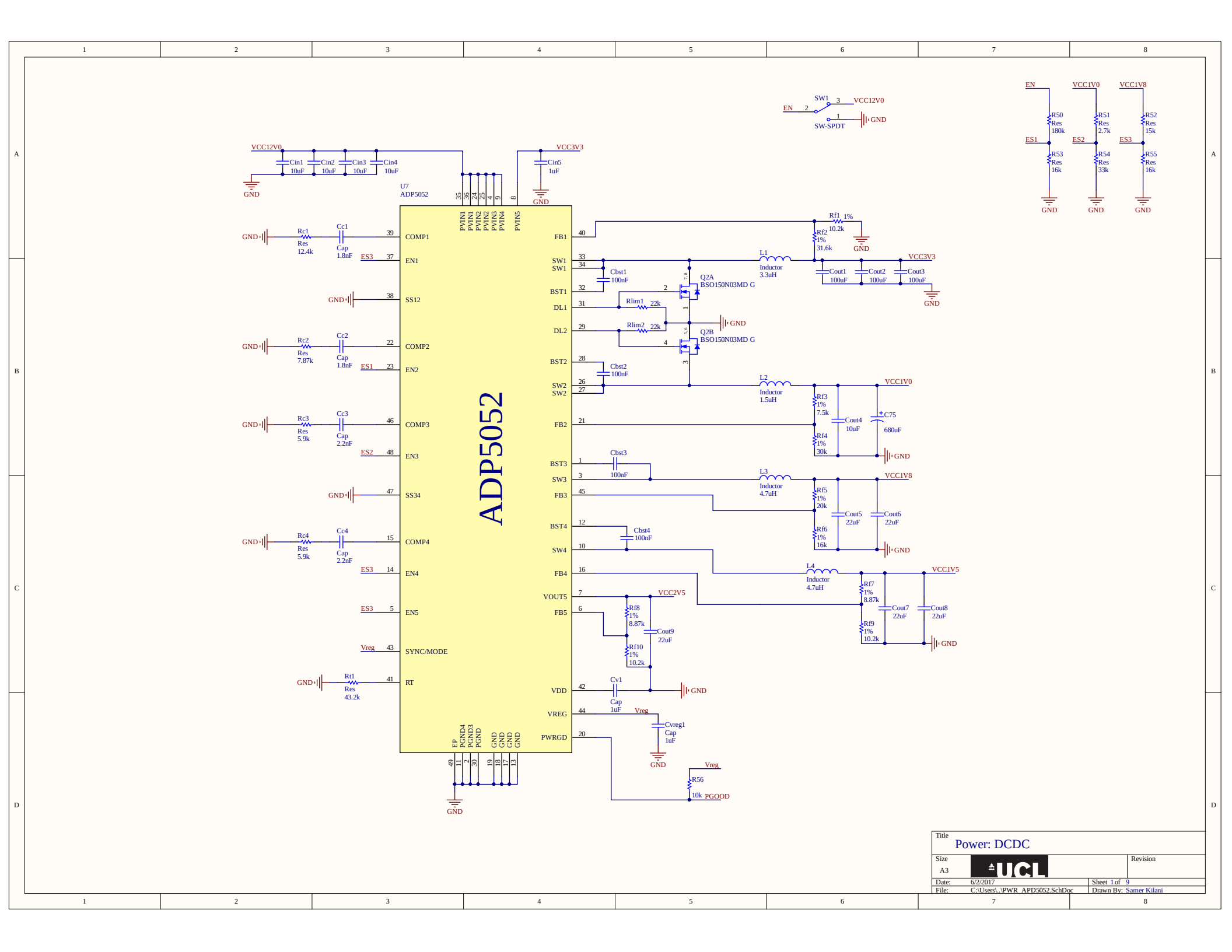
ADP5052
U7
ADP5052
VCC12V0
VCC3V3
VCC1V0
VCC1V8
VCC1V5
VCC2V5
GND
EN
ES1
ES2
ES3
SW1
SW-SPDT
Cin1 10uF
Cin2 10uF
Cin3 10uF
Cin4 10uF
Cin5 1uF
R50 Res 180k
R53 Res 16k
R51 Res 2.7k
R54 Res 33k
R52 Res 15k
R55 Res 16k
PVIN1
PVIN1
PVIN2
PVIN3
PVIN4
PVIN5
COMP1
EN1
SS12
COMP2
EN2
COMP3
EN3
SS34
COMP4
EN4
EN5
SYNC/MODE
RT
FB1
SW1
SW1
BST1
DL1
DL2
BST2
SW2
SW2
FB2
BST3
SW3
FB3
BST4
SW4
FB4
VOUT5
FB5
VDD
VREG
PWRGD
EP
PGND4
PGND3
PGND
GND
GND
GND
GND
Rc1 Res 12.4k
Cc1 Cap 1.8nF
Rc2 Res 7.87k
Cc2 Cap 1.8nF
Rc3 Res 5.9k
Cc3 Cap 2.2nF
Rc4 Res 5.9k
Cc4 Cap 2.2nF
Rt1 Res 43.2k
Vreg
Rf1 1%
Rf2 1% 31.6k
10.2k
L1 Inductor 3.3uH
Cout1 100uF
Cout2 100uF
Cout3 100uF
Cbst1 100nF
Q2A BSO150N03MD G
Q2B BSO150N03MD G
Rlim1 22k
Rlim2 22k
Cbst2 100nF
L2 Inductor 1.5uH
Rf3 1% 7.5k
Rf4 1% 30k
Cout4 10uF
C75 680uF
Cbst3 100nF
L3 Inductor 4.7uH
Rf5 1% 20k
Rf6 1% 16k
Cout5 22uF
Cout6 22uF
Cbst4 100nF
L4 Inductor 4.7uH
Rf7 1% 8.87k
Rf8 1% 8.87k
Rf9 1% 10.2k
Rf10 1% 10.2k
Cout7 22uF
Cout8 22uF
Cout9 22uF
Cv1 Cap 1uF
Cvreg1 Cap 1uF
R56 10k
PGOOD
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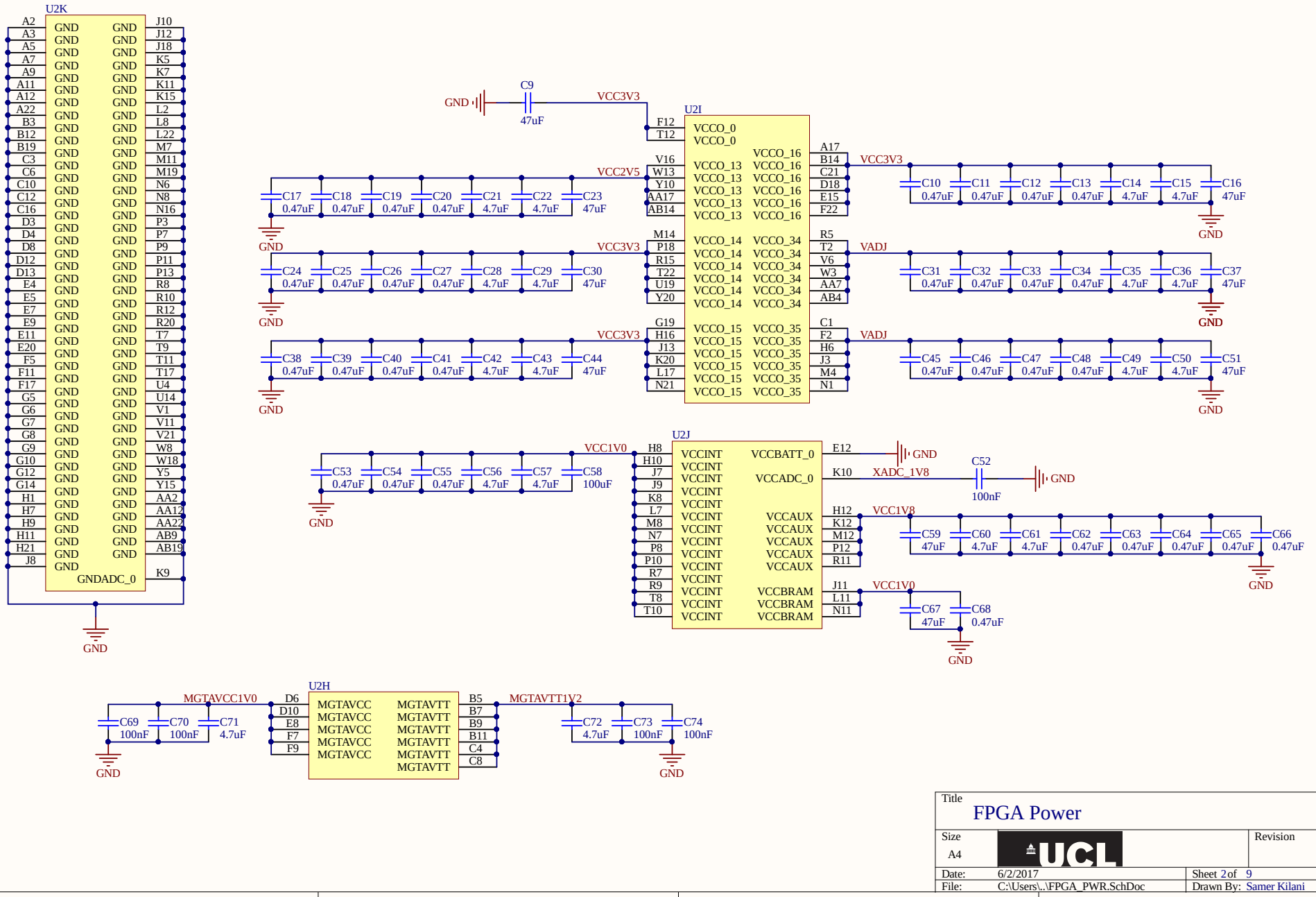
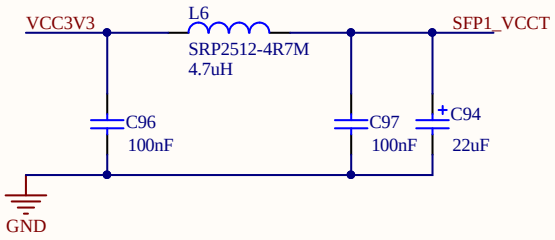
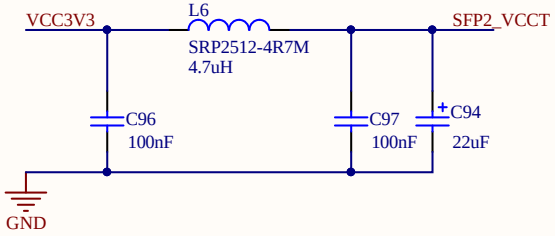
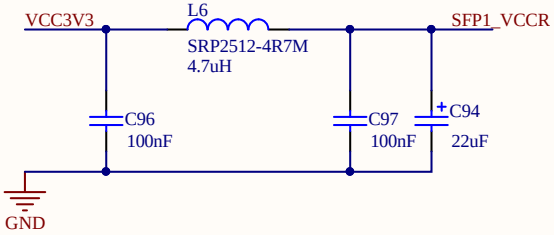
Power: DCDC
Size
A3
Revision
Date: 6/2/2017
Sheet 1 of 9
File: C:\Users\..\PWR_APD5052.SchDoc
Drawn By: Samer Kilani

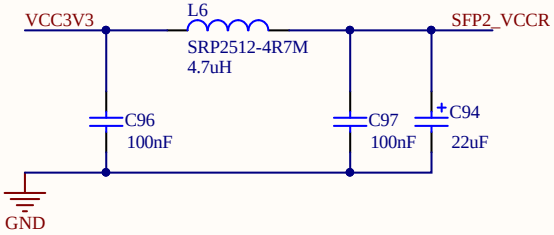


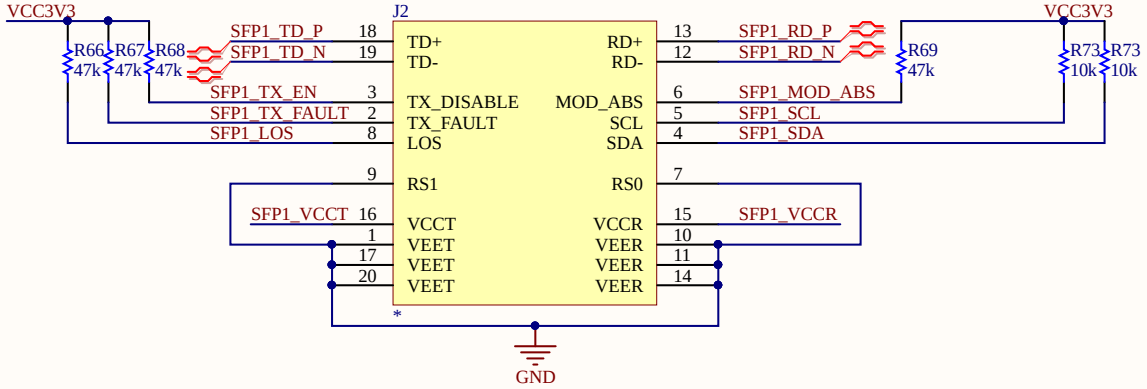
Title	FPGA Power
Size	A4
Revision	
Date:	6/2/2017
Sheet	2 of 9
File:	C:\Users\..\FPGA_PWR.SchDoc
Drawn By:	Samer Kilani

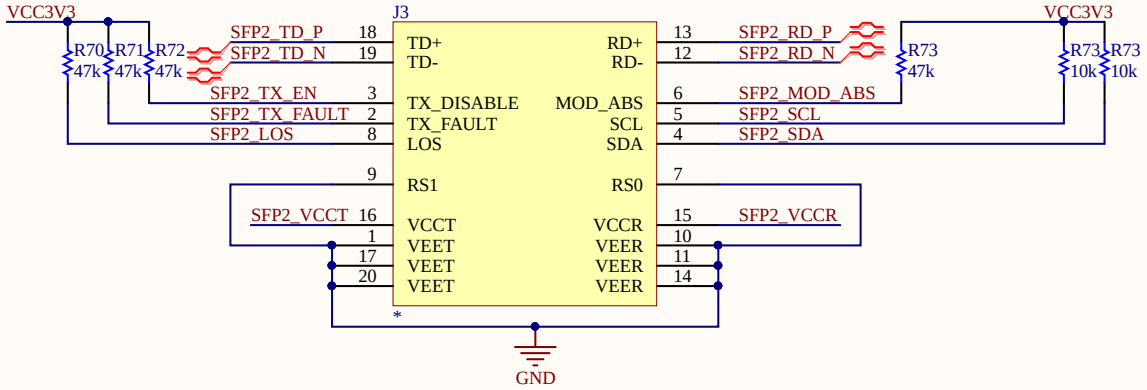












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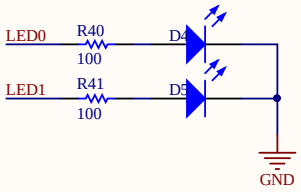
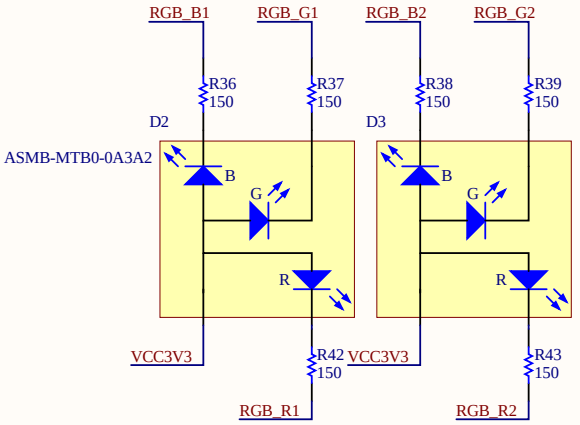
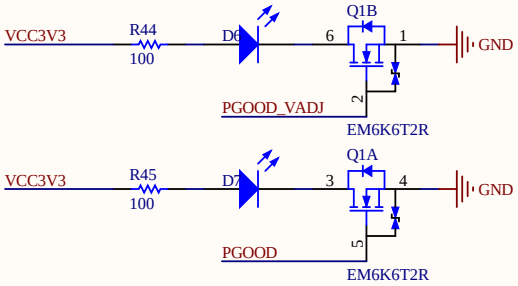
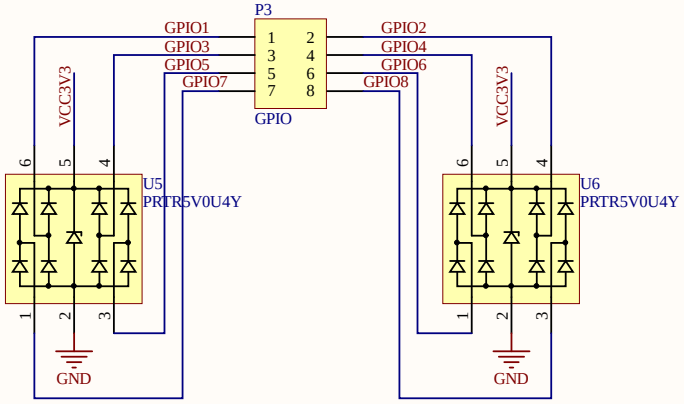
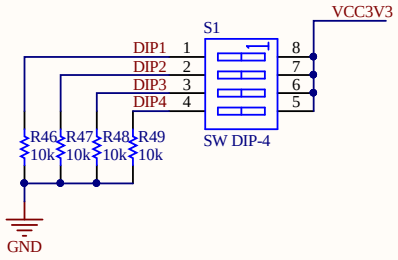
Size: Orcad A	UCL	Revision
Date: 6/2/2017		Sheet 3 of 9
File: C:\Users\..\SFP.SchDoc		Drawn By: Samer Kilani











Title	IO		
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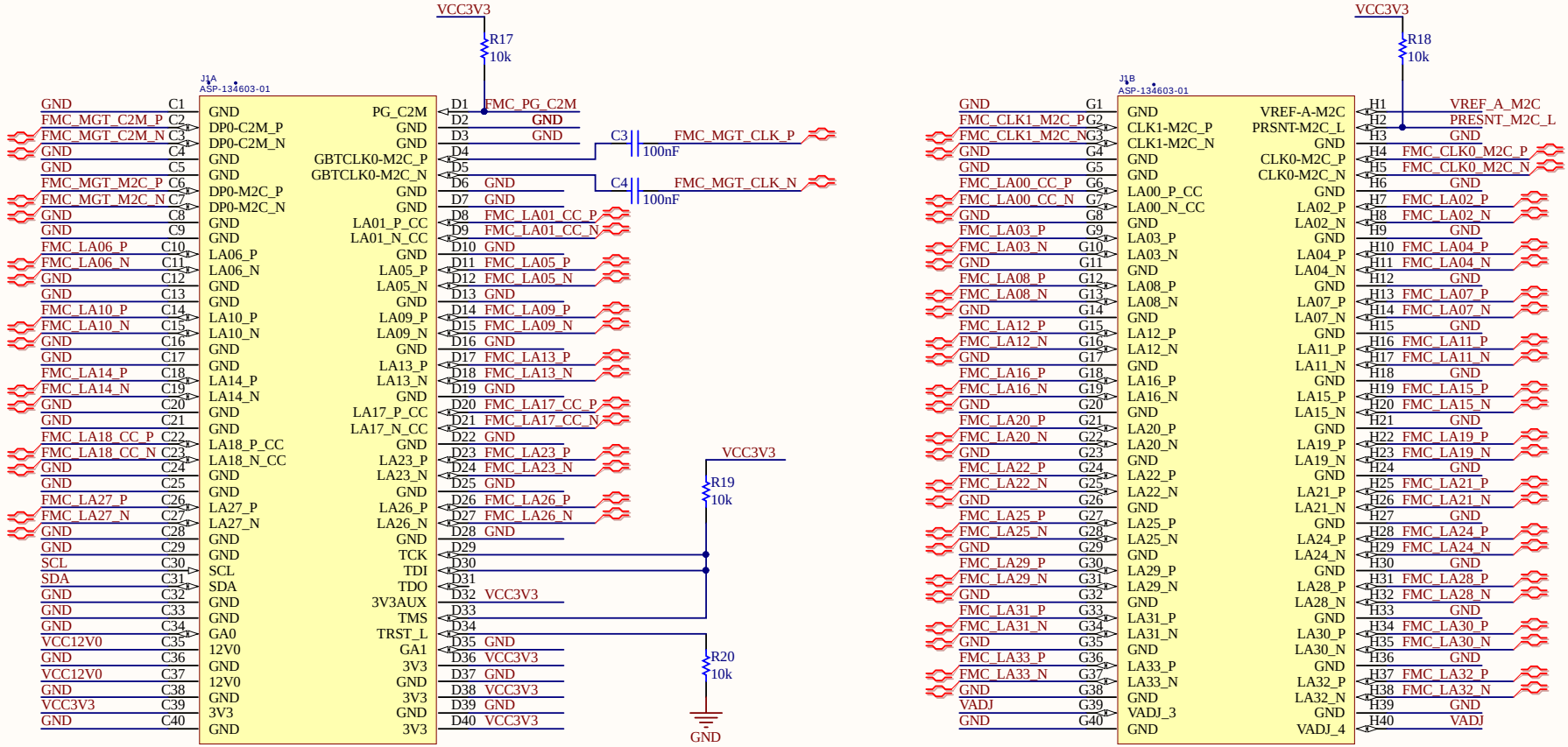
File:	C:\Users\..\IO.SchDoc	Drawn By: Samer Kilani	



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Size	A4	UCL	Revision
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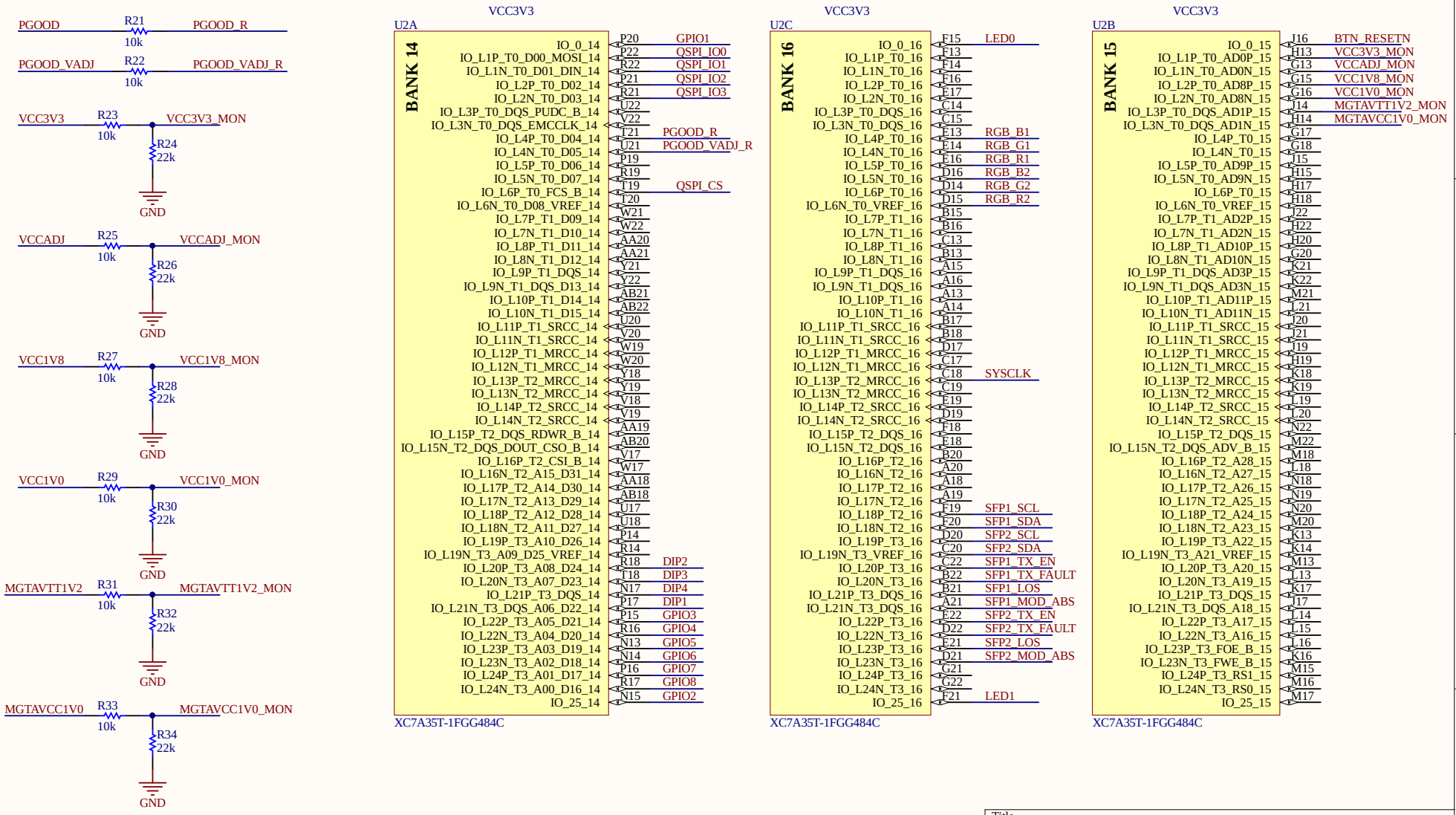
File:	C:\Users\..\FMC.SchDoc	Drawn By: Samer Kilani	


PGOOD
R21
10k
PGOOD_R
PGOOD_VADJ
R22
10k
PGOOD_VADJ_R
VCC3V3
R23
10k
VCC3V3_MON
R24
22k
GND
VCCADJ
R25
10k
VCCADJ_MON
R26
22k
GND
VCC1V8
R27
10k
VCC1V8_MON
R28
22k
GND
VCC1V0
R29
10k
VCC1V0_MON
R30
22k
GND
MGTAVTT1V2
R31
10k
MGTAVTT1V2_MON
R32
22k
GND
MGTAVCC1V0
R33
10k
MGTAVCC1V0_MON
R34
22k
GND
VCC3V3
U2A
BANK 14
IO_0_14 P20 GPIO1
IO_L1P_T0_D00_MOSI_14 P22 QSPI_IO0
IO_L1N_T0_D01_DIN_14 R22 QSPI_IO1
IO_L2P_T0_D02_14 P21 QSPI_IO2
IO_L2N_T0_D03_14 R21 QSPI_IO3
IO_L3P_T0_DQS_PUDC_B_14 U22
IO_L3N_T0_DQS_EMCCLK_14 V22
IO_L4P_T0_D04_14 T21 PGOOD_R
IO_L4N_T0_D05_14 U21 PGOOD_VADJ_R
IO_L5P_T0_D06_14 P19
IO_L5N_T0_D07_14 R19
IO_L6P_T0_FCS_B_14 T19 QSPI_CS
IO_L6N_T0_D08_VREF_14 T20
IO_L7P_T1_D09_14 W21
IO_L7N_T1_D10_14 W22
IO_L8P_T1_D11_14 AA20
IO_L8N_T1_D12_14 AA21
IO_L9P_T1_DQS_14 Y21
IO_L9N_T1_DQS_D13_14 Y22
IO_L10P_T1_D14_14 AB21
IO_L10N_T1_D15_14 AB22
IO_L11P_T1_SRCC_14 U20
IO_L11N_T1_SRCC_14 V20
IO_L12P_T1_MRCC_14 W19
IO_L12N_T1_MRCC_14 W20
IO_L13P_T2_MRCC_14 Y18
IO_L13N_T2_MRCC_14 Y19
IO_L14P_T2_SRCC_14 V18
IO_L14N_T2_SRCC_14 V19
IO_L15P_T2_DQS_RDWR_B_14 AA19
IO_L15N_T2_DQS_DOUT_CSO_B_14 AB20
IO_L16P_T2_CSI_B_14 V17
IO_L16N_T2_A15_D31_14 W17
IO_L17P_T2_A14_D30_14 AA18
IO_L17N_T2_A13_D29_14 AB18
IO_L18P_T2_A12_D28_14 U17
IO_L18N_T2_A11_D27_14 U18
IO_L19P_T3_A10_D26_14 P14
IO_L19N_T3_A09_D25_VREF_14 R14
IO_L20P_T3_A08_D24_14 R18 DIP2
IO_L20N_T3_A07_D23_14 T18 DIP3
IO_L21P_T3_DQS_14 N17 DIP4
IO_L21N_T3_DQS_A06_D22_14 P17 DIP1
IO_L22P_T3_A05_D21_14 P15 GPIO3
IO_L22N_T3_A04_D20_14 R16 GPIO4
IO_L23P_T3_A03_D19_14 N13 GPIO5
IO_L23N_T3_A02_D18_14 N14 GPIO6
IO_L24P_T3_A01_D17_14 P16 GPIO7
IO_L24N_T3_A00_D16_14 R17 GPIO8
IO_25_14 N15 GPIO2
XC7A35T-1FGG484C
VCC3V3
U2C
BANK 16
IO_0_16 F15 LED0
IO_L1P_T0_16 F13
IO_L1N_T0_16 F14
IO_L2P_T0_16 F16
IO_L2N_T0_16 E17
IO_L3P_T0_DQS_16 C14
IO_L3N_T0_DQS_16 C15
IO_L4P_T0_16 E13 RGB_B1
IO_L4N_T0_16 E14 RGB_G1
IO_L5P_T0_16 E16 RGB_R1
IO_L5N_T0_16 D16 RGB_B2
IO_L6P_T0_16 D14 RGB_G2
IO_L6N_T0_VREF_16 D15 RGB_R2
IO_L7P_T1_16 B15
IO_L7N_T1_16 B16
IO_L8P_T1_16 C13
IO_L8N_T1_16 B13
IO_L9P_T1_DQS_16 A15
IO_L9N_T1_DQS_16 A16
IO_L10P_T1_16 A13
IO_L10N_T1_16 A14
IO_L11P_T1_SRCC_16 B17
IO_L11N_T1_SRCC_16 B18
IO_L12P_T1_MRCC_16 D17
IO_L12N_T1_MRCC_16 C17
IO_L13P_T2_MRCC_16 C18 SYSCLK
IO_L13N_T2_MRCC_16 C19
IO_L14P_T2_SRCC_16 E19
IO_L14N_T2_SRCC_16 D19
IO_L15P_T2_DQS_16 F18
IO_L15N_T2_DQS_16 E18
IO_L16P_T2_16 B20
IO_L16N_T2_16 A20
IO_L17P_T2_16 A18
IO_L17N_T2_16 A19
IO_L18P_T2_16 F19 SFP1_SCL
IO_L18N_T2_16 F20 SFP1_SDA
IO_L19P_T3_16 D20 SFP2_SCL
IO_L19N_T3_VREF_16 C20 SFP2_SDA
IO_L20P_T3_16 C22 SFP1_TX_EN
IO_L20N_T3_16 B22 SFP1_TX_FAULT
IO_L21P_T3_DQS_16 B21 SFP1_LOS
IO_L21N_T3_DQS_16 A21 SFP1_MOD_ABS
IO_L22P_T3_16 E22 SFP2_TX_EN
IO_L22N_T3_16 D22 SFP2_TX_FAULT
IO_L23P_T3_16 E21 SFP2_LOS
IO_L23N_T3_16 D21 SFP2_MOD_ABS
IO_L24P_T3_16 G21
IO_L24N_T3_16 G22
IO_25_16 F21 LED1
XC7A35T-1FGG484C
VCC3V3
U2B
BANK 15
IO_0_15 J16 BTN_RESETN
IO_L1P_T0_AD0P_15 H13 VCC3V3_MON
IO_L1N_T0_AD0N_15 G13 VCCADJ_MON
IO_L2P_T0_AD8P_15 G15 VCC1V8_MON
IO_L2N_T0_AD8N_15 G16 VCC1V0_MON
IO_L3P_T0_DQS_AD1P_15 J14 MGTAVTT1V2_MON
IO_L3N_T0_DQS_AD1N_15 H14 MGTAVCC1V0_MON
IO_L4P_T0_15 G17
IO_L4N_T0_15 G18
IO_L5P_T0_AD9P_15 J15
IO_L5N_T0_AD9N_15 H15
IO_L6P_T0_15 H17
IO_L6N_T0_VREF_15 H18
IO_L7P_T1_AD2P_15 J22
IO_L7N_T1_AD2N_15 H22
IO_L8P_T1_AD10P_15 H20
IO_L8N_T1_AD10N_15 G20
IO_L9P_T1_DQS_AD3P_15 G21
IO_L9N_T1_DQS_AD3N_15 K22
IO_L10P_T1_AD11P_15 M21
IO_L10N_T1_AD11N_15 L21
IO_L11P_T1_SRCC_15 J20
IO_L11N_T1_SRCC_15 J21
IO_L12P_T1_MRCC_15 J19
IO_L12N_T1_MRCC_15 H19
IO_L13P_T2_MRCC_15 K18
IO_L13N_T2_MRCC_15 K19
IO_L14P_T2_SRCC_15 L19
IO_L14N_T2_SRCC_15 L20
IO_L15P_T2_DQS_15 N22
IO_L15N_T2_DQS_ADV_B_15 M22
IO_L16P_T2_A28_15 M18
IO_L16N_T2_A27_15 L18
IO_L17P_T2_A26_15 N18
IO_L17N_T2_A25_15 N19
IO_L18P_T2_A24_15 N20
IO_L18N_T2_A23_15 M20
IO_L19P_T3_A22_15 K13
IO_L19N_T3_A21_VREF_15 K14
IO_L20P_T3_A20_15 M13
IO_L20N_T3_A19_15 L13
IO_L21P_T3_DQS_15 K17
IO_L21N_T3_DQS_A18_15 J17
IO_L22P_T3_A17_15 L14
IO_L22N_T3_A16_15 L15
IO_L23P_T3_FOE_B_15 L16
IO_L23N_T3_FWE_B_15 K16
IO_L24P_T3_RS1_15 M15
IO_L24N_T3_RS0_15 M16
IO_25_15 M17
XC7A35T-1FGG484C
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FPGA Banks 1
Size
A4
UCL
Revision
Date: 6/2/2017
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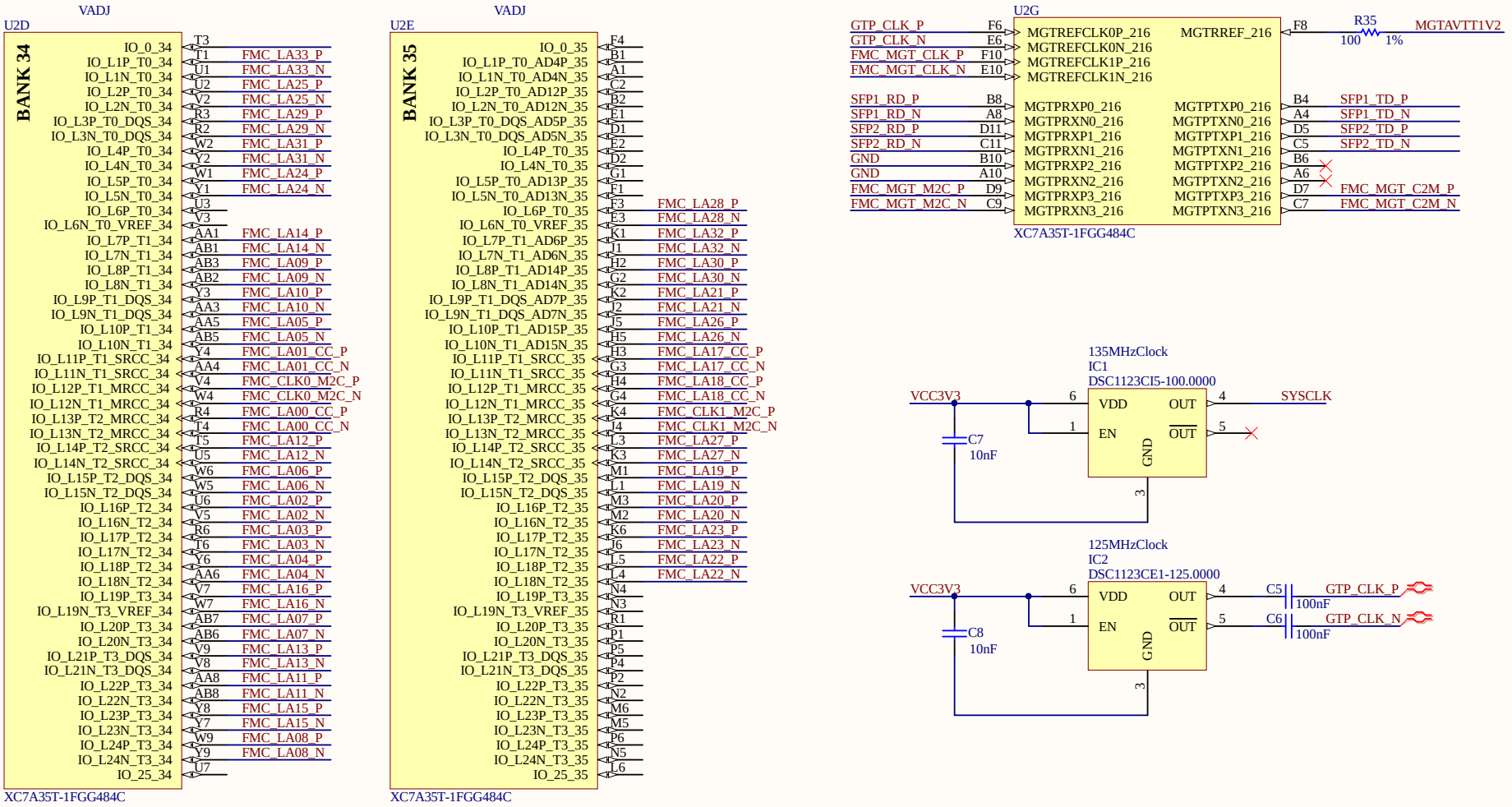
Sheet 6 of 9
Drawn By: Samer Kilani



Title	FPGA Banks 2	
Size A4	UCL	Revision
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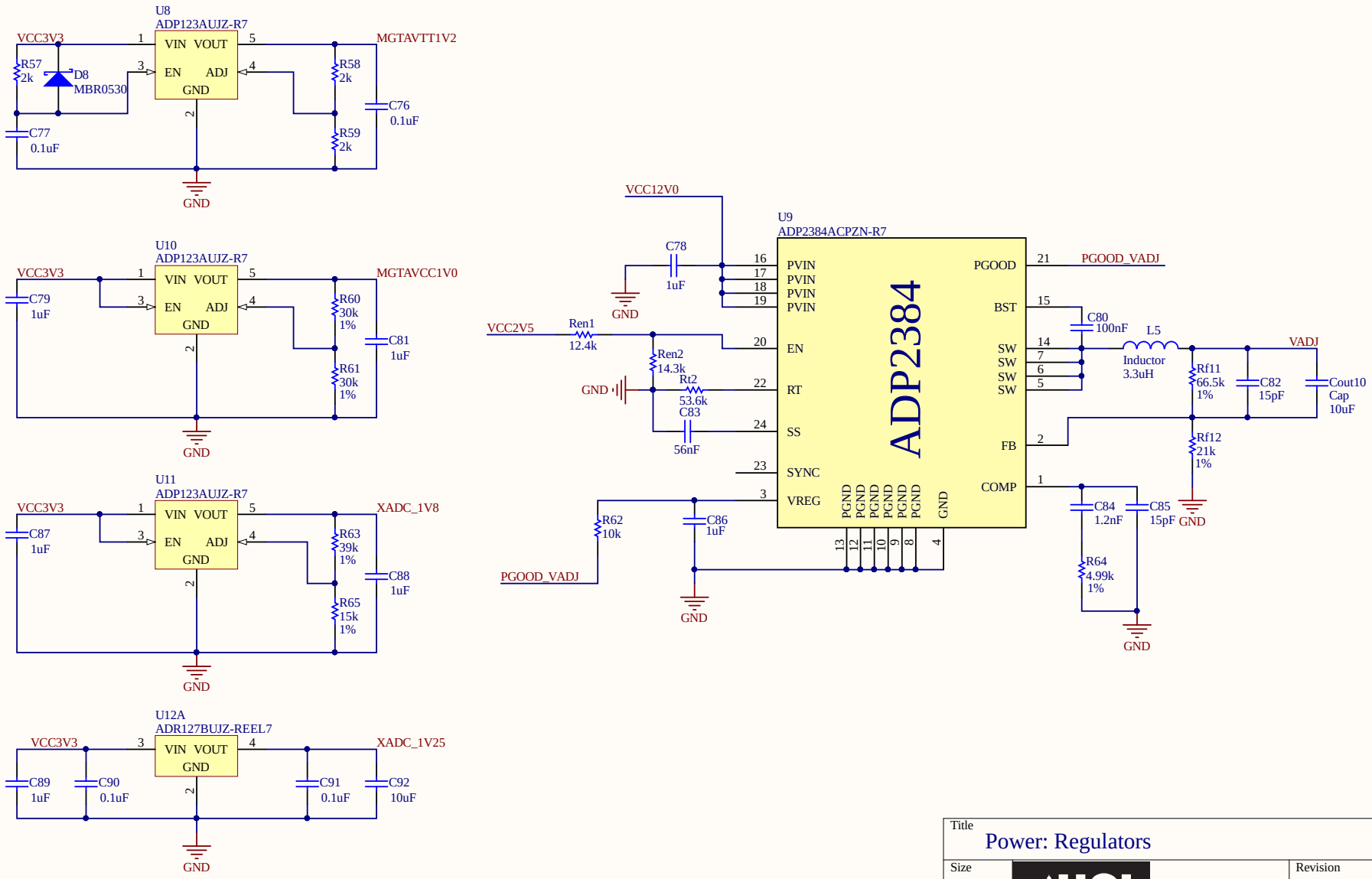
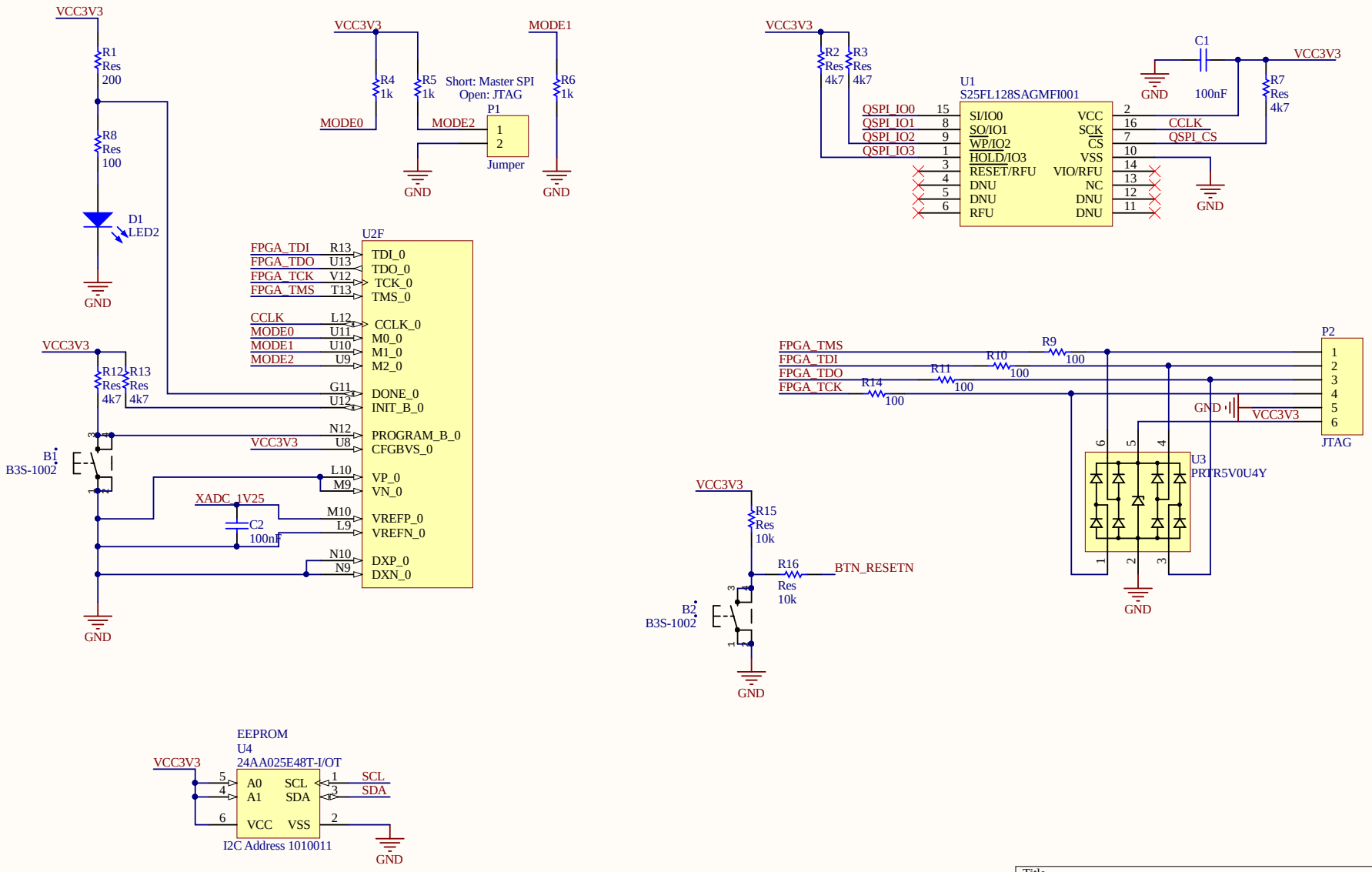
File: C:\Users\..\FPGA_Banks2.SchDoc		Drawn By: Samer Kilani



Title	Power: Regulators		
Size	A4		Revision
Date:	6/2/2017	Sheet 8 of 9	
File:	C:\Users\..\Regulators.SchDoc	Drawn By: Samer Kilani	



Title	FPGA Configuration		
Size	A4		Revision
Date:	6/2/2017	Sheet 9 of 9	
File:	C:\Users\..\Config.SchDoc	Drawn By:	Samer Kilani