


Freescale Semiconductor



COMEXPRESS CARRIER

		Drawing Title: COMEXPRESS CARRIER		Page Title: <PageTitle>	Document Number SCH-26479 PDF: SPF-26479	Engineer Name	Size Custom	Date: Friday, October 22, 2010	ICAP Classification: FCP:___ FIUO: X PUBL:___	
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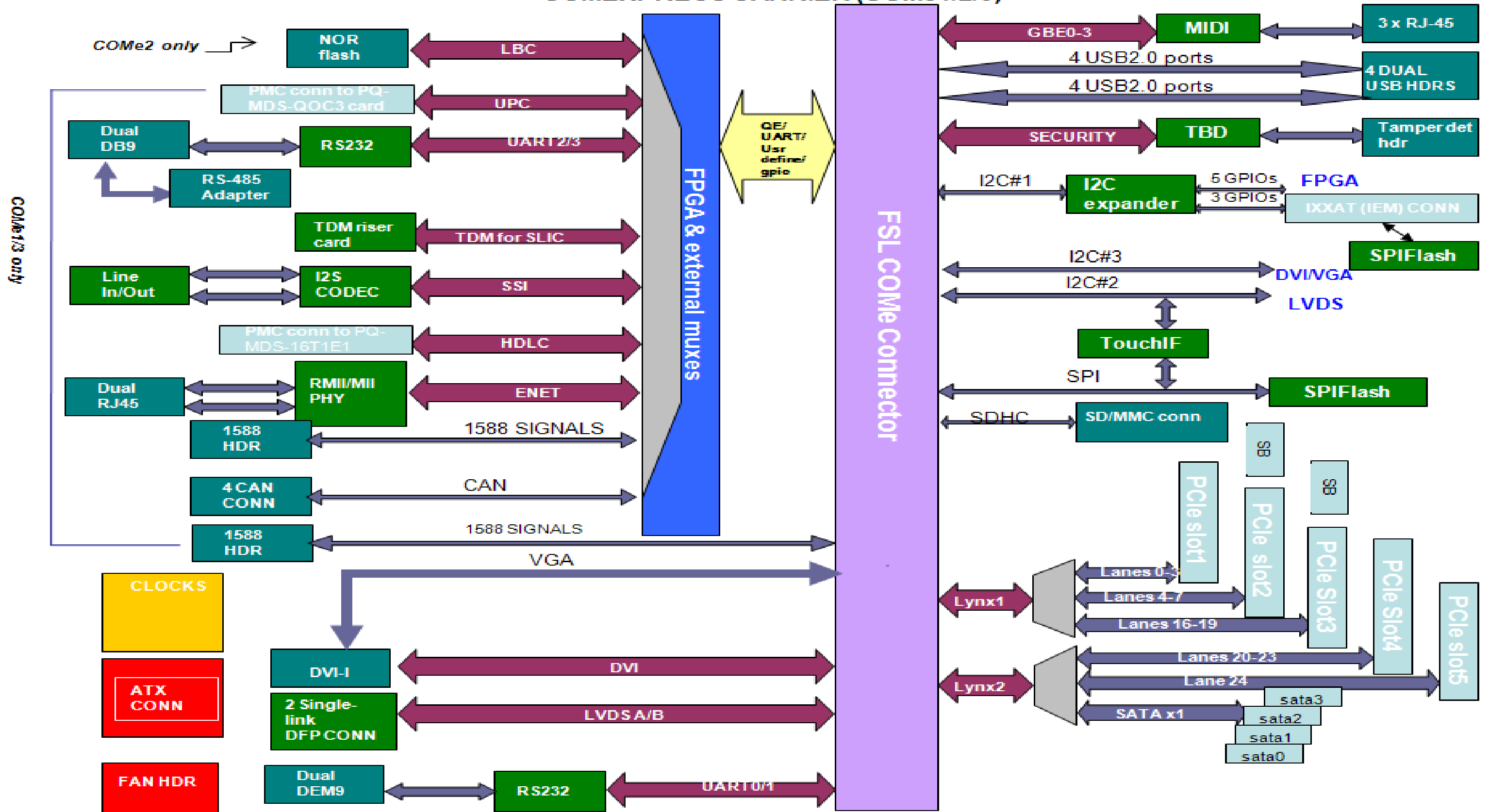
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Version Rev	DATE	Change
A	5/28/2010	FIRST PROTOTYPE
B	10/13/2010	RESPIN FOR PROTOTYPE B PER ECN
XXX	NA	XXX

All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only. Contact your Freescale representative to obtain the latest information on this product.

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System Block Diagram #2

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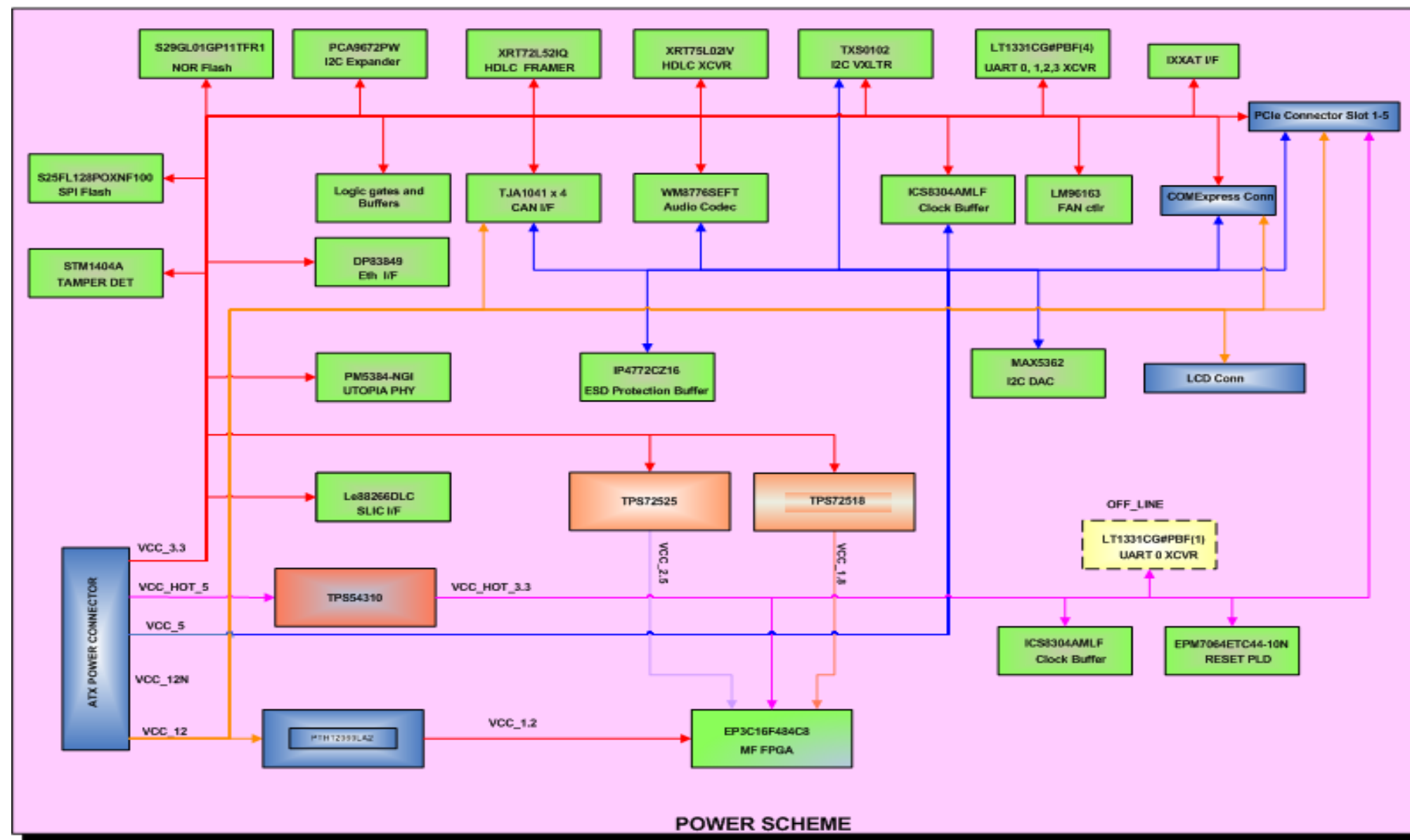
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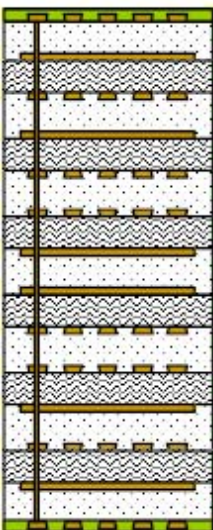


Part Number: Freescale_170-24679_via

Contact: Martin Thompson

Phone: 408-938-7231

Date: 4/22/10

Cu			Layer	Thick. (mils)	Cu Foil wt (oz)		DK	Lam. Thick. (mils)	Description
1	2.00	0.5 oz							Foil, 0.5 oz
2	1.20	1 oz					3.86	3.68	Prepreg 370HR 3313(59) 18Gx24
3	0.60	0.5 oz					3.96	6.00	Core 370HR 6mils 1080/3313 0.5 oz / 1 oz 18.25Gx24.25
4	1.20	1 oz					3.68	5.59	Prepreg 370HR 1080(68Y1080(68) 18Gx24
5	0.60	0.5 oz					3.96	8.00	Core 370HR 8mils 2x3313 0.5 oz / 1 oz 18.25Gx24.25
6	0.60	0.5 oz					3.90	3.98	Prepreg 370HR 2116(57) 18Gx24
7	1.20	1 oz					3.96	8.00	Core 370HR 8mils 2x3313 0.5 oz / 1 oz 18.25Gx24.25
8	1.20	1 oz					3.98	8.25	Prepreg 370HR 2116(53Y2116(53) 18Gx24
9	0.60	0.5 oz					3.96	8.00	Core 370HR 8mils 2x3313 0.5 oz / 1 oz 18.25Gx24.25
10	0.60	0.5 oz					3.90	3.98	Prepreg 370HR 2116(57) 18Gx24
11	1.20	1 oz					3.96	8.00	Core 370HR 8mils 2x3313 0.5 oz / 1 oz 18.25Gx24.25
12	0.60	0.5 oz					3.68	5.59	Prepreg 370HR 1080(68Y1080(68) 18Gx24
13	1.20	1 oz					3.96	6.00	Core 370HR 6mils 1080/3313 0.5 oz / 1 oz 18.25Gx24.25
14	2.00	0.5 oz					3.86	3.68	Prepreg 370HR 3313(59) 18Gx24 Foil, 0.5 oz
Layers	Drill Type	Via Fill		89.53	Thickness over Laminate				
1 - 14	PTH	—		93.53	Thickness over Copper				
				94.93	Thickness over Soldermask				

Impedance Table

Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (ohms)	Target Linewidth (mils)	Edge Coupled Pitch * (mils)	Reference Layers	Modelled Linewidth (mils)	Modelled Impedance (ohms)	CoPlaner Space (mils)
1	Single Ended	Yes	50.00	+/-5	5.75	0.00	(2)	5.75	50.49	
1	Edge Coupled Differential	Yes	100.00	+/-10	4.50	12.00	(2)	4.50	100.13	
3	Edge Coupled Differential	---	100.00	+/-10	4.50	10.00	(2, 4)	4.50	98.45	
3	Edge Coupled Differential	---	90.00	+/-9	5.25	10.00	(2, 4)	5.25	89.70	
3	Edge Coupled Differential	---	92.00	+/-9.2	5.00	10.00	(2, 4)	5.00	92.48	
3	Single Ended	---	50.00	+/-5	5.50	0.00	(2, 4)	5.50	49.71	
3	Edge Coupled Differential	---	120.00	+/-12	3.50	14.00	(2, 4)	3.50	118.99	
5	Edge Coupled Differential	---	120.00	+/-12	4.25	12.00	(4, 7)	4.25	119.31	
5	Edge Coupled Differential	---	100.00	+/-10	5.00	10.00	(4, 7)	5.00	101.95	
5	Edge Coupled Differential	---	90.00	+/-9	6.00	10.00	(4, 7)	6.00	90.59	
5	Edge Coupled Differential	---	92.00	+/-9.2	5.75	10.00	(4, 7)	5.75	93.30	
5	Single Ended	---	50.00	+/-5	9.00	0.00	(4, 7)	9.00	50.16	
6	Edge Coupled Differential	---	120.00	+/-12	4.25	12.00	(4, 7)	4.25	119.31	
6	Edge Coupled Differential	---	100.00	+/-10	5.00	10.00	(4, 7)	5.00	101.95	
6	Edge Coupled Differential	---	90.00	+/-9	6.00	10.00	(4, 7)	6.00	90.59	
6	Edge Coupled Differential	---	92.00	+/-9.2	5.75	10.00	(4, 7)	5.75	93.30	
6	Single Ended	---	50.00	+/-5	9.00	0.00	(4, 7)	9.00	50.16	
9	Edge Coupled Differential	---	120.00	+/-12	4.25	12.00	(8, 11)	4.25	119.31	
9	Edge Coupled Differential	---	100.00	+/-10	5.00	10.00	(8, 11)	5.00	101.95	
9	Edge Coupled Differential	---	90.00	+/-9	6.00	10.00	(8, 11)	6.00	90.59	
9	Edge Coupled Differential	---	92.00	+/-9.2	5.75	10.00	(8, 11)	5.75	93.30	
9	Single Ended	---	50.00	+/-5	9.00	0.00	(8, 11)	9.00	50.16	
10	Edge Coupled Differential	---	120.00	+/-12	4.25	12.00	(8, 11)	4.25	119.31	
10	Edge Coupled Differential	---	100.00	+/-10	5.00	10.00	(8, 11)	5.00	101.95	
10	Edge Coupled Differential	---	90.00	+/-9	6.00	10.00	(8, 11)	6.00	90.59	
10	Edge Coupled Differential	---	92.00	+/-9.2	5.75	10.00	(8, 11)	5.75	93.30	
10	Single Ended	---	50.00	+/-5	9.00	0.00	(8, 11)	9.00	50.16	
12	Edge Coupled Differential	---	100.00	+/-10	4.50	10.00	(11, 13)	4.50	98.45	
12	Edge Coupled Differential	---	90.00	+/-9	5.25	10.00	(11, 13)	5.25	89.70	
12	Edge Coupled Differential	---	92.00	+/-9.2	5.00	10.00	(11, 13)	5.00	92.48	
12	Single Ended	---	50.00	+/-5	5.50	0.00	(11, 13)	5.50	49.71	
12	Edge Coupled Differential	---	120.00	+/-12	3.50	14.00	(11, 13)	3.50	118.99	
14	Single Ended	Yes	50.00	+/-5	5.75	0.00	(13)	5.75	50.49	
14	Edge Coupled Differential	Yes	100.00	+/-10	4.50	12.00	(13)	4.50	100.13	

* Edge Coupled Pitch is measured from the center line of one differential trace to the center line of the other.

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PCB Stackup

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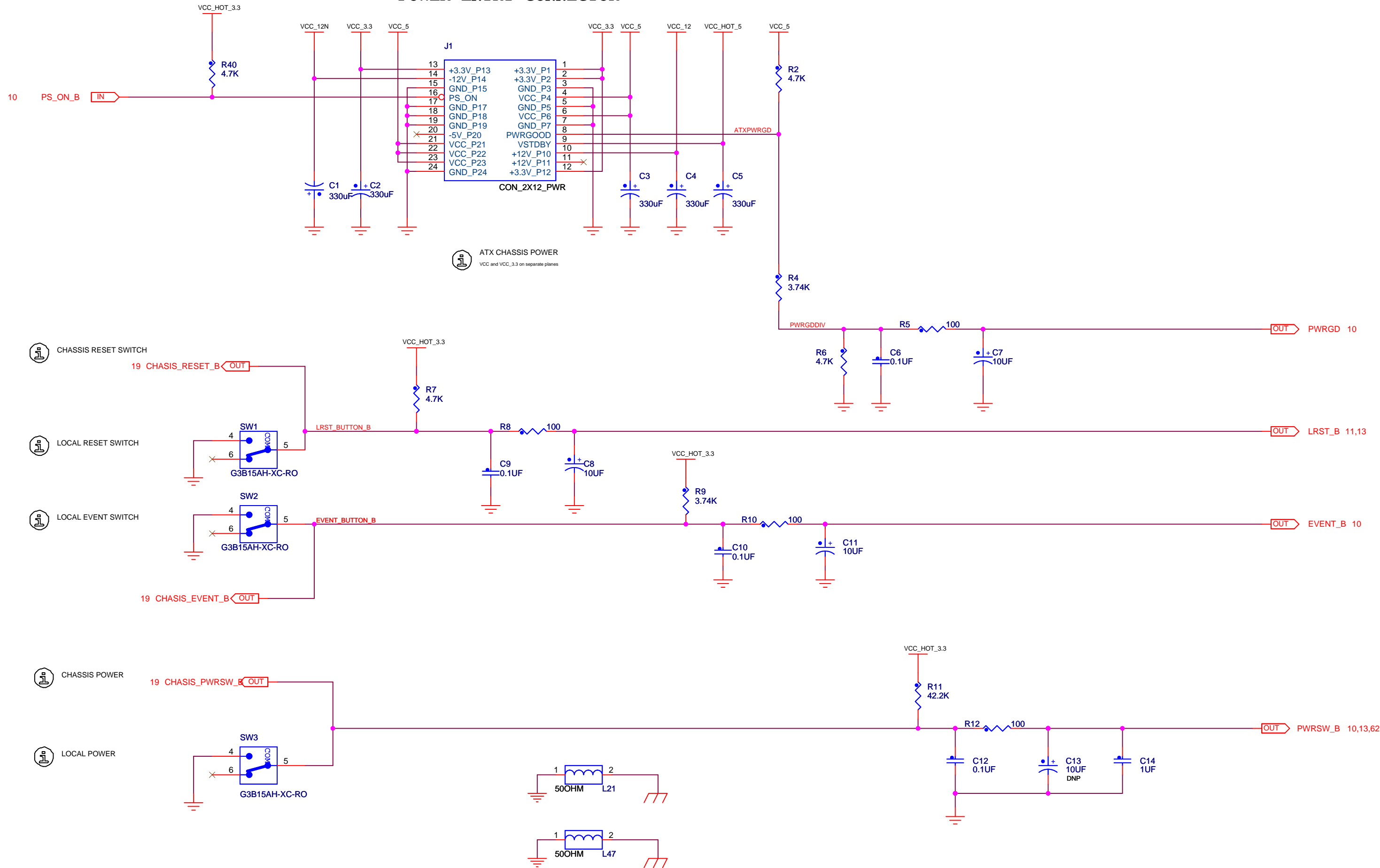
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POWER ENTRY CONNECTOR



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Power Entry, Chassis I/O

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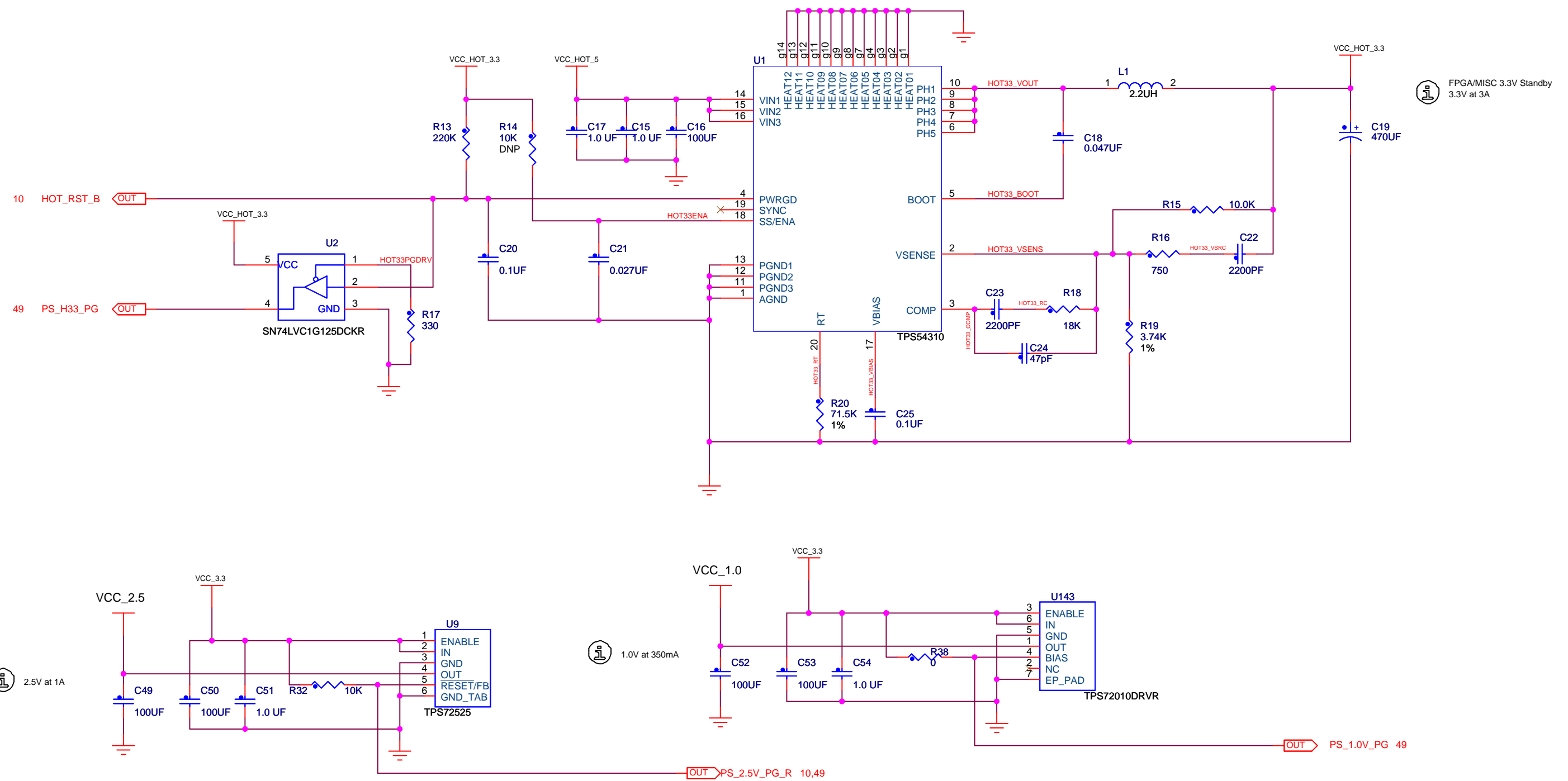
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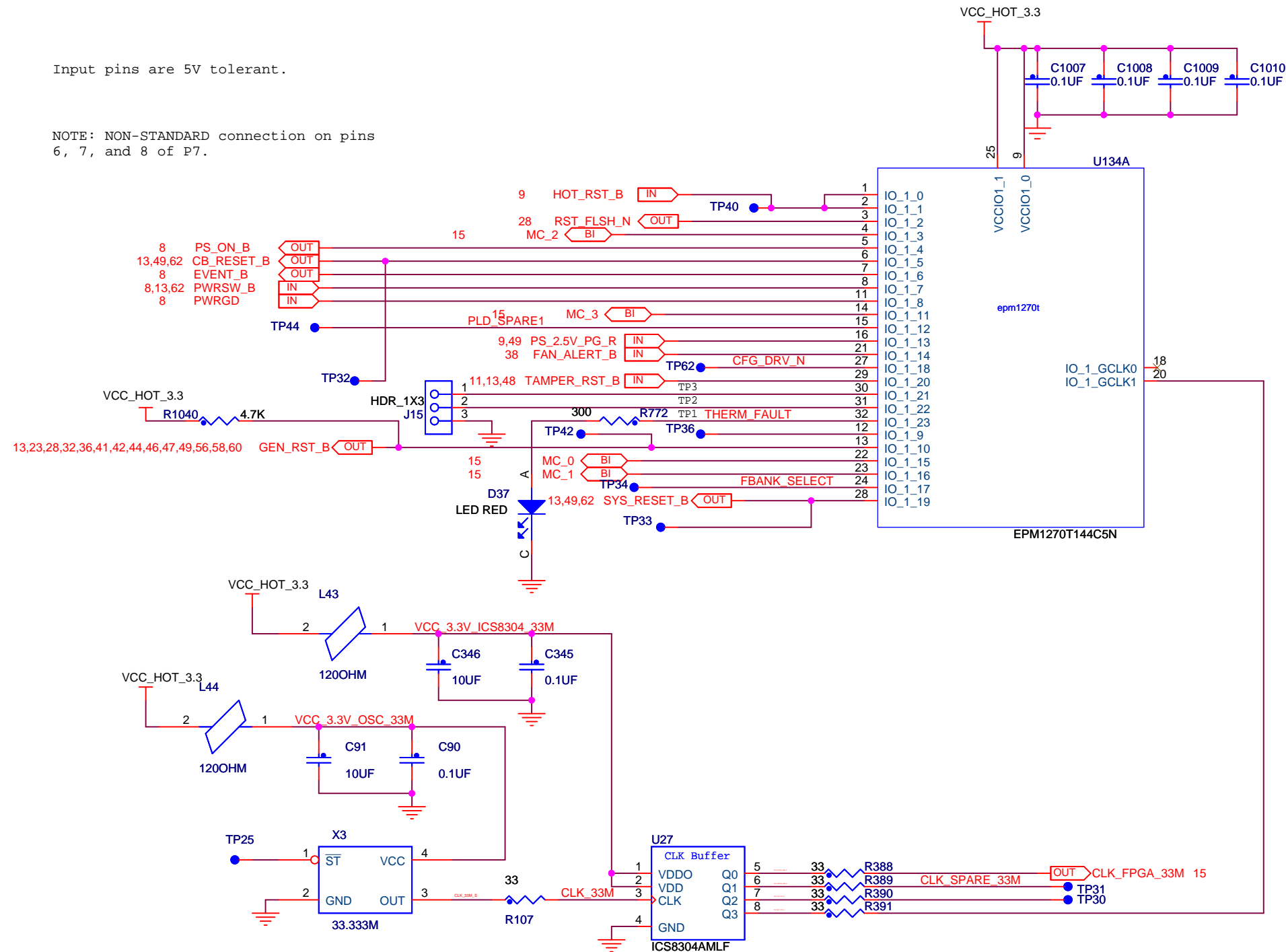
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5V to 3.3V Step Down Regulator



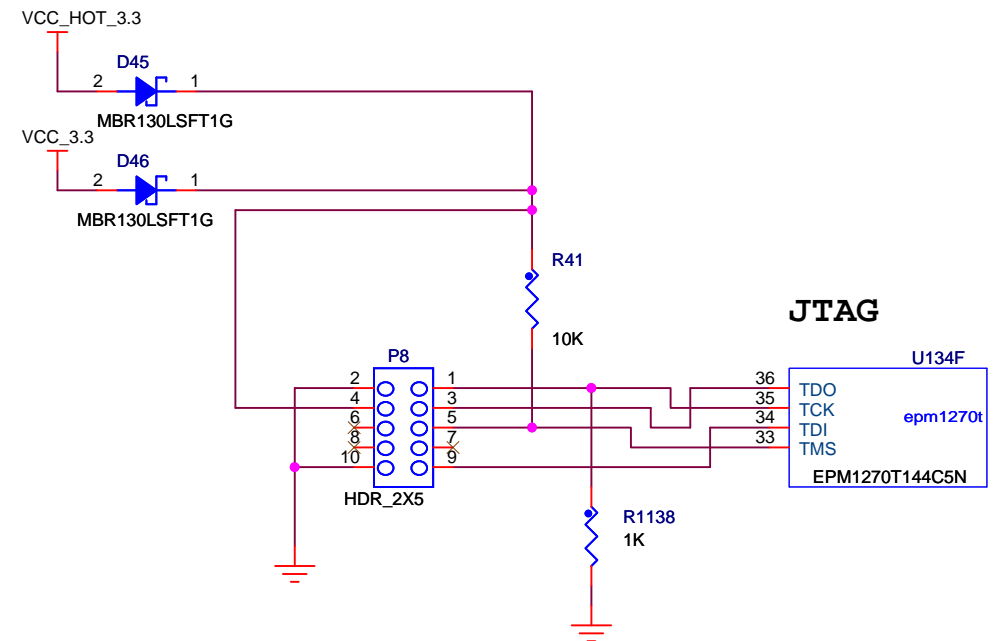
Input pins are 5V tolerant.

NOTE: NON-STANDARD connection on pins 6, 7, and 8 of P7.



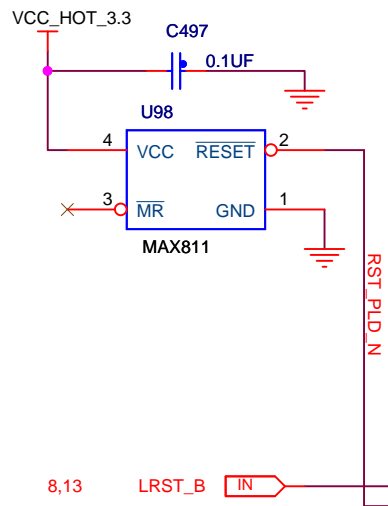
CLOCK Generation for CPLD

CPLD POWER

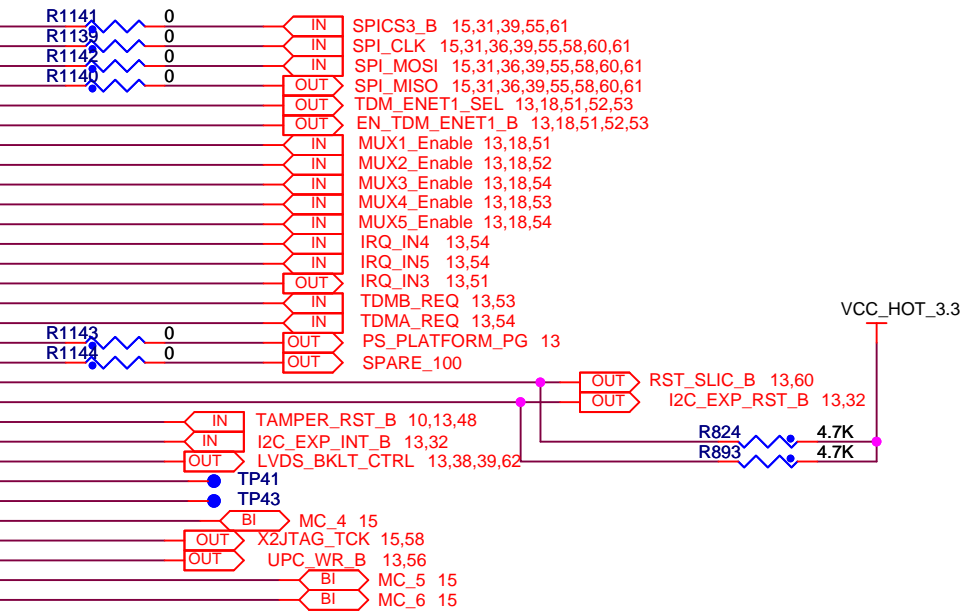
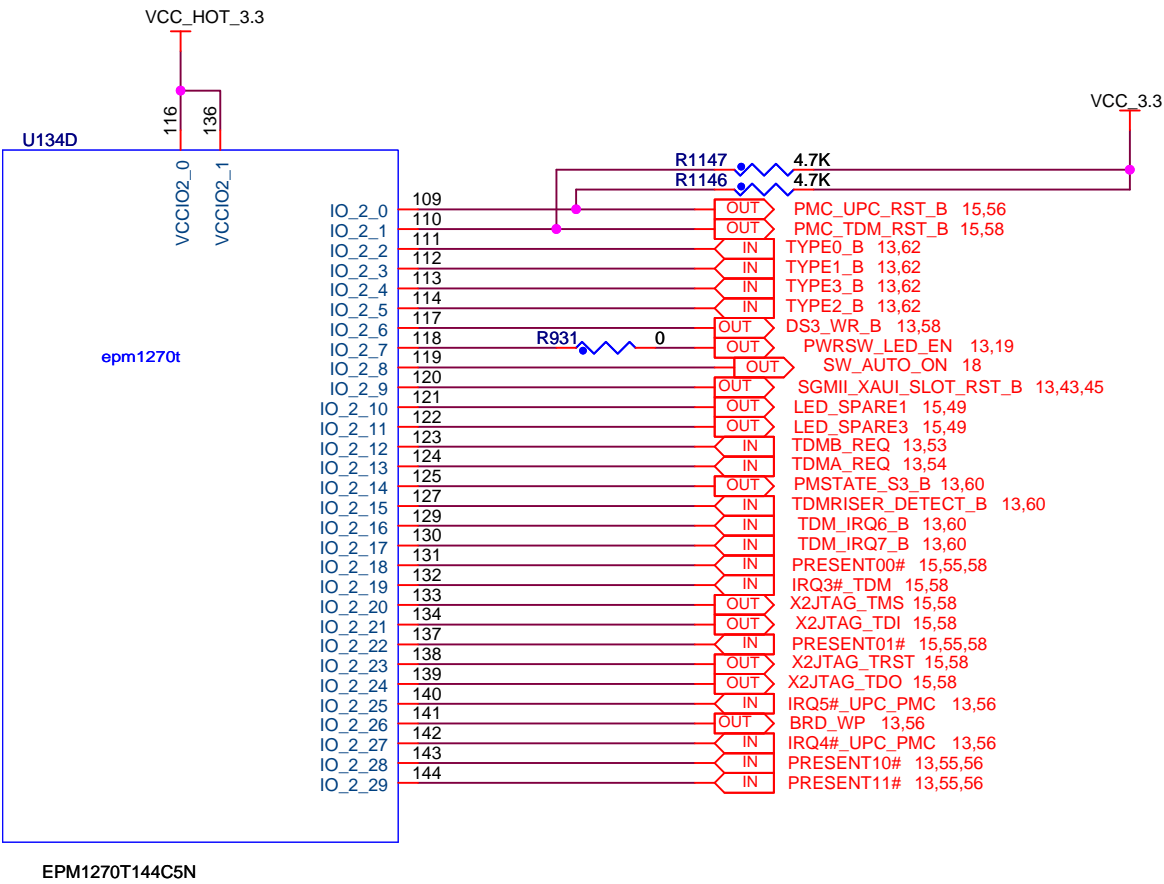
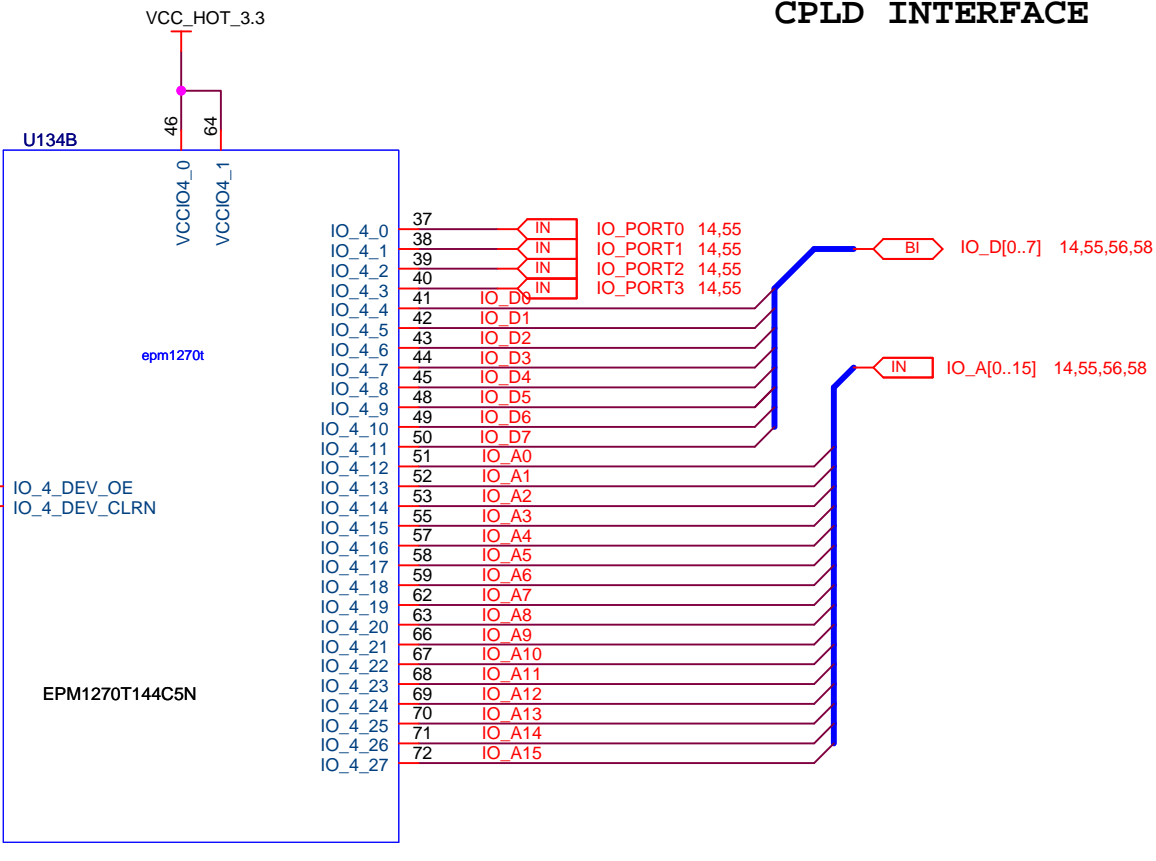


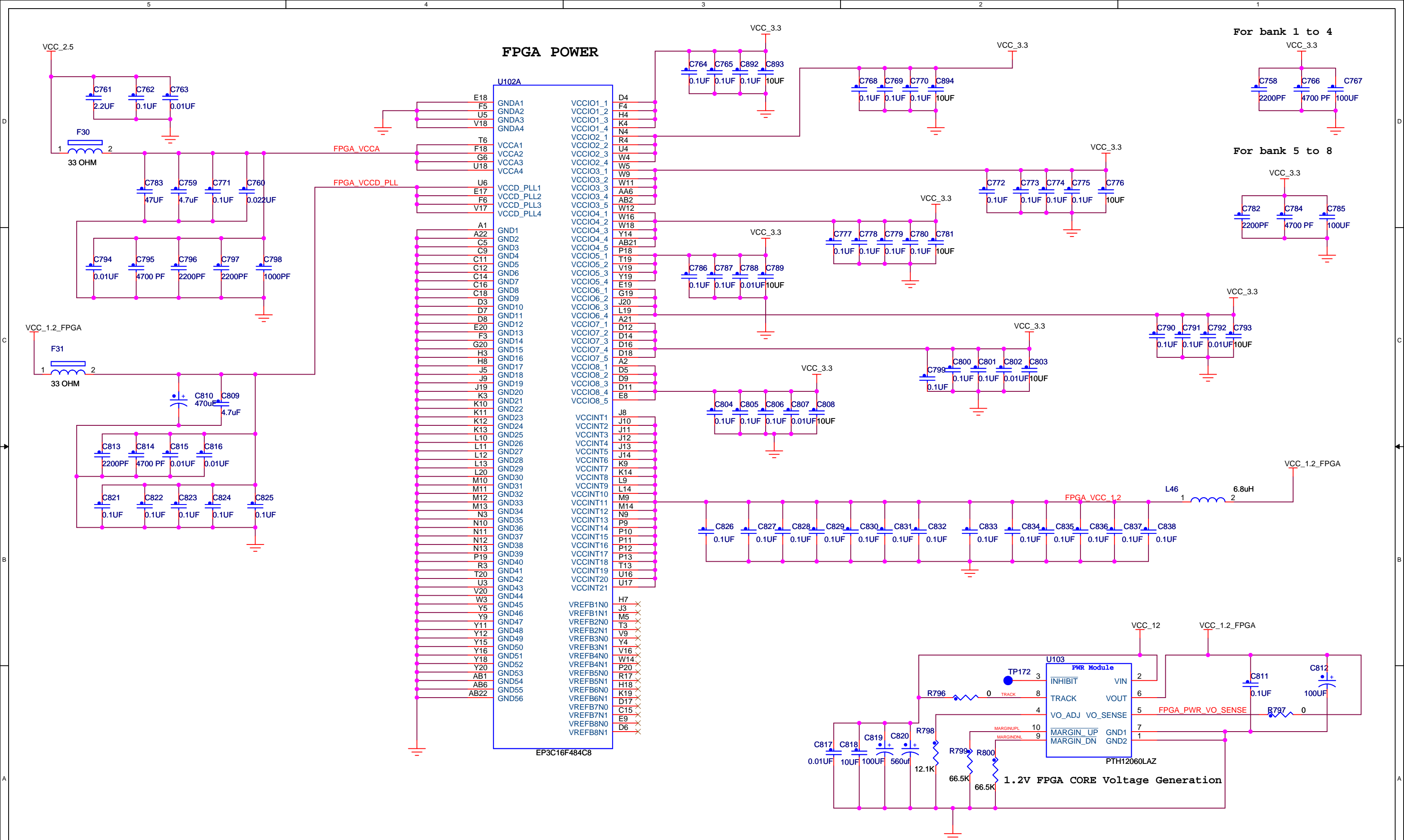
JTAG

RESET for CPLD

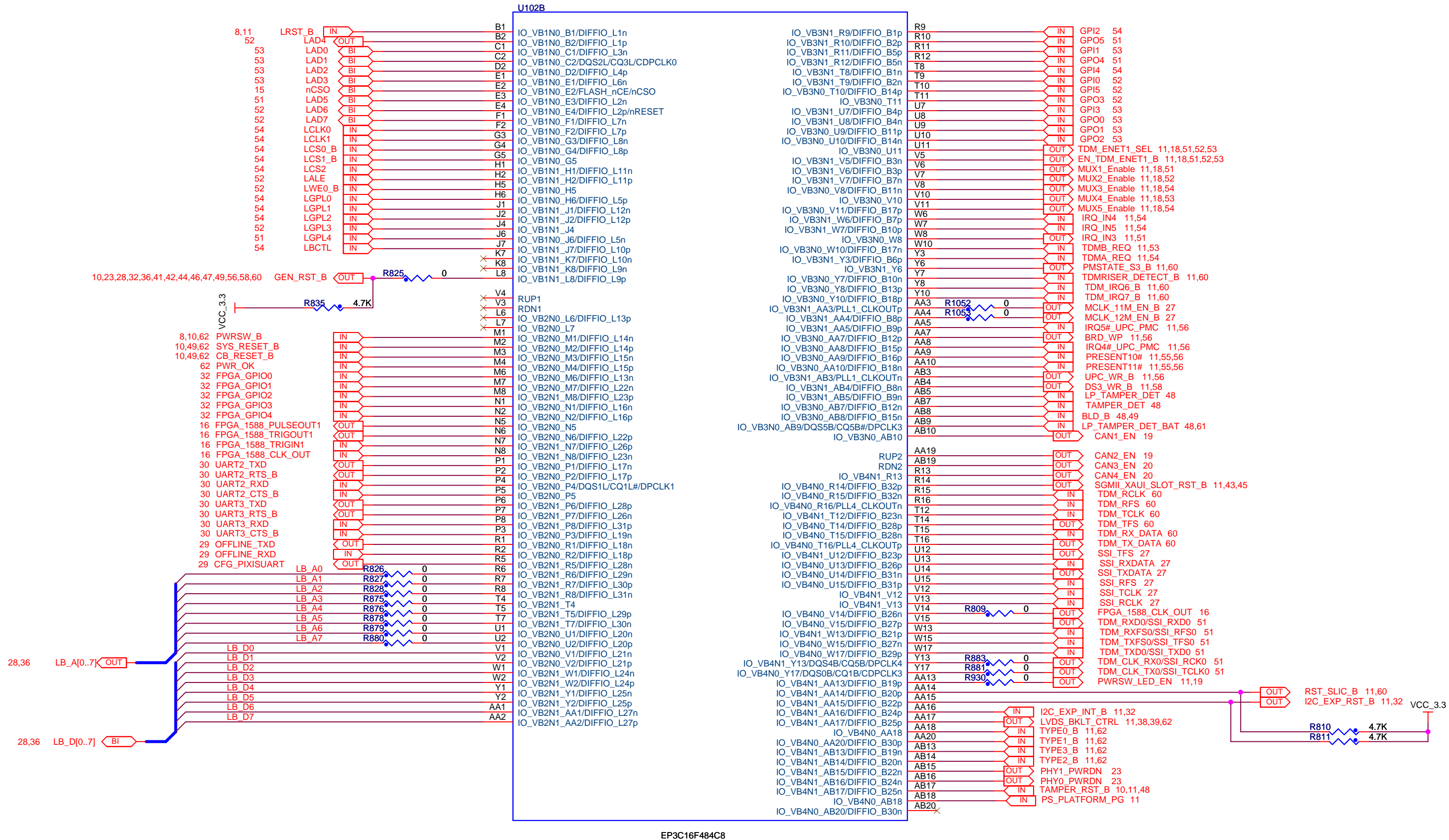


CPLD INTERFACE





FPGA INTERFACE



FPGA INTERFACE

U102C

- T17 RUP3
- T18 RDN3
- N22 DIFFIO_R21n
- N21 DIFFIO_R21p
- M15 IO_VB5N1_M15/DIFFIO_R29n
- M16 IO_VB5N0_M16
- M19 IO_VB5N0_M19/DIFFIO_R19p
- M20 IO_VB5N0_M20/DIFFIO_R19n
- M22 IO_VB5N0_M21/DIFFIO_R20p
- N14 IO_VB5N0_M22/DIFFIO_R20n
- N15 IO_VB5N1_N14
- N16 IO_VB5N1_N15/DIFFIO_R29p
- N17 IO_VB5N0_N16
- N18 IO_VB5N0_N17/DIFFIO_R22n
- N19 IO_VB5N0_N18/DQS1R/CQ1R#/DPCLK6
- N20 IO_VB5N0_N19/DIFFIO_R23p
- P14 IO_VB5N0_N20/DIFFIO_R23n
- P15 IO_VB5N1_P14
- P16 IO_VB5N1_P15/DIFFIO_R30n
- P17 IO_VB5N1_P16/DIFFIO_R30p
- P21 IO_VB5N1_P17
- P22 IO_VB5N0_P21/DIFFIO_R24p
- R18 IO_VB5N0_P22/DIFFIO_R24n
- R19 IO_VB5N0_R18/DIFFIO_R26n
- R20 IO_VB5N0_R19/DIFFIO_R26p
- R21 IO_VB5N1_R20
- R22 IO_VB5N0_R21/DIFFIO_R25p
- U19 IO_VB5N0_R22/DIFFIO_R25n
- U20 IO_VB5N1_U19/DIFFIO_R32p
- U21 IO_VB5N0_U21/DIFFIO_R32n
- U22 IO_VB5N0_U22/DIFFIO_R27p
- V21 IO_VB5N0_U22/DIFFIO_R27n
- V22 IO_VB5N1_V21/DIFFIO_R28p
- W19 IO_VB5N1_V22/DIFFIO_R28n
- W20 IO_VB5N1_W19/DIFFIO_R34p
- W21 IO_VB5N1_W20/CQ3R#/CDPCLK4
- W22 IO_VB5N1_W21/DIFFIO_R31p
- Y21 IO_VB5N1_W22/DIFFIO_R31n
- Y22 IO_VB5N1_Y21/DIFFIO_R33p
- AA21 IO_VB5N1_Y22/DIFFIO_R33n
- AA22 IO_VB5N1_AA21/DIFFIO_R35p
- AA22 IO_VB5N1_AA22/DIFFIO_R35n
- K21 DIFFIO_R16p
- L21 DIFFIO_R17p
- L22 DIFFIO_R17n
- C21 IO_VB6N0_C21/DIFFIO_R4p
- C22 IO_VB6N0_C22/DIFFIO_R4n
- D20 IO_VB6N0_D20/DIFFIO_R2p
- D21 IO_VB6N0_D21/DIFFIO_R7p
- D22 IO_VB6N0_D22/DIFFIO_R7n
- E21 IO_VB6N0_E21/DIFFIO_R9p/nOE
- E22 IO_VB6N0_E22/DIFFIO_R9n/nWE
- F17 IO_VB6N0_F17/DIFFIO_R1n
- F19 IO_VB6N0_F19/DIFFIO_R6p/RDY
- F20 IO_VB6N0_F20/DIFFIO_R6n/nAVD
- F21 IO_VB6N0_F21/DIFFIO_R11p
- F22 IO_VB6N1_F22/DIFFIO_R11n
- G17 IO_VB6N0_G17/DIFFIO_R1p
- H16 IO_VB6N0_H16/DIFFIO_R8p
- H17 IO_VB6N0_H17/DIFFIO_R5p
- H19 IO_VB6N0_H19/DIFFIO_R10p
- H20 IO_VB6N0_H20/DIFFIO_R10n
- H21 IO_VB6N1_H21/DIFFIO_R13p
- H22 IO_VB6N1_H22/DIFFIO_R13n

- 37,63 VGA_I2C3_CK
- 37,63 VGA_I2C3_DAT
- 19 CAN1_RXD
- 19 CAN1_TXD
- 19 CAN2_RXD
- 19 CAN2_TXD
- 20 CAN3_RXD
- 20 CAN3_TXD
- 20 CAN4_RXD
- 20 CAN4_TXD
- 54 CAN3_TX
- 54 CAN3_RX
- 54 CAN1_TX
- 54 CAN1_RX
- 54 CAN4_TX
- 52 CAN4_RX
- 52 CAN2_TX
- 52 CAN2_RX

- FPGA_STATUS_LED1
- FPGA_STATUS_LED2
- FPGA_STATUS_LED3
- FPGA_STATUS_LED4
- FPGA_STATUS_LED5
- FPGA_STATUS_LED6

- 11,55 IO_PORT0
- 11,55 IO_PORT1
- 11,55 IO_PORT2
- 11,55 IO_PORT3

- 11,55,56,58 IO_D[0..7]
- 11,55,56,58 IO_A[0..15]

- IO_A0
- IO_A1
- IO_A2
- IO_A3
- IO_A4
- IO_A5
- IO_A6
- IO_A7
- IO_A8
- IO_A9
- IO_A10
- IO_A11
- IO_A12
- IO_A13
- IO_A14
- IO_A15

- IO_VB6N1_J15
- IO_VB6N1_J16/DIFFIO_R14n
- IO_VB6N0_J17/DIFFIO_R8n
- IO_VB6N1_J18
- IO_VB6N1_J21/DIFFIO_R15p
- IO_VB6N1_J22/DQS0R/CQ1R/DPCLK7
- IO_VB6N1_K15
- IO_VB6N1_K16/DIFFIO_R14p
- IO_VB6N1_K17/DIFFIO_R12n
- IO_VB6N1_K18/DIFFIO_R12p
- IO_VB6N1_L15/DIFFIO_R18p
- IO_VB6N1_L16/DIFFIO_R18n

- IO_VB7N1_A16/DIFFIO_T24n
- IO_VB7N0_A18/DIFFIO_T27n
- IO_VB7N0_A20/PLL2_CLKOUTn
- IO_VB7N1_B16/DIFFIO_T24p
- IO_VB7N0_B20/PLL2_CLKOUTp
- IO_VB7N0_C17
- IO_VB7N0_C19/DIFFIO_T29n
- IO_VB7N0_C21/DIFFIO_T29p
- IO_VB7N0_D19/DIFFIO_T29p
- IO_VB7N1_E12
- IO_VB7N7_E13
- IO_VB7N0_E15/DIFFIO_T26p
- IO_VB7N0_E16/DIFFIO_T32p
- IO_VB7N1_F12/DIFFIO_T23p
- IO_VB7N0_F14/DQS0T/CQ1T/CDPCLK6
- IO_VB7N0_U21/DIFFIO_T31n
- IO_VB7N0_F16/DIFFIO_T32n
- IO_VB7N1_G12/DIFFIO_T21n
- IO_VB7N1_G13
- IO_VB7N0_G14
- IO_VB7N0_G15/DIFFIO_T30n
- IO_VB7N0_G16/DIFFIO_T31p
- IO_VB7N1_H12/DIFFIO_T22p
- IO_VB7N1_H13/DIFFIO_T22n
- IO_VB7N0_H14/DIFFIO_T28p
- IO_VB7N0_H15/DIFFIO_T28n

- IO_VB8N1_A4/DIFFIO_T5n
- IO_VB8N0_A10/DIFFIO_T14n
- IO_VB8N1_B5
- IO_VB8N1_C3/DIFFIO_T2n
- IO_VB8N0_C10
- IO_VB8N0_D10/DIFFIO_T15n
- IO_VB8N1_E5/PLL3_CLKOUTp
- IO_VB8N1_E6/PLL3_CLKOUTn
- IO_VB8N1_E7
- IO_VB8N0_E10/DIFFIO_T15p
- IO_VB8N1_F7/DIFFIO_T1n
- IO_VB8N1_F9/DIFFIO_T6n
- IO_VB8N1_G7/DIFFIO_T1p
- IO_VB8N1_G8/DIFFIO_T4p
- IO_VB8N0_G9/DIFFIO_T8p
- IO_VB8N0_G10/DIFFIO_T8n
- IO_VB8N0_G11
- IO_VB8N0_H9/DIFFIO_T7p
- IO_VB8N0_H10/DIFFIO_T7n
- IO_VB8N0_H11

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- NORCS_B 18,28
- NORWE_B 18,28
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- I2C1_DAT 27,32,55,61
- I2C2_CLK 38,39,56,58,62
- I2C2_DAT 38,39,56,58,62

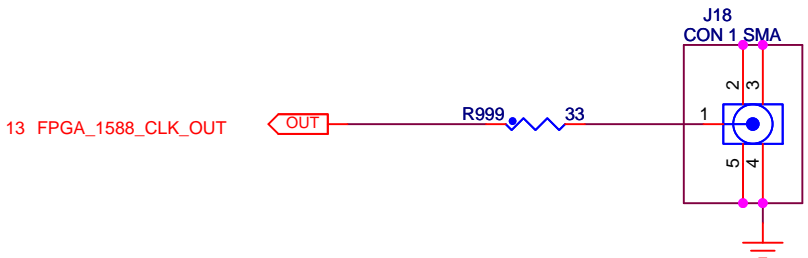
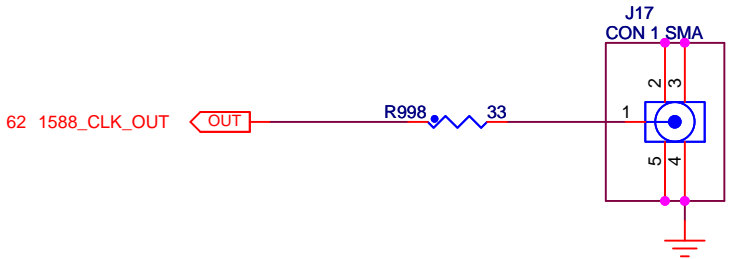
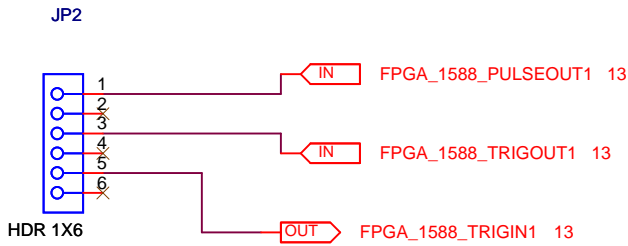
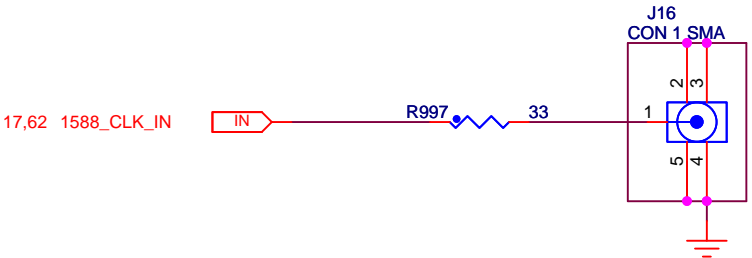
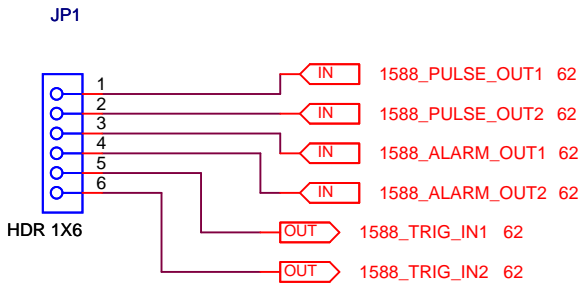
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- LGPL1_F 56,58
- LGPL2_F 56,58
- LGPL3_F 56,58
- LGPL4_F 56,58
- LCS2_B 56,58
- LB_A8 36
- LB_A9 36
- LB_A10 36
- LB_A11 36
- LB_A12 36
- LB_D8 36
- LB_D9 36
- LB_D10 36
- LB_D11 36
- LB_D12 36
- LB_D13 36
- LB_D14 36
- LB_D15 36
- LB_RD_B 36
- LB_WR_B 36
- IXXAT_CS_B 36
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- EMI2_SEL0 18,26
- EMI2_SEL1 18,26

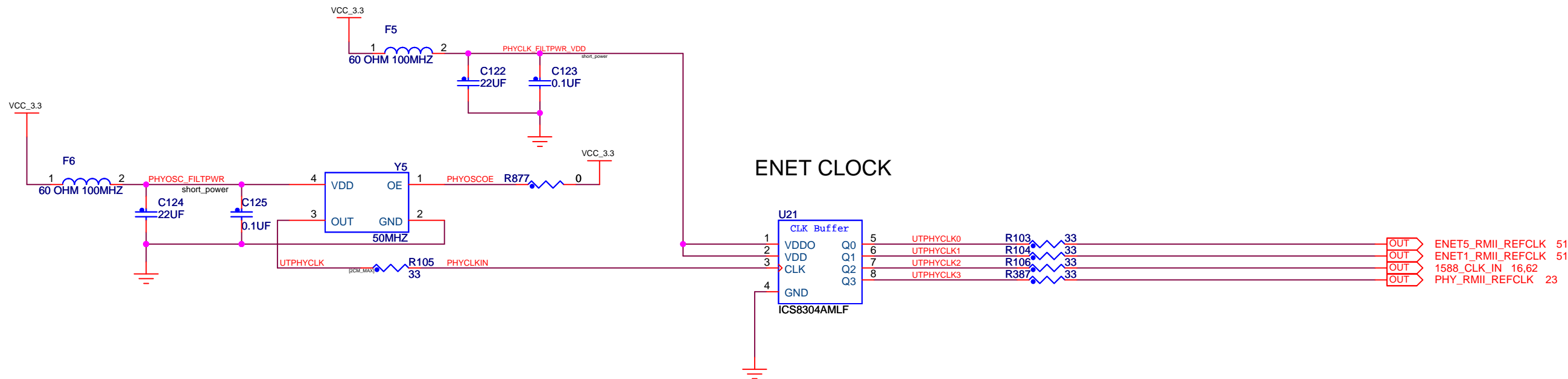
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- TP63
- TP64
- TP65

- CE_PB21/TAMPER_DET 61
- CE_PB22 61
- CE_PB23_FPGA 54
- CE_PB29/LP_TAMPER_DET 61
- CE_PB30 61
- CE_PB31 61
- IRQ_OUT_B/IRQ_OUT 61
- IRQ00/IRQ_IN0 43,45,61
- IRQ01/IRQ_IN1 61
- IRQ02/IRQ_IN2 61

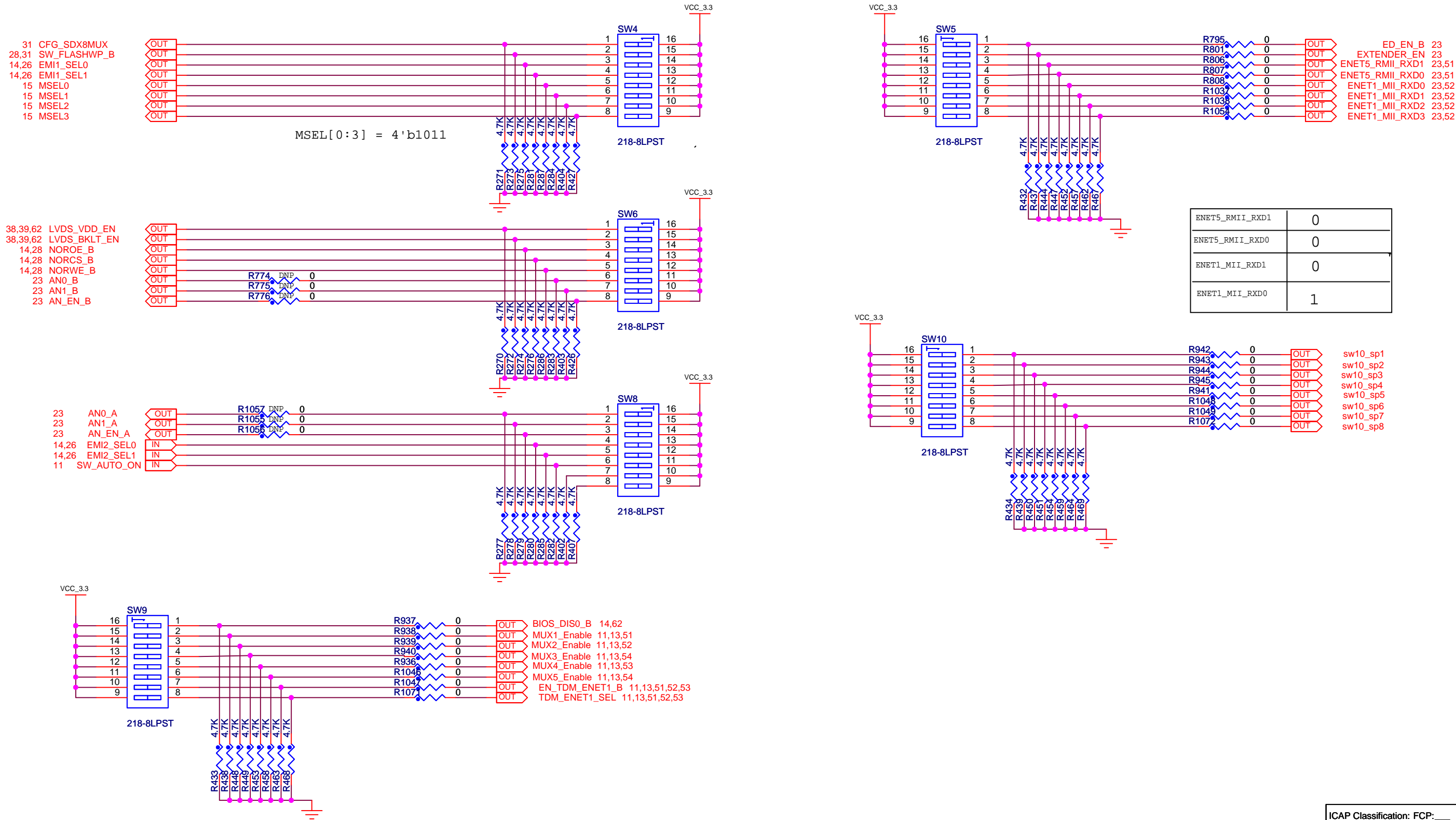
EP3C16F484C8

1588 INTERFACE





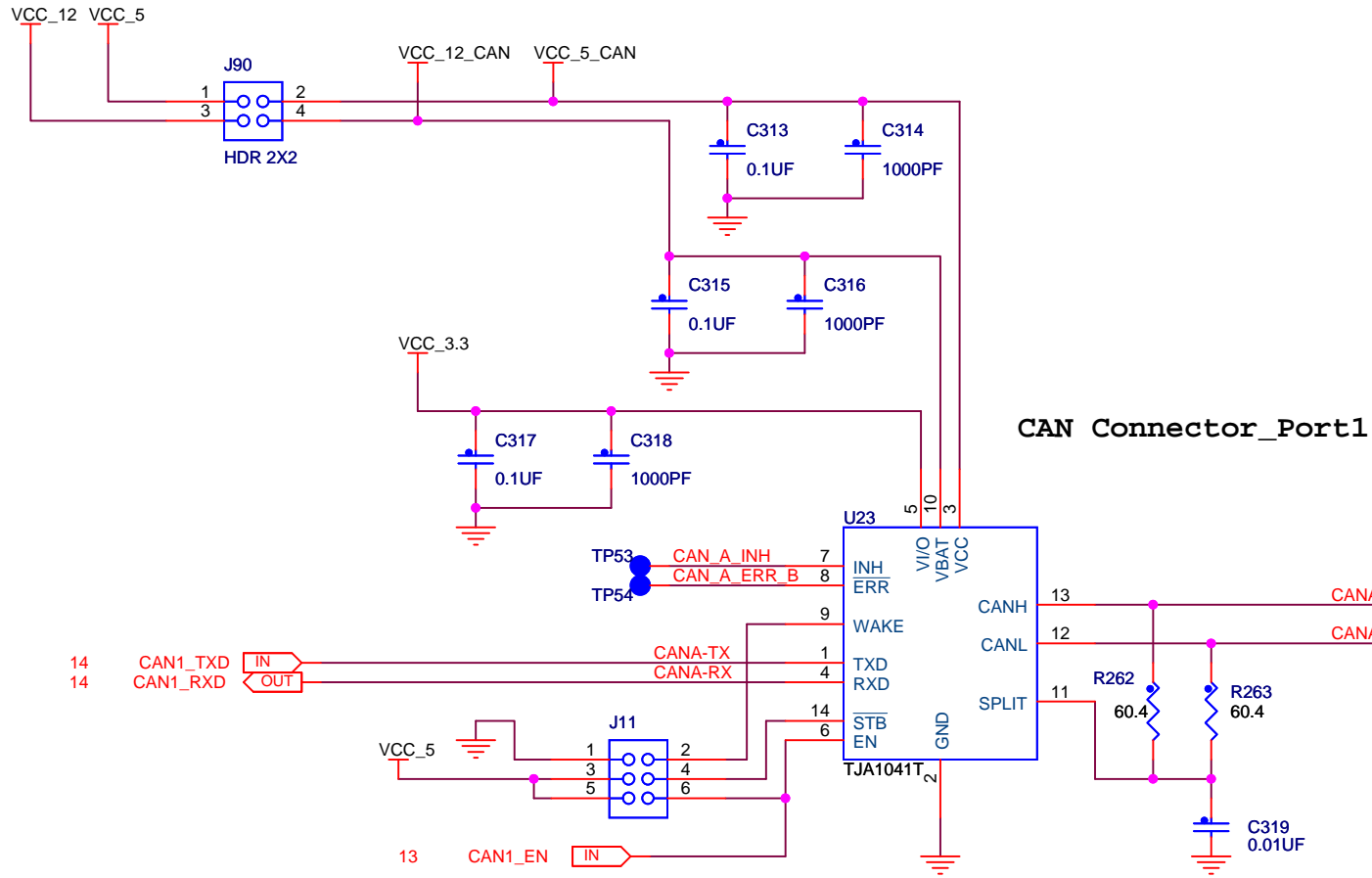
CONFIGURATION SWITCHES



ENET5_RMII_RXD1	0
ENET5_RMII_RXD0	0
ENET1_MII_RXD1	0
ENET1_MII_RXD0	1

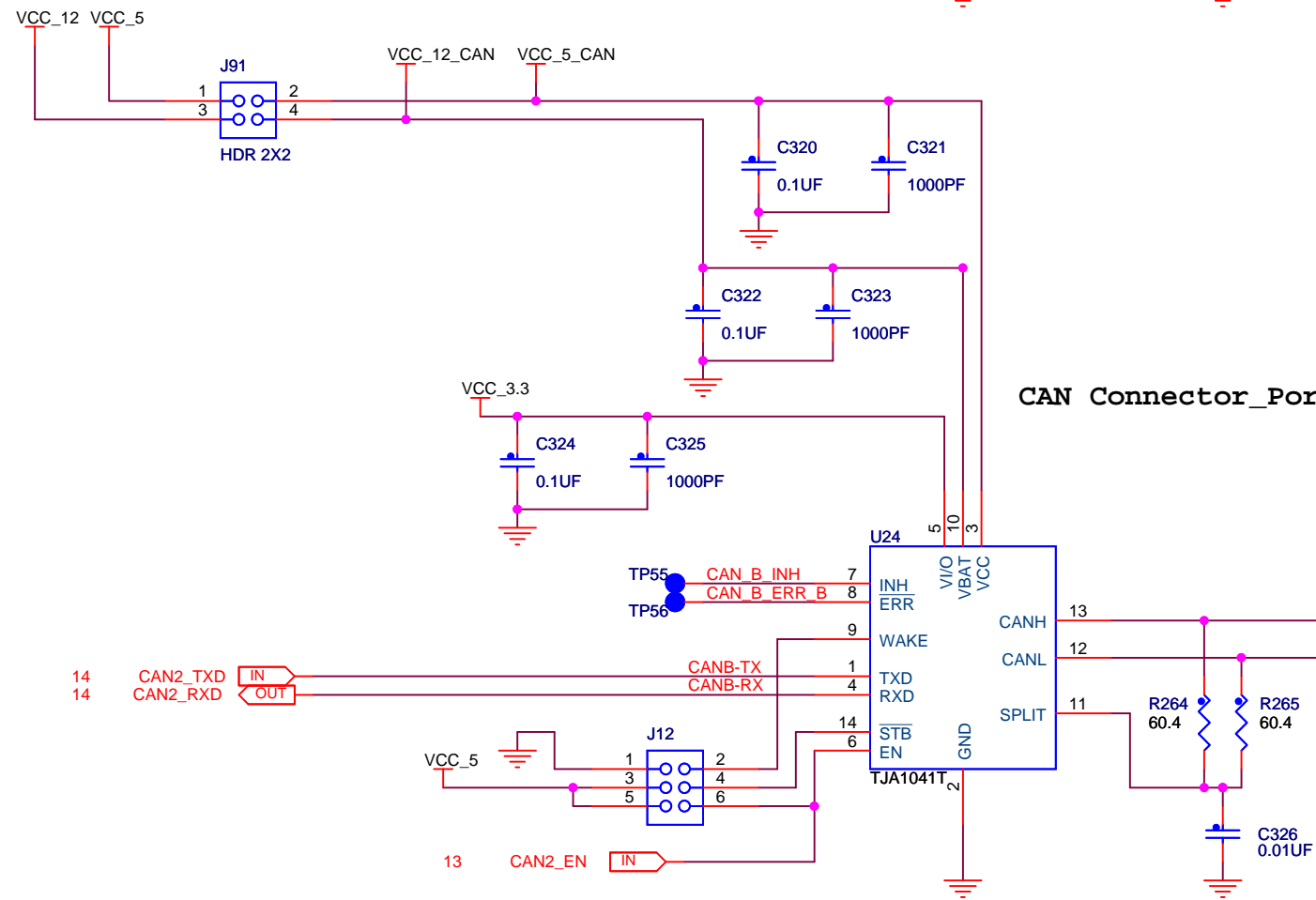
sw10_sp1	0
sw10_sp2	0
sw10_sp3	0
sw10_sp4	0
sw10_sp5	0
sw10_sp6	0
sw10_sp7	0
sw10_sp8	0

CANA

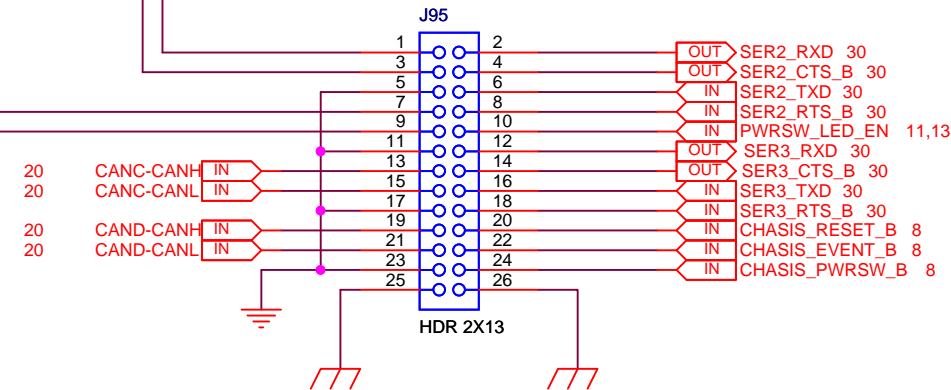


CAN Connector_Port1

CANB

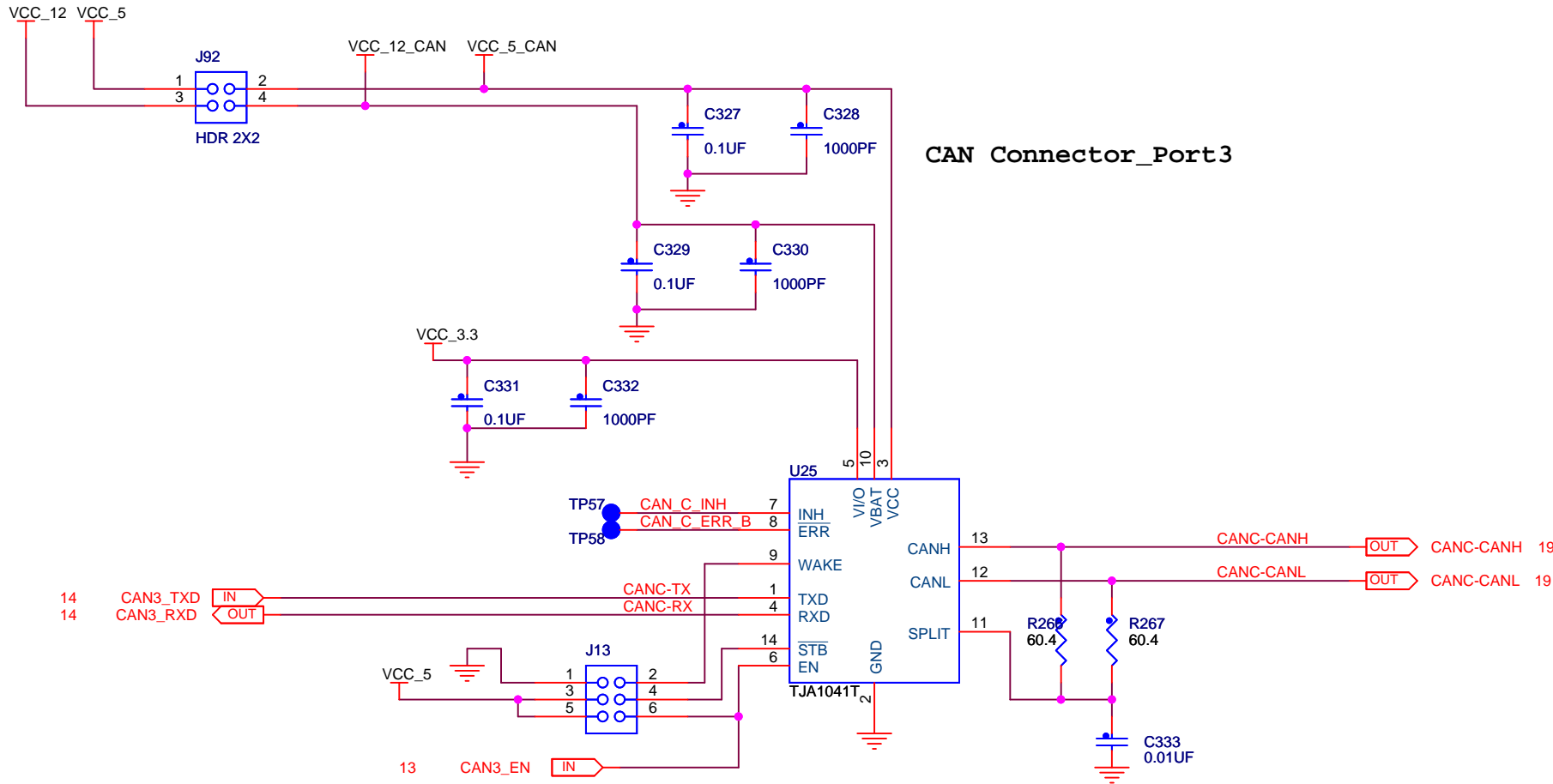


CAN Connector_Port2

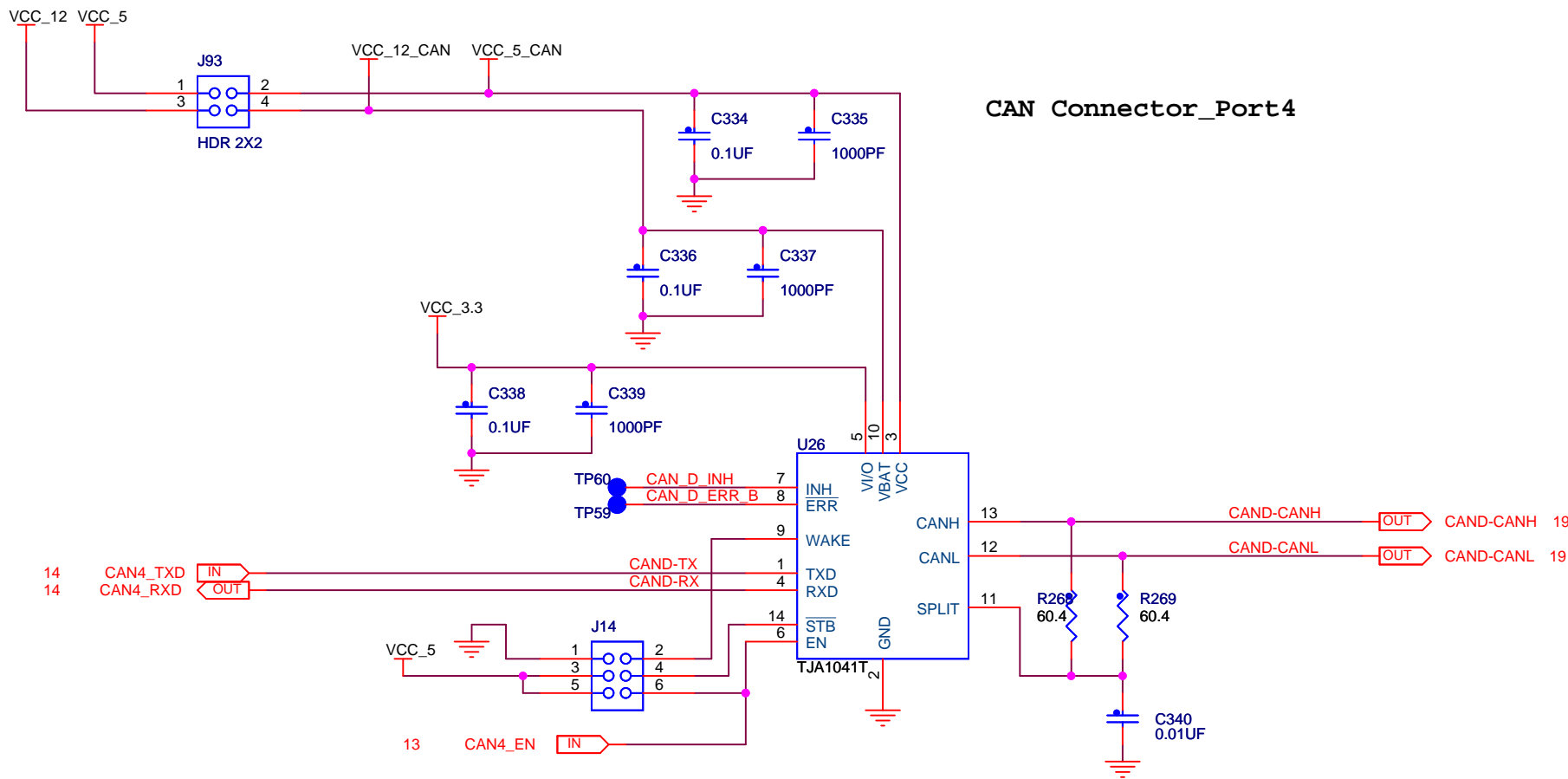


ICAP Classification: FCP:___ FIUO: X PUBL:___

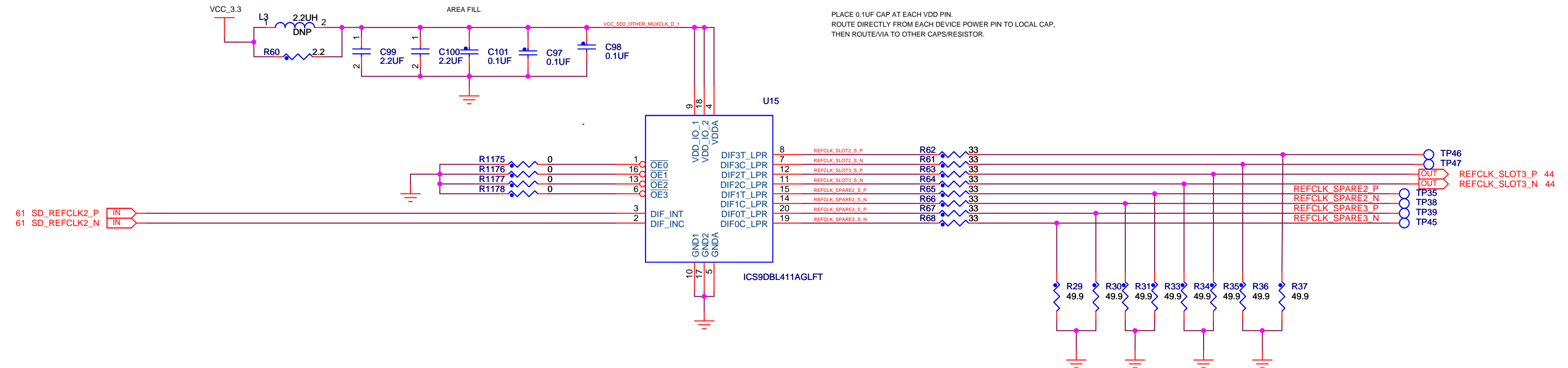
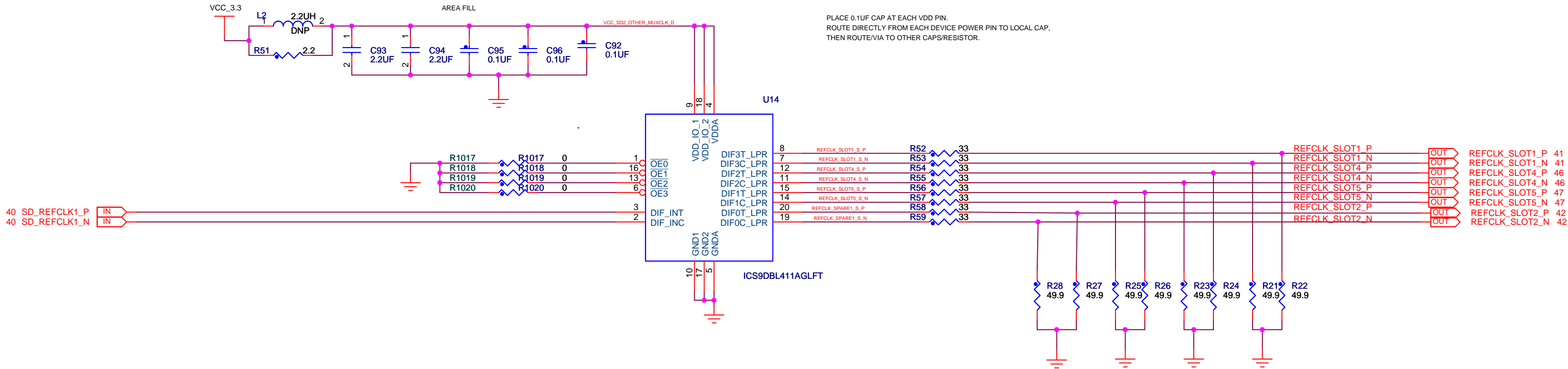
CANC

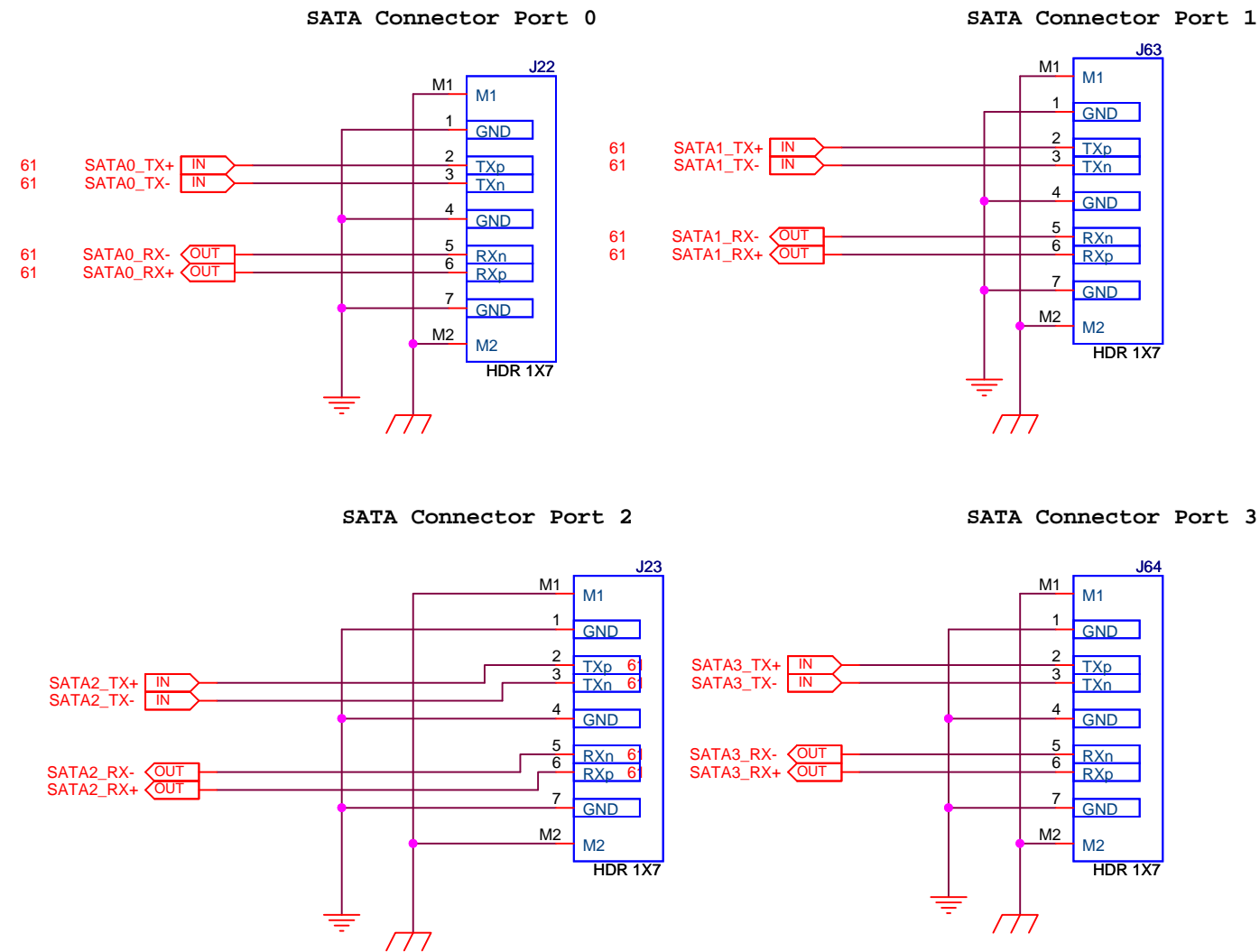


CAND

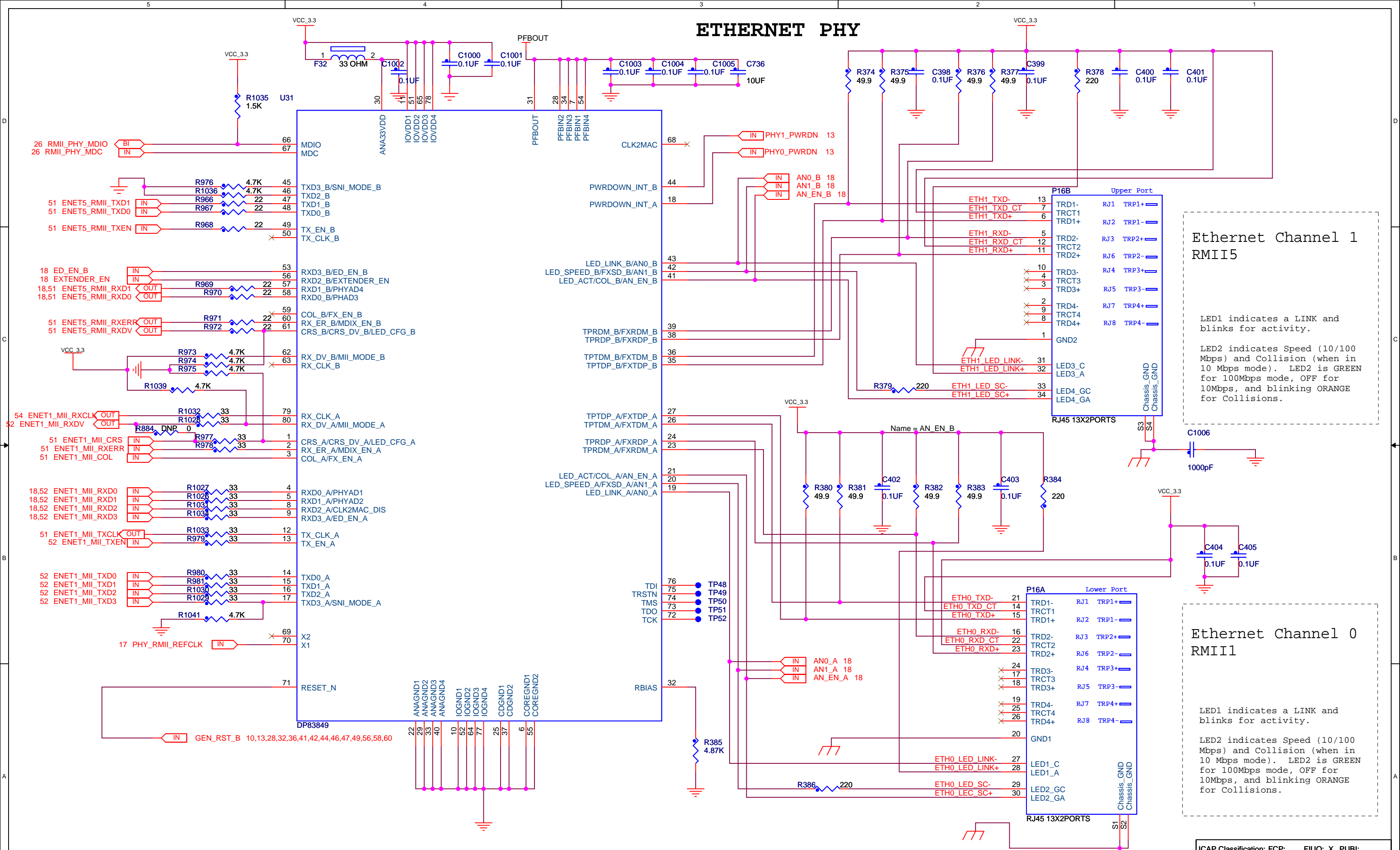


SERDES REFCLK BUFFER





ETHERNET PHY



Ethernet Channel 1
RMII5

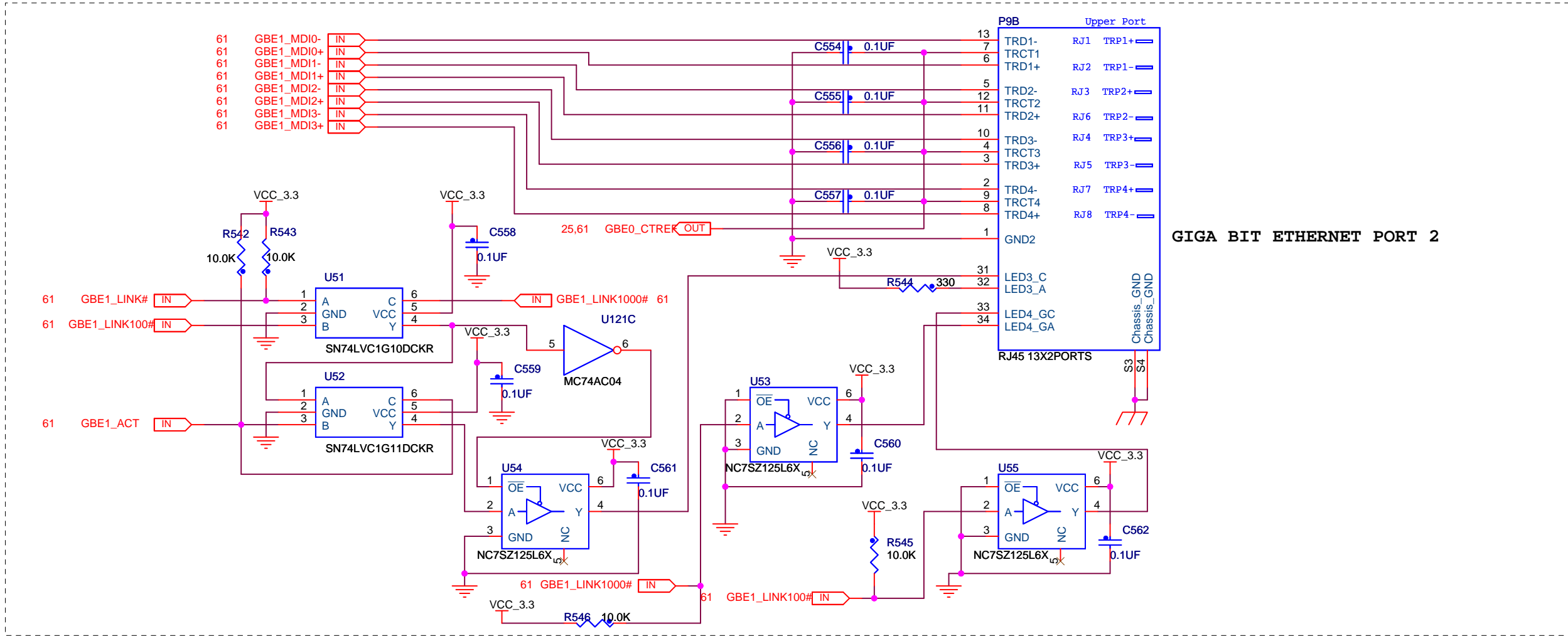
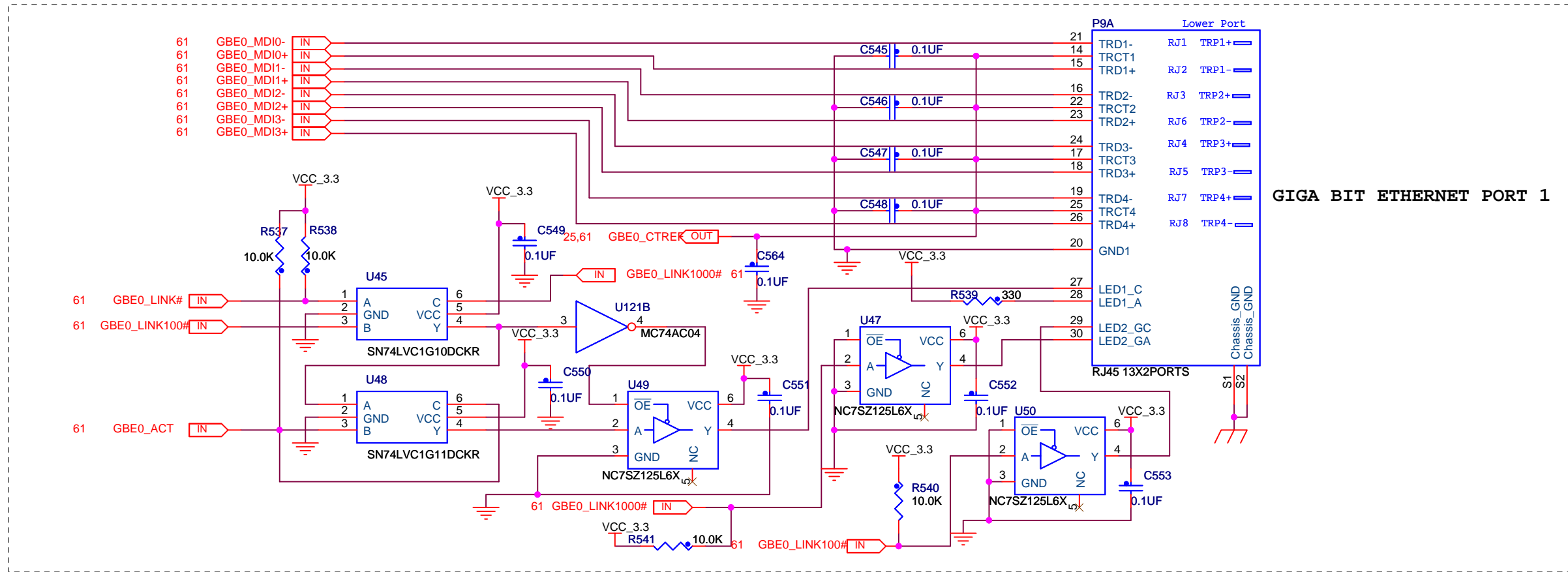
LED1 indicates a LINK and
blinks for activity.

LED2 indicates Speed (10/100
Mbps) and Collision (when in
10 Mbps mode). LED2 is GREEN
for 100Mbps mode, OFF for
10Mbps, and blinking ORANGE
for Collisions.

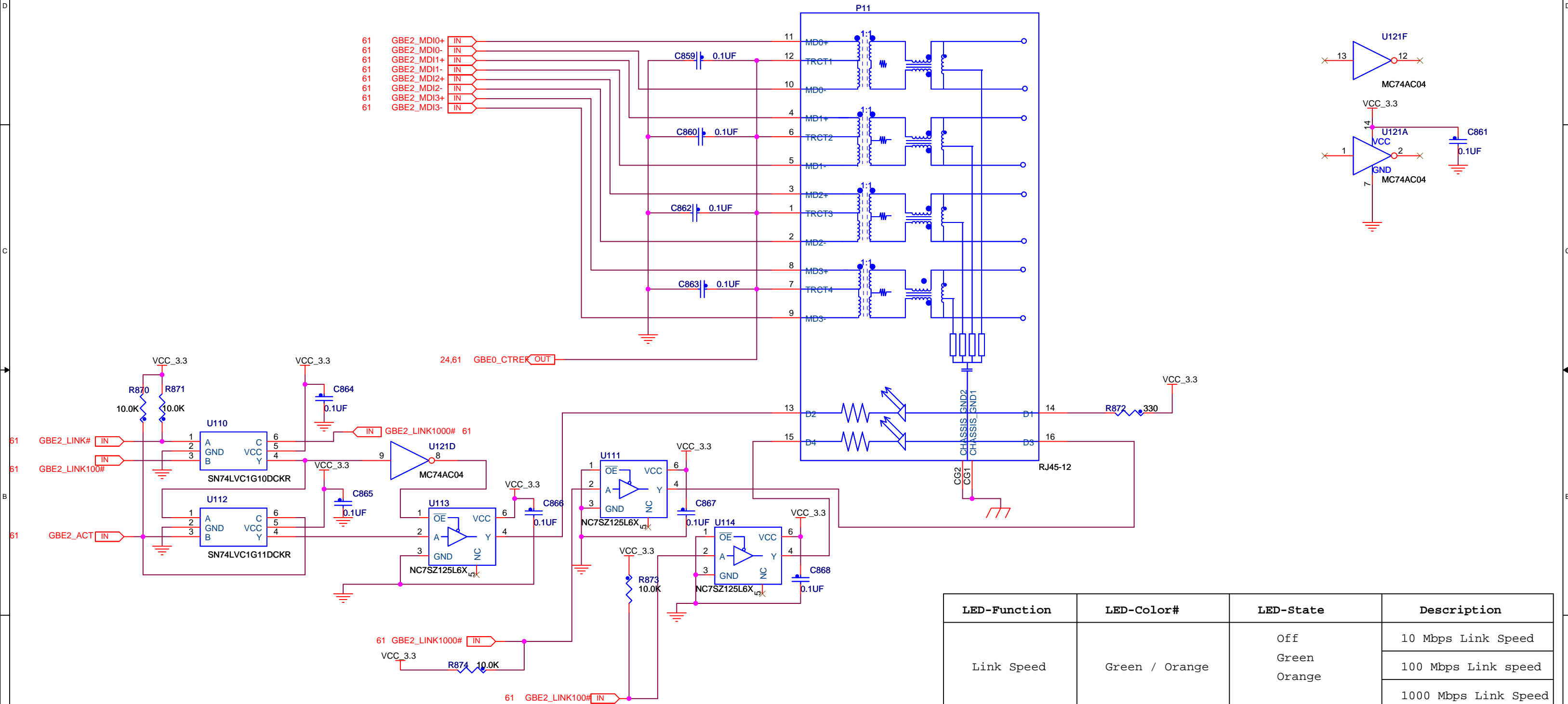
Ethernet Channel 0
RMII1

LED1 indicates a LINK and
blinks for activity.

LED2 indicates Speed (10/100
Mbps) and Collision (when in
10 Mbps mode). LED2 is GREEN
for 100Mbps mode, OFF for
10Mbps, and blinking ORANGE
for Collisions.

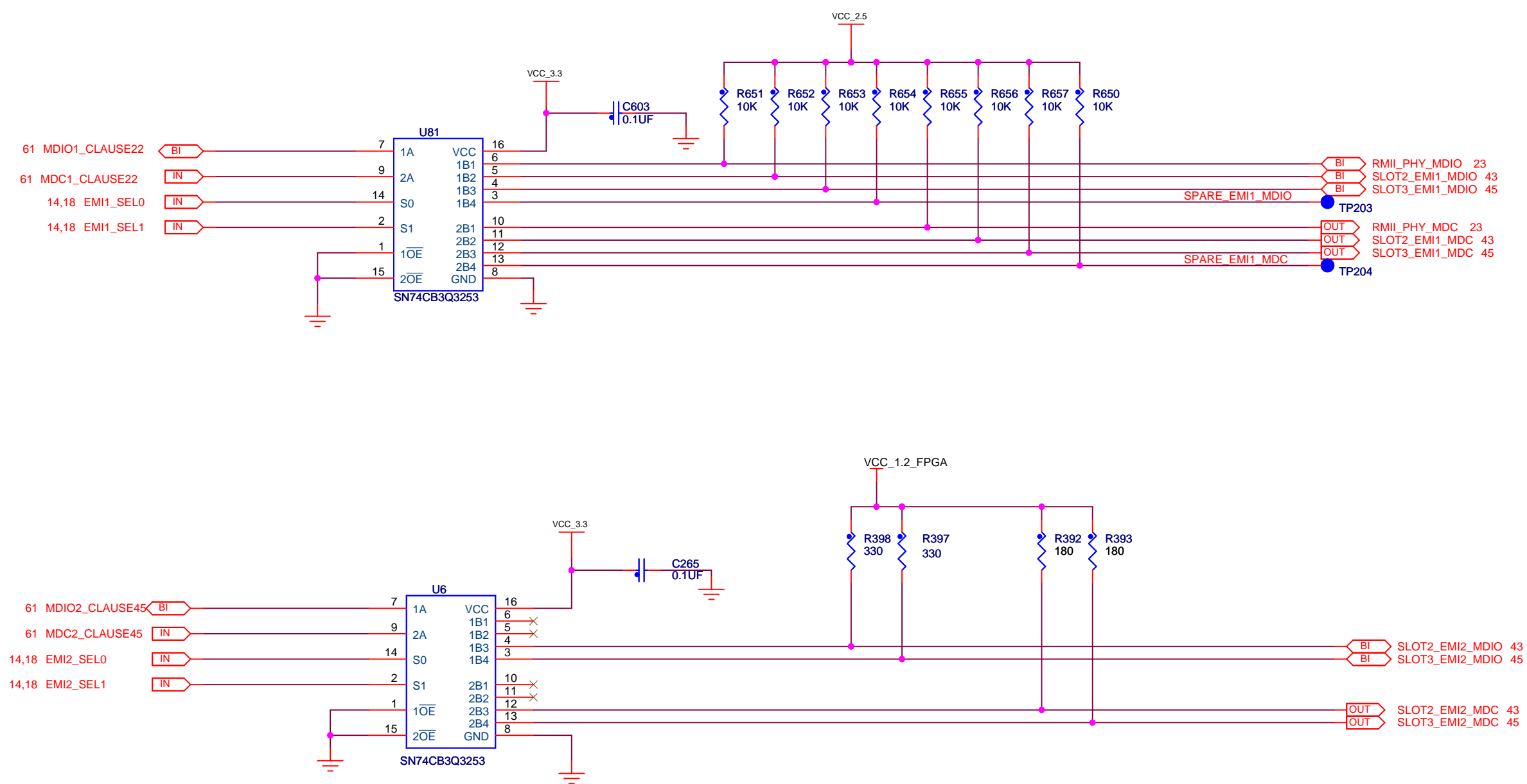


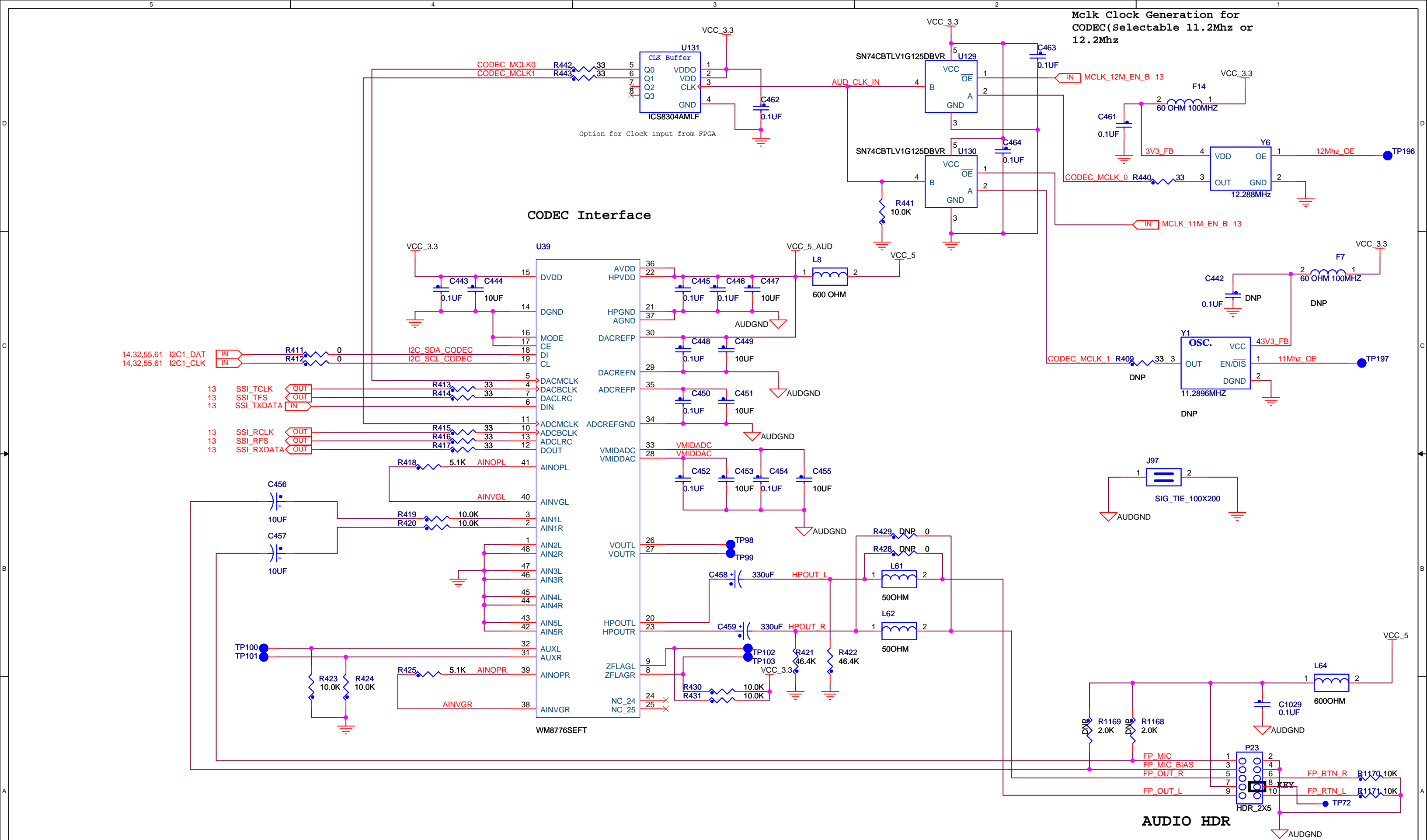
GIGA BIT ETHERNET PORT 3



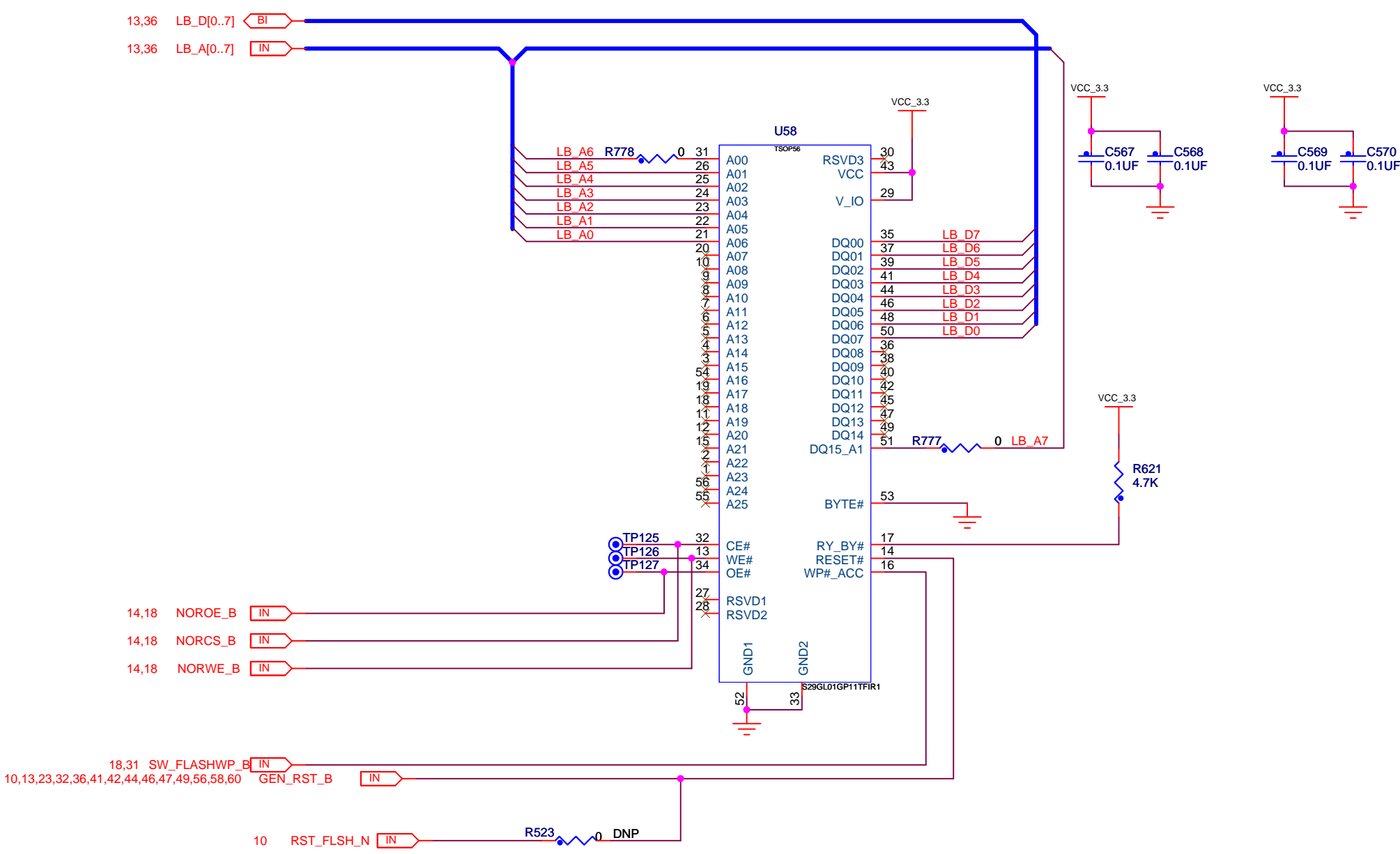
LED-Function	LED-Color#	LED-State	Description
Link Speed	Green / Orange	Off	10 Mbps Link Speed
		Green	100 Mbps Link speed
		Orange	1000 Mbps Link Speed
Link Status & Activity	Yellow	Off	No Link
		Steady On	Link established, No Activity
		Blinking	Link established, Activity

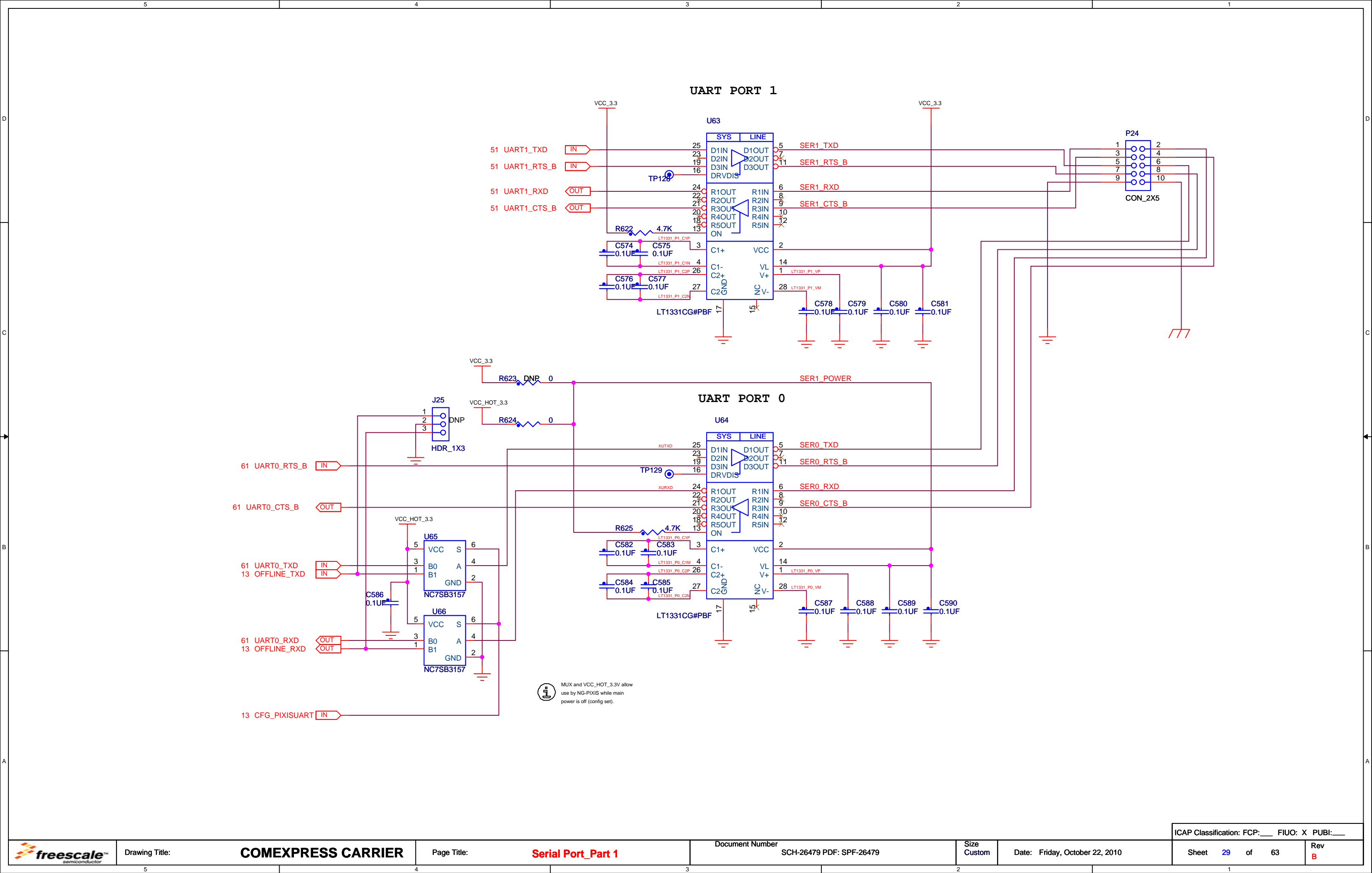
MANAGEMENT BUS MUXING



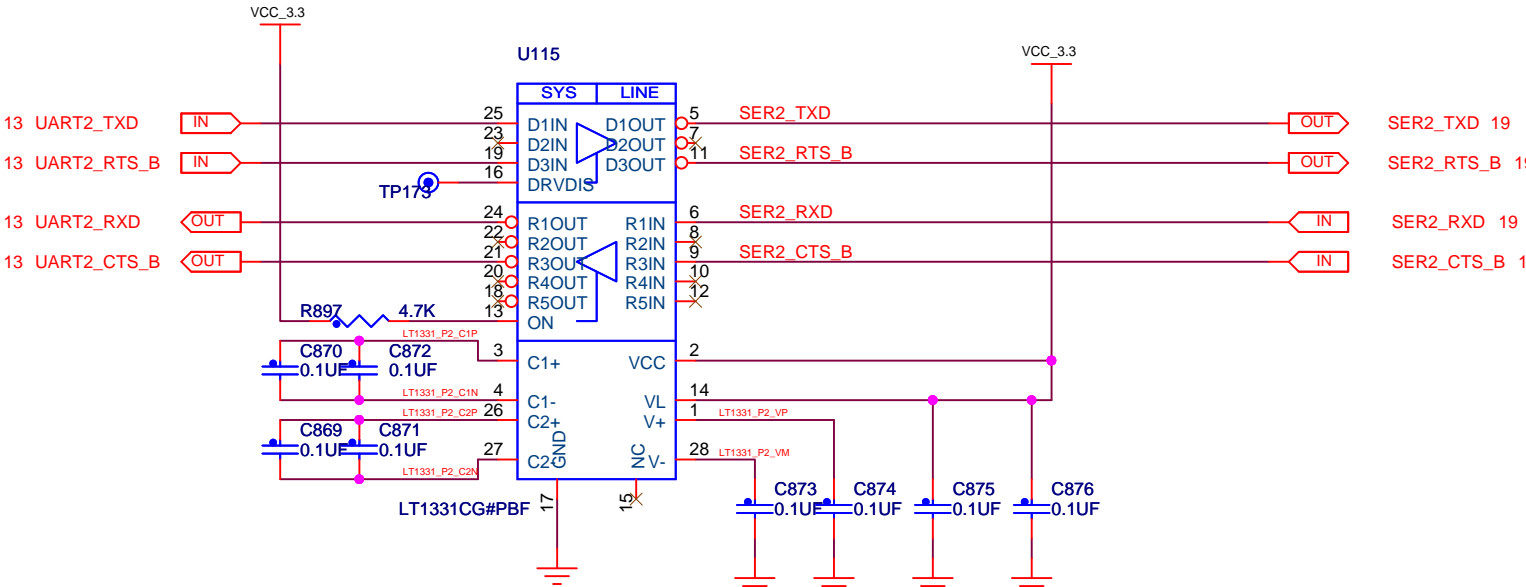


NOR FLASH

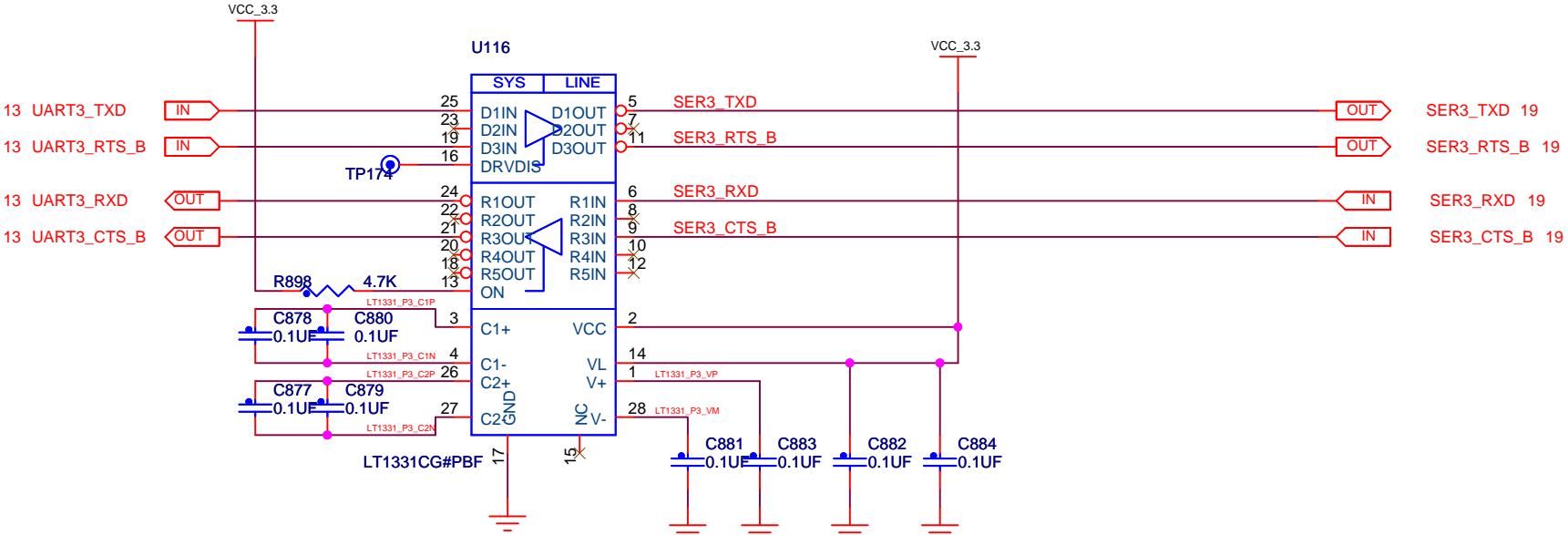




UART Port 2



UART Port :



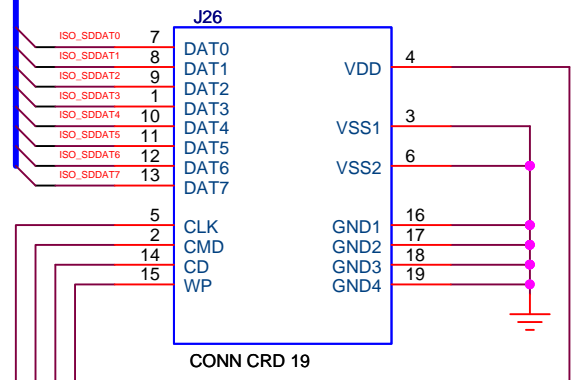
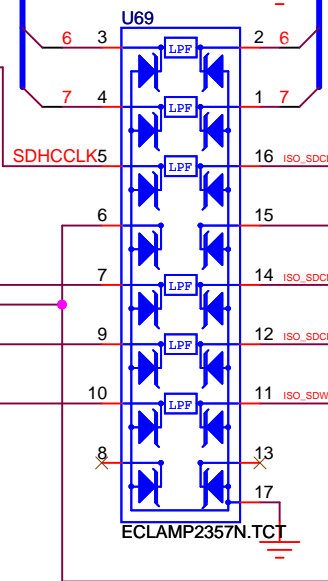
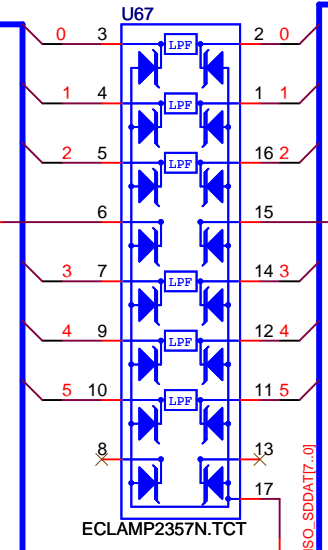
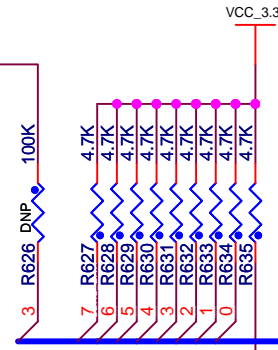
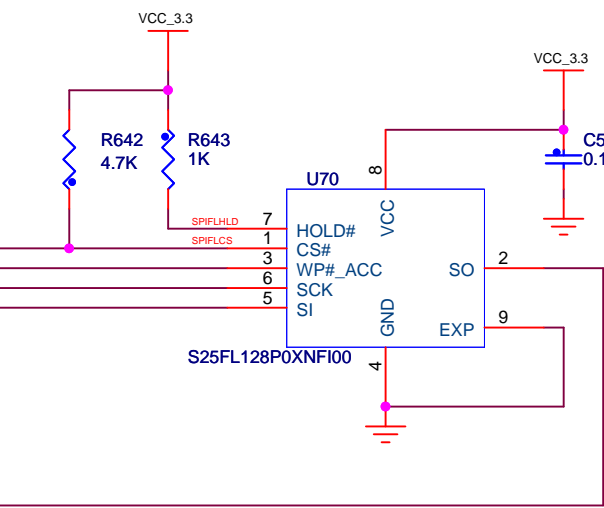
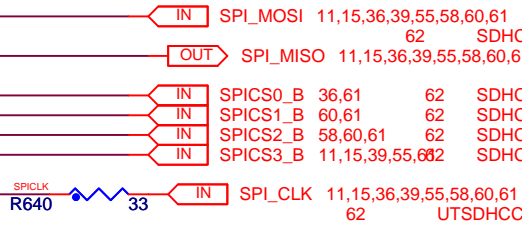
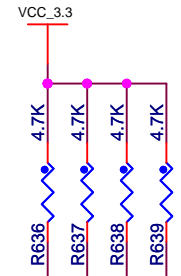
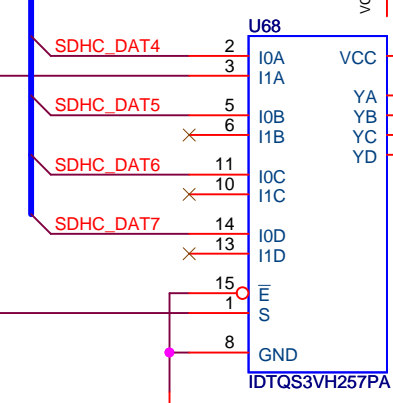
IIC3_SCL and IIC3_SDA P4080 = SDHC
CD and WP, resp.

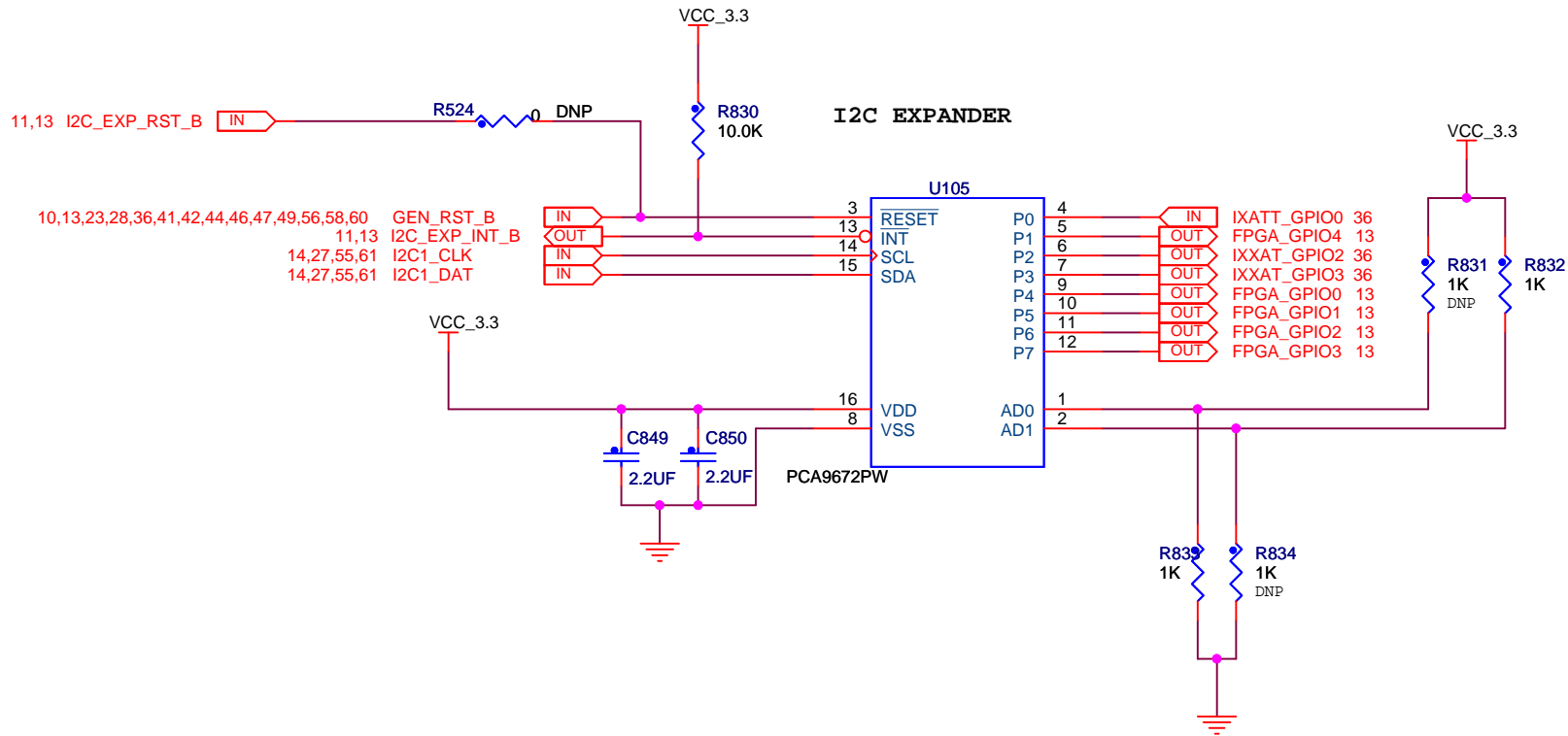
SD_DAT3 = Card Detect
Populate pulldown for MMC
but populate pullup for
SDHC Mode.

62 SDHC_CD_B OUT
62 SDHC_WP_B OUT

18 CFG_SDx8MUX IN

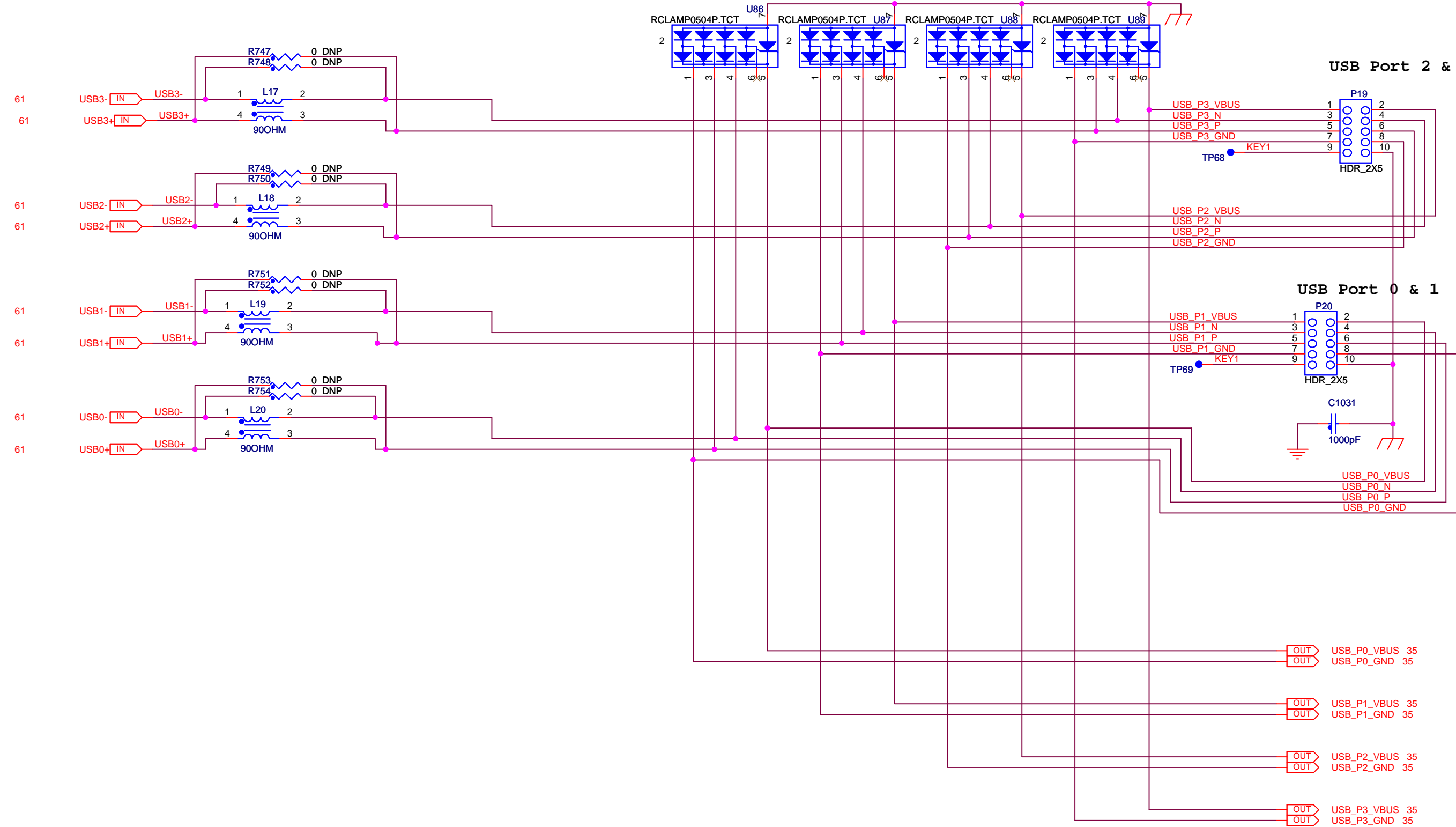
18,28 SW_FLASHWP_B IN



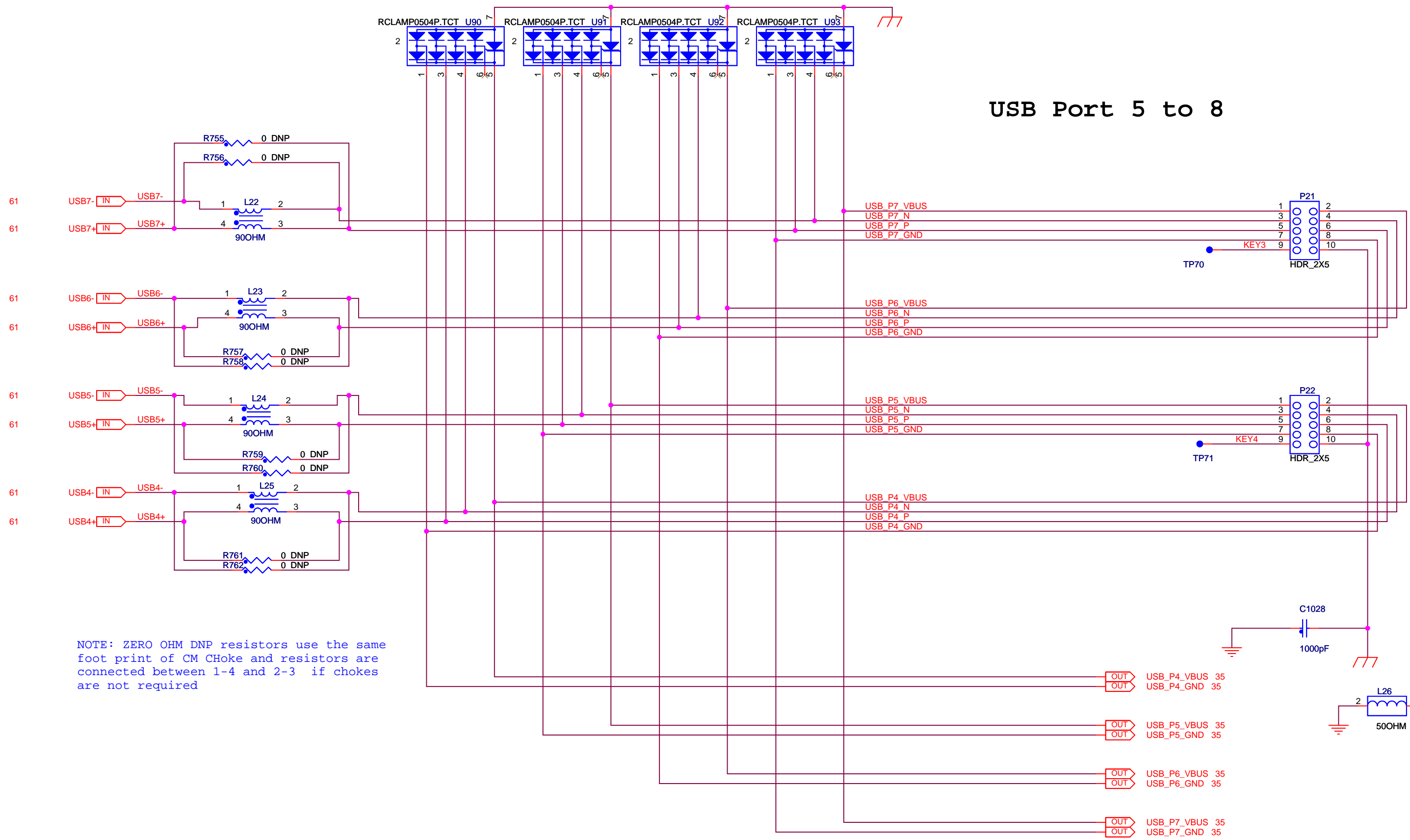


USB PORTS 1 to 4

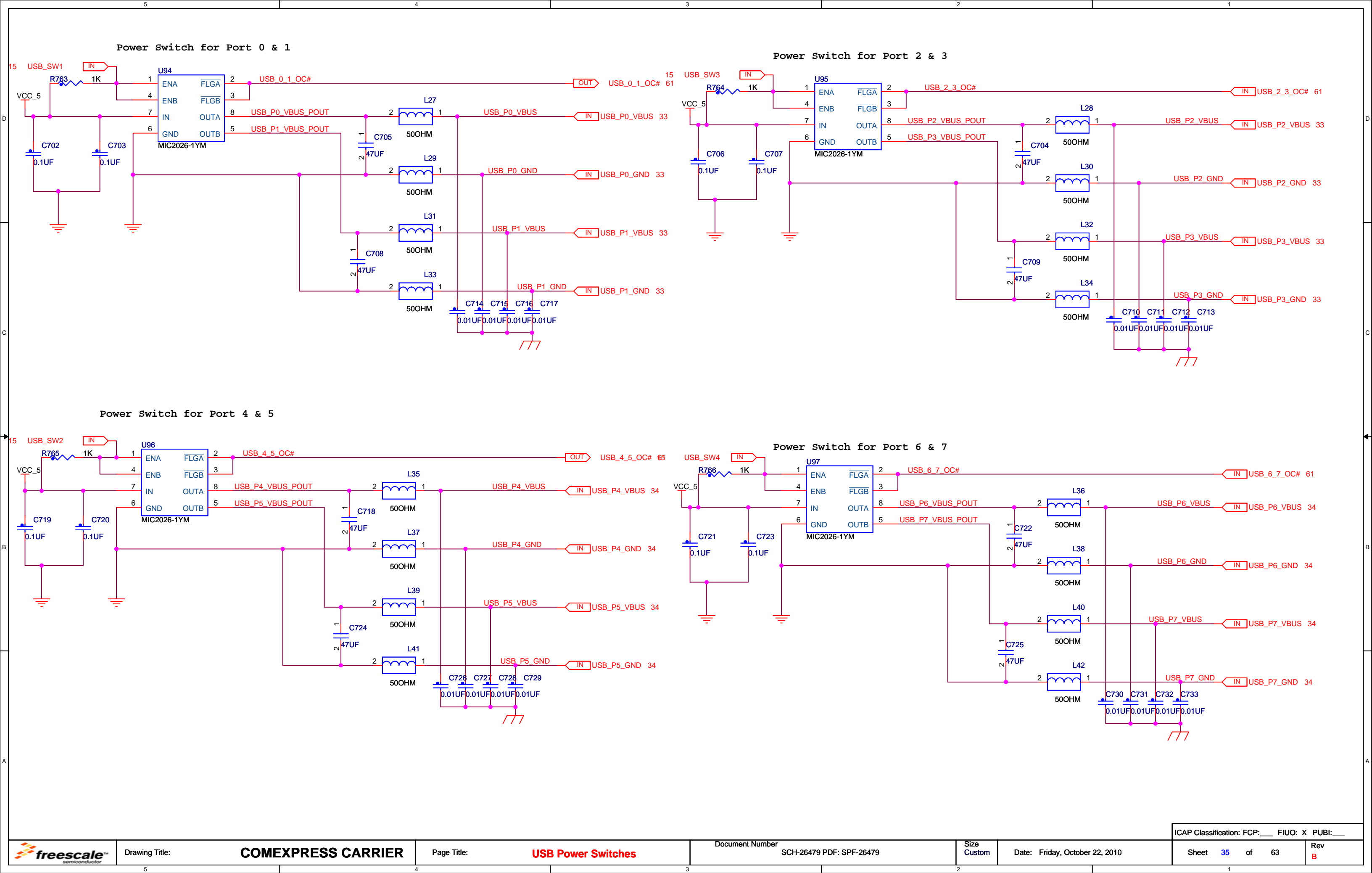
NOTE: ZERO OHM DNP resistors use the same foot print of CM Choke and resistors are connected between 1-4 and 2-3 if chokes are not required

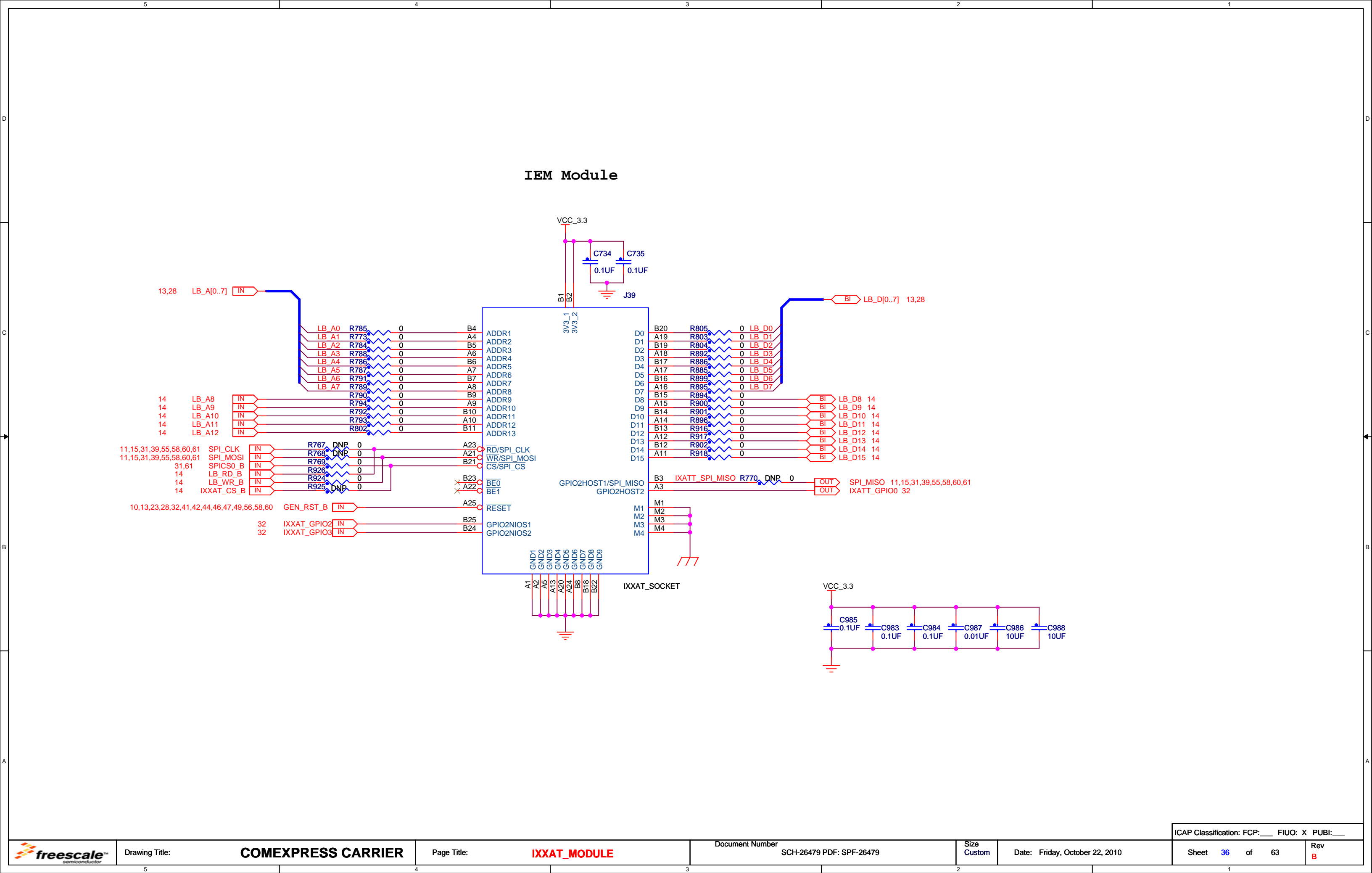


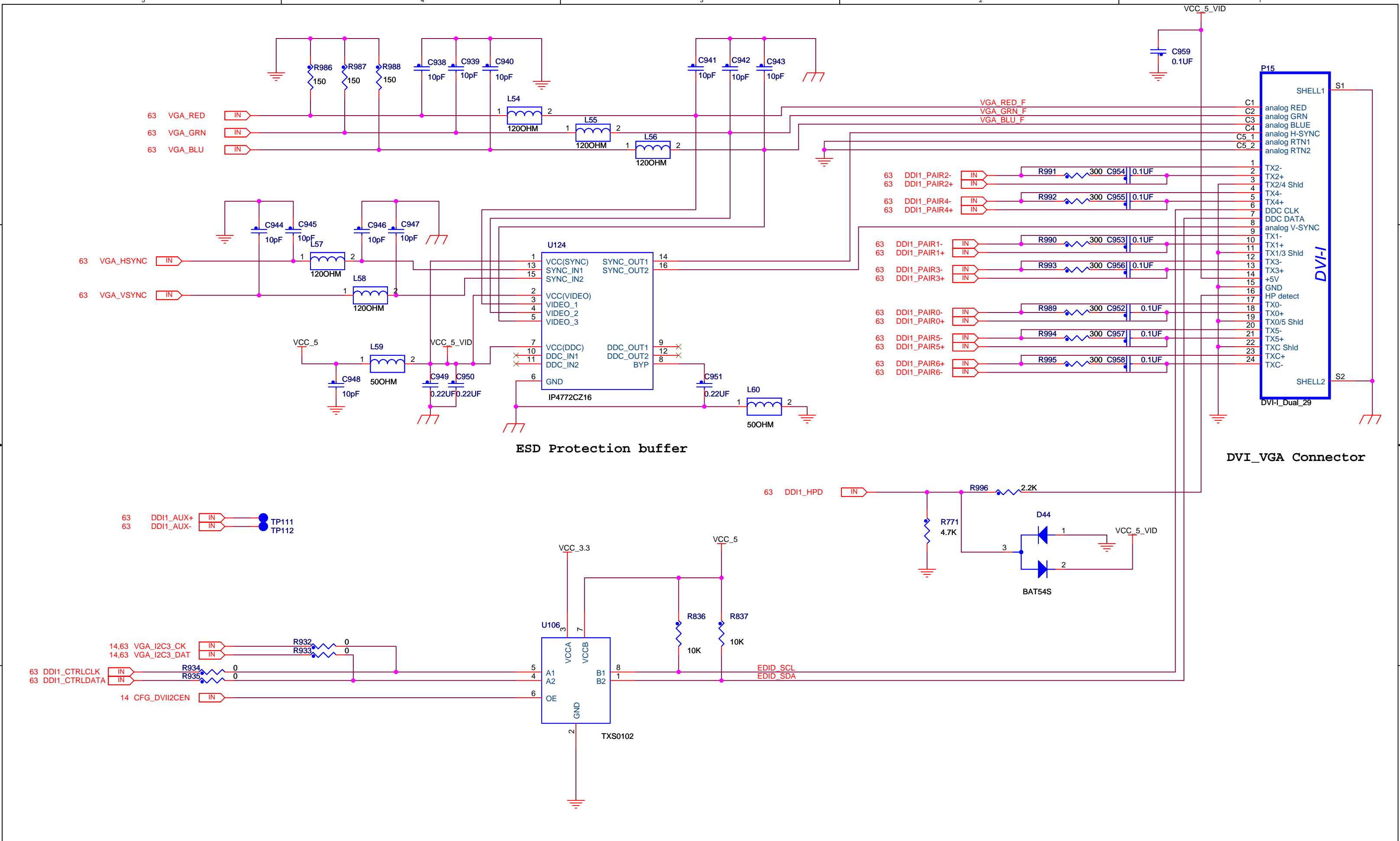
USB Port 5 to 8

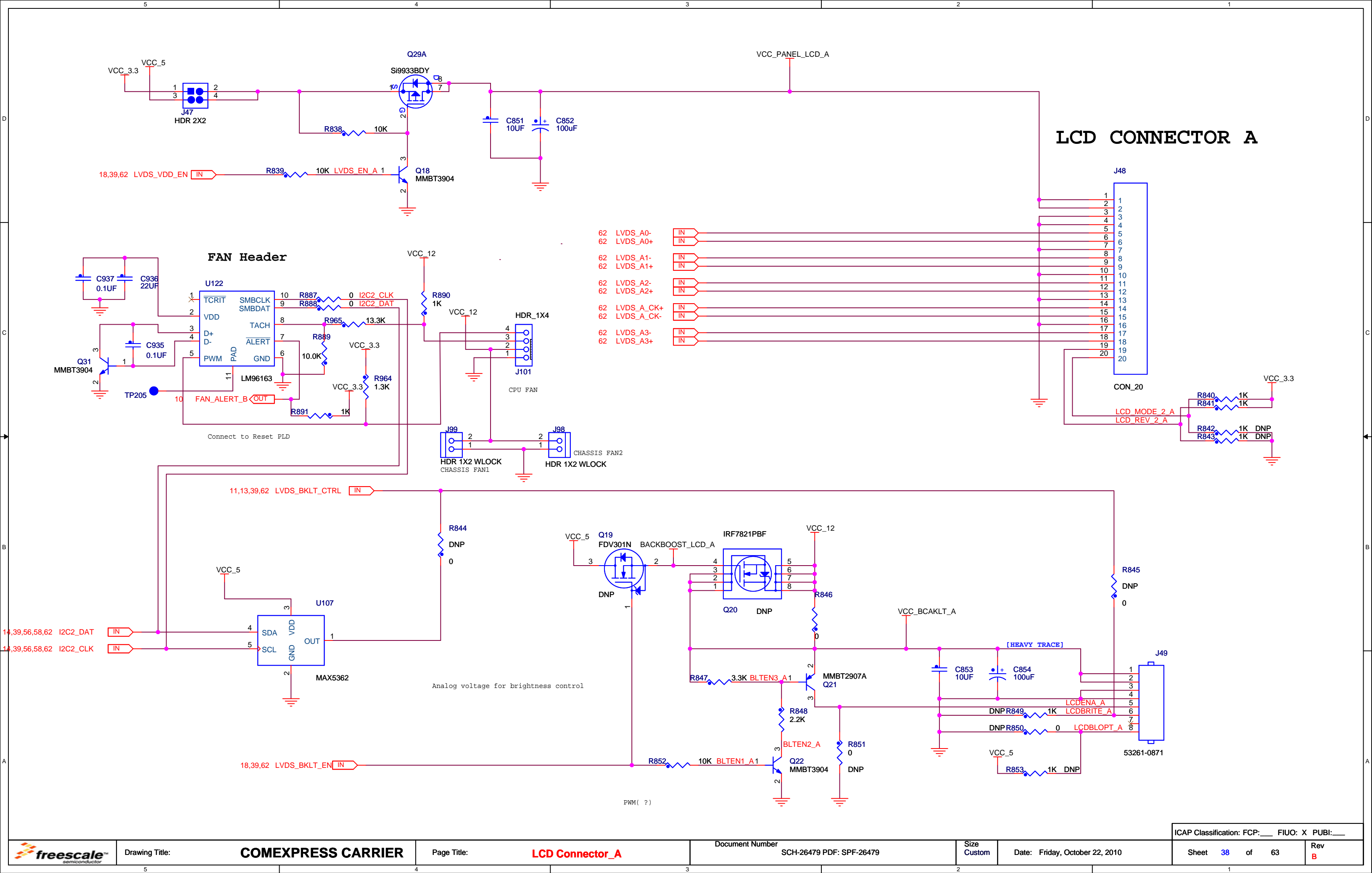


NOTE: ZERO OHM DNP resistors use the same foot print of CM CHoke and resistors are connected between 1-4 and 2-3 if chokes are not required

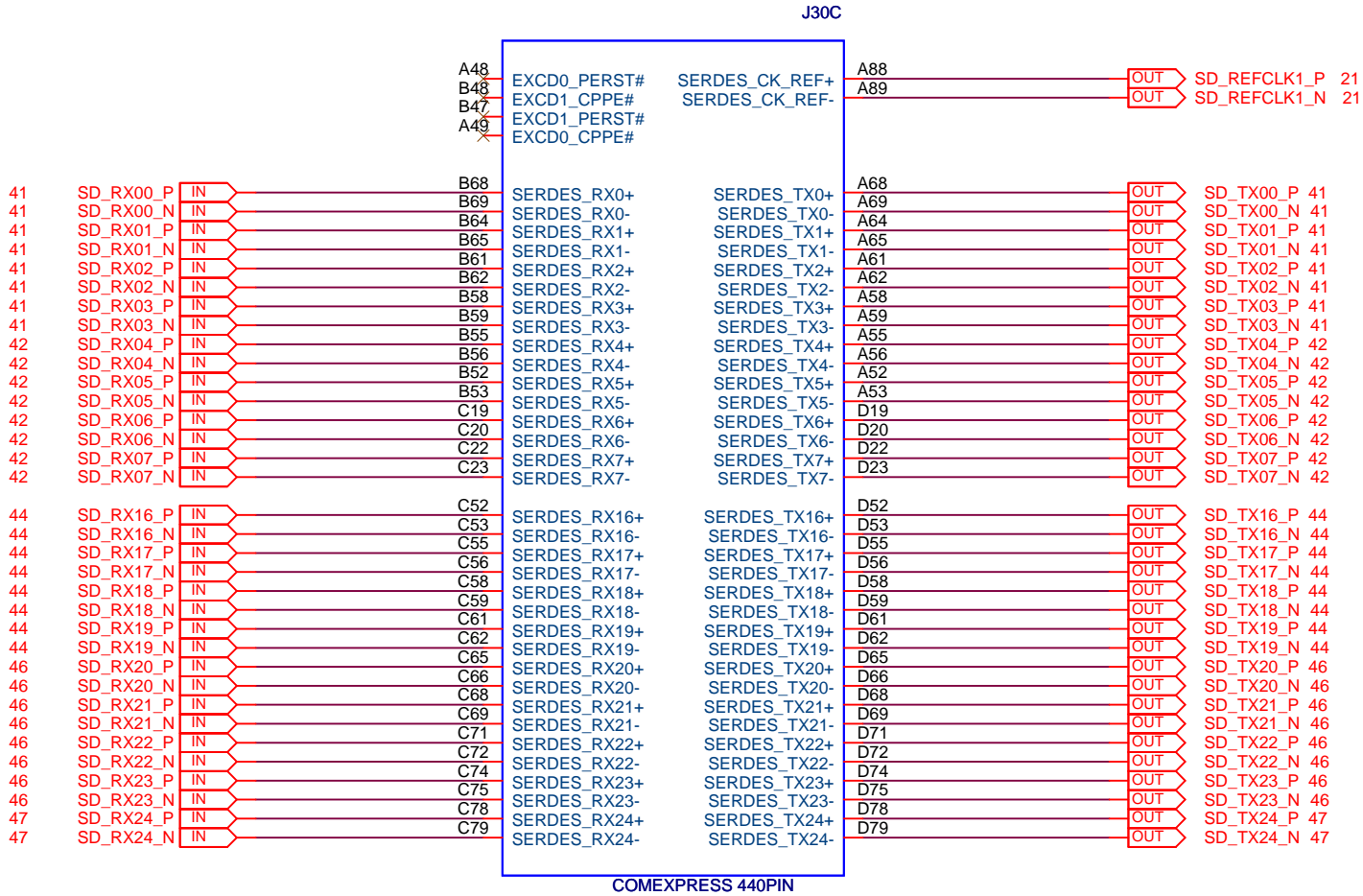








SERDES - COMe CONNECTOR



Drawing Title:

COMEXPRESS CARRIER

Page Title:

P4080 SERDES

Document Number

SCH-26479 PDF: SPF-26479

Size
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Date: Friday, October 22, 2010

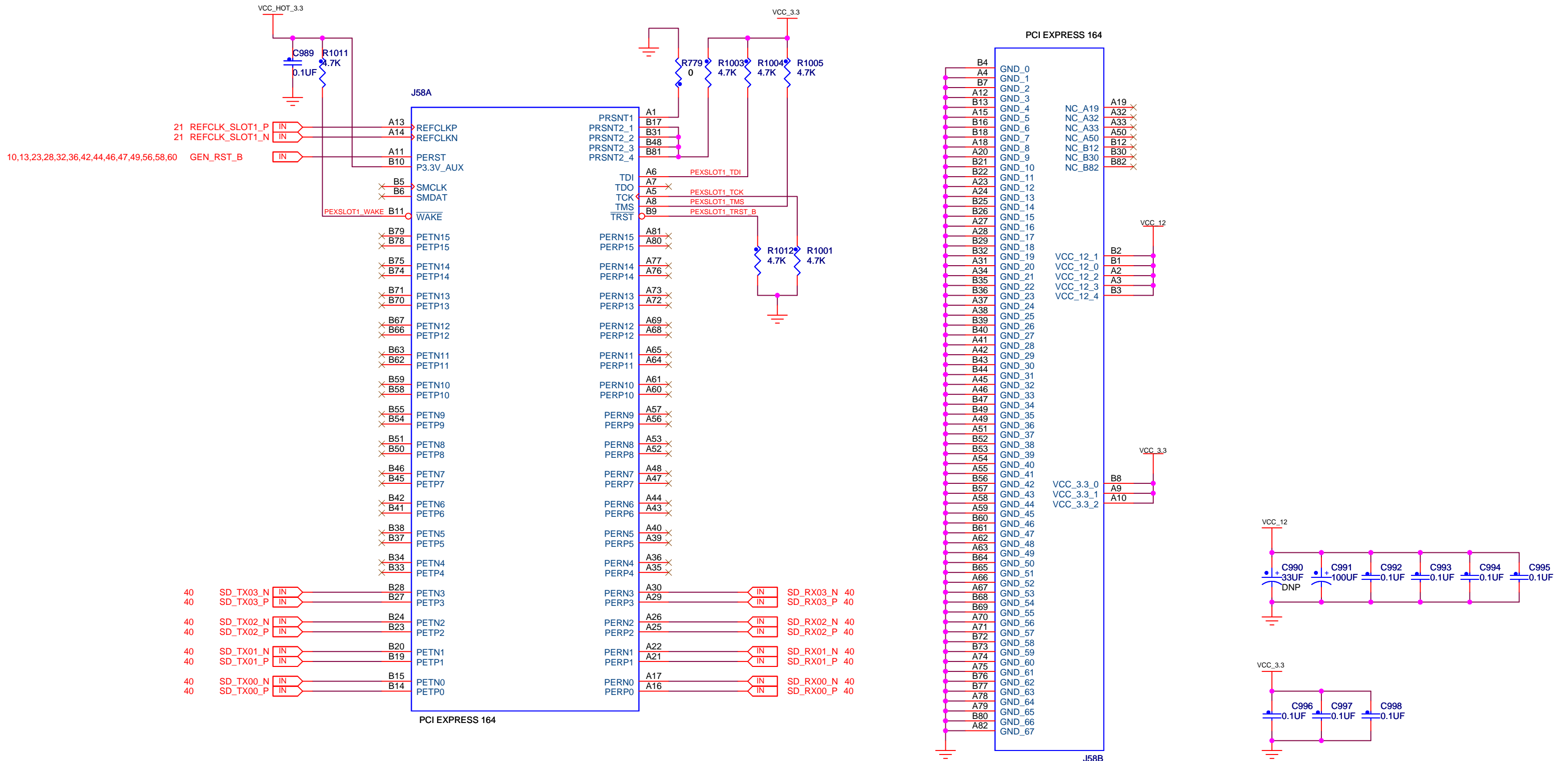
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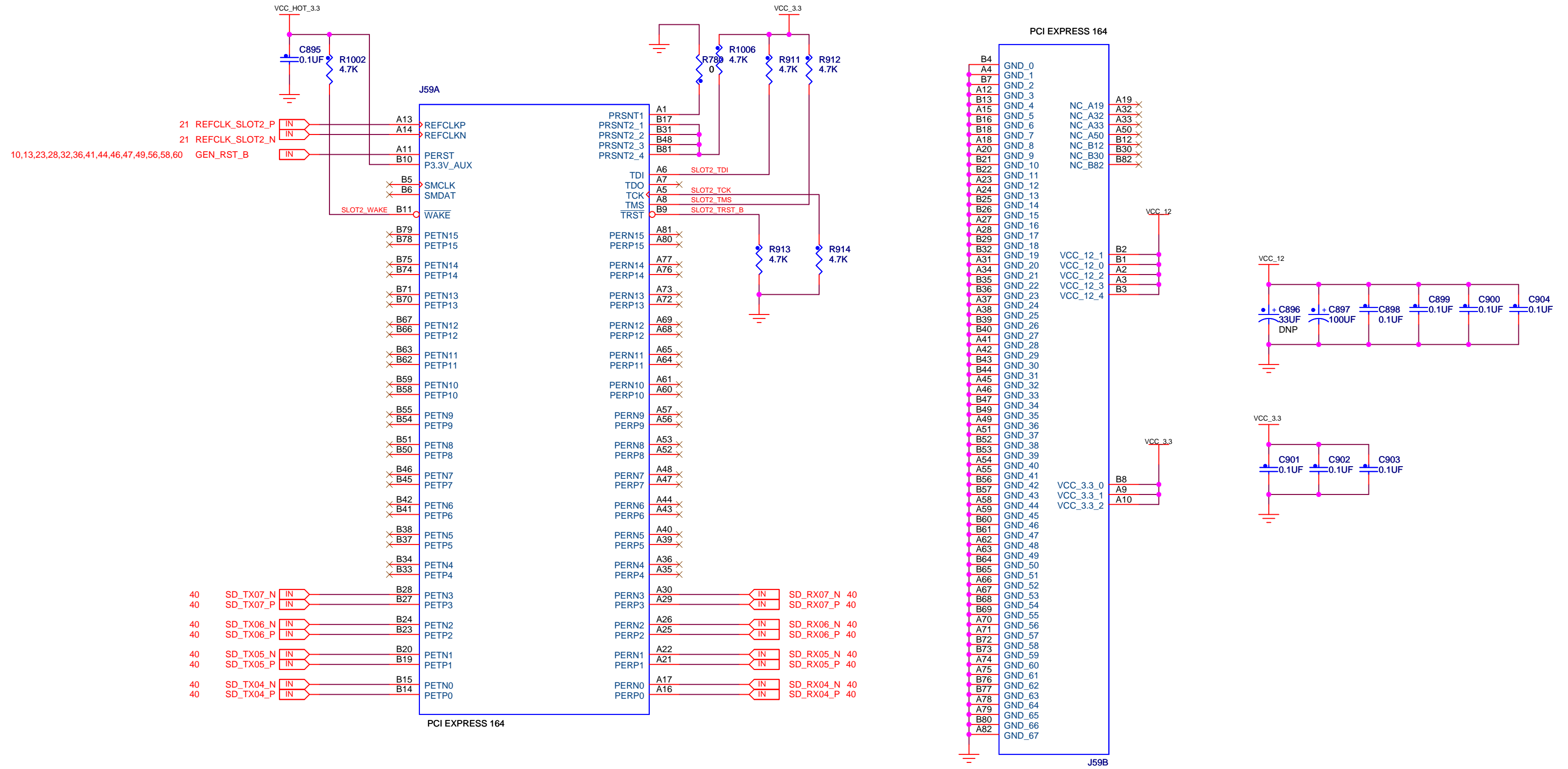
Rev

B

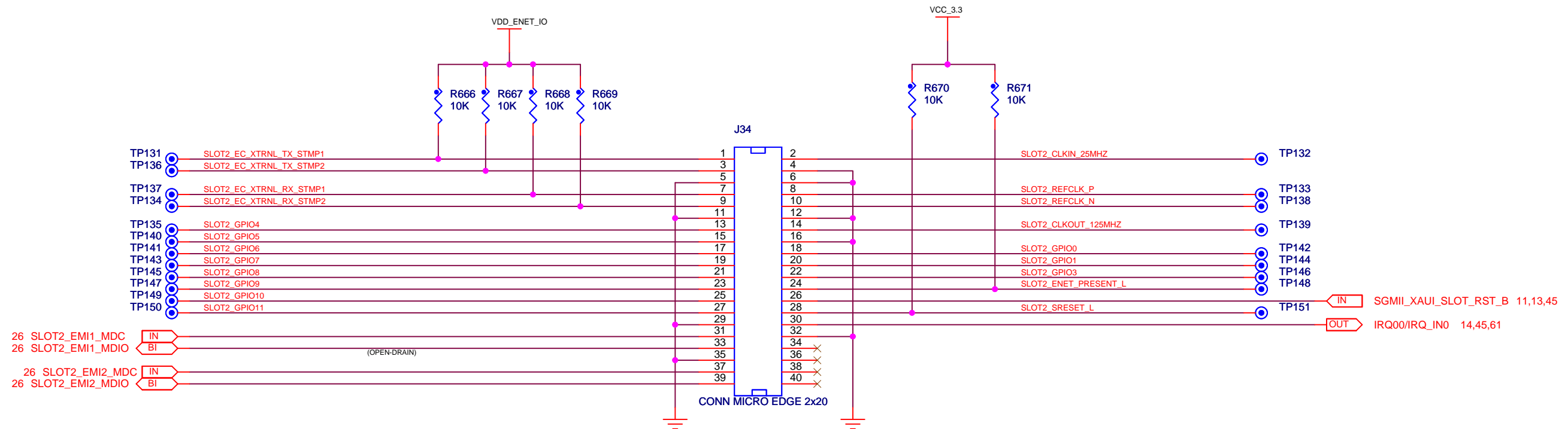
SLOT 1 (PEX/SRIO) CONNECTOR



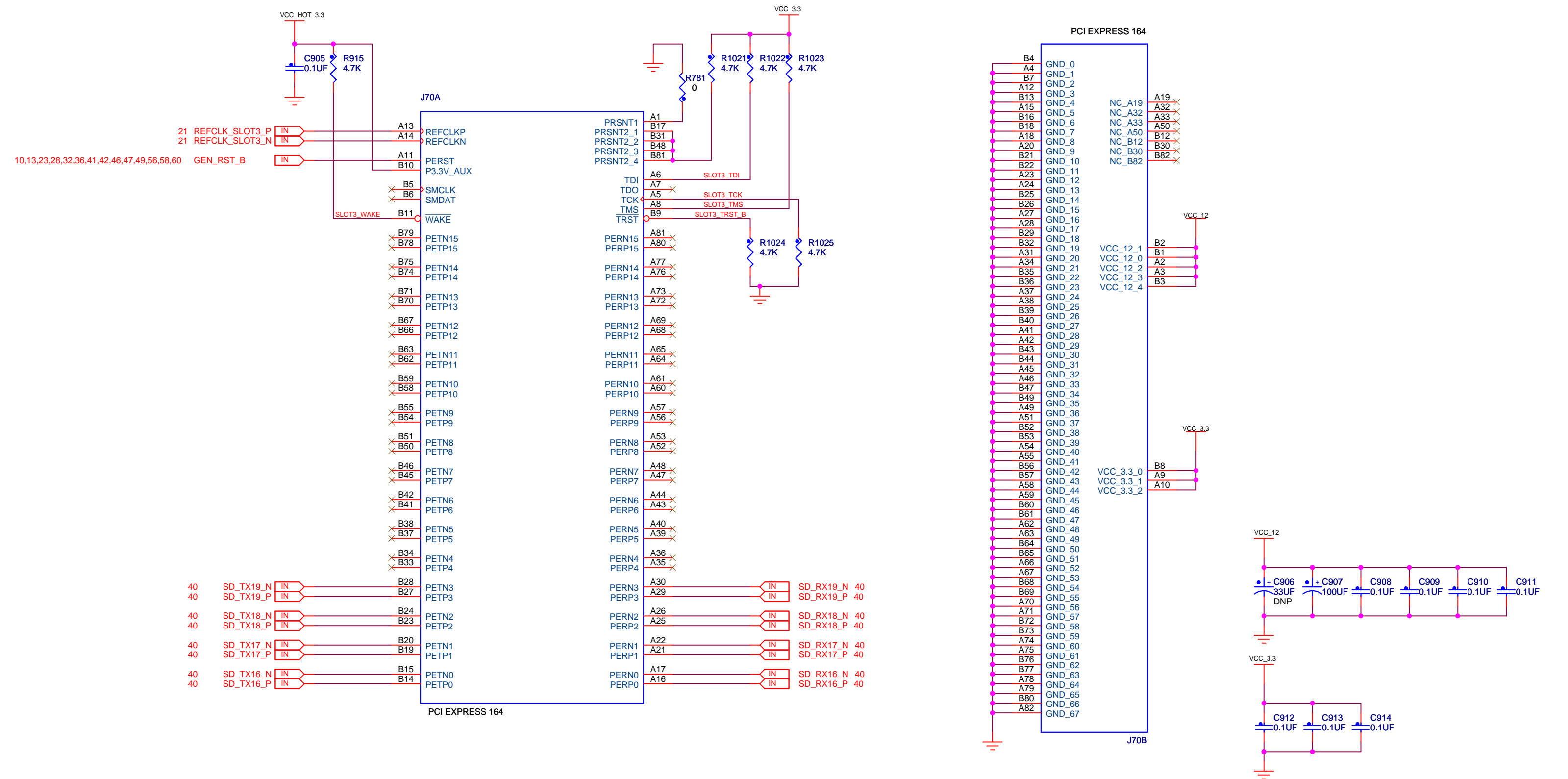
SLOT 2 (PEX/SRIO/SGMII) MAIN (PART 1 OF 2) CONNECTOR



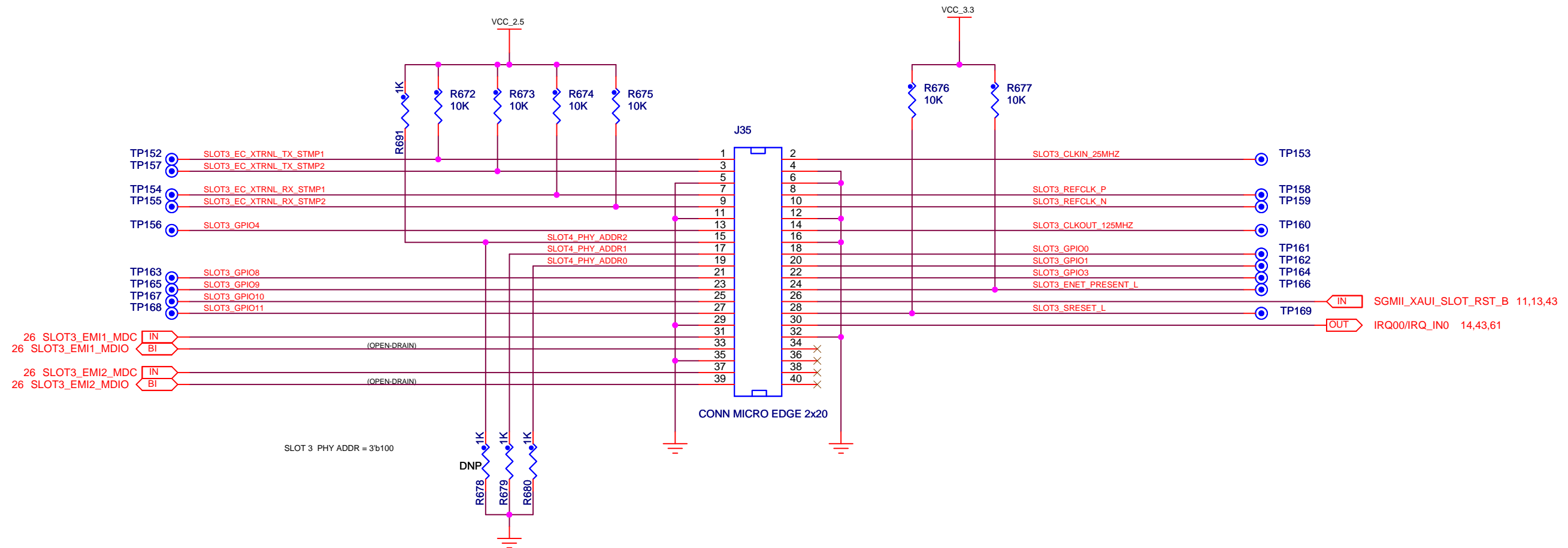
SLOT 2 (PEX/SGMII) SIDEBAND (PART 2 OF 2) CONNECTOR

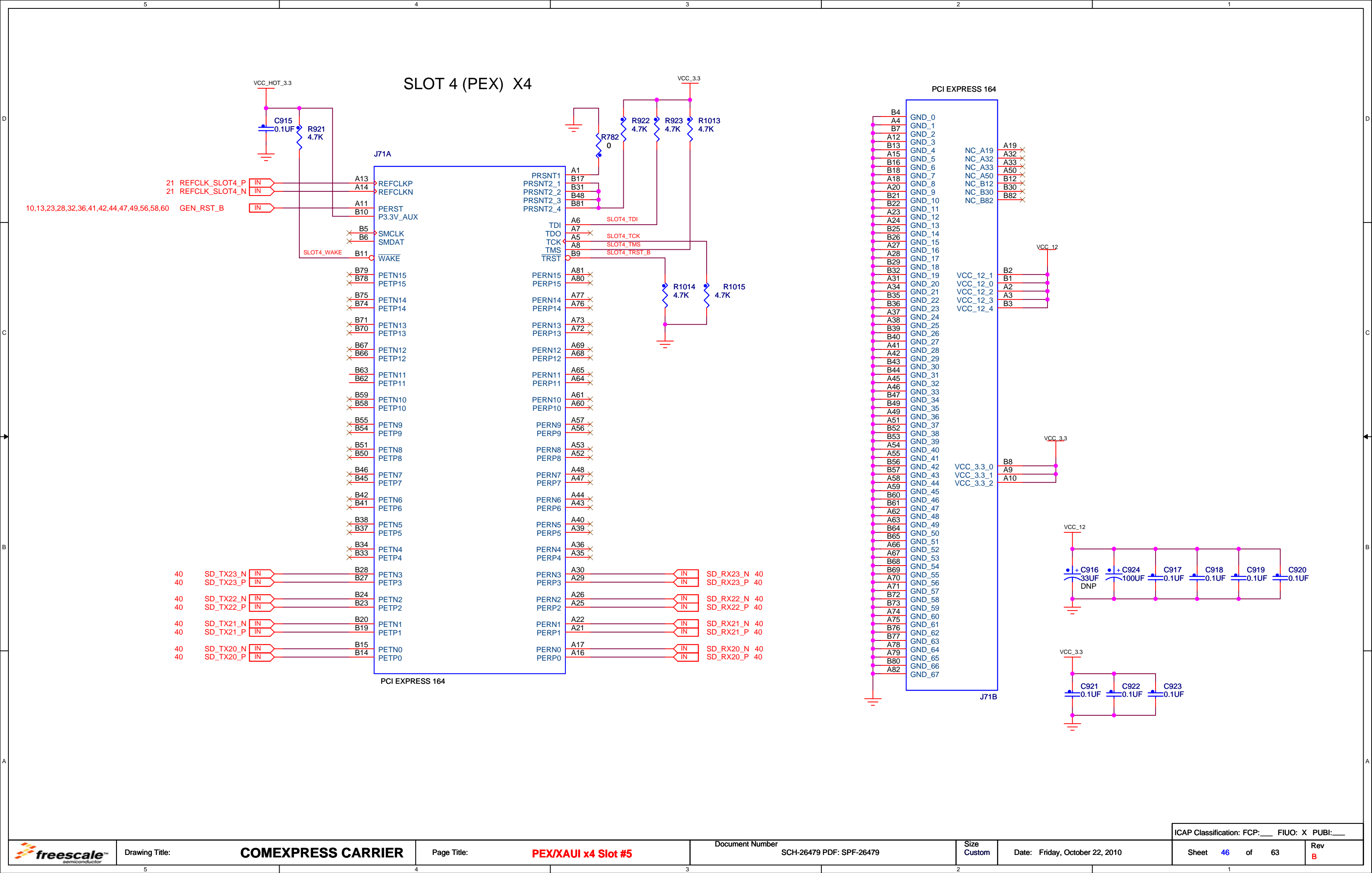


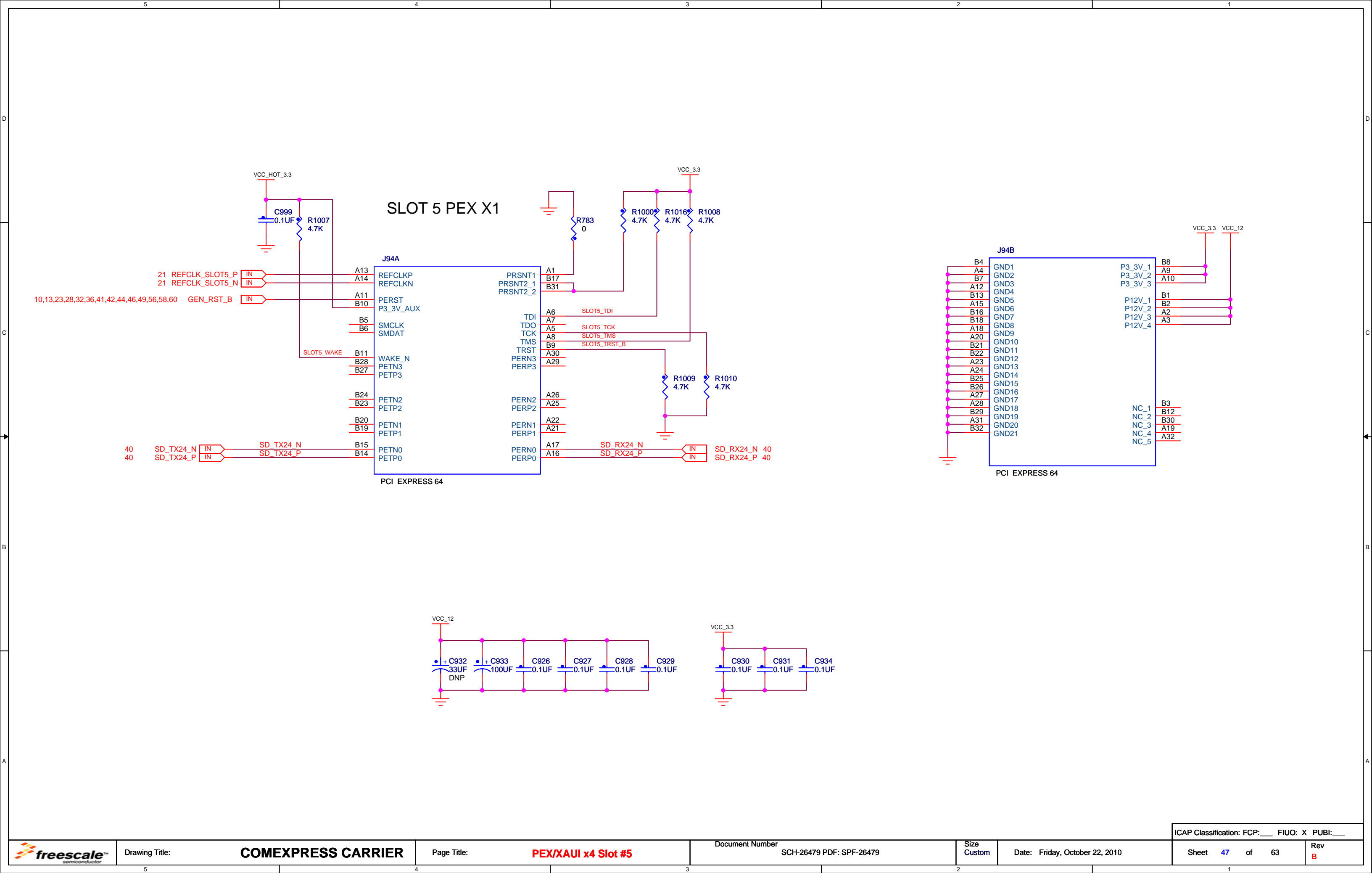
SLOT 3 (XAUI/SGMII) MAIN (PART 1 OF 2) CONNECTOR



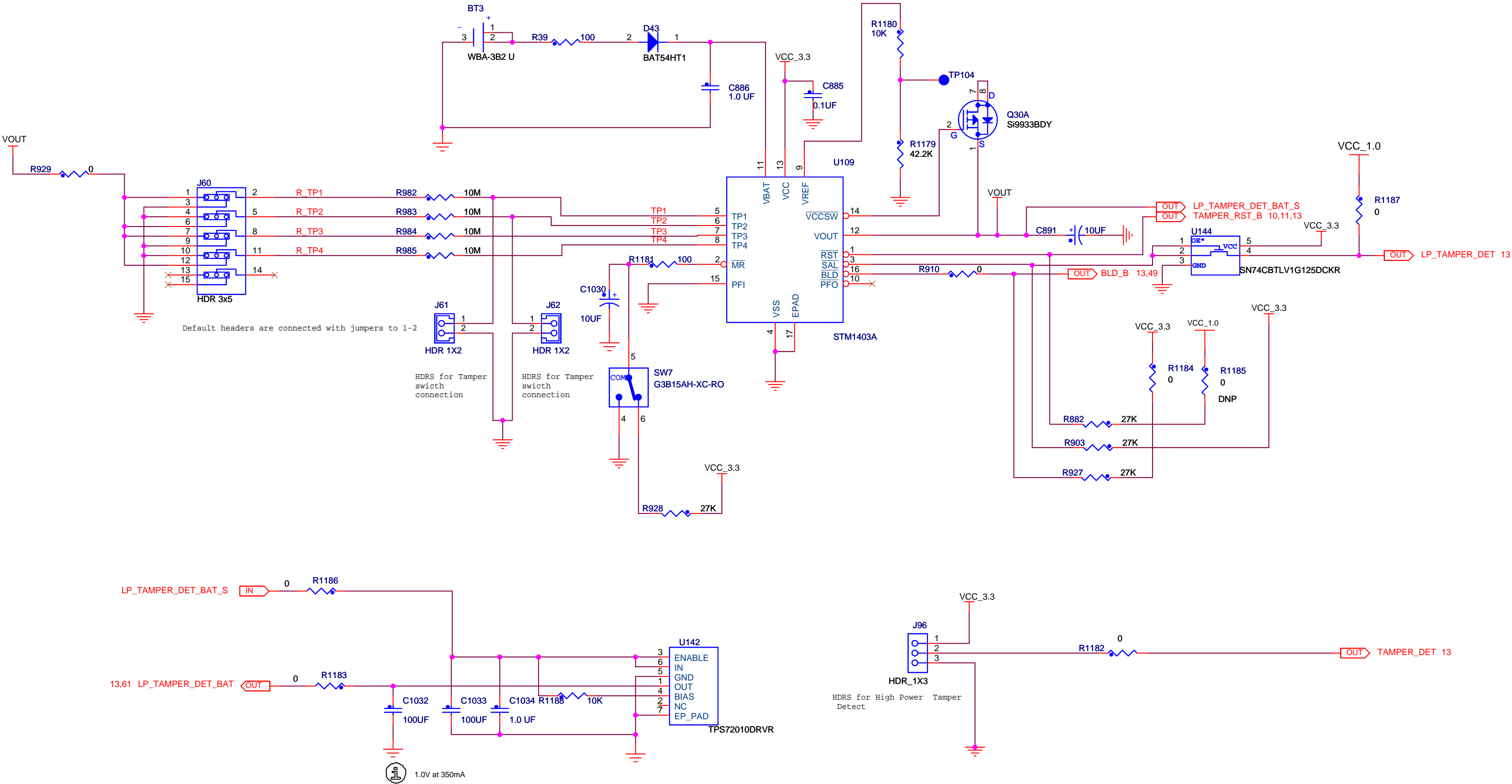
SLOT 3 (XAUI/SGMII/SRIO) SIDEBAND (PART 2 OF 2) CONNECTOR



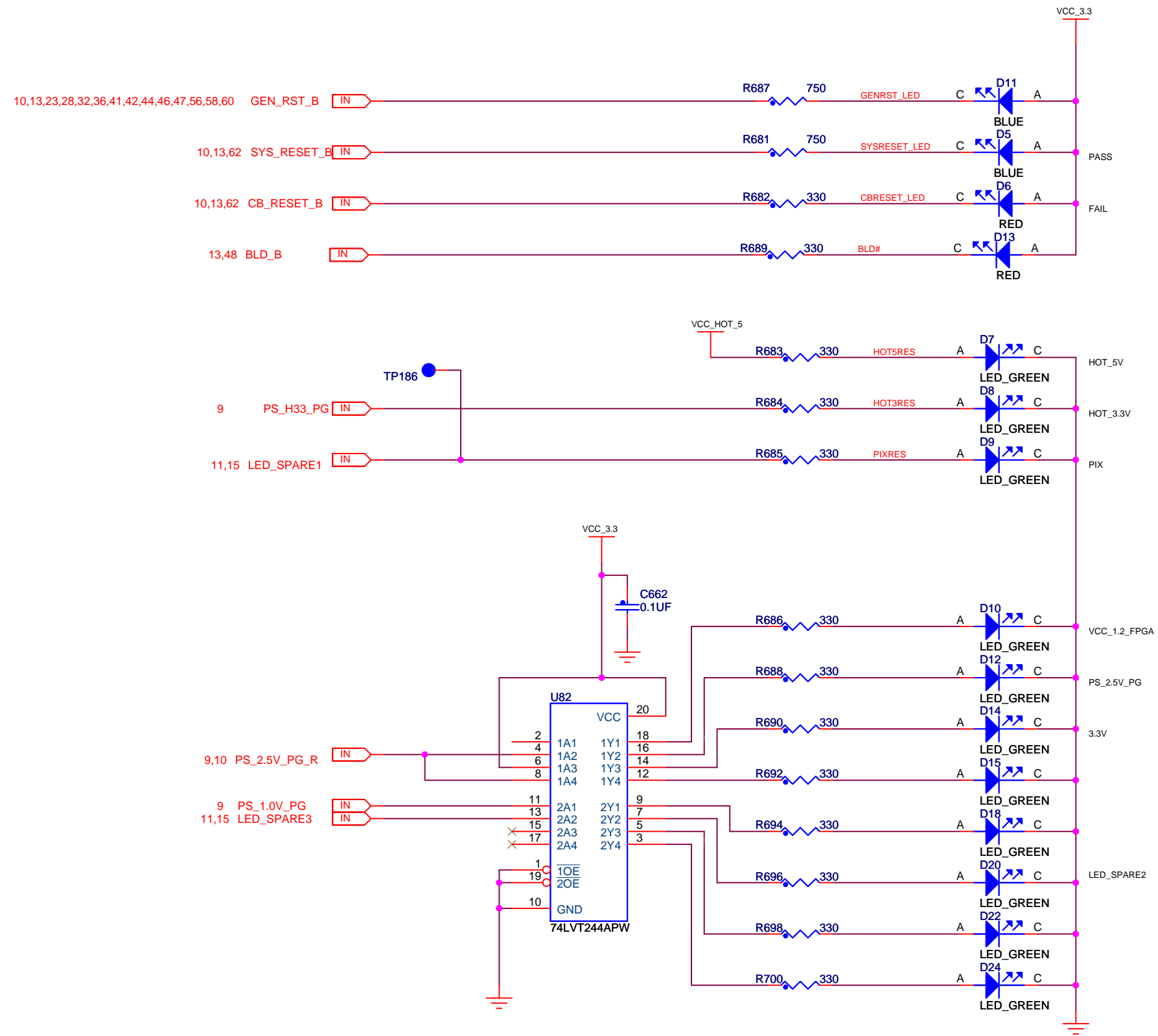




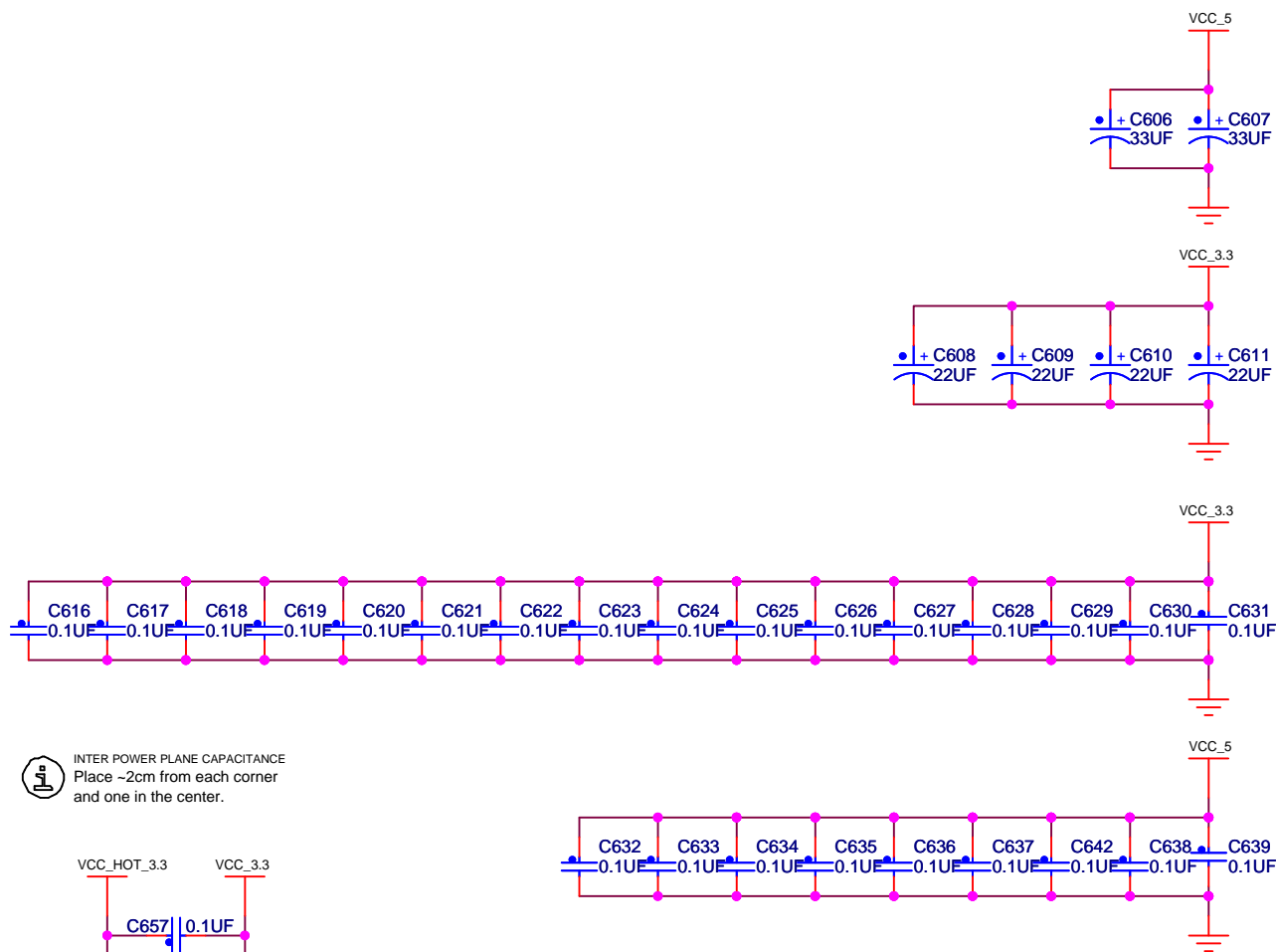
TAMPER DETECT INTERFACE



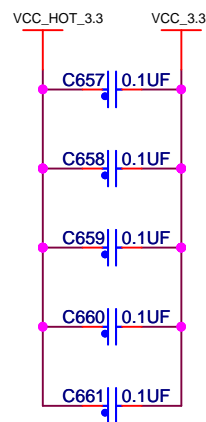
DEBUG LED INDICATION



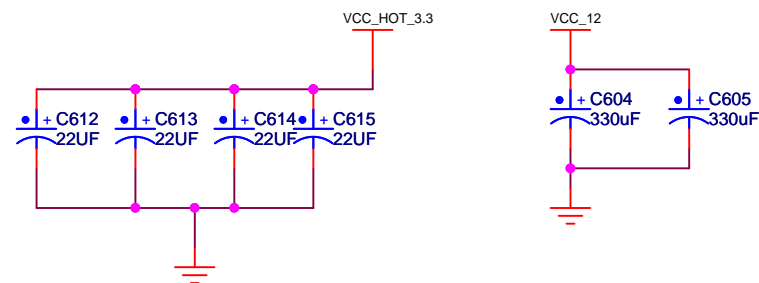
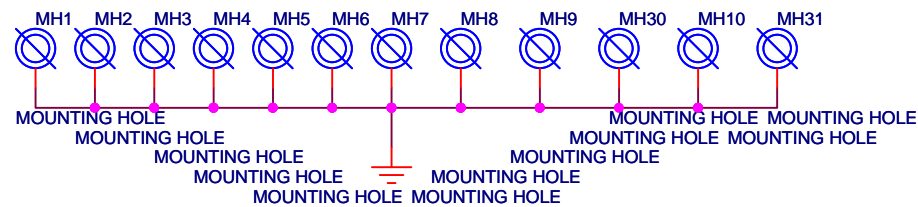
DECOUPLING CAPACITORS



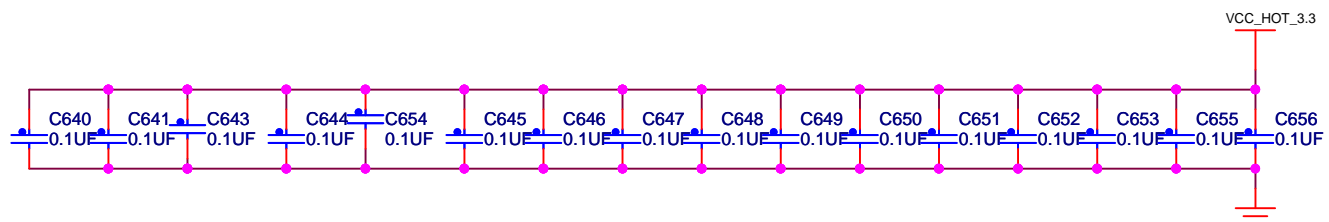
INTER POWER PLANE CAPACITANCE
Place ~2cm from each corner
and one in the center.



CHASSIS MOUNTING HOLES
ATX Chassis: 10 holes.

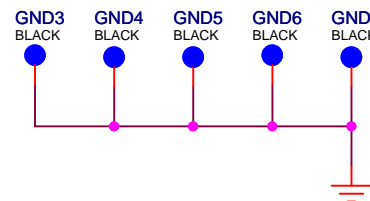


GLOBAL HF CAPACITANCE
Place in a grid ~5cm everywhere.

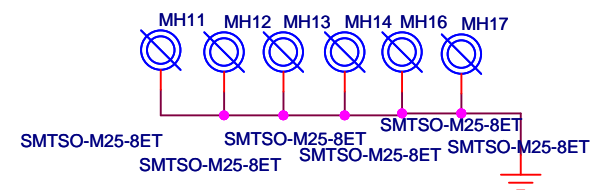


ATX Chassis: 11standoffs holes.

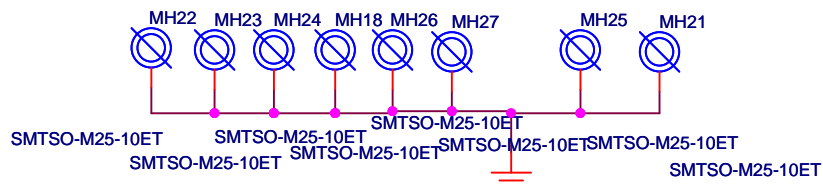
GROUND TEST POINTS
Place in each corner and center



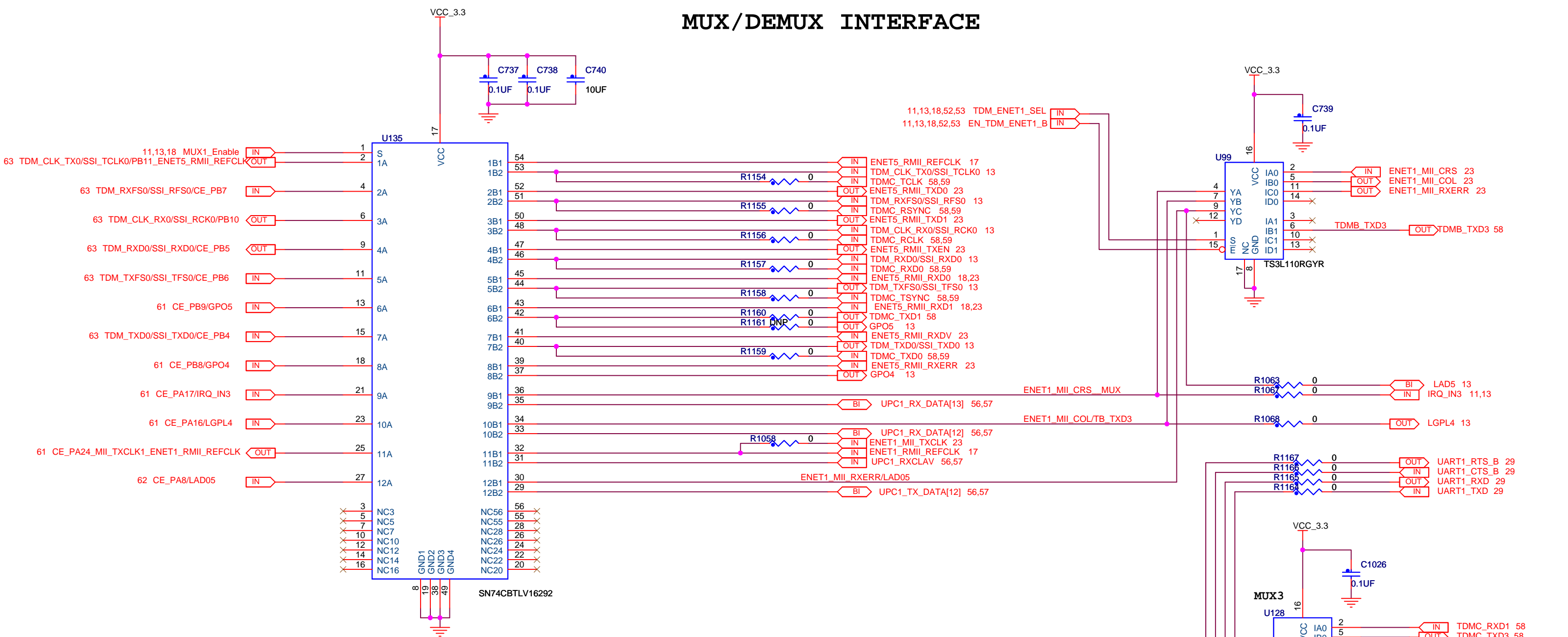
11 STANDOFFS MOUNTING HOLES FOR COMe MODULES



8 STANDOFFS MOUNTING HOLES FOR PMC CARDS 0 & 1



MUX/DEMUX INTERFACE



	MUX1_Enable		TDM_ENET1_SEL		EN_TDM_ENET1_B	
	Low	High	Low	High	Low	High
ENET5_RMII	*					
ENET1_RMII	*		*		*	
TDMB(NIBBLE)	*			*	*	
TDMC(Nibble)		*	*		*	
TDMD(Serial)				*	*	
UTOPIA		*				
GPIO		*				
LBC	*					
INTR	*					

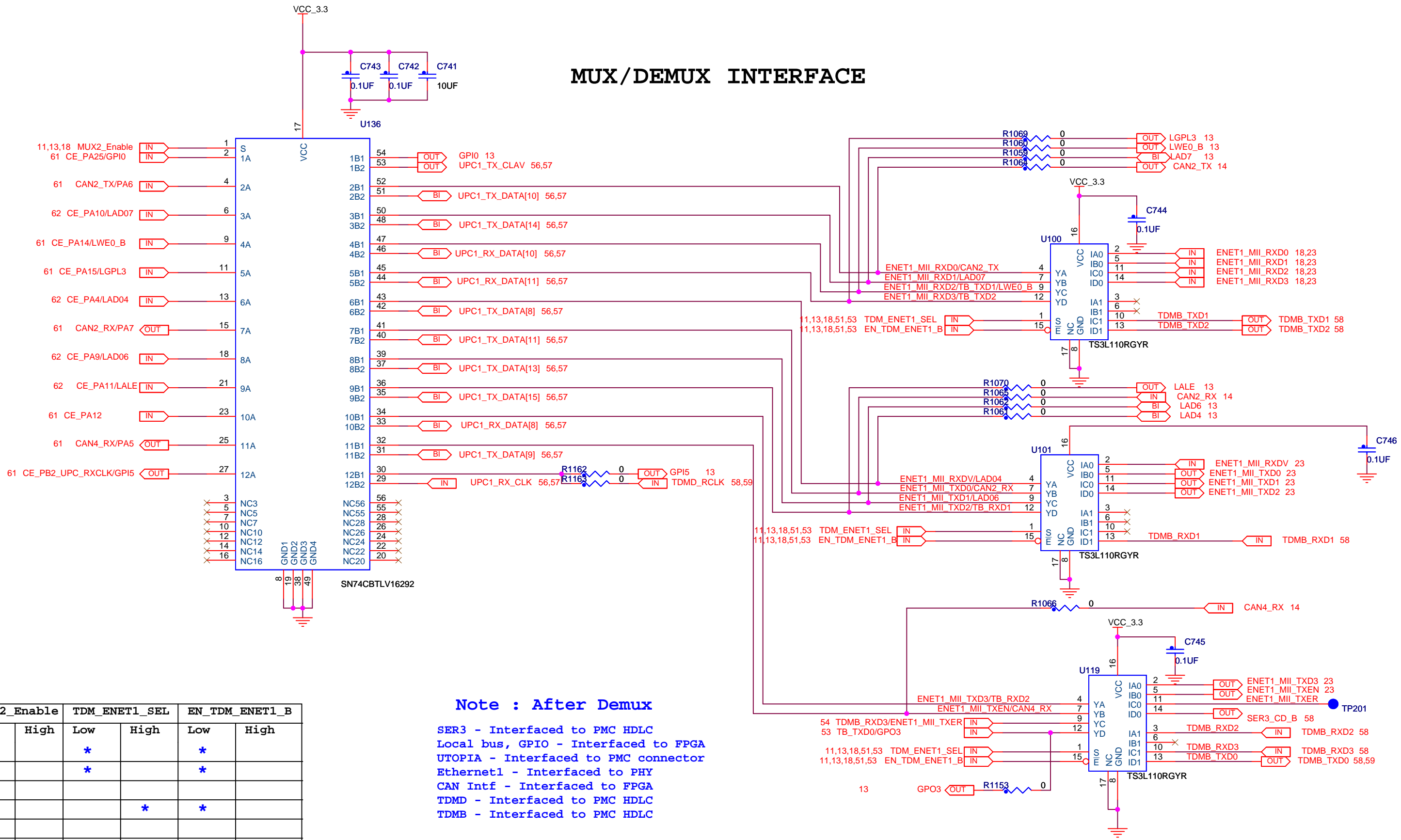
Note : After Demux

TDMB - Interfaced to PMC HDLC
TDMC - Interfaced to TDM RISER, PMC HDLC
TDMD - Interfaced to PMC HDLC
TDM/SSI - Interfaced to FPGA
Local bus, GPIO, INTR - Interfaced to FPGA
UART1 - Interfaced to Transceiver
UTOPIA - Interfaced to PMC connector
Ethernet1, 5 - Interfaced to PHY

After Mux

All Signals - Interfaced to COMe connector

MUX/DEMUX INTERFACE



Note : After Demux

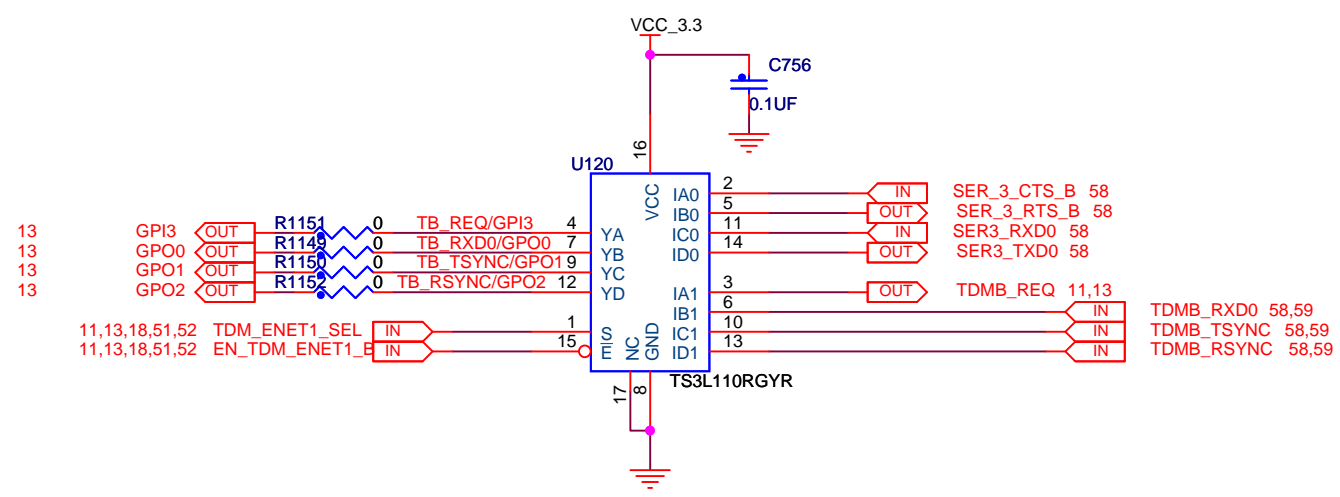
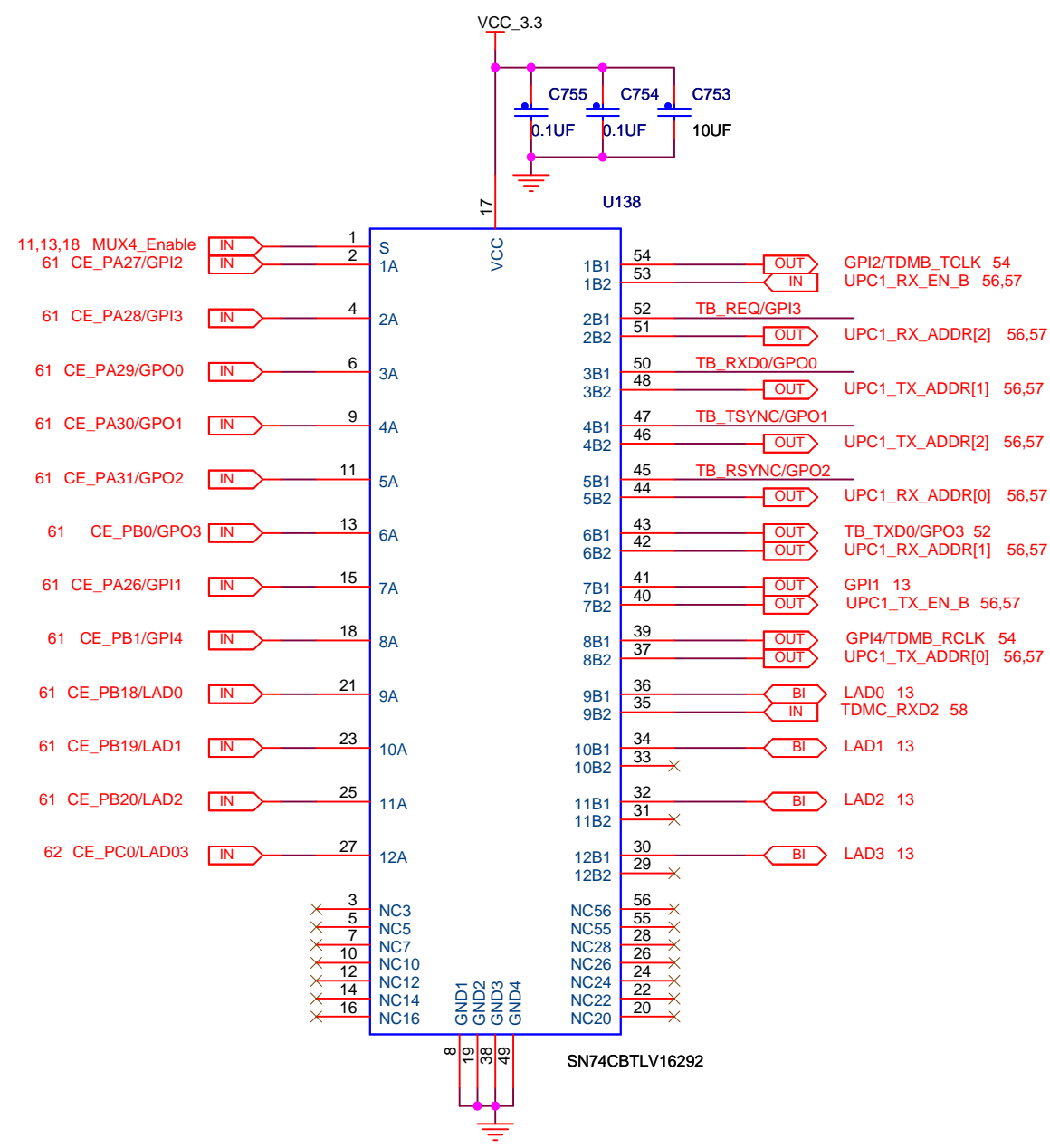
SER3 - Interfaced to PMC HDLC
Local bus, GPIO - Interfaced to FPGA
UTOPIA - Interfaced to PMC connector
Ethernet1 - Interfaced to PHY
CAN Intf - Interfaced to FPGA
TDMD - Interfaced to PMC HDLC
TDMB - Interfaced to PMC HDLC

After Mux

All Signals - Interfaced to COME connector

	MUX2_Enable		TDM_ENET1_SEL		EN_TDM_ENET1_B	
	Low	High	Low	High	Low	High
SER3	*		*		*	
ENET1_RMII	*		*		*	
CAN INTF	*					
TDMB(NIBBLE)	*			*	*	
TDMD(Serial)	*					
UTOPIA		*				
GPIO/INTR	*					
LBC	*					

MUX/DEMUX INTERFACE



Note : After Demux

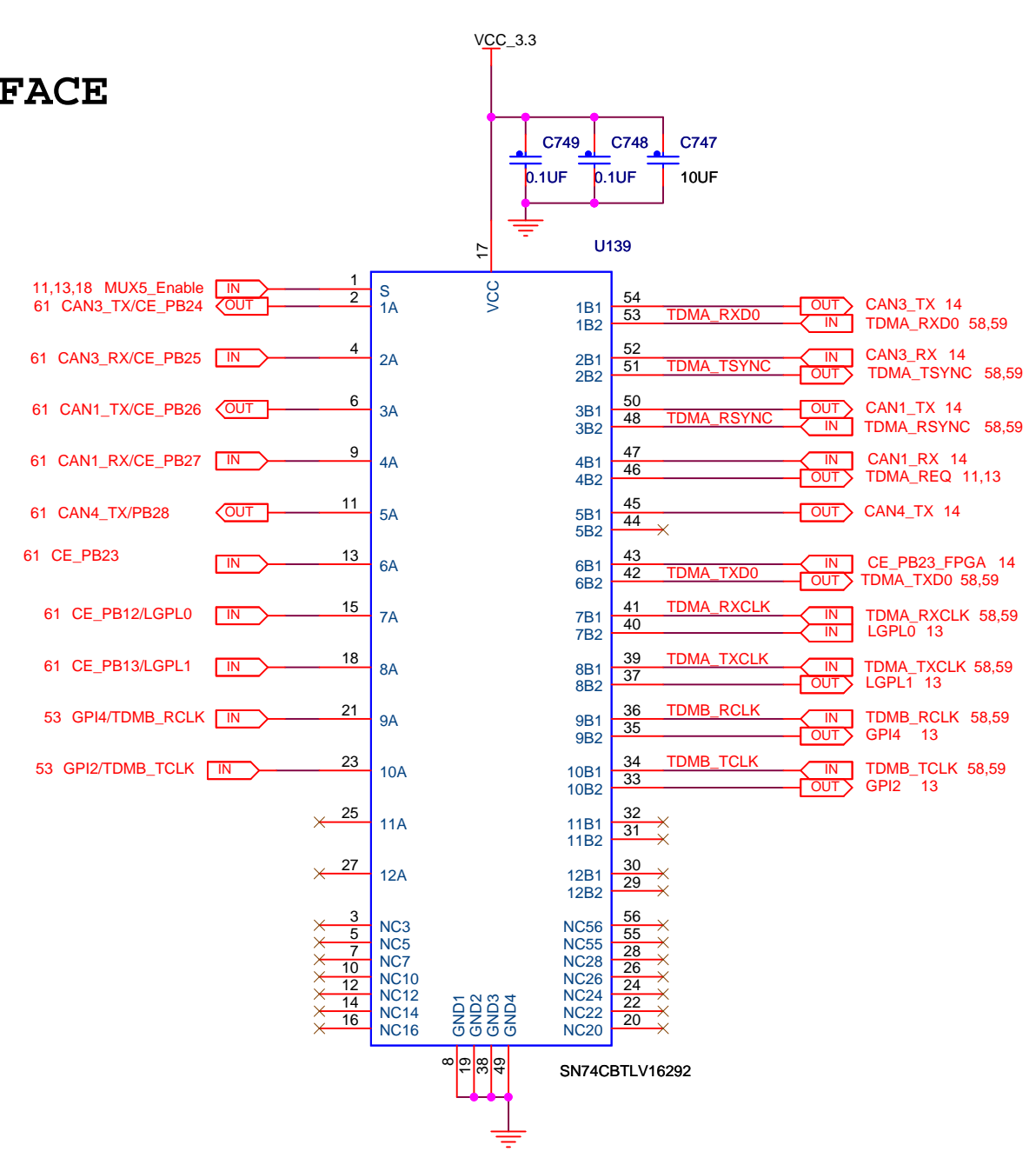
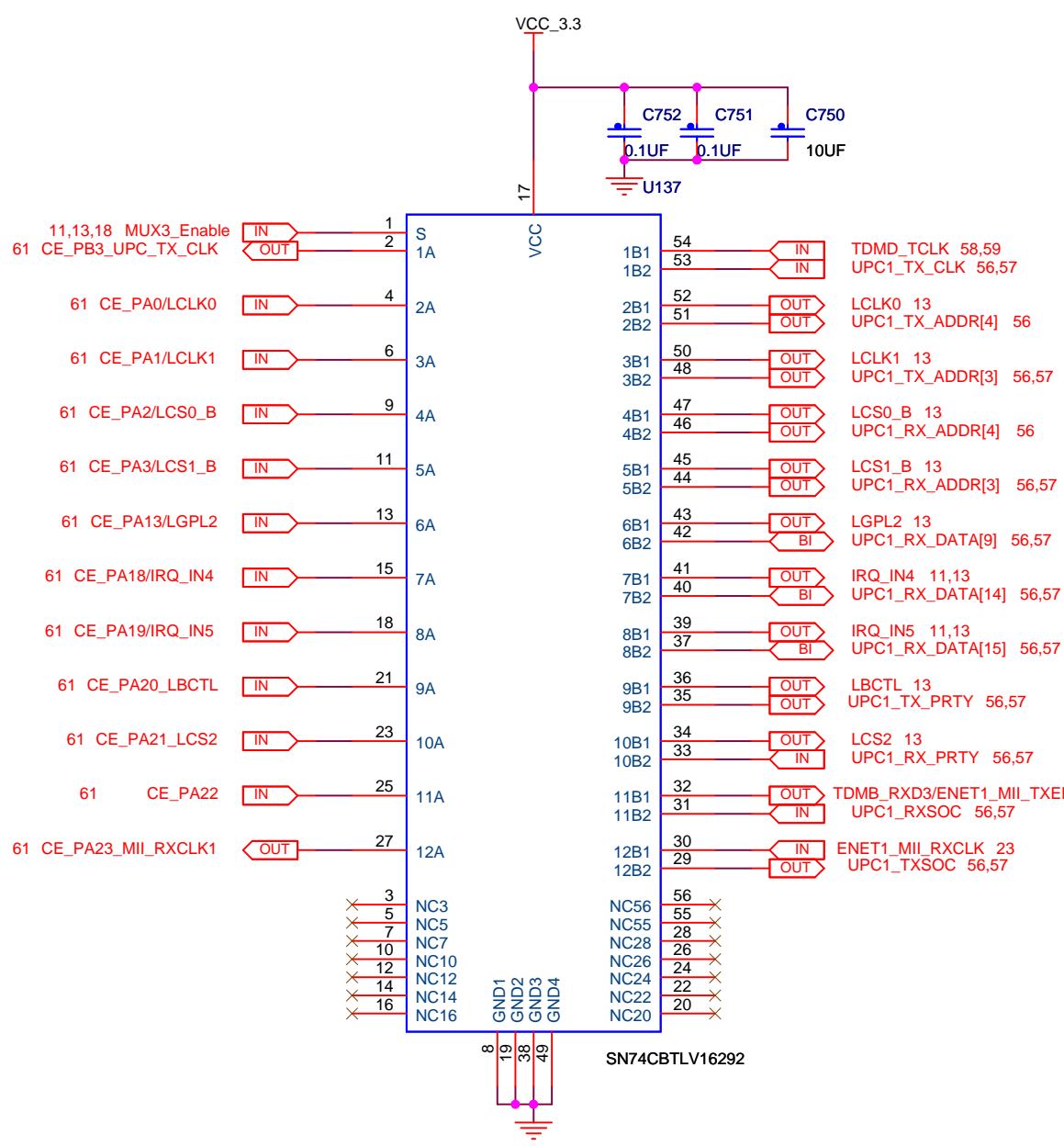
SER3 - Interfaced to PMC HDLC
Local bus, GPIO - Interfaced to FPGA
UTOPIA - Interfaced to PMC connector
TDMB - Interfaced to PMC HDLC
TDMC - Interfaced to PMC HDLC

After Mux

All Signals - Interfaced to COME connector

	MUX3_Enable		TDM_ENET1_SEL		EN_TDM_ENET1_B	
	Low	High	Low	High	Low	High
SER3	*		*		*	
TDMB (NIBBLE)	*			*	*	
UTOPIA		*				
GPIO/INTR	*			*	*	
LBC	*					
TDMC		*				

MUX/DEMUX INTERFACE



Note : After Demux

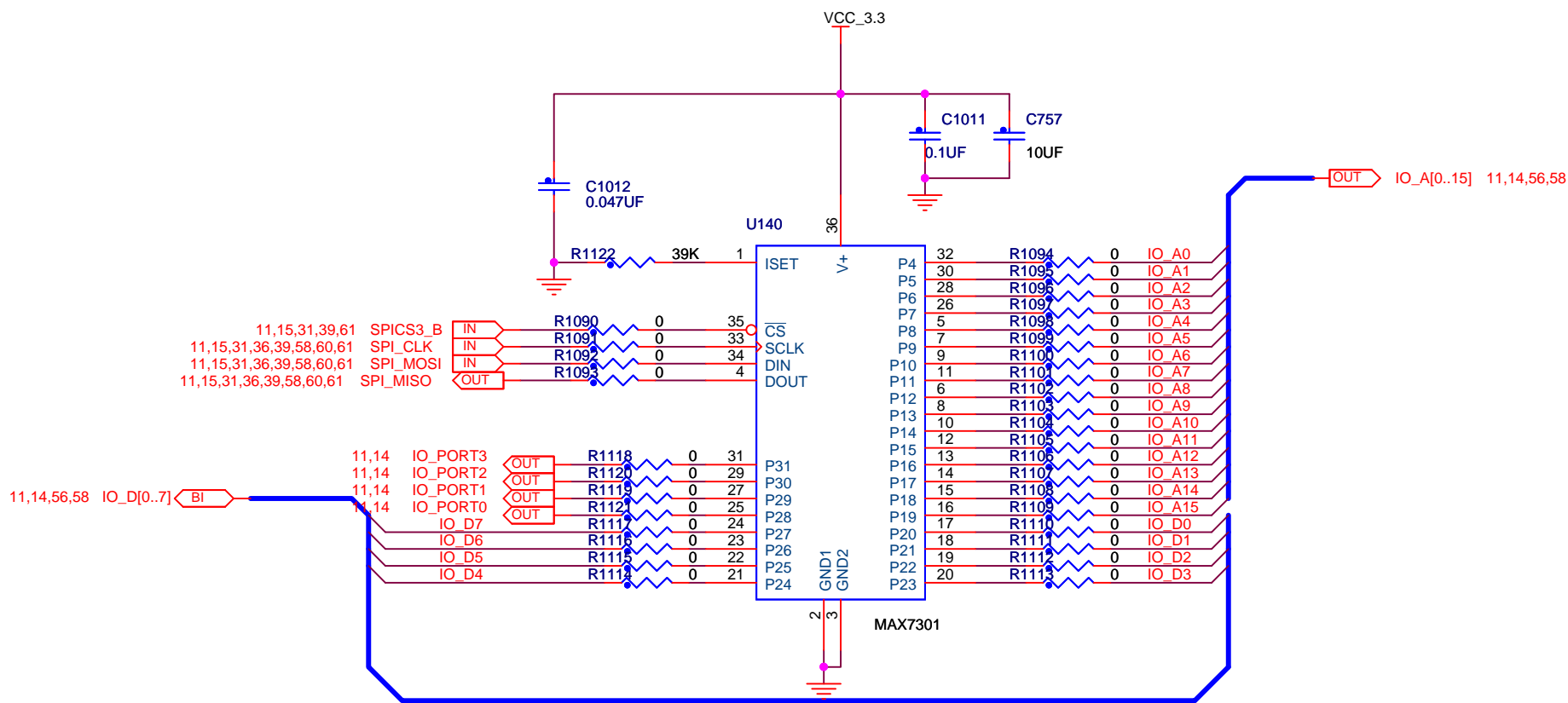
TDMA - Interfaced to PMC HDLC
Local bus, GPIO - Interfaced to FPGA
UTOPIA - Interfaced to PMC connector
Ethernet1 - Interfaced to PHY
CAN Intf - Interfaced to FPGA
TDMD - Interfaced to PMC HDLC
TDMB - Interfaced to PMC HDLC

After Mux

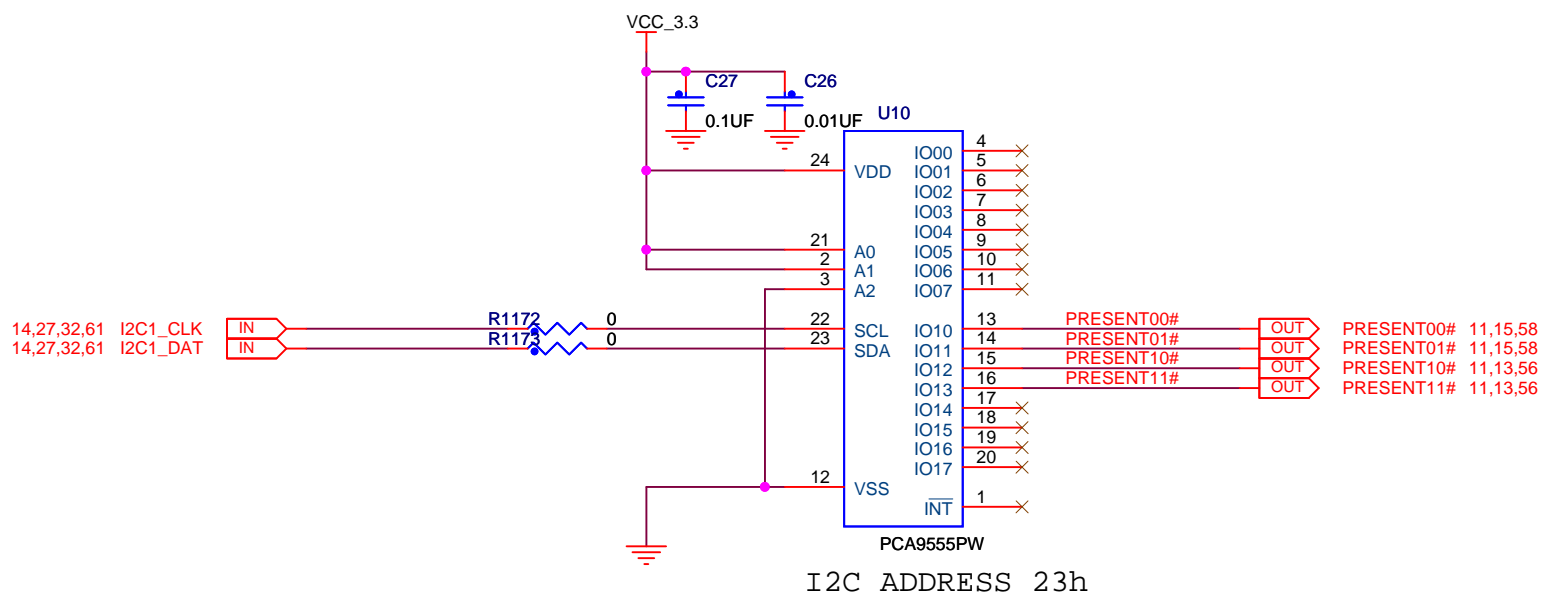
All Signals - Interfaced to COME connector

	MUX4_Enable		MUX5_Enable	
	Low	High	Low	High
TDMA				*
ENET1_RMII	*			
CAN INTF			*	
TDMB(NIBBLE)			*	
TDMD(Serial)	*			
UTOPIA		*		
GPIO/INTR	*			*
LBC	*			*

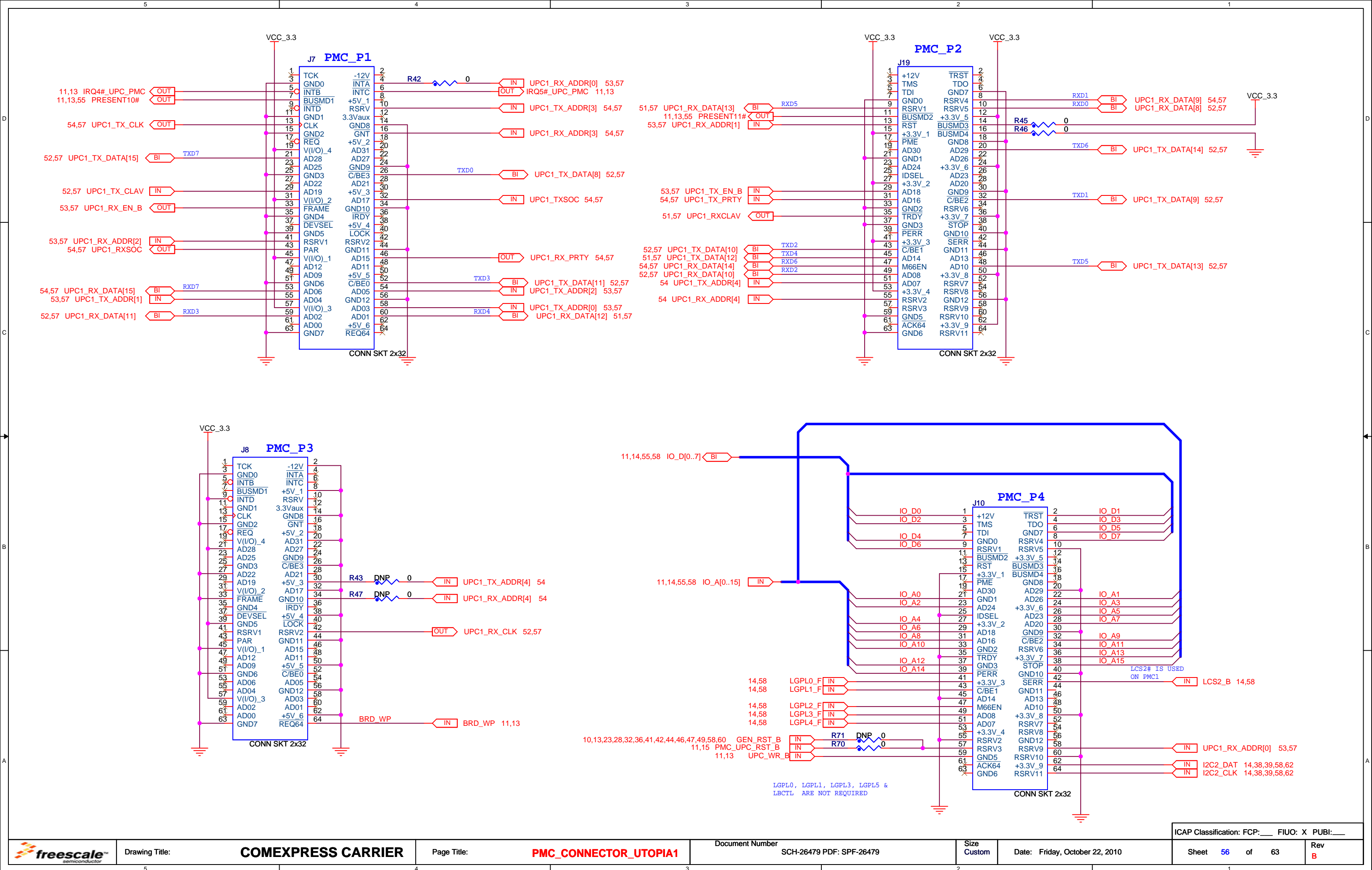
IO EXPANDER

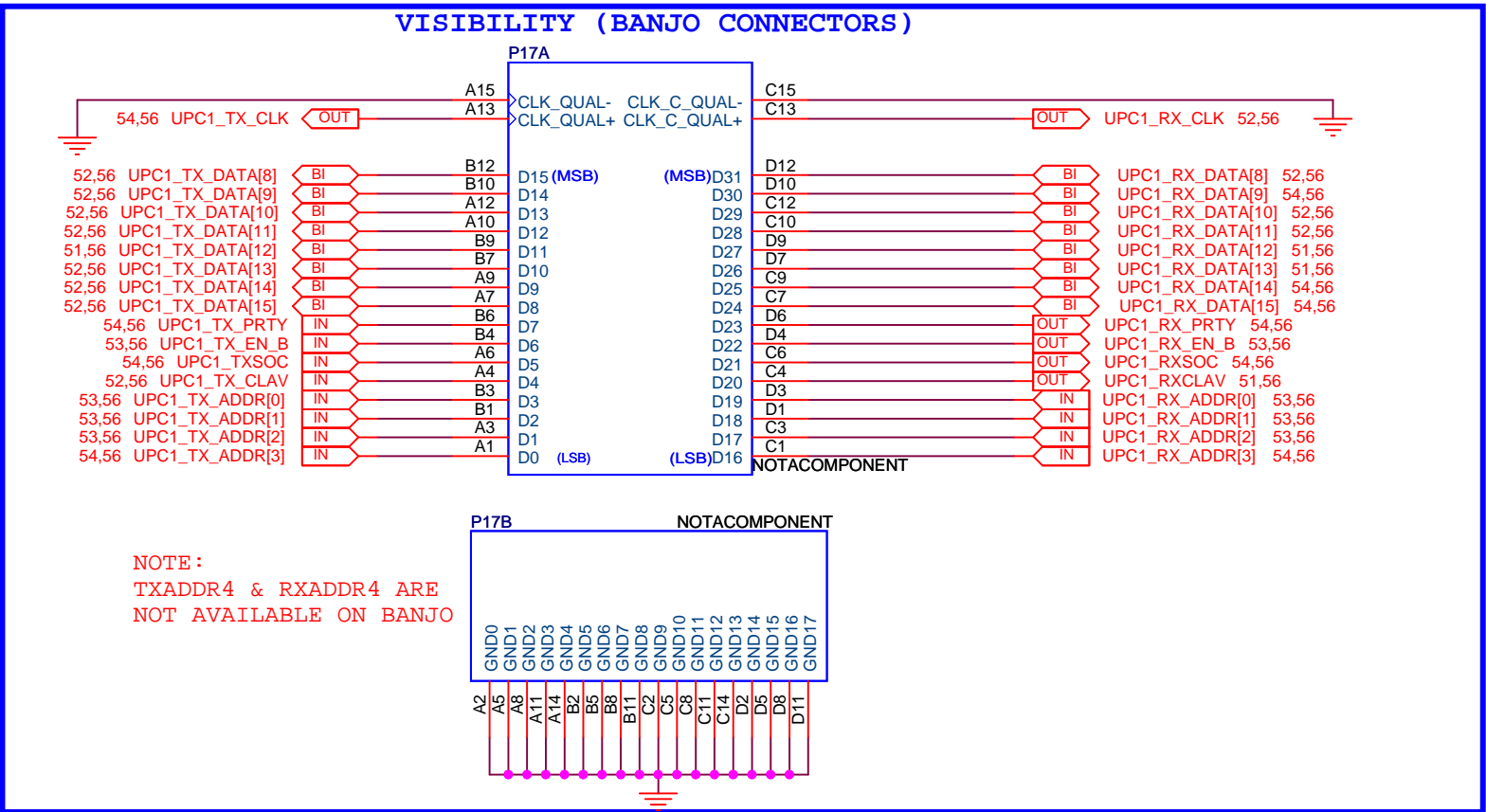
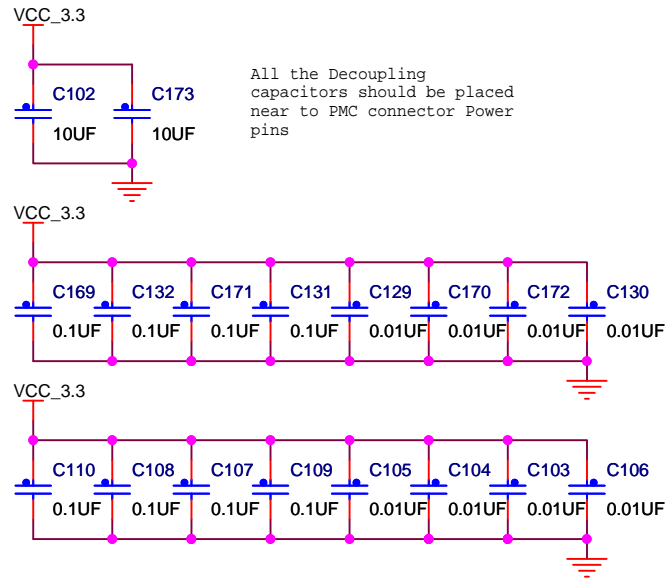


PMC0&1 PRESENCE DETECTION



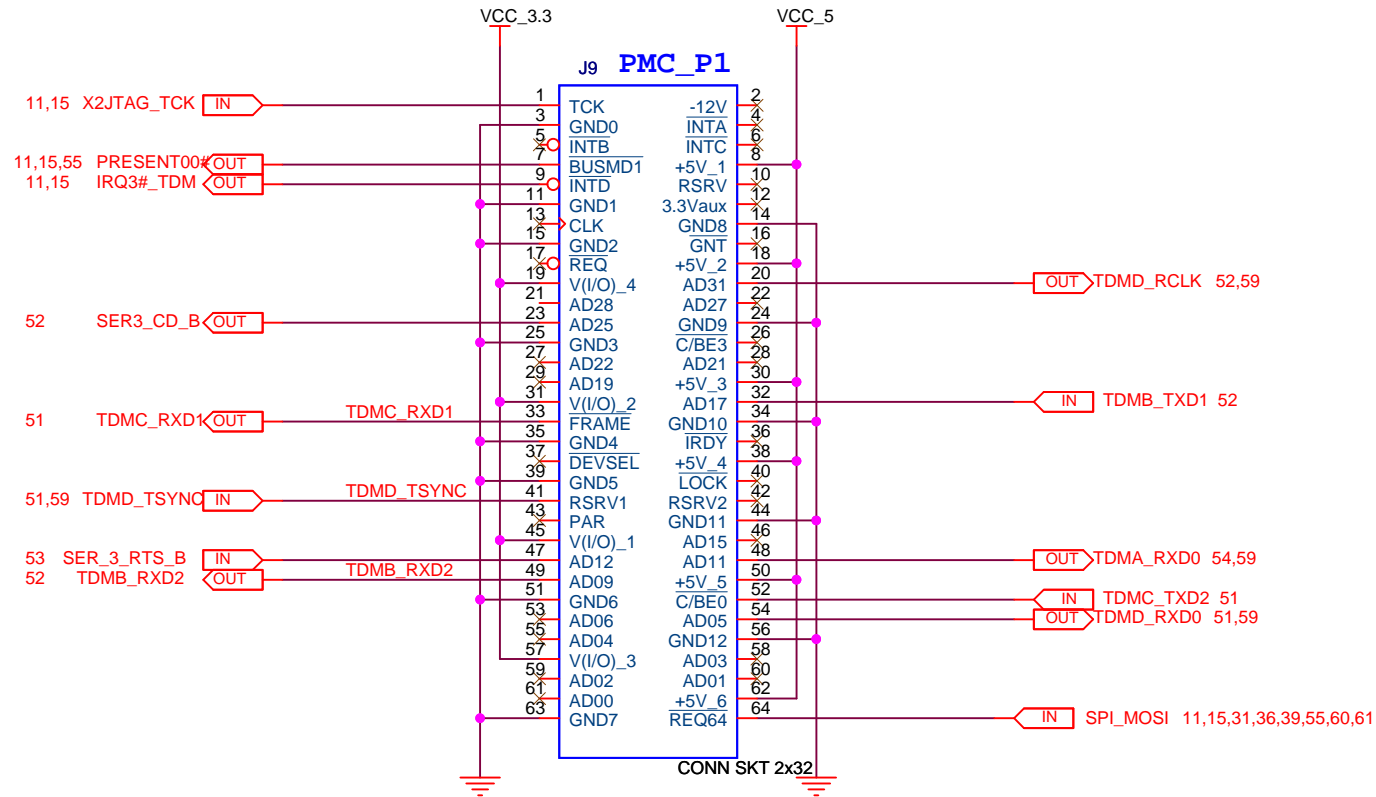
I2C ADDRESS 23h



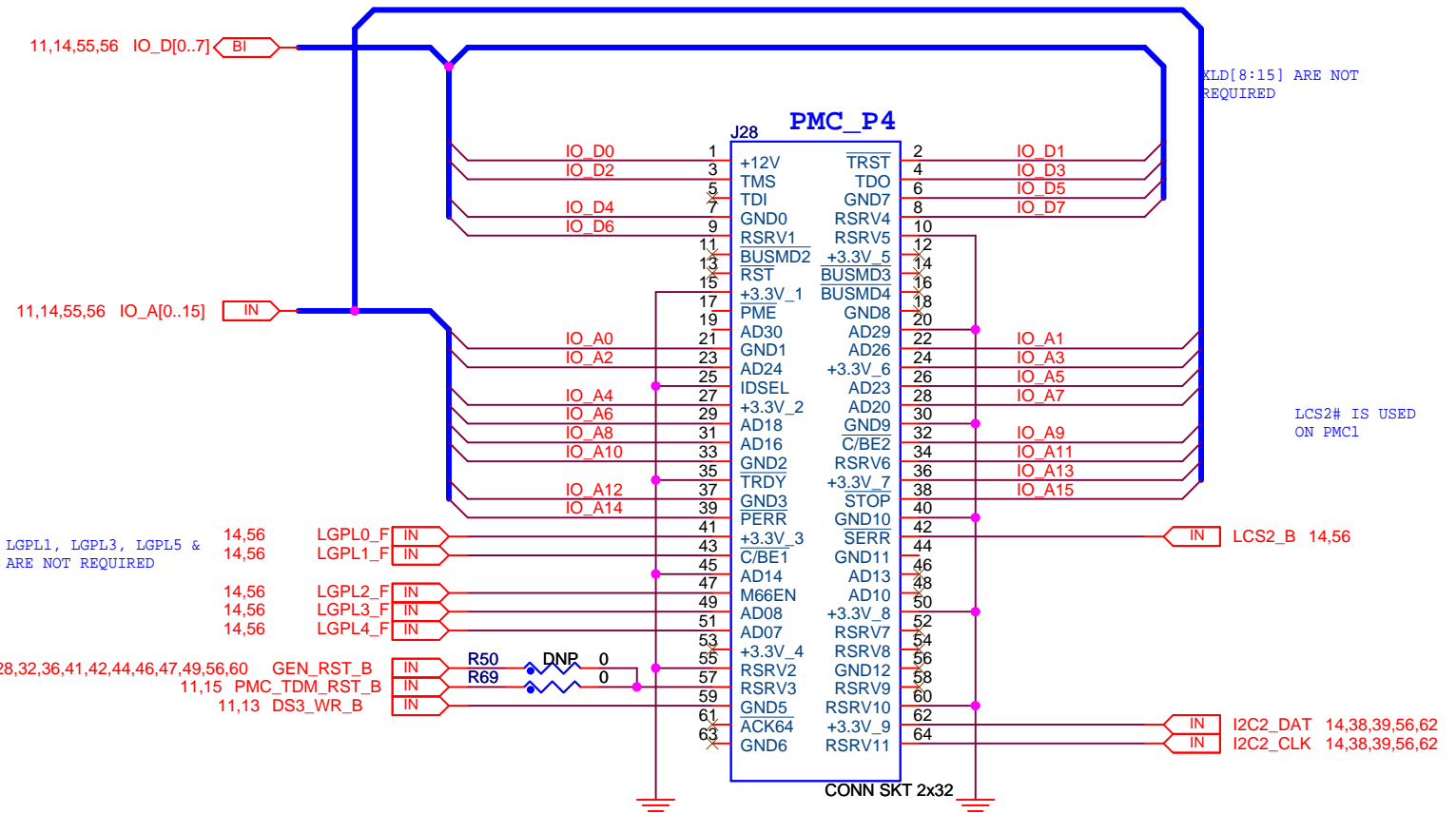
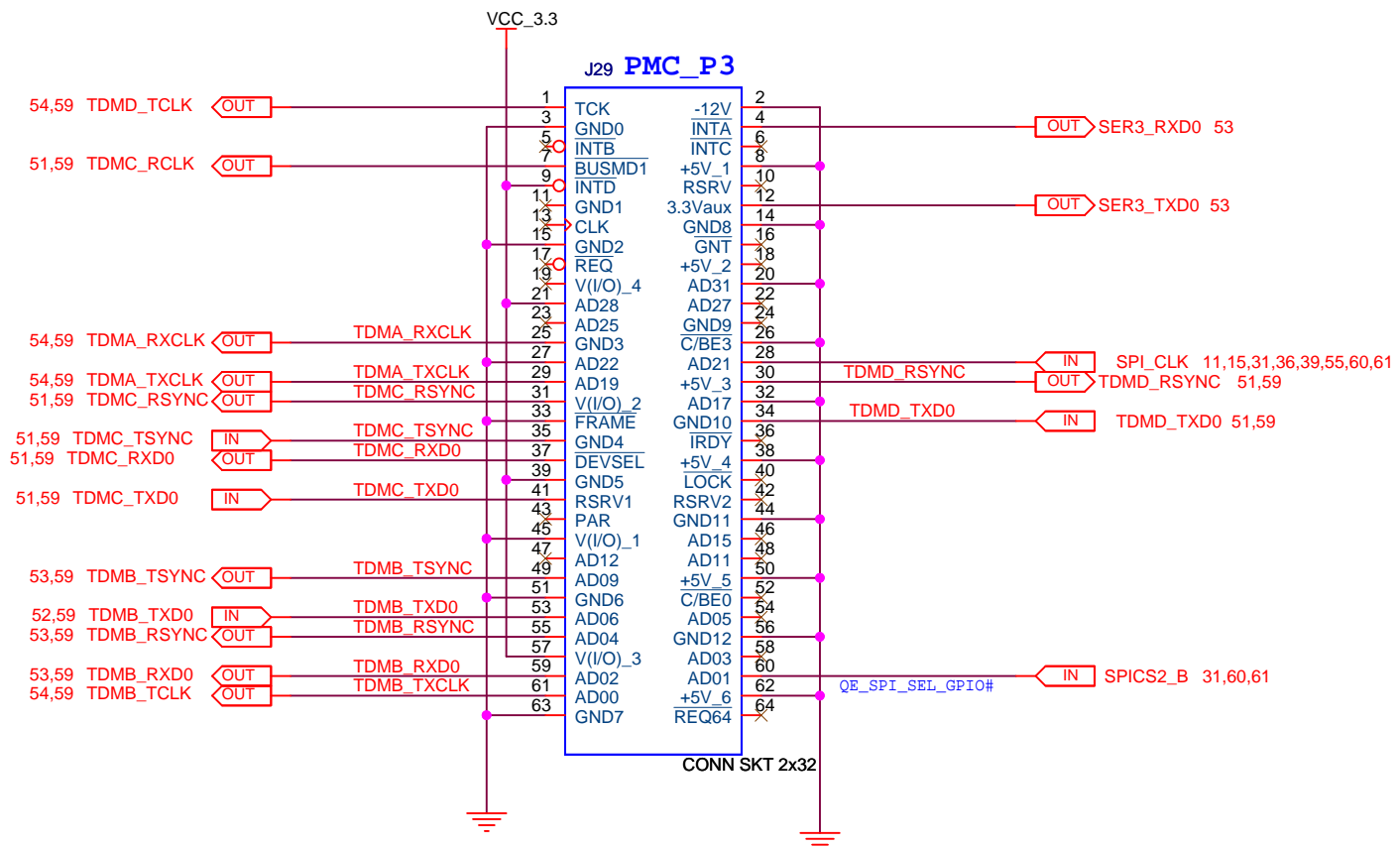
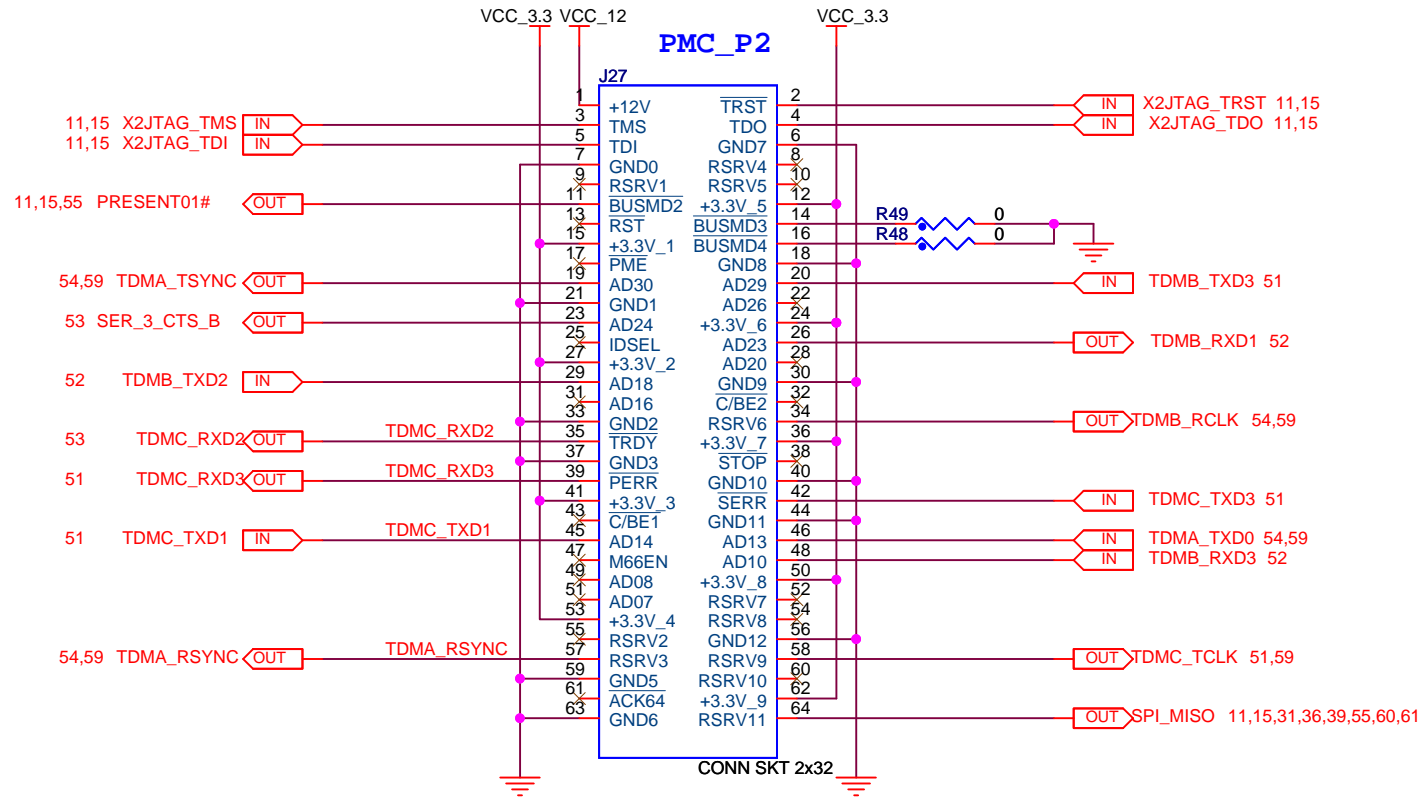


UPC1 CONNECTED TO PMC1

TDMA, TDMB*,
TDMC*, TDMD
*-Nibble mode



Note :TDMA, TDMB,TDMC,TDMD,SER3 ports brought from the Multiplexer



Drawing Title:

COMEXPRESS CARRIER

Page Title:

PMC0_Connector_TDM1

Document Number

SCH-26479 PDF: SPF-26479

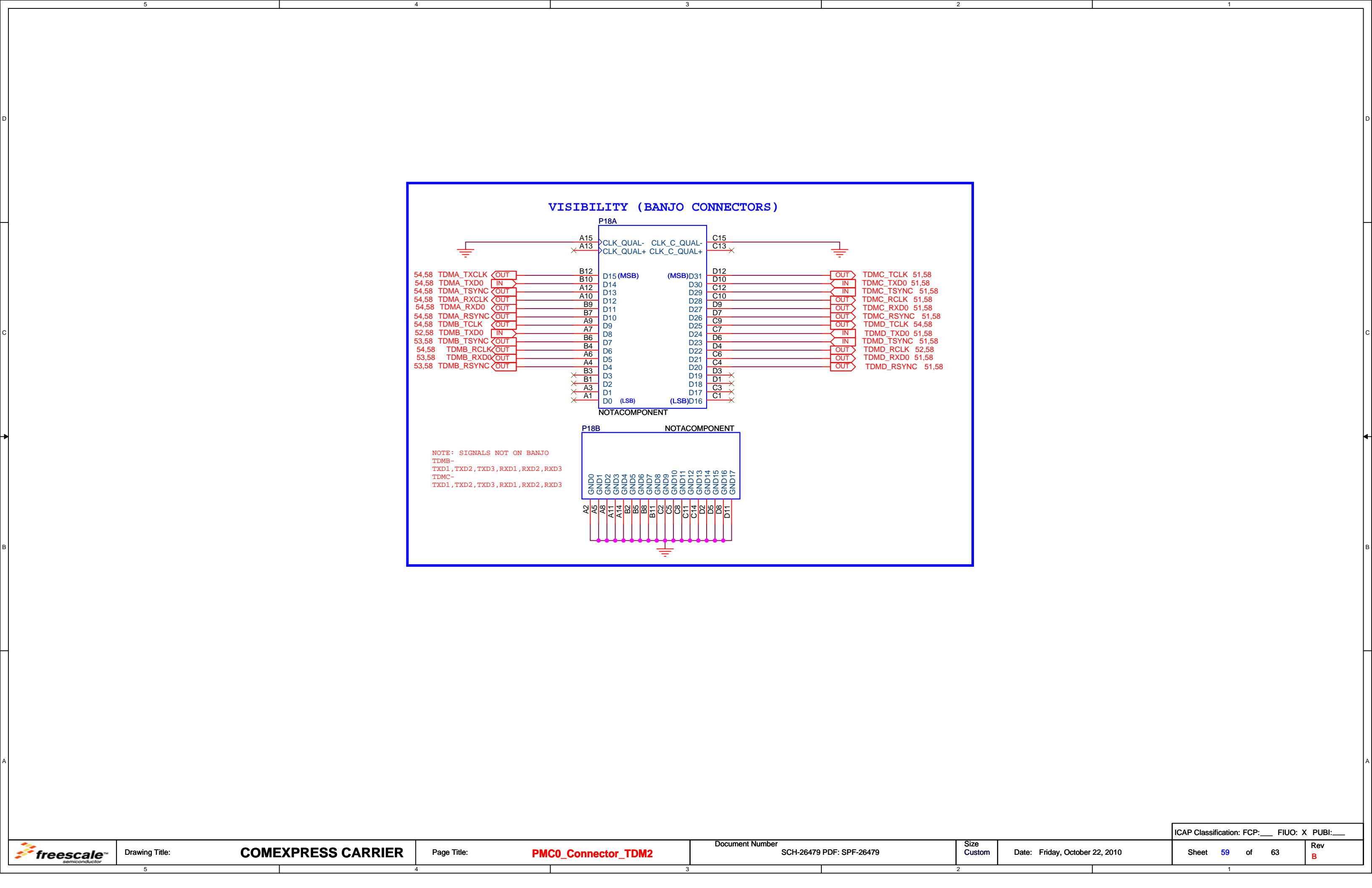
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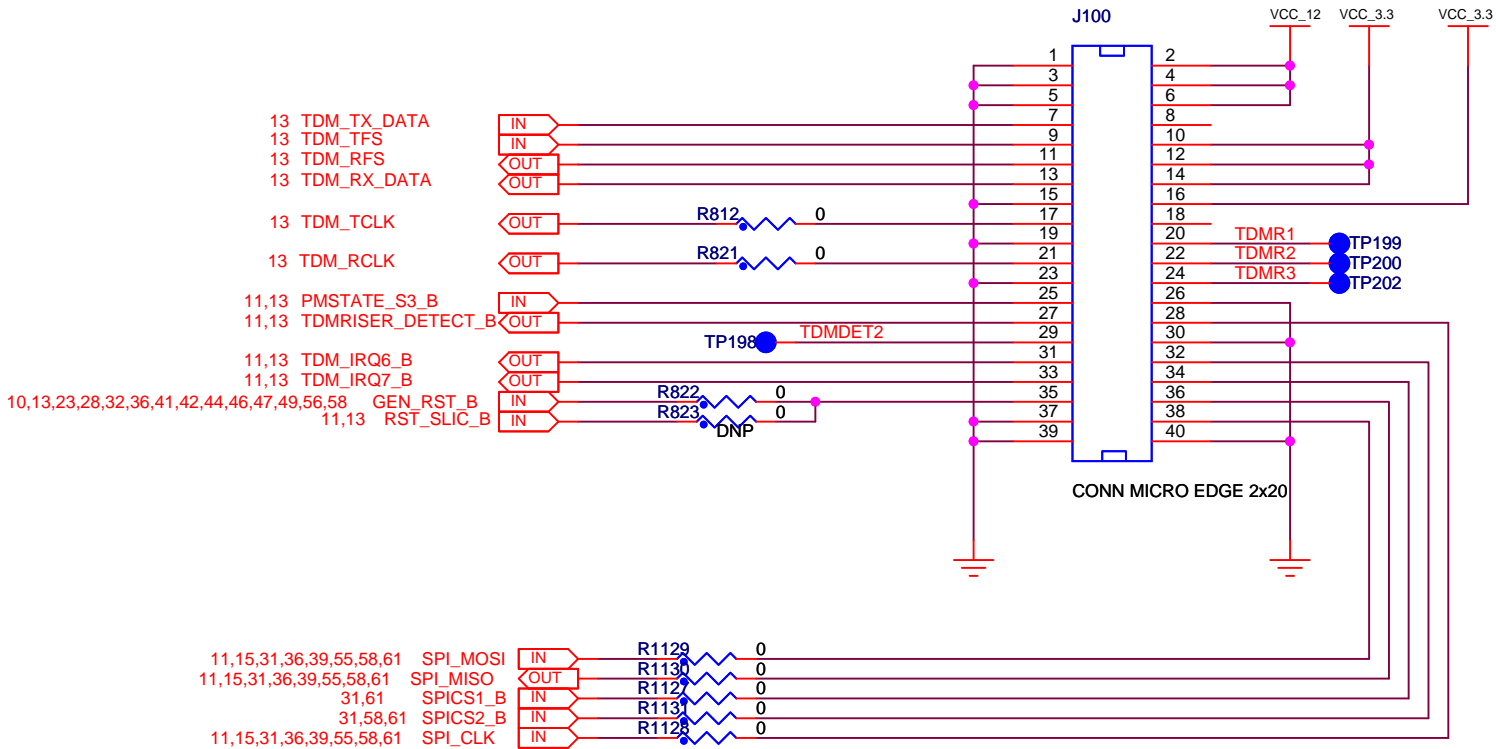
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TDM RISER CARD CONNECTIVITY



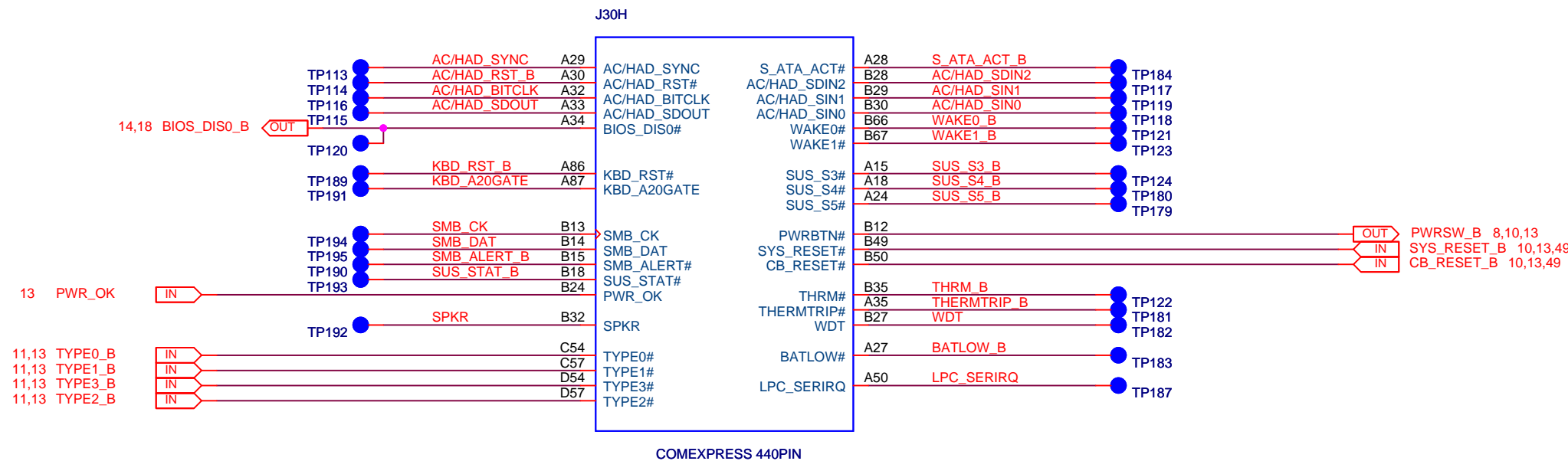
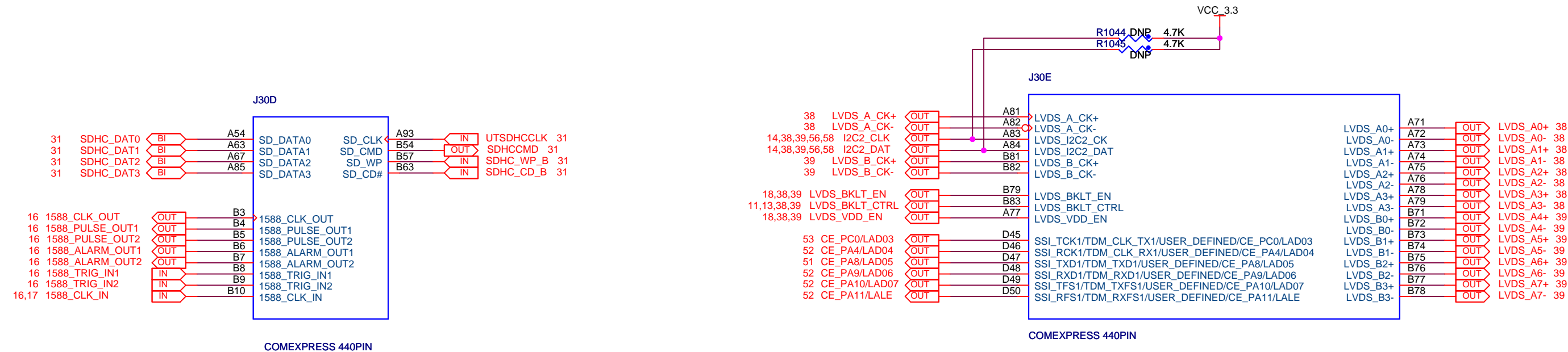
J30B



J30G



COM EXPRESS CONNECTOR



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