Design Guidelines

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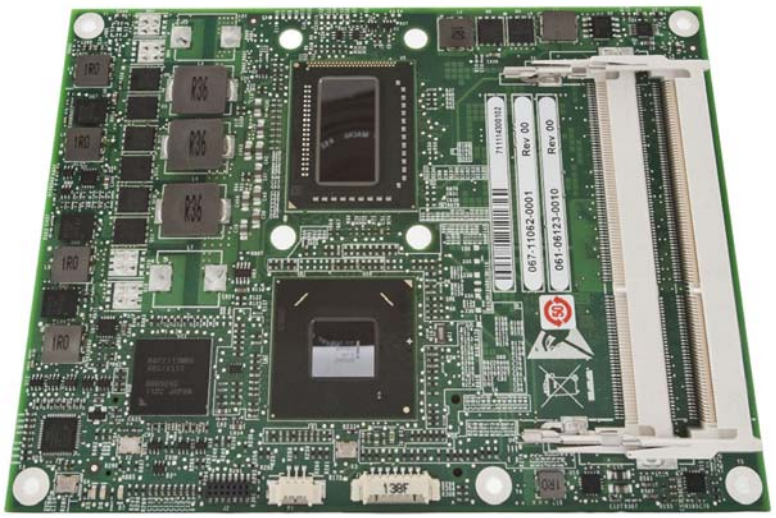

COM EXPRESS®

FOR USE WITH COM EXPRESS R2.0 MODULES
CEQM67

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Preface

About this manual

This document is an addendum to the *PICMG® COM Express™ Carrier Design Guide*. This document describes special considerations and guidelines for designing a carrier board for Radisys® COM Express R2.0 Type 6 modules.

These design guidelines also include a brief introduction to thermal validation procedures at the system level, as well as instructions on redesigning a COM Express R1.0 Type 2 carrier board for use with a COM Express R2.0 Type 6 module.

In Radisys publications, COM Express R2.0 modules or carrier boards refer to compliance with the *PICMG COM.0 COM Express Base Specification, Revision 2.0*. Modules compliant with *PICMG COM.0 COM Express Base Specification, Revision 1.0* are referred to as COM Express R1.0 modules or carrier boards.

Compliance with the PICMG specification makes Radisys COM Express modules easy to integrate into your product design, resulting in shorter time to market and lower development costs.

In addition to this design guide, it is recommended that you obtain the following PICMG documentation from www.picmg.org for complete guidelines on designing a fully COM Express-compliant carrier board.

- *PICMG COM.0 COM Express Base Specification, Revision 2.0*
- *PICMG COM.0 COM Express Base Specification, Revision 1.0*
- *PICMG COM Express Carrier Board Design Guide*

Note: At the time of this publication, the PICMG organization has not yet announced availability of the *PICMG COM Express Carrier Board Design Guide* for COM Express 2.0 modules. Consequently, this addendum is developed based on the current *PICMG COM Express Carrier Board Design Guide* for COM Express R1.0 modules. The *PICMG COM.0 COM Express Base Specification, Revision 1.0* may also be a necessary reference before the newer PICMG documentation is available.

Safety notices

Electrostatic discharge

WARNING! The Radisys COM Express modules and carrier boards contain static-sensitive components and should be handled with care. Failure to employ adequate anti-static measures can cause irreparable damage to components.

Electrostatic discharge (ESD) damage can result in partial or complete device failure, performance degradation, or reduced operation life. To avoid ESD damage, the following precautions are strongly recommended.

- Keep the COM Express module in its ESD shielding bag until you are ready to install it.
- Before touching the COM Express module, attach an ESD wrist strap to your wrist and connect its other end to a known ground.
- Handle the COM Express module only in an area that has its working surfaces, floor coverings, and chairs connected to a known ground.
- Hold the COM Express module only by its edges and mounting hardware. Avoid touching components and connector pins.

For further information on ESD, visit www.esda.org.

Where to get more product information

Visit the Radisys Web site for product information and other resources. Downloads (manuals, release notes, software, etc.) are available at www.radisys.com.

See the following resources for information on the COM Express module and the development carrier board from Radisys:

- **Hardware reference and system functionality.** The *Radisys COM Express Module Product Manual* provides details for the features, interfaces, and functionality of the COM Express module.
- **Installation and initial setup instructions.** The *Radisys COM Express Module Quick Start Guide* provides the steps for assembling a COM Express system. A Radisys development carrier board is typically used as a sample carrier board in this document.
- **BIOS configuration information.** The *Radisys BIOS Setup Utility Specification* describes the BIOS setup utility interfaces and configuration options. Typically, the BIOS developed based on this document can be used in the BIOS flash ROM on the COM Express module, and may also be used on the carrier board's BIOS flash ROM.
- **Schematics of a Radisys development carrier board.** Radisys provides development carrier boards, which can be used as a reference for designing a custom carrier board. For example, the CR300 carrier board provides comprehensive interfaces and functionality for a COM Express 2.0-compliant system.

  Note: The schematics are confidential and proprietary for Radisys. Contact Radisys to request the document after signing a non-disclosure agreement (NDA).

Chapter 1

COM Express Signals

When designing your own carrier board for Radisys modules, pay close attention to COM Express signal pull-up and pull-down implementations.

The following table shows the purpose and usage of specific COM Express pinouts on Radisys modules.

Table 1. CEQM67 COM Express signal design notes

Pin #	Signal	Purpose and usage
A15	SUS_S3#	Buffered output, no pull up needed
A18	SUS_S4#	Buffered output, no pull up needed
A24	SUS_S5#	Buffered output, no pull up needed
A27	BATLOW#	EC internal pull-up on module to 3.3V SBY
A28	(S)ATA_ACT#	Buffered output, no pull up needed
A34	BIOS_DISABLE#	EC internal pull-up to 3.3V standby on module
A35	THRMTRIP#	Output from EC, sink current at V_{OL}<1.6mA, source current at V_{OH}<0.2mA
A38	USB_6_7_OC#	• Pull up to 3.3V suspend on module with an 8.2K Ω resistor • Open drain output from carrier to module
A44	USB_2_3_OC#	• Pull up to 3.3V suspend on module with an 8.2K Ω resistor • Open drain output from carrier to module
A48	EXCD0_PERST#	Pull up to 3.3V on module with a 10K Ω resistor
A49	EXCD0_CPPE#	Pull up to 3.3V on module with a 10K Ω resistor
A50	LPC_SERIRQ	Pull up to 3.3V on module with an 8.2K Ω resistor
A54	GPI0	Pull up to 3.3V on module with an 8.2K Ω resistor
A63	GPI1	Pull up to 3.3V on module with an 8.2K Ω resistor
A67	GPI2	• GPI2/ICCMON • Pull up to 3.3V on module with a 10K Ω resistor
A77	LVDS_VDD_EN	Pull down to ground
A83	LVDS_I2C_CK	Pull up to 3.3V on module with a 2.2K Ω resistor
A84	LVDS_I2C_DAT	Pull up to 3.3V on module with a 2.2K Ω resistor
A85	GPI3	• GPI3/ACPRESENT • Pull up to 3.3V on module with a 10K Ω resistor
A86	RSVD(KBD_RST#)	NC
A87	RSVD(KBD_A20GATE)	NC
A92	SPI_MISO	No pull-up or pull-down on carrier
A94	SPI_CLK	No pull-up or pull-down on carrier
A95	SPI_MOSI	No pull-up or pull-down on carrier
A96	TPM_PP	NC on module
A97	TYPE10#	NC for COM R2.0
A98	SER1_TX	Diode isolated on module
A99	SER1_RX	Diode isolated on module
A101	SER2_TX	NC on module
A102	SER2_RX	NC on module

Table 1. CEQM67 COM Express signal design notes (continued)

Pin #	Signal	Purpose and usage
A103	LID#	Diode isolated on module
B3	LPC_FRAME#	No pull-up on carrier
B4	LPC_AD0	No pull-up on carrier
B5	LPC_AD1	No pull-up on carrier
B6	LPC_AD2	No pull-up on carrier
B7	LPC_AD3	No pull-up on carrier
B8	LPC_DRQ0#	No pull-up on carrier
B9	LPC_DRQ1#	No pull-up on carrier
B12	PWRBTN#	Pull up to 3.3V standby on module with a 100K Ω resistor
B13	SMB_CK	Pull up to 3.3V standby on module with a 8.2K Ω resistor
B14	SMB_DAT	Pull up to 3.3V standby on module with a 8.2K Ω resistor
B15	SMB_ALERT#	EC internal pull-up to 3.3V standby on module
B24	PWR_OK	• Output from carrier, mandatory for module to power on • Pull down on module with 100K Ω resistor
B27	WDT	WDT, output from EC, sink current at V_{OL}<1.6mA, source current at V_{OH} <0.2mA
B28	AC_SDIN2	PCH integrated pull-down resistor
B29	AC_SDIN1	PCH integrated pull-down resistor
B30	AC_SDIN0	PCH integrated pull-down resistor
B32	SPKR	Pull up to 3.3V on module with a 1K Ω resistor
B33	I2C_CK	Pull up to 3.3V standby on module with a 2.2K Ω resistor
B34	I2C_DAT	Pull up to 3.3V standby on module with a 2.2K Ω resistor
B35	THRM#	Pull up to 3.3V on module with a 10K Ω resistor
B38	USB_4_5_OC#	• Pull up to 3.3V suspend on module with an 8.2K Ω resistor • Open drain output from carrier to module
B44	USB_0_1_OC#	• Pull up to 3.3V suspend on module with an 8.2K Ω resistor • Open drain output from carrier to module
B47	EXCD1_PERST#	Pull up to 3.3V on module with a 10K Ω resistor
B48	EXCD1_CPPE#	Pull up to 3.3V on module with a 10K Ω resistor
B49	SYS_RESET#	EC internal pull-up to 3.3V standby on module
B66	WAKE0#	EC internal pull-up to 3.3V standby on module
B67	WAKE1#	EC internal pull-up to 3.3V standby on module
B79	LVDS_BKLT_EN	Pull down on module with a 100K Ω resistor
B88	BIOS_DIS1#	EC internal pull-up to 3.3V standby on module
B89	VGA_RED	Pull down on carrier with a 150 Ω resistor
B91	VGA_GRN	Pull down on carrier with a 150 Ω resistor
B92	VGA_BLU	Pull down on carrier with a 150 Ω resistor
B95	VGA_I2C_CK	Pull up to 3.3V on module with a 2.2K Ω resistor
B96	VGA_I2C_DAT	Pull up to 3.3V on module with a 2.2K Ω resistor
B97	SPI_CS#	No pull-up or pull-down on carrier
B101	FAN_PWMOUT	Diode isolated on module
B102	FAN_TACHIN	Diode isolated on module
B103	SLEEP#	Diode isolated on module

Table 1. CEQM67 COM Express signal design notes (continued)

Pin #	Signal	Purpose and usage
C3	USB_SSRX0-	NC on module
C4	USB_SSRX0+	NC on module
C6	USB_SSRX1-	NC on module
C7	USB_SSRX1+	NC on module
C9	USB_SSRX2-	NC on module
C10	USB_SSRX2+	NC on module
C12	USB_SSRX3-	NC on module
C13	USB_SSRX3+	NC on module
C15	DDI1_PAIR6+	• SDVO_STALL+ • AC couple on carrier
C16	DDI1_PAIR6-	• SDVO_STALL- • AC couple on carrier
C19	PCIE_RX6+	AC couple on carrier
C20	PCIE_RX6-	AC couple on carrier
C24	DDI1_HPD	Pull down on module with a 100K Ω resistor
C25	DDI1_PAIR4+	• SDVO_INT+ • AC couple on carrier
C26	DDI1_PAIR4-	• SDVO_INT- • AC couple on carrier
C29	DDI1_PAIR5+	• SDVO_TVCLKIN+ • AC couple on carrier
C30	DDI1_PAIR5-	• SDVO_TVCLKIN- • AC couple on carrier
C32	DDI2_AUX+	DDI2_AUX+
C33	DDI2_AUX-	DDI2_AUX-
C34	DDI2_CTRLCLK	Pull up to 3.3V on module with a 2.2K Ω resistor
C36	DDI3_AUX+	DDI3_AUX+
C37	DDI3_AUX-	DDI3_AUX-
C38	DDI3_CTRLCLK	Pull up to 3.3V on a module with a 2.2K Ω resistor
C39	DDI3_PAIR0+	AC couple on carrier
C40	DDI3_PAIR0-	AC couple on carrier
C42	DDI3_PAIR1+	AC couple on carrier
C43	DDI3_PAIR1-	AC couple on carrier
C44	DDI3_HPD	Pull down on module with a 100K Ω resistor
C46	DDI3_PAIR2+	AC couple on carrier
C47	DDI3_PAIR2-	AC couple on carrier
C49	DDI3_PAIR3+	AC couple on carrier
C50	DDI3_PAIR3-	AC couple on carrier
C73	SDVO_I2C_DAT	Pull up to 3.3V on a module with a 2.2K Ω resistor
D3	USB_SSTX0-	NC on module
D4	USB_SSTX0+	NC on module
D6	USB_SSTX1-	NC on module

Table 1. CEQM67 COM Express signal design notes (continued)

Pin #	Signal	Purpose and usage
D7	USB_SSTX1+	NC on module
D9	USB_SSTX2-	NC on module
D10	USB_SSTX2+	NC on module
D12	USB_SSTX3-	NC on module
D13	USB_SSTX3+	NC on module
D15	DDI1_AUX+	DDI1_AUX+
D16	DDI1_AUX-	DDI1_AUX-
D26	DDI1_PAIR0+	AC couple on carrier
D27	DDI1_PAIR0-	AC couple on carrier
D29	DDI1_PAIR1+	AC couple on carrier
D30	DDI1_PAIR1-	AC couple on carrier
D32	DDI1_PAIR2+	AC couple on carrier
D33	DDI1_PAIR2-	AC couple on carrier
D34	DDI2_CTRLDATA	Pull up to 3.3V on a module with a 2.2K Ω resistor
D36	DDI1_PAIR3+	AC couple on carrier
D37	DDI1_PAIR3-	AC couple on carrier
D38	DDI3_CTRLDATA	Pull up to 3.3V on a module with a 2.2K Ω resistor
D39	DDI2_PAIR0+	AC couple on carrier
D40	DDI2_PAIR0-	AC couple on carrier
D42	DDI2_PAIR1+	AC couple on carrier
D43	DDI2_PAIR1-	AC couple on carrier
D44	DDI2_HPD	Pull down on module with a 100K Ω resistor
D46	DDI2_PAIR2+	AC couple on carrier
D47	DDI2_PAIR2-	AC couple on carrier
D49	DDI2_PAIR3+	AC couple on carrier
D50	DDI2_PAIR3-	AC couple on carrier
D54	PEG_LANE_RV#	Pull up to 3.3V on module with a 100K Ω resistor
D73	DDI1_CTRLCLK	Pull up to 3.3V on module with a 2.2 Ω resistor

Chapter 2

Design Addendum to PICMG Documentation

In this chapter, design guidelines apply to the CEQM67 modules unless otherwise stated.

COM Express interfaces

This chapter covers special considerations for designing interfaces and features for your Radisys COM Express system. For a description of supported interfaces and features, refer to the *Product Manual* and *System Setup Utility Specification* for your Radisys COM Express module.

Note: There may be some known deviations from the PICMG specification due to design limitations of the processor and chipset. Refer to the *Product Manual* for details.

HDA digital audio interfaces

The newer Intel chipsets support only High Definition Audio (HDA), which has replaced the legacy AC'97 audio CODEC.

Do not connect AC_SDIN[0:2] to a one-way buffer, to ground, or to the power supply directly, since AC_SDIN[0:2] are bidirectional signals.

- When the system BIOS initializes audio CODECs during system startup, the HDA controller will allocate the physical addresses for the corresponding devices on the carrier board.
- After the system boots successfully, AC_SDIN[0:2] will serve as HDA data input lines.

SATA

The *PICMG COM.0 COM Express Base Specification* states that the SATA signal length on the COM Express carrier board should be no longer than three inches. It is recommended that you shorten your trace length as much as possible to attain the best signal quality.

To reduce the length of the SATA trace, place the SATA connector close to the board-to-board interconnectors. Avoid stubs and minimize the number of vias through the entire trace.

Table 2 shows the SATA 2.0/3.0 trace routing guidelines.

Table 2. SATA 2.0/3.0 trace routing guidelines

Parameter	Routing guidelines
Transfer rate	• 3 Gbps/lane for SATA 2.0 • 6 Gbps/lane for SATA 3.0
Maximum signal length allowance on carrier	3 inches
Differential impedance	100 Ω
Single-ended impedance	55 Ω
Spacing between RX pair and TX pairs (inter-pairs)	Min. 20mil
Spacing between differential pairs and high-speed periodic signals	Min. 50mil
Spacing between differential pairs and low-speed non-periodic signals	Min. 20mil

Table 2. SATA 2.0/3.0 trace routing guidelines (continued)

Parameter	Routing guidelines
Length matching between differential pairs (intra-pair)	Max. 5mil
Length matching between RX and TX pairs (inter-pair)	• No strict electrical requirements. • Keep difference within a 3-inch delta to minimize latency.
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plain	GND referenced preferred.
Spacing from edge of plane	Min. 40mil

SMBus/I^{2}C

DC specifications

The Radisys modules support high power SMBus devices, as defined in the *System Management Bus (SMBus) Specification Version 2.0*. Approximately 4mA of current sink is provided by the module while the system maintains the SMBus signal output low voltage $V_{OL,MAX}$ at 0.4V.

High power SMBus devices can be routed directly to the SMBus pins on the board-to-board interconnectors. However, if you are designing an interface for low power SMBus devices, such as a smart battery subsystem, you can route the SMBus trace through bus buffers to the device. Refer to the schematics of the CR300 carrier board for examples.

I/O address

The SMBus and I^{2}C bus devices on your carrier board must not conflict with addresses on the module. Refer to the *Product Manual* for information about SMBus and I^{2}C bus addresses used on the module.

DDI

The DDI signal length on the COM Express carrier board should be no longer than seven inches for the auxiliary link and five inches for the main link. It is recommended that you shorten your trace length as much as possible to attain the best signal quality.

To reduce the length of the DDI trace, place the DDI connector close to the board-to-board interconnectors. Avoid stubs and minimize the number of vias through the entire trace.

Table 3 shows the DDI trace routing guidelines.

Table 3. DDI (DP/HDMI/SDVO) trace routing guidelines

Parameter	Routing guidelines
Maximum signal length allowance on carrier	• 7 inches for Auxiliary link • 5 inches for DDI main link
Differential impedance	90 Ω
Single-ended Impedance	50 Ω

Table 3. DDI (DP/HDMI/SDVO) trace routing guidelines (continued)

Parameter	Routing guidelines
Spacing between RX pair and TX pairs (inter-pairs)	Min. 20mil
Spacing between differential pairs and high-speed periodic signals	Min. 50mil
Spacing between differential pairs and low-speed non-periodic signals	Min. 20mil
Length matching between differential pairs (intra-pair)	Max. 5mil
Length matching between RX and TX pairs (inter-pair)	• No strict electrical requirements. • Keep difference within a 3-inch delta to minimize latency.
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plain	GND referenced preferred.
Spacing from edge of plane	Min. 40mil

PCI Express

The PCI Express signal length on the COM Express carrier board should be no longer than seven inches. It is recommended that you shorten your trace length as much as possible to attain the best signal quality.

To reduce the length of the PCI Express trace, place the PCI Express connector close to the board-to-board interconnectors. Avoid stubs and minimize the number of vias through the entire trace.

Table 4 shows the PCI Express 2.0 trace routing guidelines.

Table 4. PCI Express 2.0 trace routing guidelines

Parameter	Routing guidelines
Transfer rate/PCIe lane	5 Gbps
Maximum signal length allowance on carrier	7 inches
Differential impedance	85 Ω
Single-ended impedance	50 Ω
Spacing between differential pairs and high-speed periodic signals	Min. 50mil
Spacing between differential pairs and low-speed non-periodic signals	Min. 20mil
Length matching between differential pairs (intra-pair)	Max. 5mil
Spacing from edge of plane	Min. 40mil

PEG

The PEG (PCI Express Graphics) signal length on the COM Express carrier board should be no longer than four inches. It is recommended that you shorten your trace length as much as possible to attain the best signal quality.

To reduce the length of the PEG trace, place the PEG connector close to the board-to-board interconnectors. Avoid stubs and minimize the number of vias through the entire trace.

A re-driver is recommended to attain the best signal integrity for traces longer than four inches.

Table 5 show the PEG trace routing guidelines.

Table 5. PEG trace routing guidelines

Parameter	Routing guidelines
Transfer rate/PCIe lane	5 Gbps
Maximum signal length allowance on carrier	4 inches
Differential impedance	85 Ω
Single-ended impedance	50 Ω
Spacing between RX pair and TX pairs (inter-pair) (s)	Min. 20mil
Spacing between differential pairs and high-speed periodic signals	Min. 50mil
Spacing between differential pairs and low-speed non-periodic signals	Min. 20mil
Length matching between differential pairs (intra-pair)	Max. 5mil
Length matching between RX and TX pairs (inter-pair)	• No strict electrical requirements. • Keep difference within a 3-inch delta to minimize latency.
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plain	GND referenced preferred.
Spacing from edge of plane	Min. 40mil

SPI

The SPI signal length on the COM Express carrier board should be no longer than 4.5 inches. It is recommended that you shorten your trace length as much as possible to attain the best signal quality.

To reduce the length of the SPI trace, place the SPI device close to the board-to-board interconnectors. Avoid stubs and minimize the number of vias through the entire trace.

Table 6 shows the SPI signal layout and trace routing guidelines.

Table 6. SPI signal layout and trace routing guidelines

Signal name	Impedance	Trace length	Length matching	Comments
SPI_MOSI	55 Ω	Max. 4.5 inches	Within one inch per segment	If there are two devices (SPI ROM and Header) on carrier, the routing is in daisy chain topology.
SPI_MISO				
SPI_CLK				
SPI_CS#				
SPI_POWER	Power for SPI devices. The trace width shall be minimally 20mil.			

USB 3.0

The USB 3.0 signal length on the COM Express carrier board should be no longer than five inches. It is recommended that you shorten your trace length as much as possible to attain the best signal quality.

To reduce the length of the USB 3.0 trace, place the USB 3.0 device close to the board-to-board interconnectors. Avoid stubs and minimize the number of vias through the entire trace.

Table 7 shows the USB 3.0 trace routing guidelines.

Table 7. USB3.0 trace routing guidelines

Parameter	Routing guidelines
Transfer rate/PCIe lane	5 Gbps
Maximum signal length allowance on carrier	5 inches
Differential impedance	90 Ω
Single-ended impedance	50 Ω
Spacing between RX pair and TX pairs (inter-pair) (s)	Min. 20mil
Spacing between differential pairs and high-speed periodic signals	Min. 50mil
Spacing between differential pairs and low-speed non-periodic signals	Min. 20mil
Length matching between differential pairs (intra-pair)	Max. 150mil
Length matching between RX and TX pairs (inter-pair)	No requirements, but try to match.
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plain	GND referenced preferred.
Spacing from edge of plane	Min. 40mil

Power and reset

ATX- and AT-style power control

ATX and AT power sequencing diagrams

Make sure that VCC_5V_SBY, if used, comes up before VCC_12V. Otherwise, your system may experience problems.

PWROK must be active after VCC_12V comes up and inactive before VCC_12V goes down.

Chapter 3

Changes and Migration Strategies

Compared to Revision 1.0 of the *PICMG COM.0 COM Express Base Specification*, the Revision 2.0 specification is an evolutionary initiative to refresh the COM Express specification in support of new technologies and interfaces. The Revision 2.0 specification also deals with legacy interface obsolescence issues.

Note: COM Express R2.0 defines three sizes of the COM Express modules and new pinout types. Refer to the *PICMG COM.0 COM Express Base Specification* for details.

COM Express R2.0 changes from R1.0

New interfaces

Digital display interfaces (in place of PCI interface)

COM Express R2.0 addresses support for up to three digital display interfaces (Port 1, Port 2, Port 3), each can support a High-Definition Multimedia Interface (HDMI), DisplayPort or DVI interfaces. Port 1 can also be configured for the SDVO interface.

- HDMI provides an audio/video interface that can carry TV and PC video signals, including HD video, along with an accompanying digital audio stream.
- DisplayPort, standardized by the Video Electronics Standards Association, drives both external displays and internal display panels.
- SDVO is demultiplexed from the PEG port but multiplexed with the digital display interface (Port 1). Multiplexing SDVO with DDI Port 1 instead of PEG is necessary due to the evolution of the underlying silicon technologies in support of the newer digital display interfaces.

Note: The PCI interface has been removed and the pins are now used to support the digital display interfaces and additional PCI Express lanes.

PCI Express

To augment the continued success and adoption of PCI Express, COM Express R2.0 adds two additional PCI Express lanes [6:7]. PCI Express Gen2 signaling is added for all PCI Express lanes.

Note: The PCI interface has been removed and the pins are now used to support the digital display interfaces and additional PCI Express lanes.

USB 3.0 (in place of IDE interface)

COM Express R1.0 supported eight USB 2.0 host ports, each composed of a single differential signal pair. USB 2.0 supported transfer speeds up to 480 Megabits per second.

The USB 3.0 specification expands upon USB capabilities and adds SuperSpeed functionality, extending transfer speeds up to 5 Gigabits per second. To ensure USB signaling rates, USB 3.0 SuperSpeed increases are achieved with the addition of two differential pairs in addition to the legacy USB 2.0 non-SuperSpeed differential pair.

To support USB 3.0, COM Express R2.0 adds support for USB 3.0 to four of the eight existing USB 2.0 ports with the addition of SuperSpeed pins for the first four USB ports.

Note: The IDE interface has been removed and the pins are now used to support SuperSpeed differential pairs for USB 3.0 ports.

Legacy obsolescence

AC'97 vs. High Definition Audio

COM Express R1.0 supported audio through an AC'97 interface supporting the Intel Audio Codec '97 standard. Similar to the evolution of the digital display interfaces, the audio interface has also evolved and upgraded COM Express R2.0 to support audio support for a High Definition Audio (HDA) interface. The AC'97 interface and HDA interfaces share the same COM Express interface pins and are largely compatible.

Serial ports

Despite advances such as USB, the serial port remains a key interface in embedded systems due to its simplicity, especially regarding the software stack required to support the interface. On COM Express R1.0 carrier boards, an individual LPC Super I/O chip was required to provide serial ports.

COM Express R2.0 adds two TTL level two-wire serial port interfaces. The carrier board can use these interfaces as-is, or add specific drivers to support other external serial interfaces such as RS-232, RS-422, or other serial signaling standards.

SPI

COM Express R1.0 supported system boot from the carrier BIOS via the BIOS_DISABLE# pin, which signals the module that the carrier BIOS should be used instead of the module BIOS. Carriers boards utilizing the BIOS_DISABLE# signal placed the alternate BIOS image in a Firmware Hub (FWH) located on the LPC interface on the carrier.

As technology has evolved, modern processor chipsets utilize the Serial Peripheral Interface (SPI) to interface to the flash device containing the BIOS image. COM Express R2.0 adds support for the SPI interface on formerly reserved pins to address obsolescence of the FWH while continuing to support the LPC interface. The LPC interface is still frequently used on carriers to support simple lower bandwidth devices.

TV Out

The TV Out interface was provided in COM Express R1.0 to support Component, Composite, and S-video analog video.

With the evolution to digital display interfaces, this interface has become largely obsolete and very infrequently used. As a result, COM Express R2.0 has removed TV Out support.

Miscellaneous pins

COM Express R2.0 also adds support for miscellaneous I/O signals commonly found in embedded and mobile systems.

- For active cooling, a fan tachometer input and pulse width modulation (PWM) output are added to enable monitoring and control of a fan subsystem without requiring an external controller.
- For mobile battery-powered applications, the sideband signals LID and SLEEP have been added in support of signaling external ACPI power management events.
- I^2C is moved to standby power rail to allow interrogation of a carrier board EEPROM for module configuration strappings.
- Multi-master support for the I^2C bus is added.
- Optional USB client support on USB port 7 is added.
- Optional SDIO support using the existing GPIO signals is added.

Redesigning a R1.0 Type 2 carrier board for R2.0 Type 6 modules

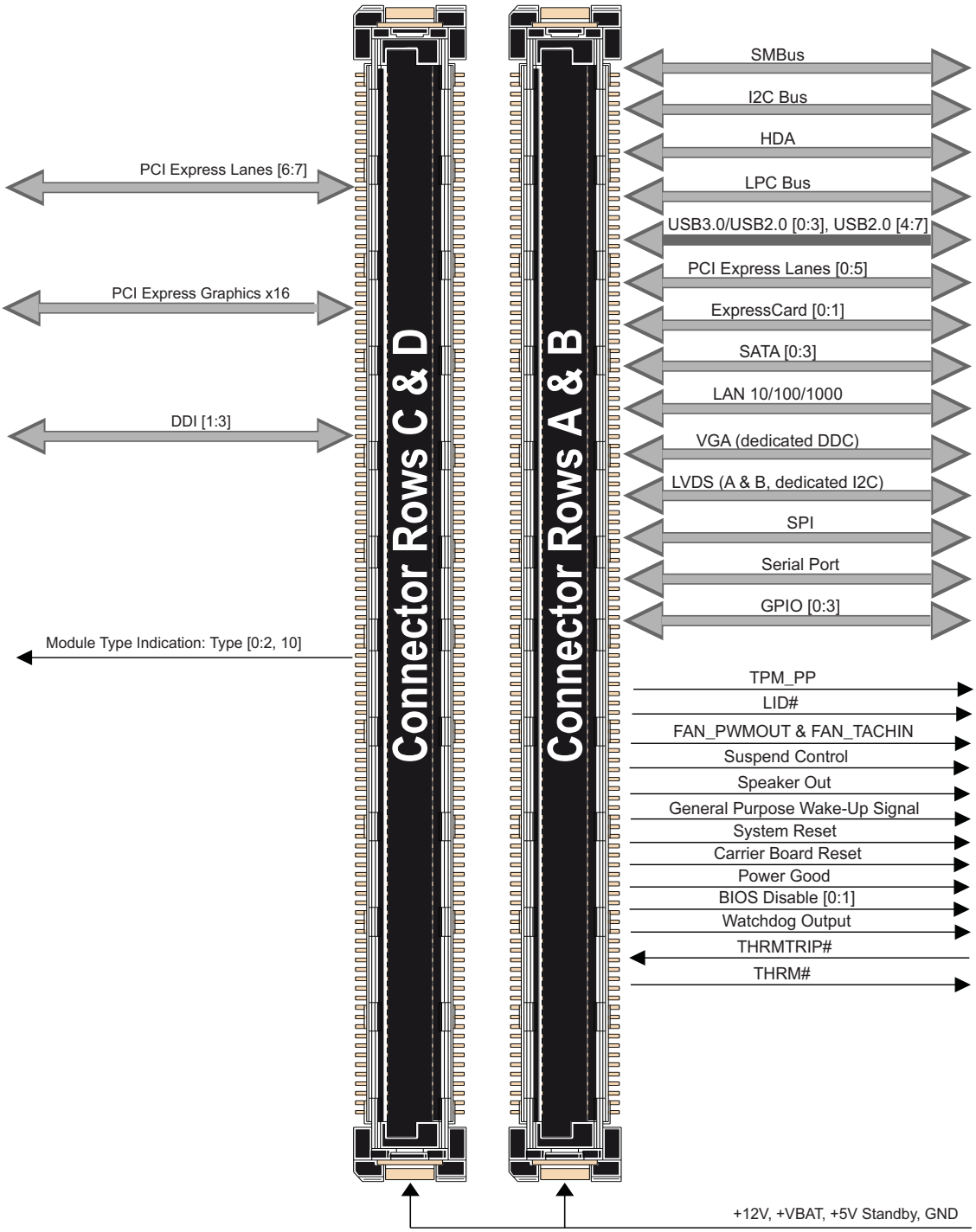
Essentially, the R2.0 Type 6 module is a technology evolution of Type 2 that drops legacy PCI and IDE interfaces in favor of digital display interfaces and USB 3.0 SuperSpeed interfaces. Changes on the A/B connector in Type 6 were kept to the absolute minimum, and provide backward compatibility with the existing R1.0 types.

If applications utilizing R1.0 Type 2 have already moved beyond using the legacy PCI and IDE interfaces, it is possible to redesign the R1.0 Type 2 carrier board to be compatible with R2.0 Type 6 to take advantage of the newer interfaces.

R2.0 Type 6 pinout representation

Figure 1 shows a graphical representation for R2 Type 6 signals on the A-B and C-D board-to-board interconnectors.

Figure 1. COM Express R2.0 Type 6 pinout representation



R1.0 Type 2 vs. R2.0 Type 6 pinout comparison

Table 8 shows the different pinout definitions on the board-to-board connectors between COM Express R1.0 Type 2 and COM Express R2.0 Type 6. For complete information on all pinouts, refer to the *PICMG COM.0 COM Express Base Specification*. Migration strategies are included when redesigning a R1.0 Type 2 carrier board to accept R2.0 Type 6 modules.

Table 8. R1.0 Type 2 vs. R2.0 Type 6 pinout comparison

Pin #	Signal		Migration strategy
	COM Express R2 Type 6	COM Express R1 Type 2	
A34	BIOS_DIS0#	BIOS_DISABLE#	No changes needed.
A86	RSVD	KBD_RST#	No changes needed.
A87	RSVD	KBD_A20GATE#	• No hardware changes needed. • For those applications previously utilizing A20_GATE#, the software and/or tools should be updated to no longer use this functionality.
A91	SPI_POWER	RSVD	No changes needed.
A92	SPI_MISO	RSVD	No changes needed.
A94	SPI_CLK	RSVD	No changes needed.
A95	SPI_MOSI	RSVD	No changes needed.
A96	TPM_PP	GND	No changes needed.
A97	TYPE10#	VCC_12V	No changes needed.
A98	SER0_TX	VCC_12V	Design serial ports isolated on carrier or no changes if the features are required
A99	SER0_RX	VCC_12V	
A101	SER1_TX	VCC_12V	
A102	SER1_RX	VCC_12V	
A103	LID#	VCC_12V	No changes needed.
B88	BIOS_DIS1#	RSVD	No changes needed. ***Note:*** This pin must not be pulled to ground.
B97	SPI_CS#	TV_DAC_A	Devices on the TV out interface should be removed.
B98	RSVD	TV_DAC_B	No changes needed.
B99	RSVD	TV_DAC_C	No changes needed.
B101	FAN_PWMOUT	VCC_12V	No changes needed.
B102	FAN_TACHIN	VCC_12V	No changes needed.
B103	SLEEP#	VCC_12V	No changes needed.

Table 8. R1.0 Type 2 vs. R2.0 Type 6 pinout comparison (continued)

Pin #	Signal		Migration strategy
	COM Express R2 Type 6	COM Express R1 Type 2	
C2	GND	IDE_D7	• Devices on the IDE and PCI interfaces should be removed. • Pull-up resistors on the IDE and PCI interfaces should be removed from the carrier board.
C3	USB_SSRX0-	IDE_D6	
C4	USB_SSRX0+	IDE_D3	
C5	GND	IDE_D15	
C6	USB_SSRX1-	IDE_D8	
C7	USB_SSRX1+	IDE_D9	
C8	GND	IDE_D2	
C9	USB_SSRX2-	IDE_D13	
C10	USB_SSRX2+	IDE_D1	
C12	USB_SSRX3-	IDE_D14	
C13	USB_SSRX3+	IDE_IORDY	
C14	GND	IDE_IOR#	
C15	DDI1_PAIR6+	PCI_PME#	
C16	DDI1_PAIR6-	PCI_GNT2#	
C17	RSVD	PCI_REQ2#	
C18	RSVD	PCI_GNT1#	
C19	PCIE_RX6+	PCI_REQ1#	
C20	PCIE_RX6-	PCI_GNT0#	
C22	PCIE_RX7+	PCI_REQ0#	
C23	PCIE_RX7-	PCI_RESET#	
C24	DDI1_HPD	PCI_AD0	
C25	DDI1_PAIR4+	PCI_AD2	
C26	DDI1_PAIR4-	PCI_AD4	
C27	RSVD	PCI_AD6	
C28	RSVD	PCI_AD8	
C29	DDI1_PAIR5+	PCI_AD10	
C30	DDI1_PAIR5-	PCI_AD12	
C32	DDI2_CTRLCLK_AUX+	PCI_AD14	
C33	DDI2_CTRLCLK_AUX-	PCI_C/BE1#	
C34	DDI2_CTRLCLK_SEL	PCI_PERR#	
C35	RSVD	PCI_LOCK#	
C36	DDI3_CTRLCLK_AUX+	PCI_DEVSEL#	
C37	DDI3_CTRLCLK_AUX-	PCI_IRDY#	
C38	DDI3_CTRLCLK_SEL	PCI_C/BE2#	
C39	DDI3_PAIR0+	PCI_AD17	
C40	DDI3_PAIR0-	PCI_AD19	
C42	DDI3_PAIR1+	PCI_AD21	
C43	DDI3_PAIR1-	PCI_AD23	

Table 8. R1.0 Type 2 vs. R2.0 Type 6 pinout comparison (continued)

Pin #	Signal		Migration strategy
	COM Express R2 Type 6	COM Express R1 Type 2	
C44	DDI3_HPD	PCI_C/BE3#	• Devices on the IDE and PCI interfaces should be removed. • Pull-up resistors on the IDE and PCI interfaces should be removed from the carrier board.
C45	RSVD	PCI_AD25	
C46	DDI3_PAIR2+	PCI_AD27	
C47	DDI3_PAIR2-	PCI_AD29	
C48	RSVD	PCI_AD31	
C49	DDI3_PAIR3+	PCI_IRQA#	
C50	DDI3_PAIR3-	PCI_IRQB#	
C73	GND	SDVO_DATA	
D2	GND	IDE_D5	• Devices on the IDE and PCI interfaces should be removed. • Pull-up resistors on the IDE and PCI interfaces should be removed from the carrier board.
D3	USB_SSTX0-	IDE_D10	
D4	USB_SSTX0+	IDE_D11	
D5	GND	IDE_D12	
D6	USB_SSTX1-	IDE_D4	
D7	USB_SSTX1+	IDE_D0	
D8	GND	IDE_REQ	
D9	USB_SSTX2-	IDE_IOW#	
D10	USB_SSTX2+	IDE_ACK#	
D12	USB_SSTX3-	IDE_IRQ	
D13	USB_SSTX3+	IDE_A0	
D14	GND	IDE_A1	
D15	DDI1_CTRLCLK_AUX+	IDE_A2	
D16	DDI1_CTRLCLK_AUX-	IDE_CS1#	
D17	RSVD	IDE_CS3#	
D18	RSVD	IDE_RESET#	
D19	PCIE_TX6+	PCI_GNT3#	
D20	PCI_TX6-	PCI_REQ3#	
D22	PCIE_TX7+	PCI_AD1	
D23	PCIE_TX7-	PCI_AD3	
D24	RSVD	PCI_AD5	
D25	RSVD	PCI_AD7	
D26	DDI1_PAIR0+	PCI_C/BE0#	
D27	DDI1_PAIR0-	PCI_AD9	
D28	RSVD	PCI_AD11	
D29	DDI1_PAIR1+	PCI_AD13	
D30	DDI1_PAIR1-	PCI_AD15	
D32	DDI1_PAIR2+	PCI_PAR	
D33	DDI1_PAIR2-	PCI_SERR#	
D34	DDI1_DDC_AUX_SEL	PCI_STOP#	

Table 8. R1.0 Type 2 vs. R2.0 Type 6 pinout comparison (continued)

Pin #	Signal		Migration strategy
	COM Express R2 Type 6	COM Express R1 Type 2	
D35	RSVD	PCI_TRDY#	• Devices on the IDE and PCI interfaces should be removed. • Pull-up resistors on the IDE and PCI interfaces should be removed from the carrier board.
D36	DDI1_PAIR3+	PCI_FRAME#	
D37	DDI1_PAIR3-	PCI_AD16	
D38	RSVD	PCI_AD18	
D39	DDI2_PAIR0+	PCI_AD20	
D40	DDI2_PAIR0-	PCI_AD22	
D42	DDI2_PAIR1+	PCI_AD24	
D43	DDI2_PAIR1-	PCI_AD26	
D44	DDI2_HPD	PCI_AD28	
D45	RSVD	PCI_AD30	
D46	DDI2_PAIR2+	PCI_IRQC#	
D47	DDI2_PAIR2-	PCI_IRQD#	
D48	RSVD	PCI_CLKRUN#	
D49	DDI2_PAIR3+	PCI_M66EN	
D50	DDI2_PAIR3-	PCI_CLK	
D57	TYPE2#	TYPE2#	This pin is pulled to ground on R2.0 Type 6 modules. This pin must not be used for pinout type detection on R1.0 Type 2 carrier boards.
D73	GND	SDVO_CLK	No changes needed.
D77	RSVD	IDE_CBLID#	No changes needed.
D97	RSVD	PEG_ENABLE#	No changes needed.

Feature summary of a migration system

Table 9 summaries the features and interfaces of a migration system comprising a standard R2.0 Type 6 module and a redesigned R1.0 Type 2 carrier board. Features of a standard R1.0 Type 2 carrier board are included in the second column as a reference.

Table 9. Features in the migration system

Standard R2.0 Type 6 module	Standard R1.0 Type 2 carrier board	Migration system
LAN port	LAN port	LAN port
SATA: 4 ports	SATA: 4 ports	SATA: 4 ports
VGA port	VGA port	VGA port
LVDS interface	LVDS interface	LVDS interface
—	TV Out	—
HDA interface	HDA Codec	HDA Codec
USB: 8 USB 2.0 ports	USB: 8 USB 2.0 ports	USB: 8 USB 2.0 ports
ExpressCard: 2 interfaces	ExpressCard: 2 interfaces	ExpressCard: 2 interfaces
LPC interface	LPC interface	LPC interface
PCI Express lanes [0:5]	PCI Express lanes [0:5]	PCI Express lanes [0:5]
PCI Express lanes [6:7]	—	—
GPIO: 4 input, 4 output	GPIO: 4 input, 4 output	GPIO: 4 input, 4 output
I^2C interface	I^2C interface	I^2C interface
SMBus interface	SMBus interface	SMBus interface
SPI interface	—	—
—	A20_GATE#	—
Serial: 2 ports	—	—
LID#	—	—
SLEEP#	—	—
TPM_PP	—	—
Fan interface	—	—
USB 3.0: 4 ports	—	—
DDI interface: 3 ports	—	—
PEG x16	PEG x16	PEG x16
—	SDVO multiplexing with PEG	—
—	IDE interface	—
—	PCI interface	—

PCI Express Gen2 migration

COM Express R2.0 Type 6 modules support both Gen1 and Gen2 PCI Express operation. The allowance for PCI Express trace lengths on the carrier board is seven inches except for PCI Express x16 signals that require a trace length shorter than 4.45 inches.

To support Gen 2 operation, the maximum allowed PCI Express trace length needs to be shorter than that for Gen 1 operation. If the existing R1.0 Type 2 carrier board does not meet the required allowance, the module needs to operate in Gen 1 mode.

Chapter 4

Thermal Design and Validation

Design considerations

To prevent the system from overheating, consider the following before designing a custom thermal solution.

- The operating environment, such as temperature and relative humidity
- The form factor of the COM Express module and the placement of the main components
- Total power targets of the COM Express platform, especially thermal limits of the main thermal sources, such as the processor, chipsets, memory modules, and Ethernet
- Height constraints, such as the chassis height and stack-up heights of the COM Express module and carrier board

For detailed information about your Radisys module, refer to the *Product Manual*.

Validation procedures

Power dissipation will vary widely according to the applications and workload. A good thermal solution can ensure the system will operate below each component‘s thermal limit under a set of specific boundary conditions. Refer to the *Product Manual* for thermal limits of the main thermal sources on your Radisys module.

To measure thermal performance accurately, it is best to perform validation tests in your specific environment and boundary conditions. Radisys thermal solutions have been validated with the following boundary conditions:

- Highest local ambient temperature that your Radisys module is designed to support
- Main thermal sources run at close to TDP

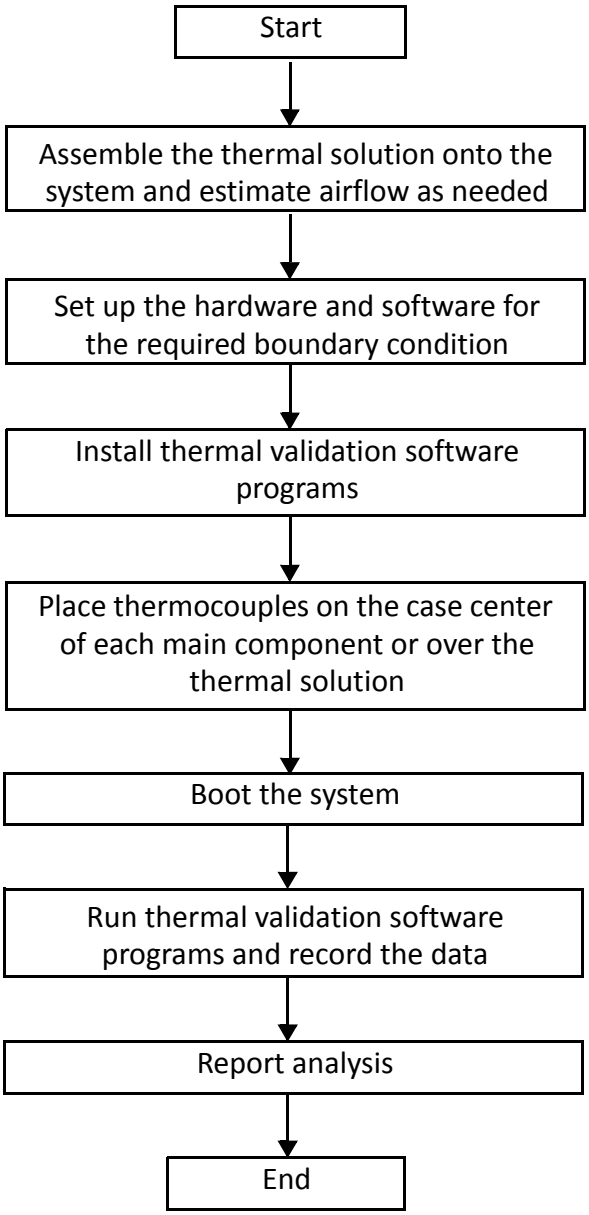
Note: Thermal efficiency is affected by the surface finish, flatness, contact area of the heat sink, applied mounting pressure, thickness of thermal interface material, and air velocity. Inaccurate power or interface resistance values can result in higher-than-expected temperatures.

General workflow

Figure 2 shows the general workflow for thermal validation. For detailed instructions, refer to the following documentation:

- For instructions on setting up the system, refer to the *Quick Start Guide*.
- For hardware features and BIOS configuration, refer to the *Product Manual* and *System Setup Utility Specification*.
- For instructions on installing and operating thermal validation software programs, refer to the software documentation.

Figure 2. General thermal validation workflow



Use standard formula to estimate the airflow requirement

When a passive heatsink or heat spreader is designed, a forced air flow may be required. Use the following formula to estimate the required airflow:

$$CFM = \frac{1.76 \times Ptotal(Watts)}{(Tout - Tin)(^{\circ}C)}$$

where P_{total} is the total power dissipated by the main thermal sources on your Radisys module, (T_{out} - T_{in}) is the temperature rise from intake to exit air (maximum allowed), and CFM is the estimated airflow requirement in cubic feet per minute.

Use software programs to run stress tests

Thermal Analysis Tool

The Thermal Analysis Tool (TAT) can be obtained from Intel Corporation, www.intel.com. TAT can perform stress tests on the processor and monitor the real-time processor junction temperature (Tj).

For further information, refer to the TAT documentation.

3DMark

The 3DMark tool can be obtained from Futuremark Corporation, www.futuremark.com. 3DMark determines the performance of graphics cards.

For further information, refer to the 3DMark documentation.

Prime

The Prime tool can be obtained from Mersenne Prime, www.mersenne.org/freesoft.htm. Different versions apply to specific operating systems.

For example, Prime95 can run under Windows XP. This tool can be configured to test various components by changing the fast fourier transform (FFT) size. Three configuration options are pre-defined:

- Small FFTs (maximum FPU stress, data fits in L2 cache, minimal RAM testing)
- In-place large FFTs (maximum heat, power consumption, some RAM testing)
- Blend (some tests on everything, extensive RAM testing)

For further information, refer to the Prime documentation.