

A

B

C

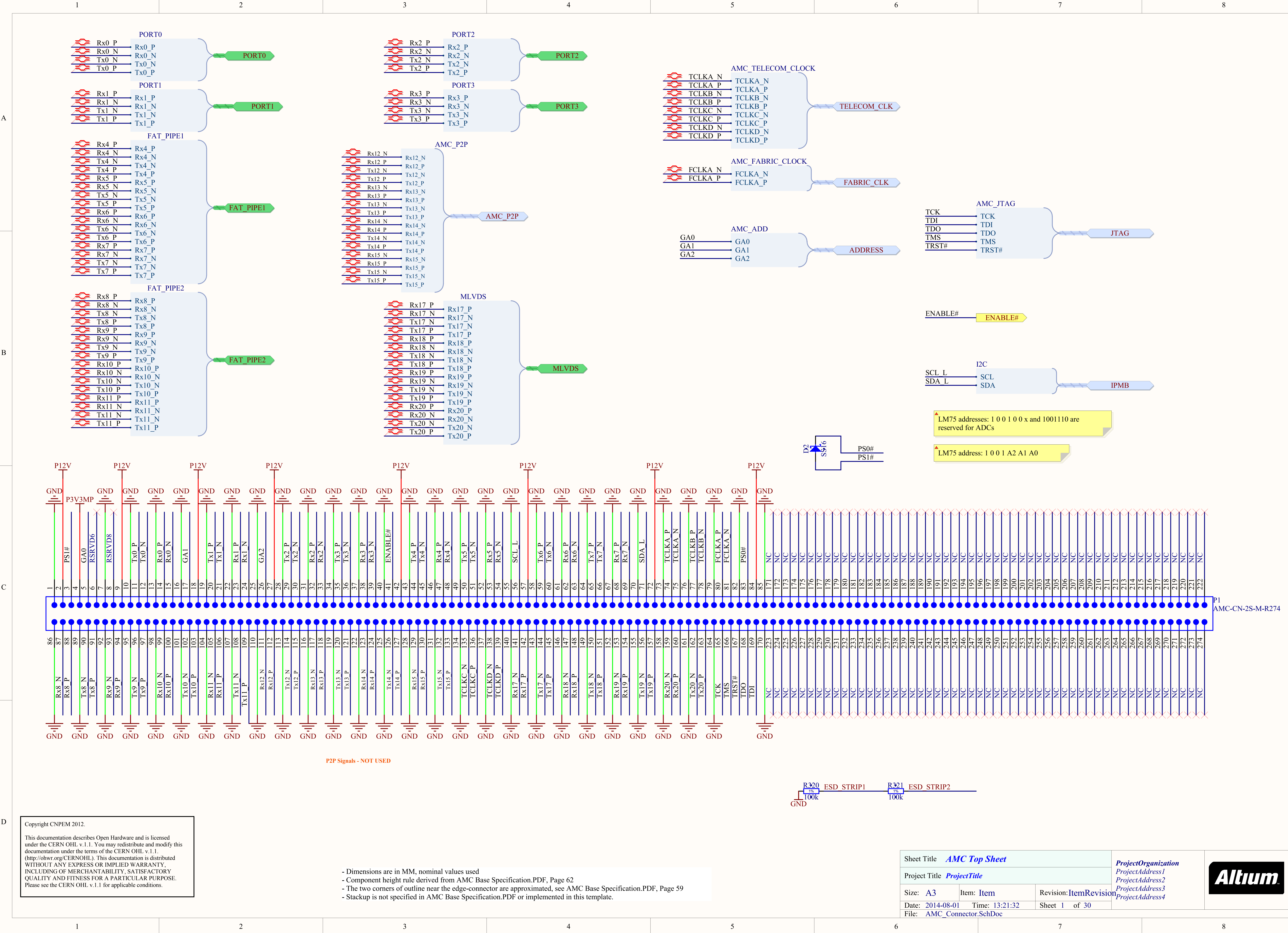
D

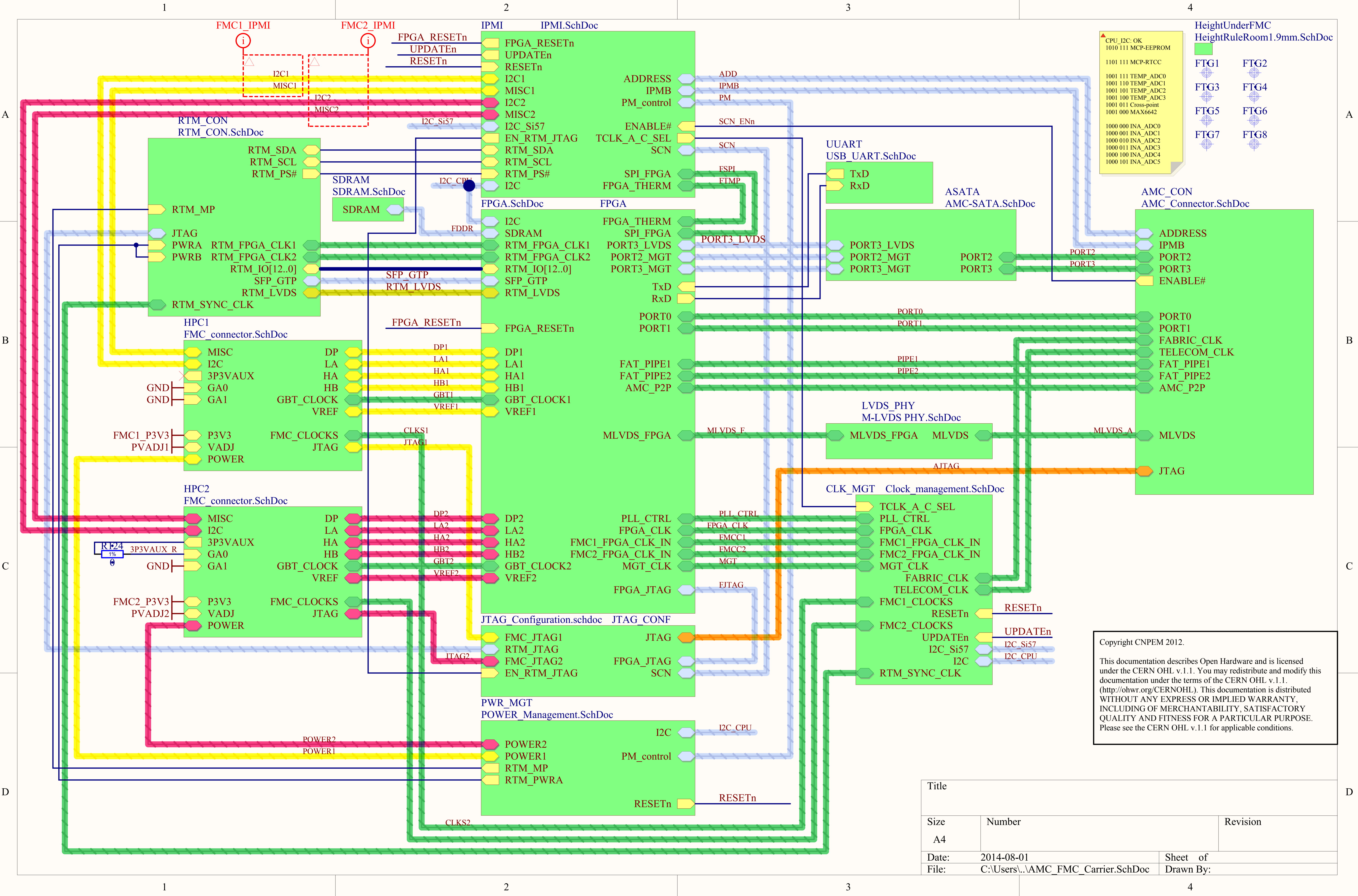
A

B

C

D





CPU\_I2C: OK  
1010 111 MCP-EEPROM  
1101 111 MCP-RTCC  
1001 111 TEMP\_ADC0  
1001 110 TEMP\_ADC1  
1001 101 TEMP\_ADC2  
1001 100 TEMP\_ADC3  
1001 011 Cross-point  
1001 000 MAX6642  
1000 000 INA\_ADC0  
1000 001 INA\_ADC1  
1000 010 INA\_ADC2  
1000 011 INA\_ADC3  
1000 100 INA\_ADC4  
1000 101 INA\_ADC5

HeightUnderFMC  
HeightRuleRoom1.9mm.SchDoc  
FTG1 FTG2  
FTG3 FTG4  
FTG5 FTG6  
FTG7 FTG8

AMC\_CON  
AMC\_Connector.SchDoc  
ADDRESS  
IPMB  
PORT2  
PORT3  
ENABLE#  
PORT0  
PORT1  
FABRIC\_CLK  
TELECOM\_CLK  
FAT\_PIPE1  
FAT\_PIPE2  
AMC\_P2P  
MLVDS  
MLVDS\_F  
MLVDS\_A  
JTAG

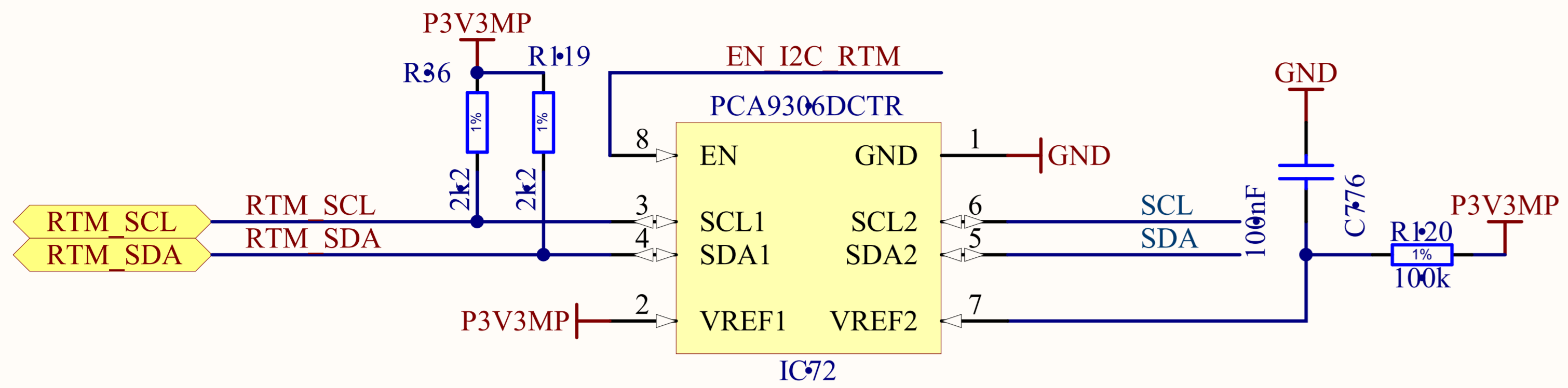
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Title		
Size	Number	Revision
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\AMC_FMC_Carrier.SchDoc	Drawn By:

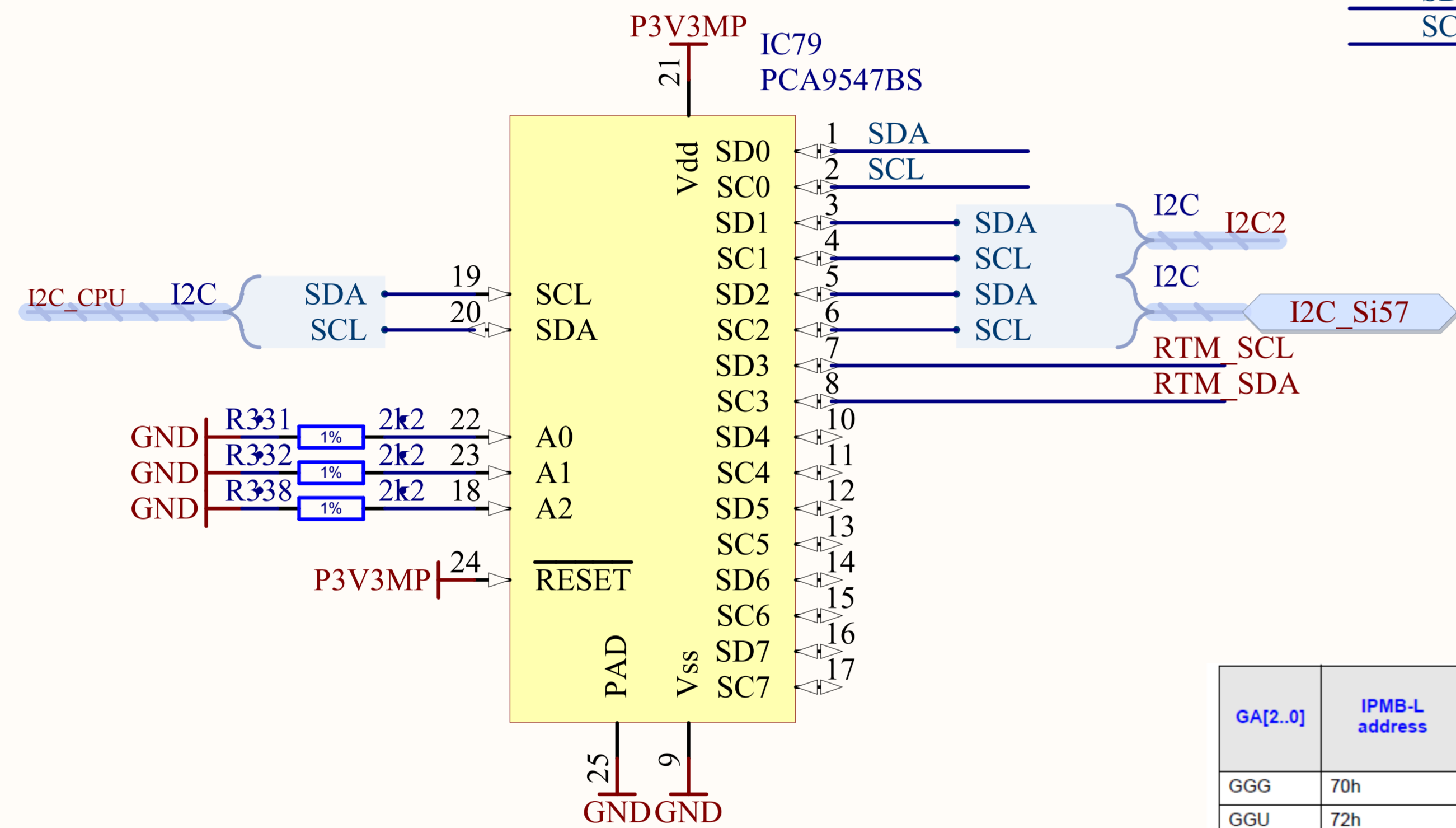




A

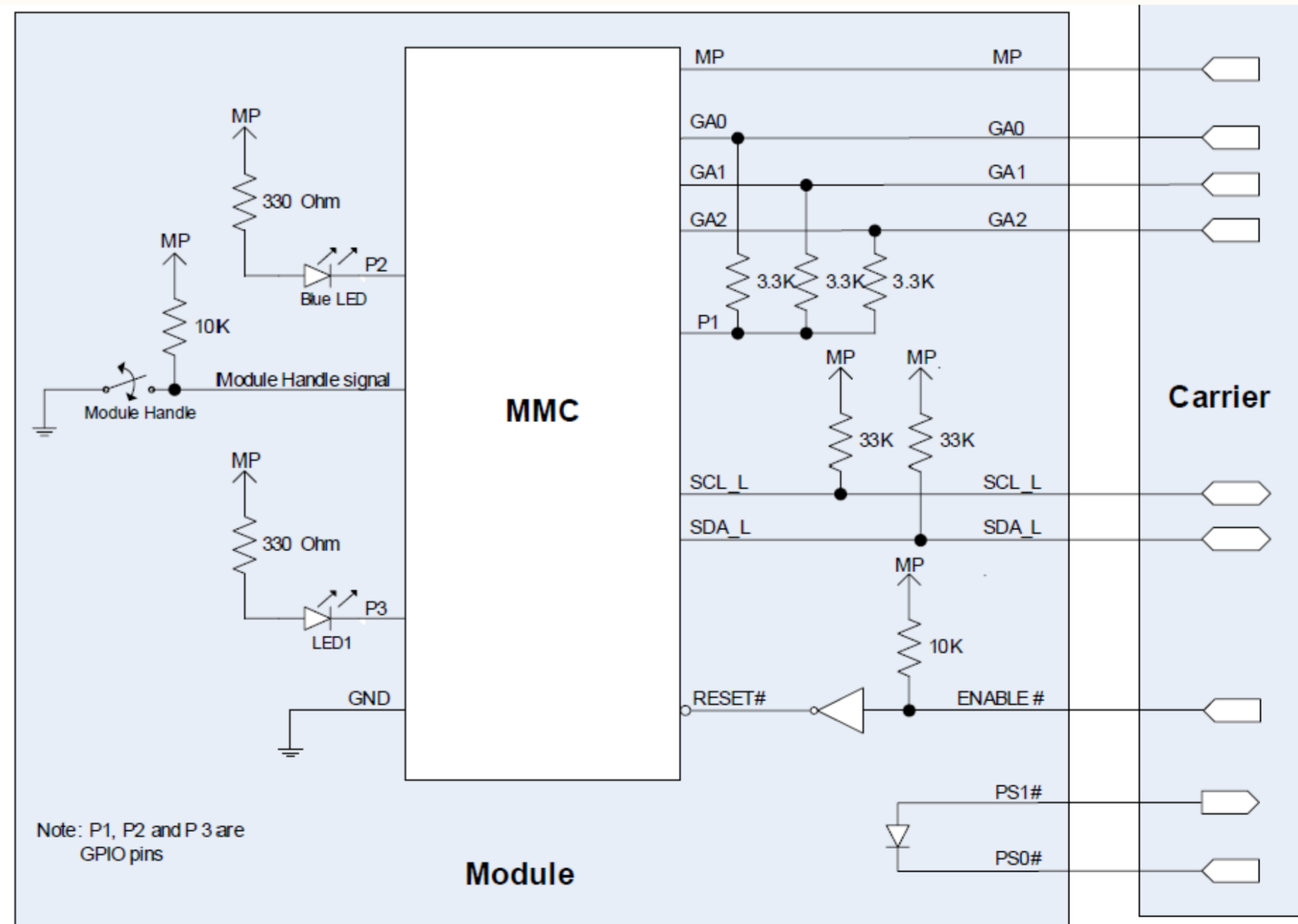


B



C

GA[2..0]	IPMB-L address	MicroTCA Carrier's AMC Slot ID	AMC Carrier AdvancedTCA Board's AMC Slot ID	Module Physical address	
				Site Number	Site type
GGG	70h	Reserved	Reserved	NA	NA
GGU	72h	1	A1	1	AMC (07h)
GUG	74h	2	A2	2	AMC (07h)
GUU	76h	3	A3	3	AMC (07h)
UGG	78h	4	A4	4	AMC (07h)
UGU	7Ah	5	B1	5	AMC (07h)
UUG	7Ch	6	B2	6	AMC (07h)
UUP	7Eh	7	B3	7	AMC (07h)
UPU	80h	8	B4	8	AMC (07h)
UPP	82h	9	NA	9	AMC (07h)
PUU	84h	10	NA	10	AMC (07h)
PUP	86h	11	NA	11	AMC (07h)
PPU	88h	12	NA	12	AMC (07h)
GGP	8Ah	NA	NA	13	AMC (07h)
GUP	8Ch	NA	NA	14	AMC (07h)
GPG	8Eh	NA	NA	15	AMC (07h)
GPU	90h	NA	NA	16	AMC (07h)
GPP	92h	NA	NA	17	AMC (07h)
UGP	94h	NA	NA	18	AMC (07h)
UPG	96h	NA	NA	19	AMC (07h)
PGG	98h	NA	NA	20	AMC (07h)
PGU	9Ah	NA	NA	21	AMC (07h)
PGP	9Ch	NA	NA	22	AMC (07h)
PUG	9Eh	NA	NA	23	AMC (07h)
PPG	A0h	NA	NA	24	AMC (07h)
UUU	A2h	NA	NA	25	AMC (07h)
PPP	A4h	NA	NA	26	AMC (07h)



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Title		
Size	Number	Revision
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\IPMI.SchDoc	Drawn By:

A

B

C

D



A

A

B

B

C

C

D

D

Changed values input caps

Changed values input caps

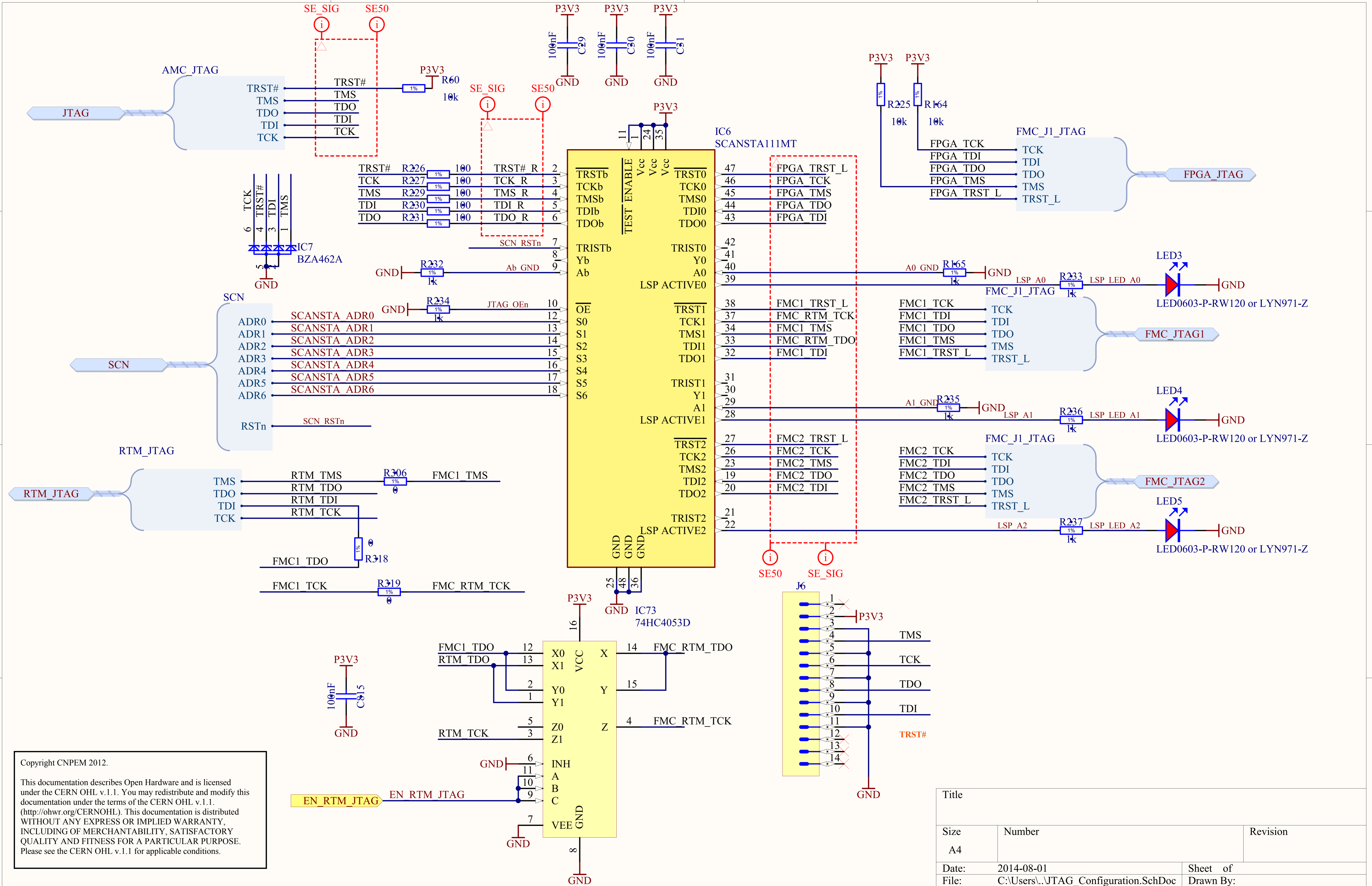
Changed values input caps

TEST2 = GND -> VREF = 0.765  
TEST2 = VSFILT -> VREF = 0.758

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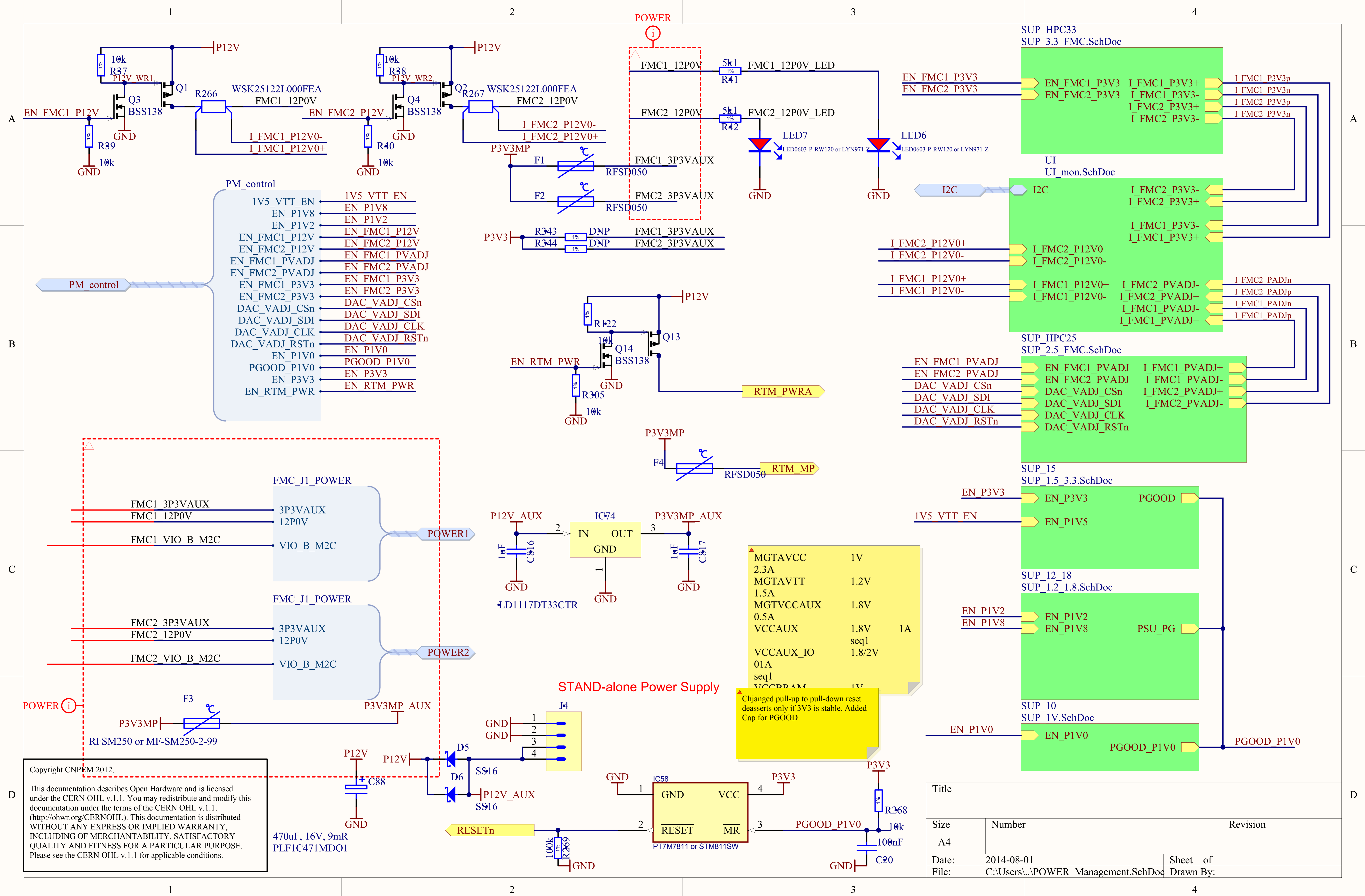
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Size	Number	Revision
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\SUP_3.3_FMC.SchDoc	Drawn By:



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Title		
Size A4	Number	Revision
Date:	2014-08-01	Sheet of
File:	C:\Users\...\JTAG Configuration.SchDoc	Drawn By:









A

A

B

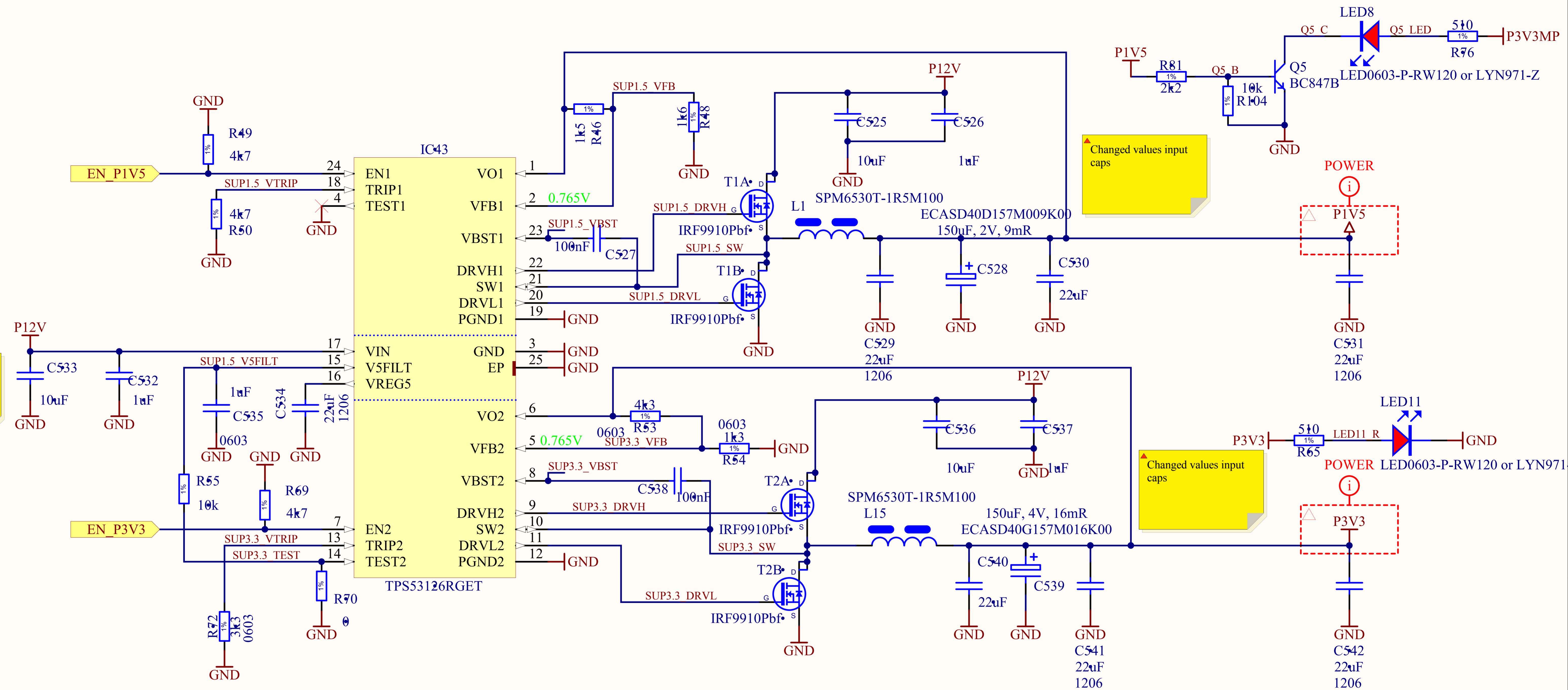
B

C

C

D

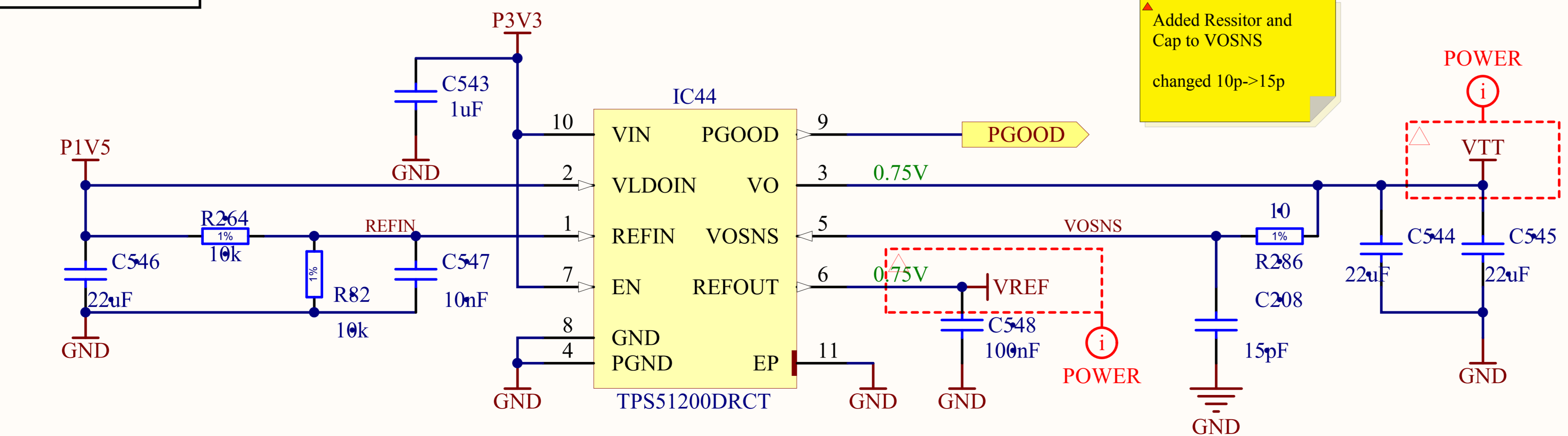
D



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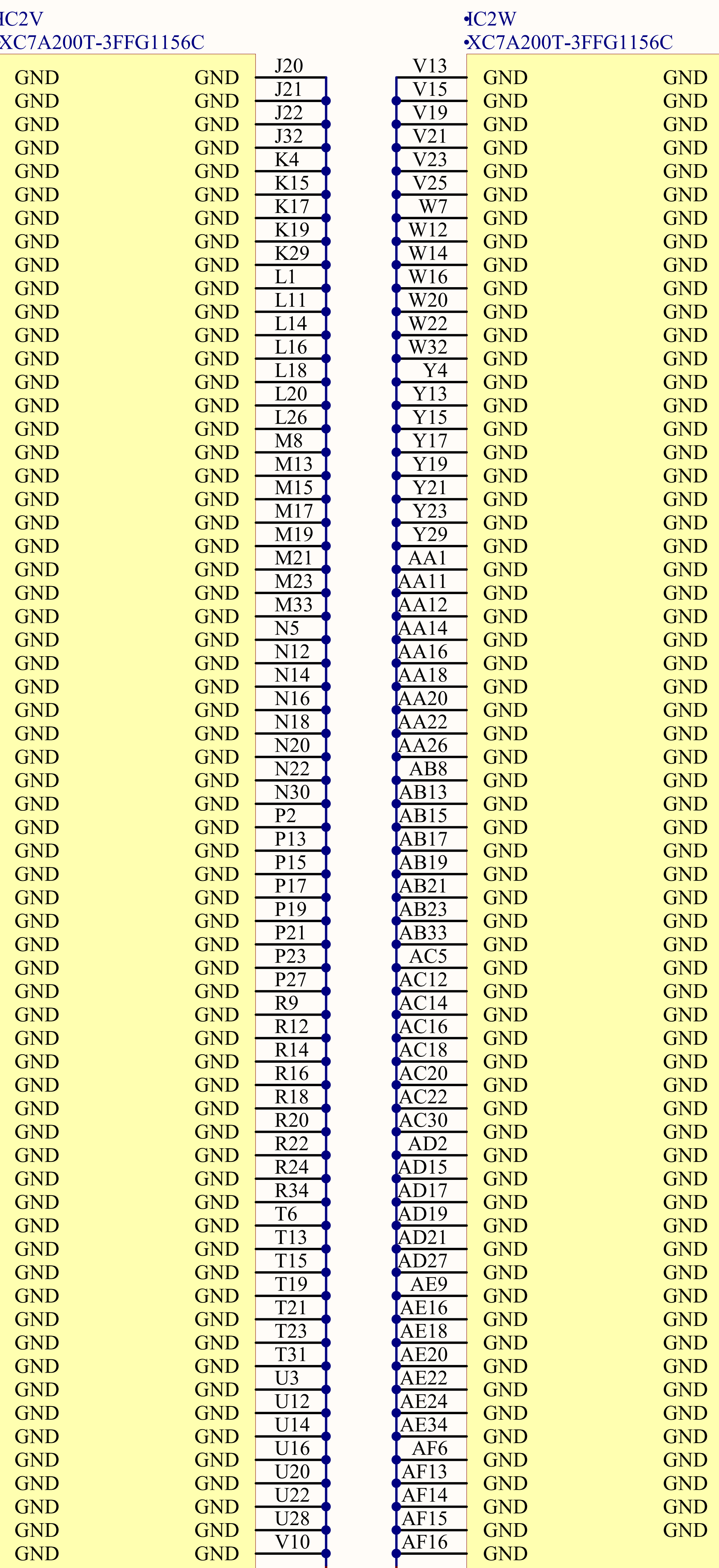
R1	R2	Ir	Vout	R1/R2	Error	
330.0 ?	100.0 ?	7.650 mA		3.290 V	3.300	0.41
%						
430.0 ?	130.0 ?	5.885 mA		3.295 V	3.308	0.18
%						
1000.0 ?	300.0 ?	2.550 mA		3.315 V	3.333	0.59
%						
1100.0 ?	330.0 ?	2.318 mA		3.315 V	3.333	0.59
%						
1200.0 ?	360.0 ?	2.125 mA		3.315 V	3.333	0.59
%						
1300.0 ?	390.0 ?	1.962 mA		3.315 V	3.333	0.59
%						
2700.0 ?	820.0 ?	0.933 mA		3.284 V	3.293	0.64
%						
3000.0 ?	910.0 ?	0.841 mA		3.287 V	3.297	0.51
%						



Title		
Size	Number	Revision
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\SUP_1.5_3.3.SchDoc	Drawn By:



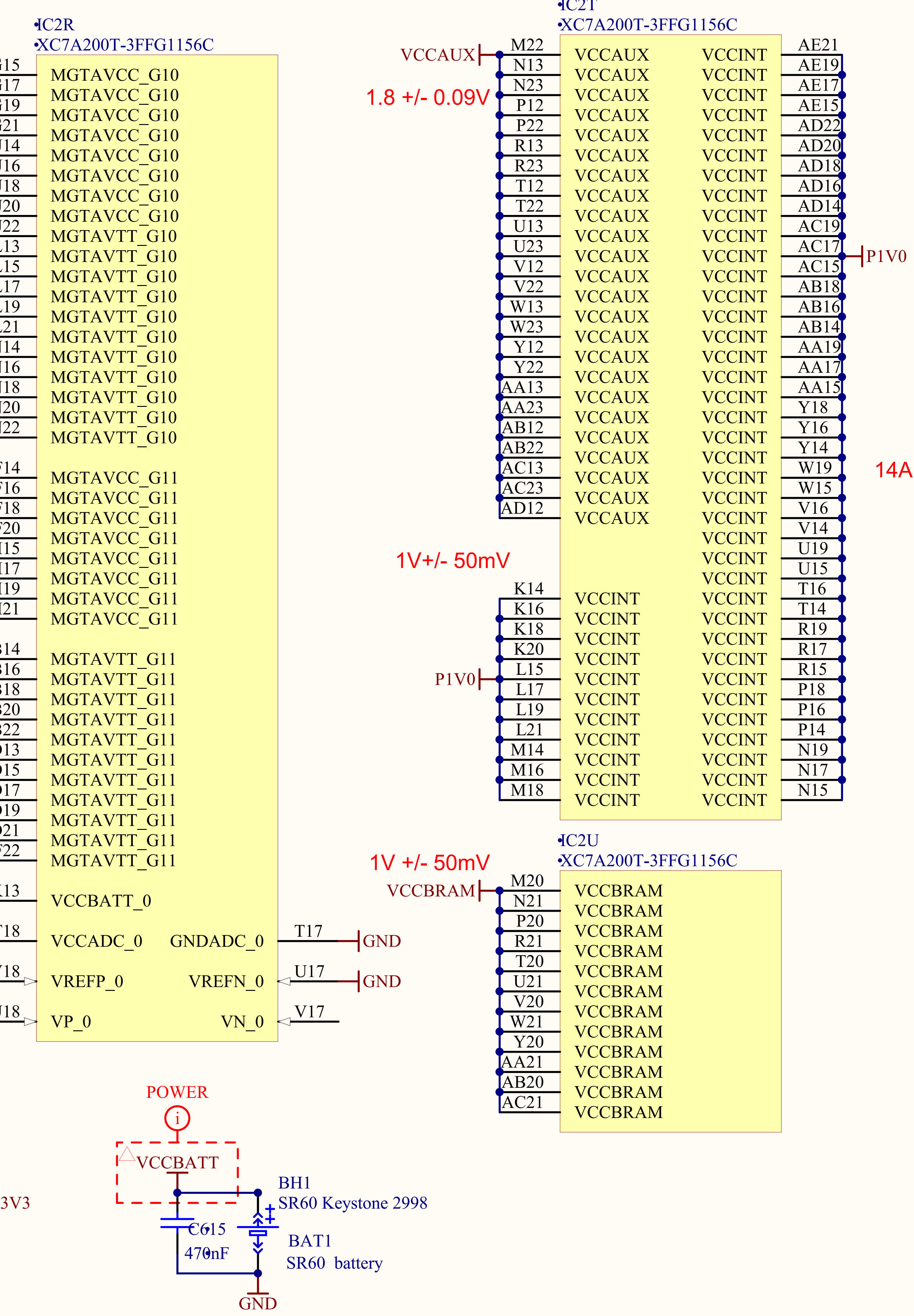
1x680uF, 2x100uF, 28x4.7uF  
42x0.47uF on PG.34



Changed TL431QDBVT -> TS3431  
This gives 1.25V instead of 2.5V

Changed pinout Pin1 = REF, Pin2 =

3x47uF, 4x4.7uF, 7x0.47uF



10

ADAC 1% 330

F

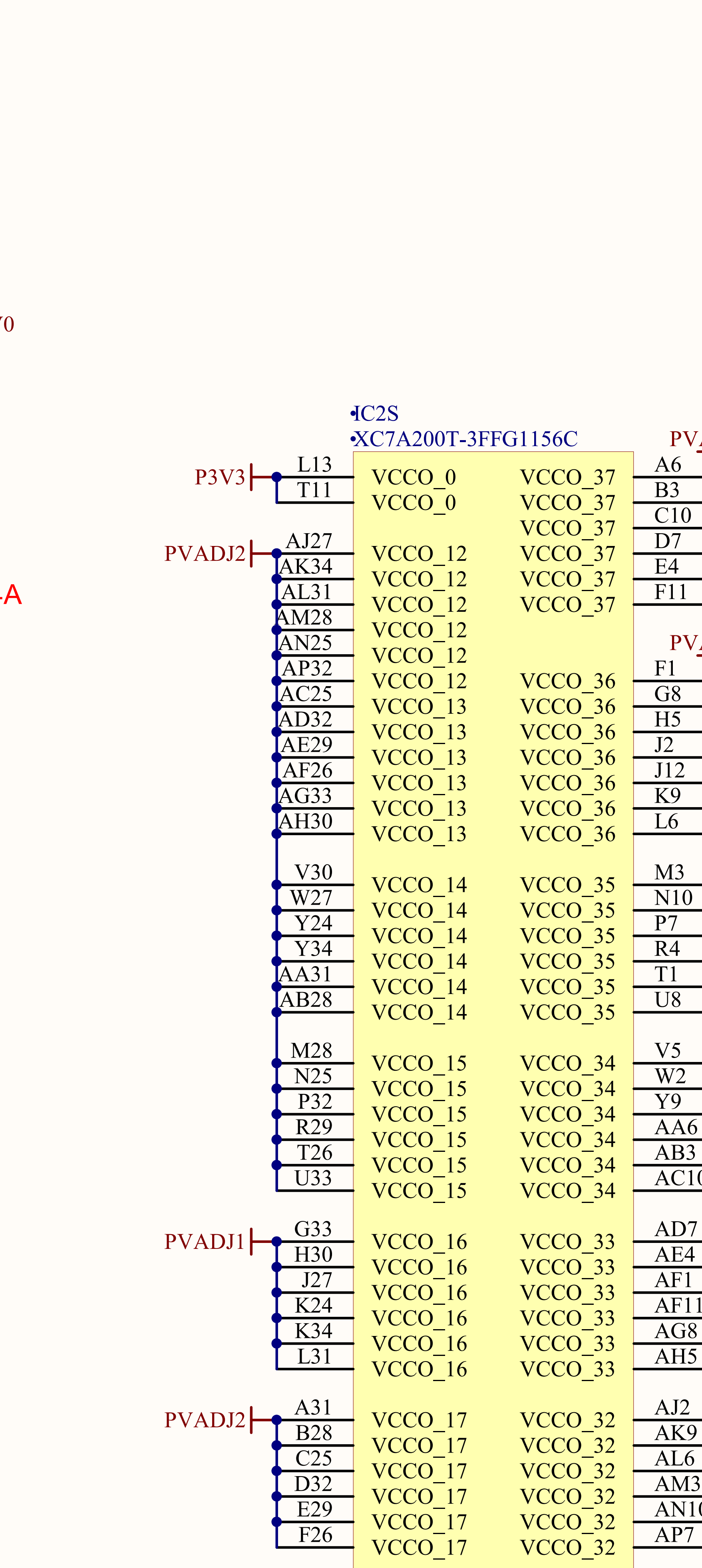
2



GND

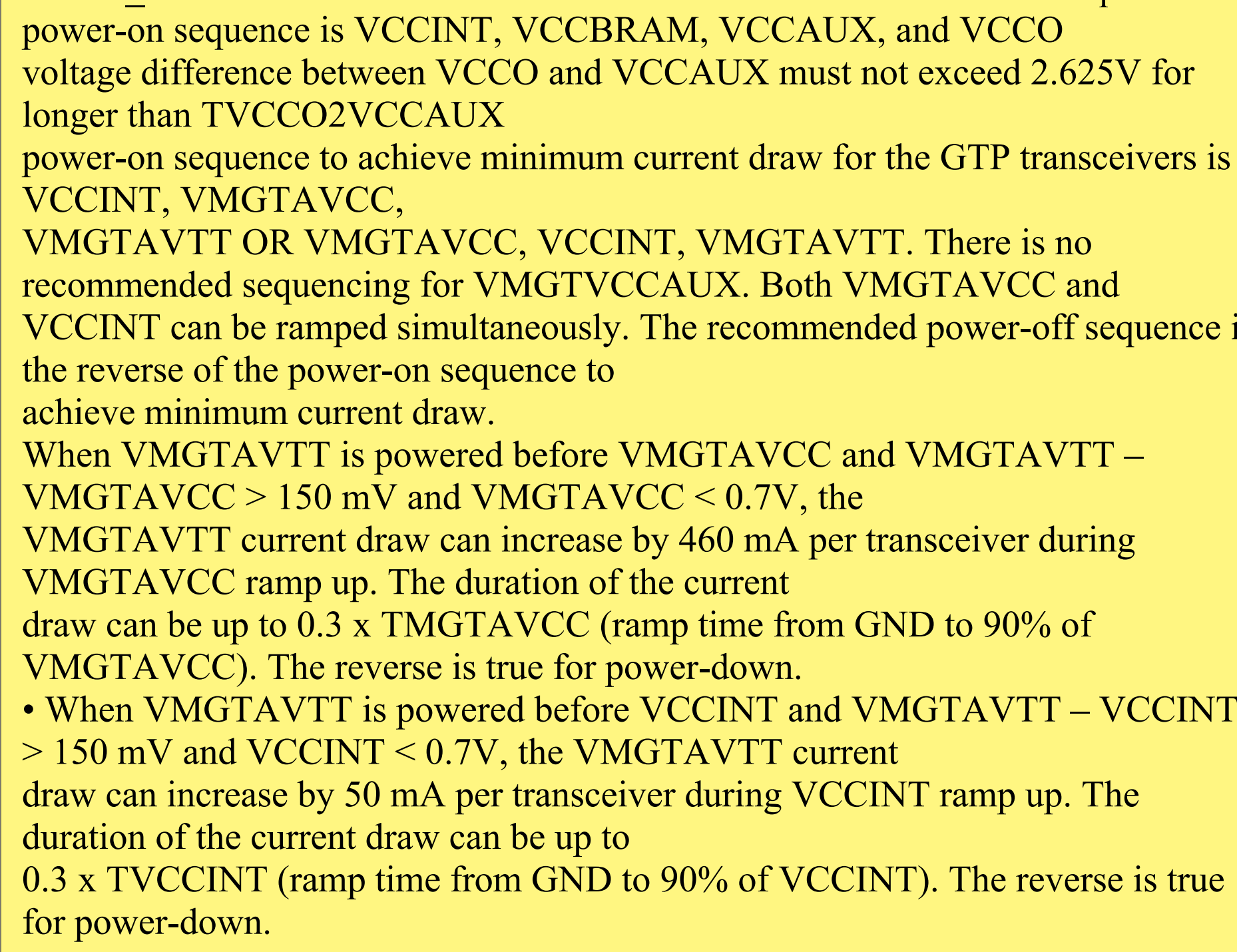
Cathode

~~2x100uF, 4x4.7uF, 8x0.47uF~~

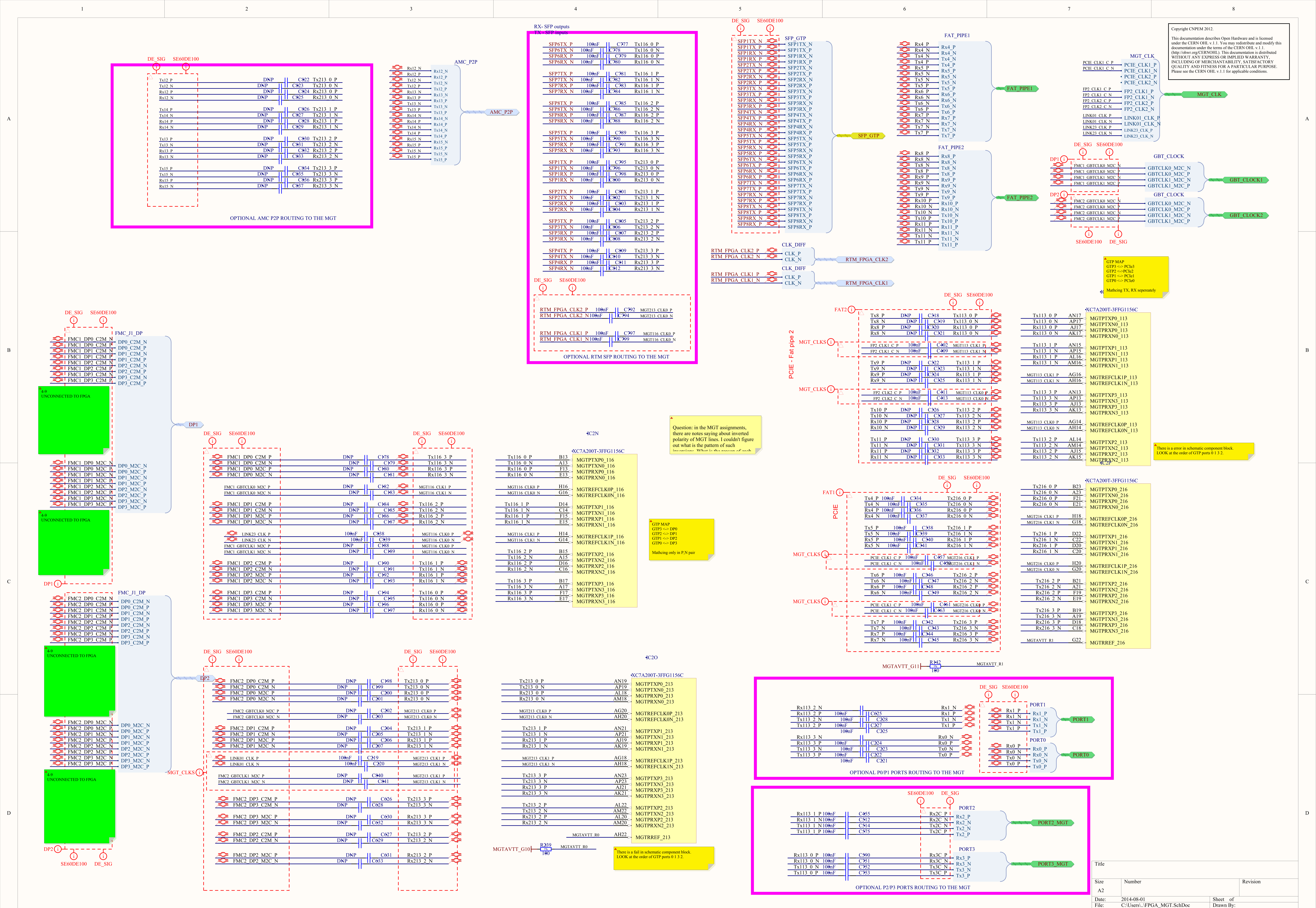


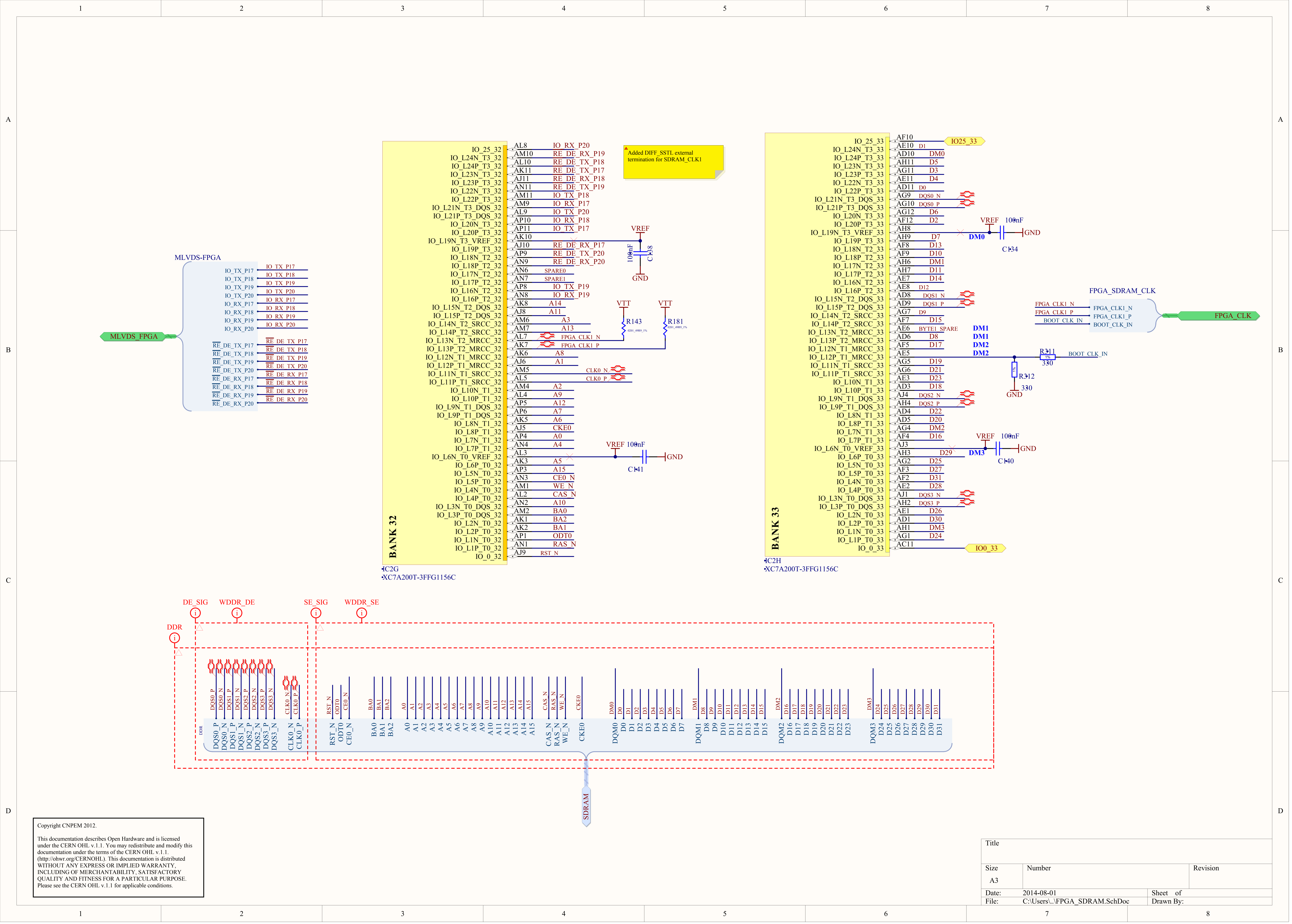
Added arbitrary power rail for 17 and 37 bank - can be changed depending on PCB routability

Bank 17 - place-holder for intermediate/bulks caps for PVADJ2

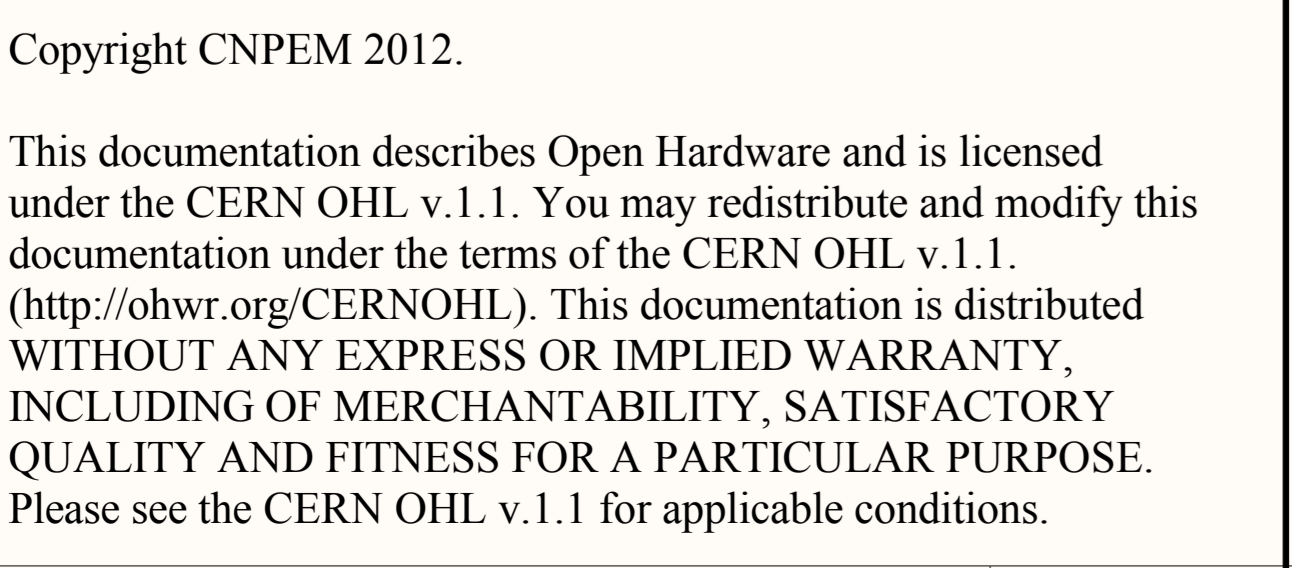


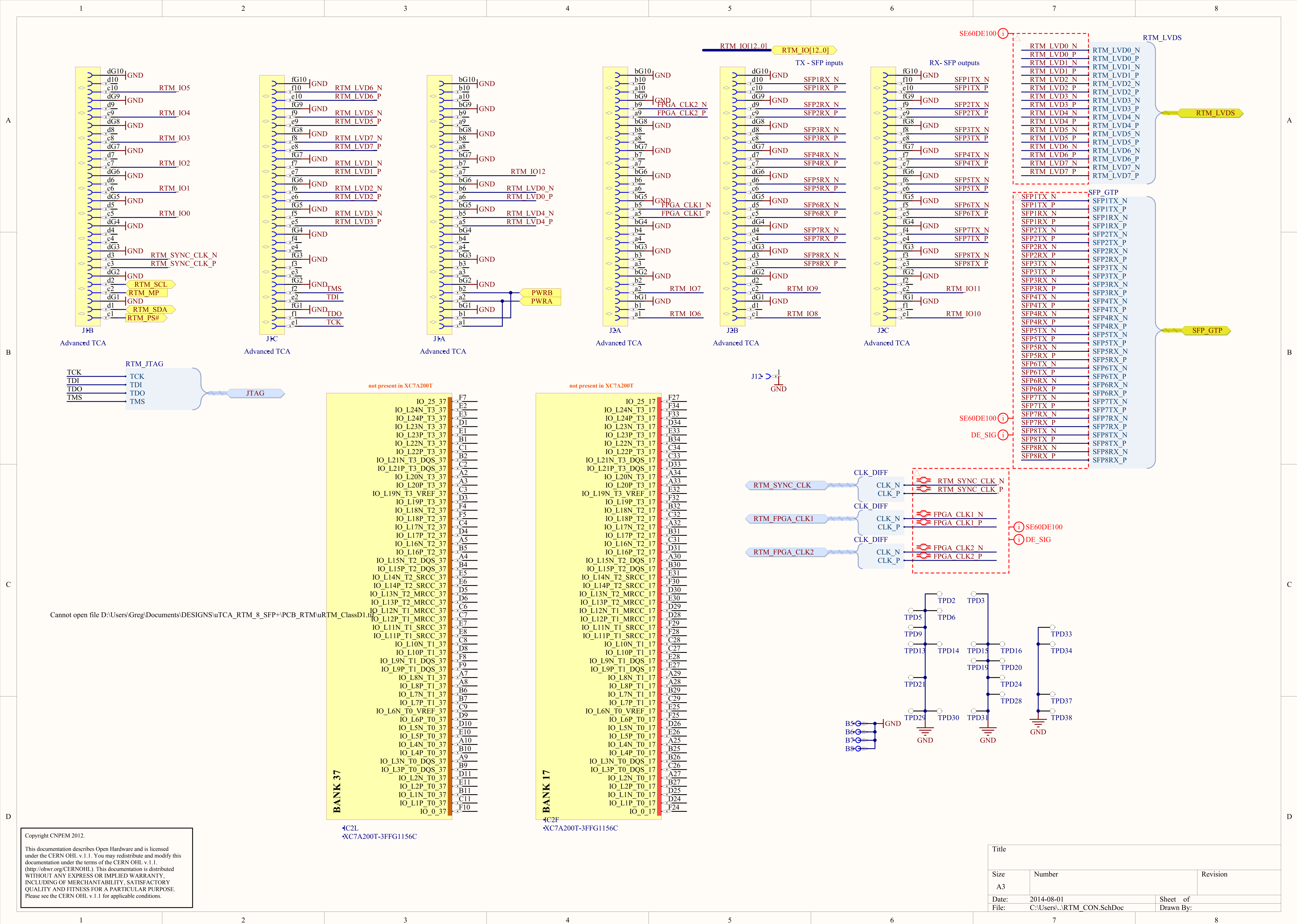
Title			
Size A2	Number		Revision
Date:	2014-08-01	Sheet	of
File:	C:\Users\... \FPGA_SUP.SchDoc	Drawn By:	











A

B

C

D

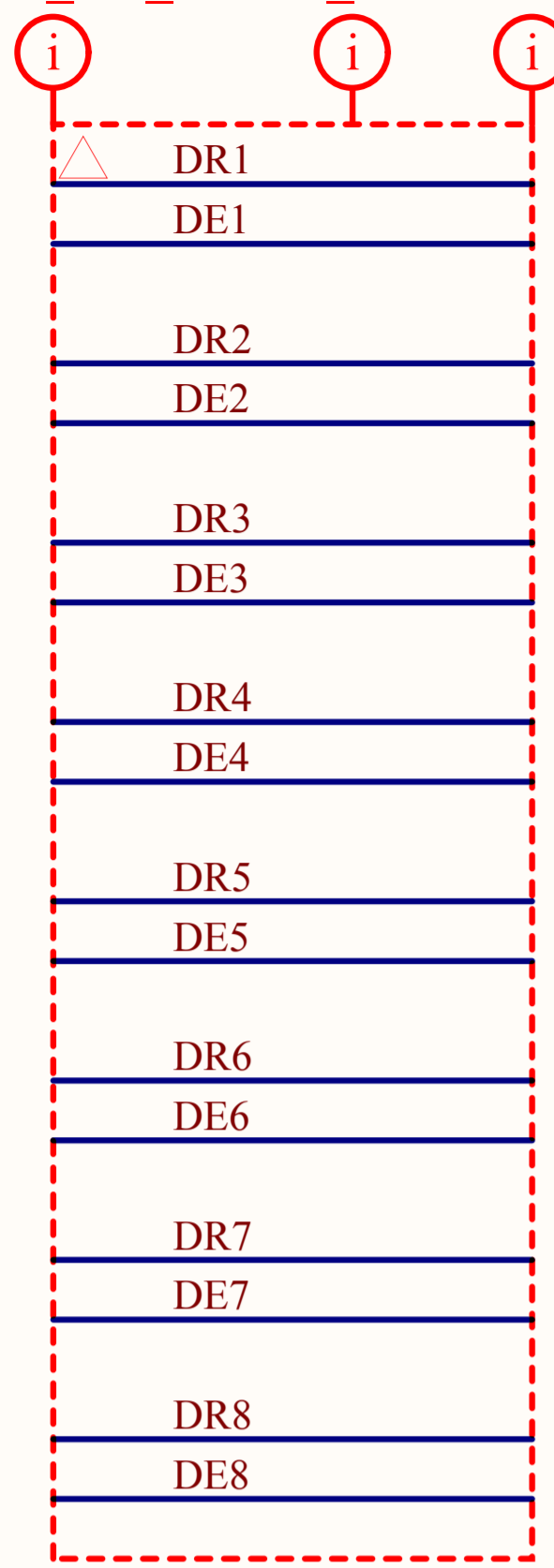
A

B

C

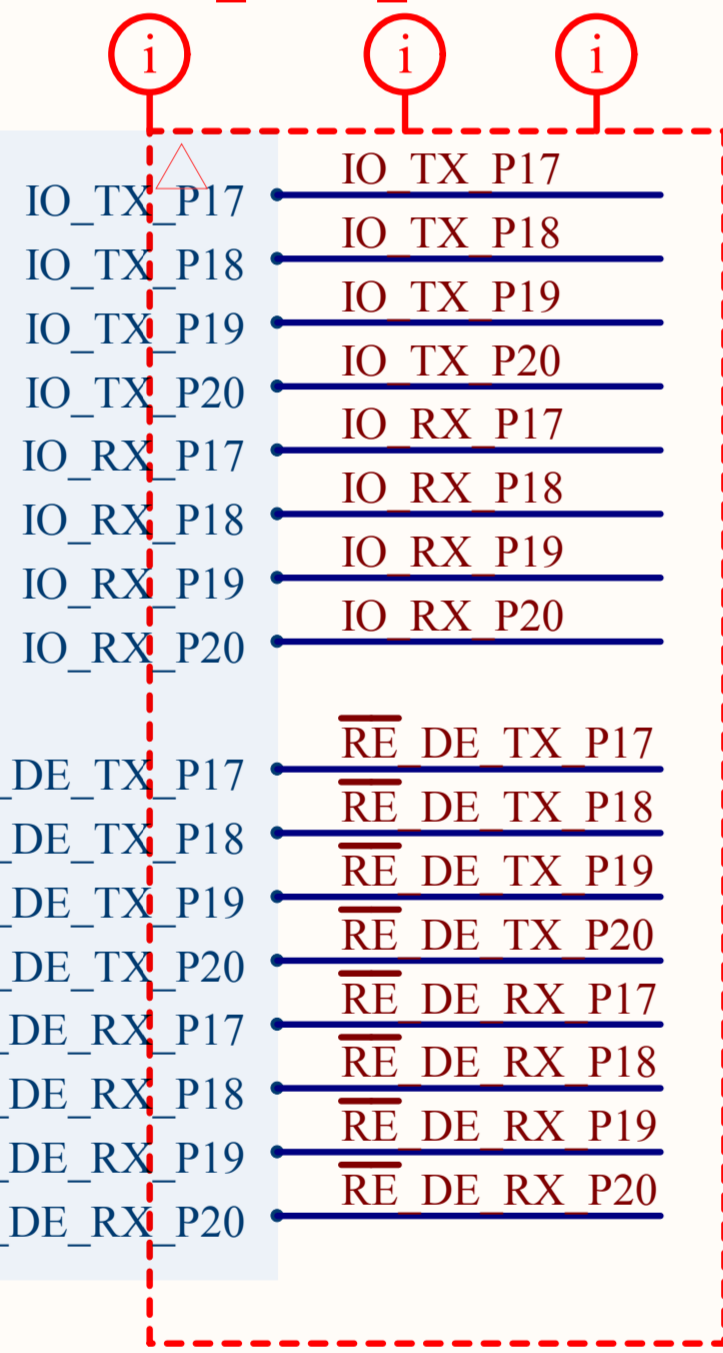
D

MLVDS\_DR\_DE SE\_SIG SE50



MLVDS\_F SE\_SIG SE50

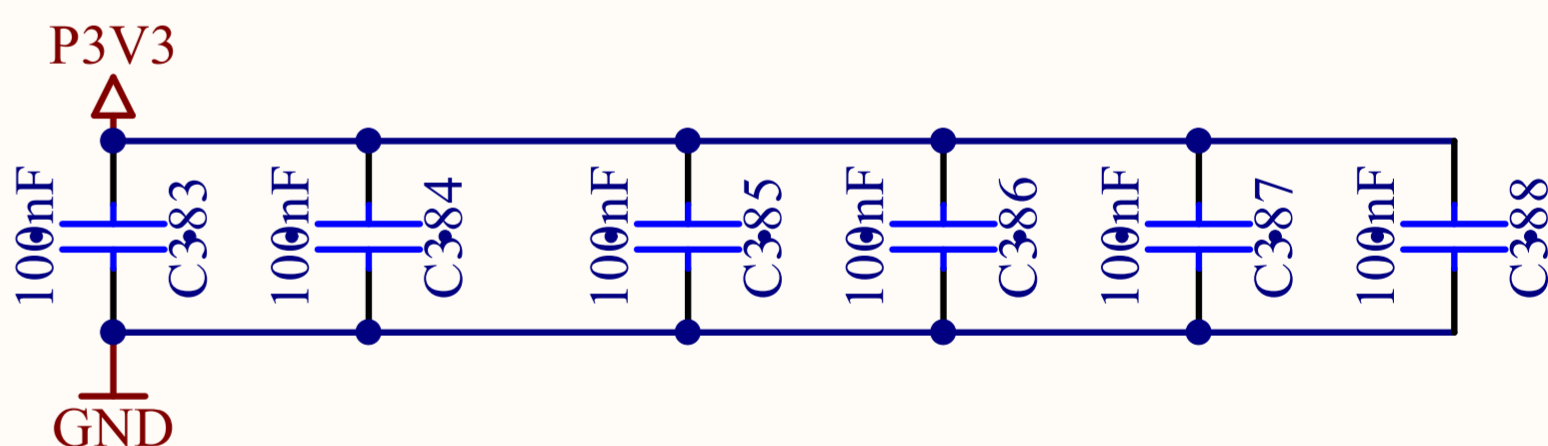
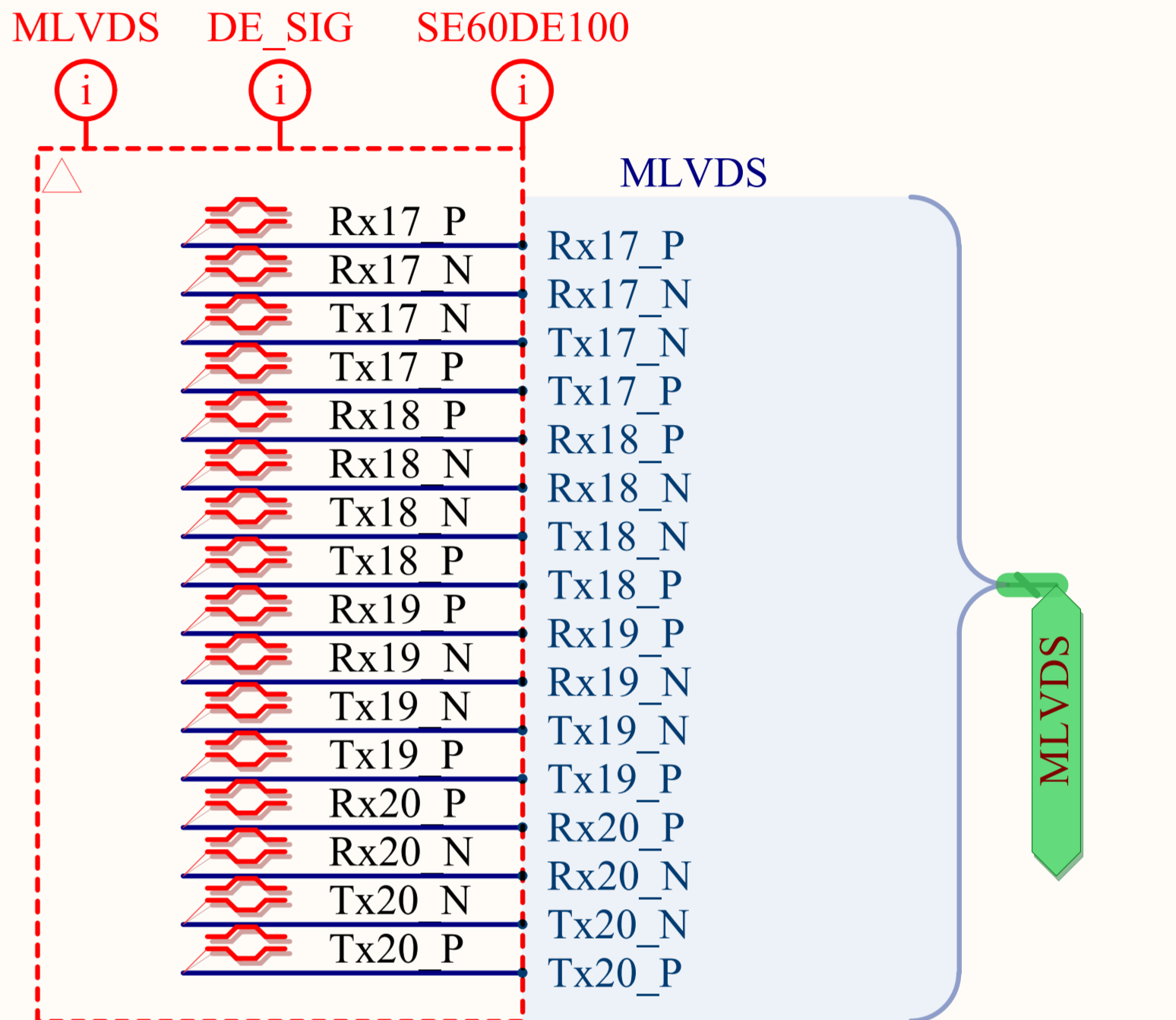
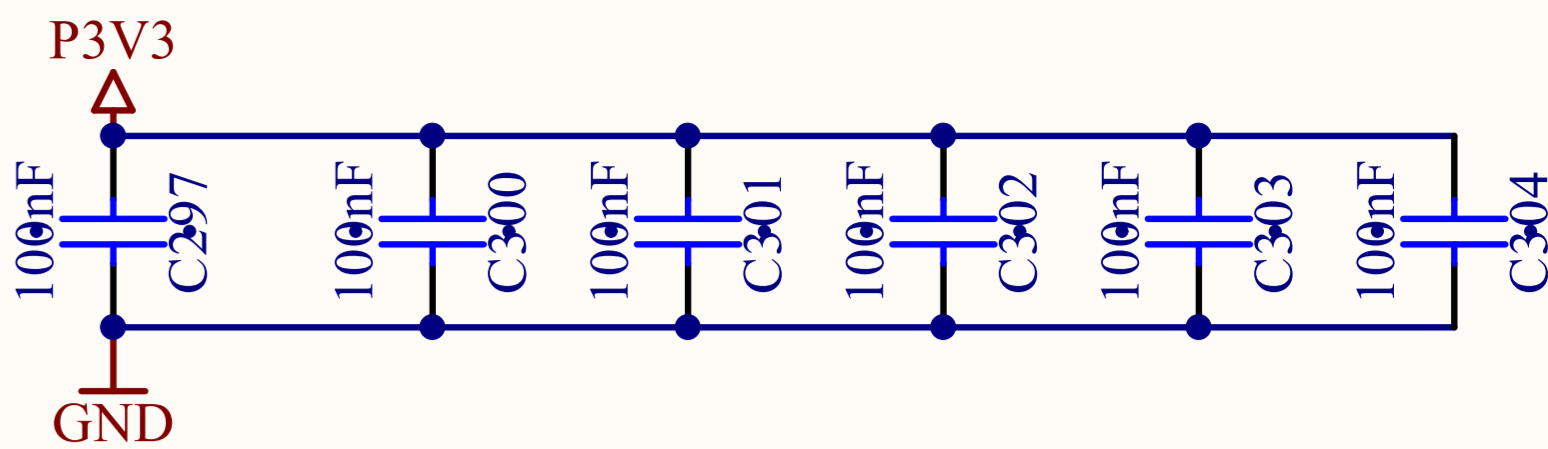
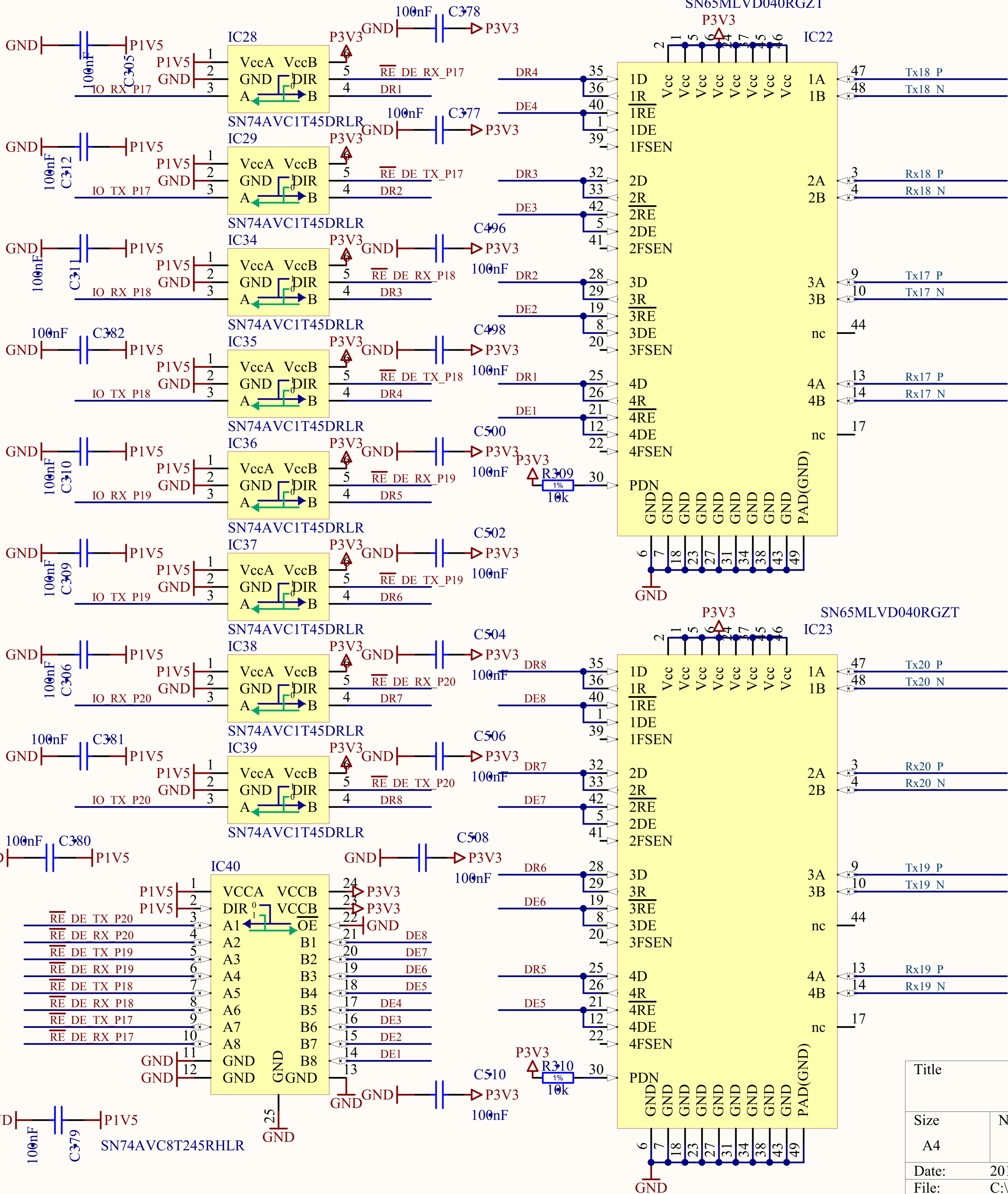
MLVDS-FPGA



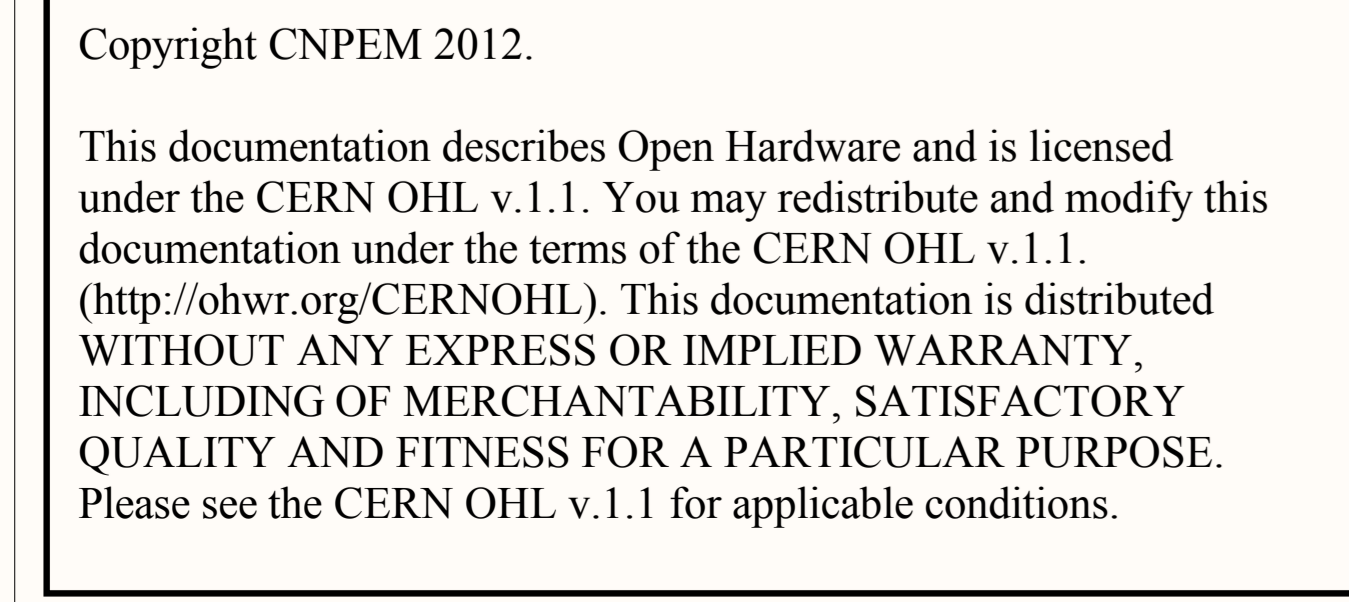
MLVDS\_FPGA

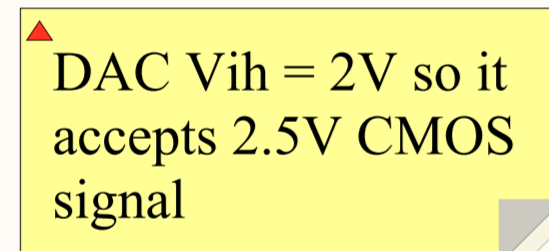
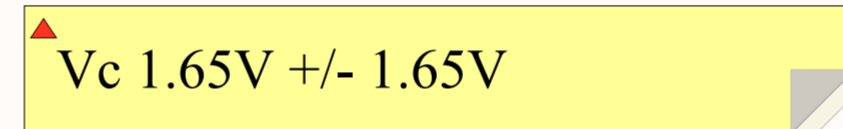
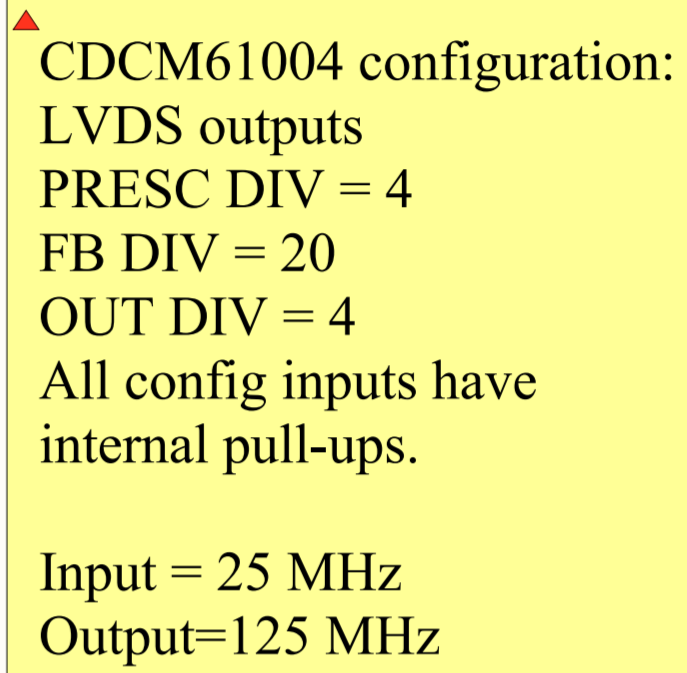
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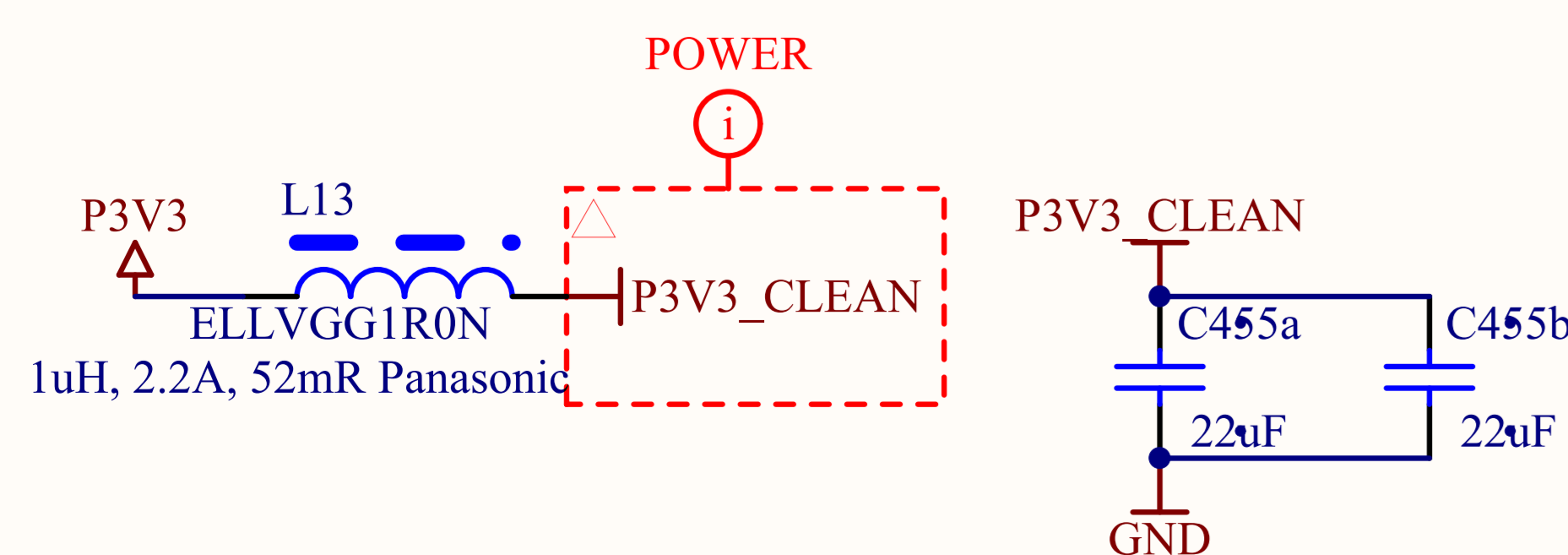
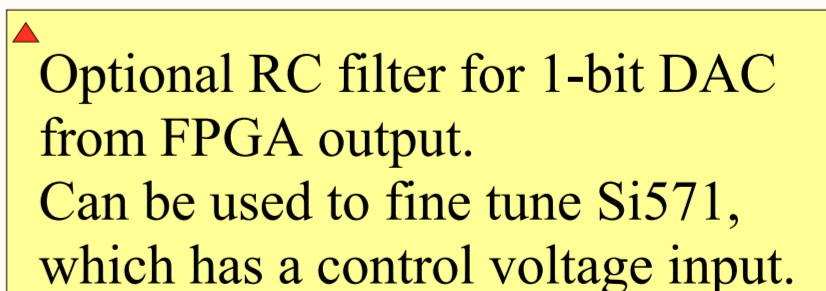


Title		
Size	Number	
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\M-LVDS PHY.SchDoc	Drawn By:





▲ Changed LM336M-2.5/NOPB to TL431QDBVT... now we have proper 2.5V

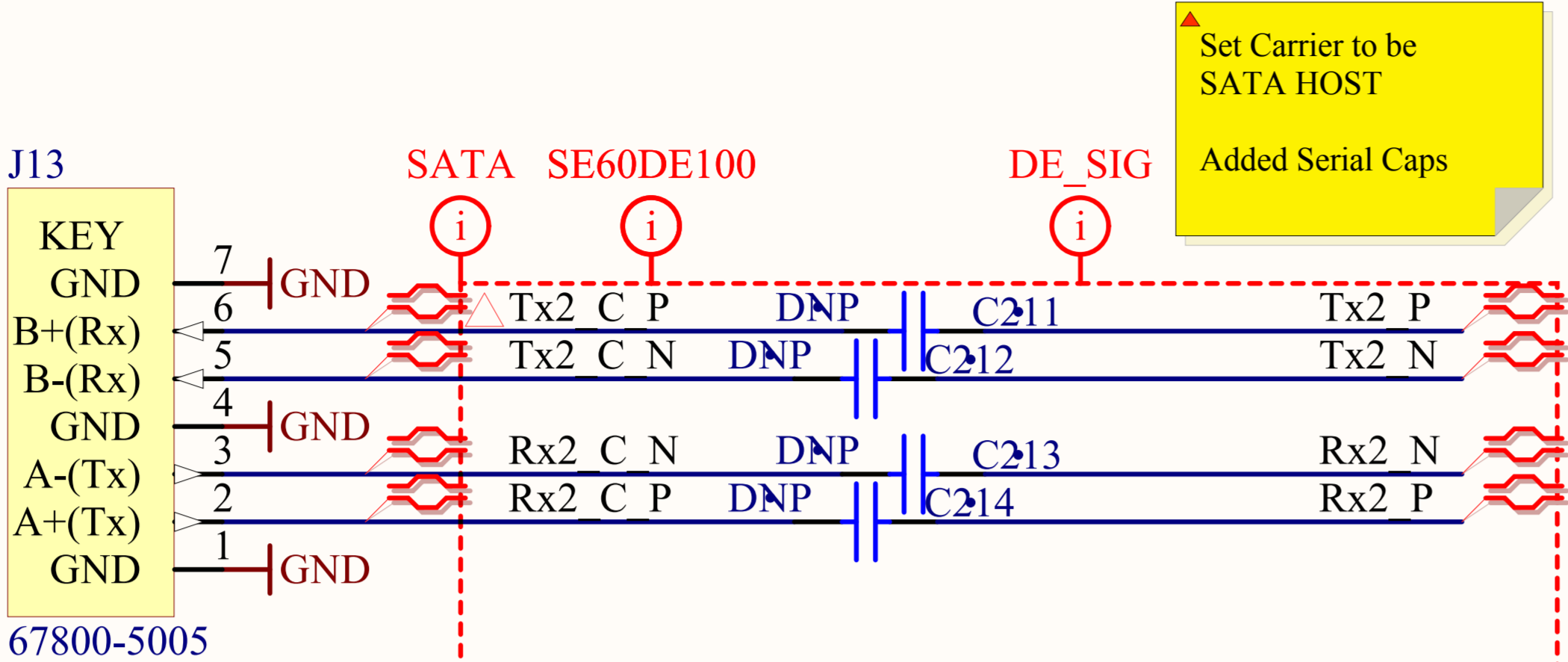


Title			
Size A3	Number		Revision
Date:	2014-08-01	Sheet	of
File:	C:\Users\...Clock WR.SchDoc	Drawn By:	

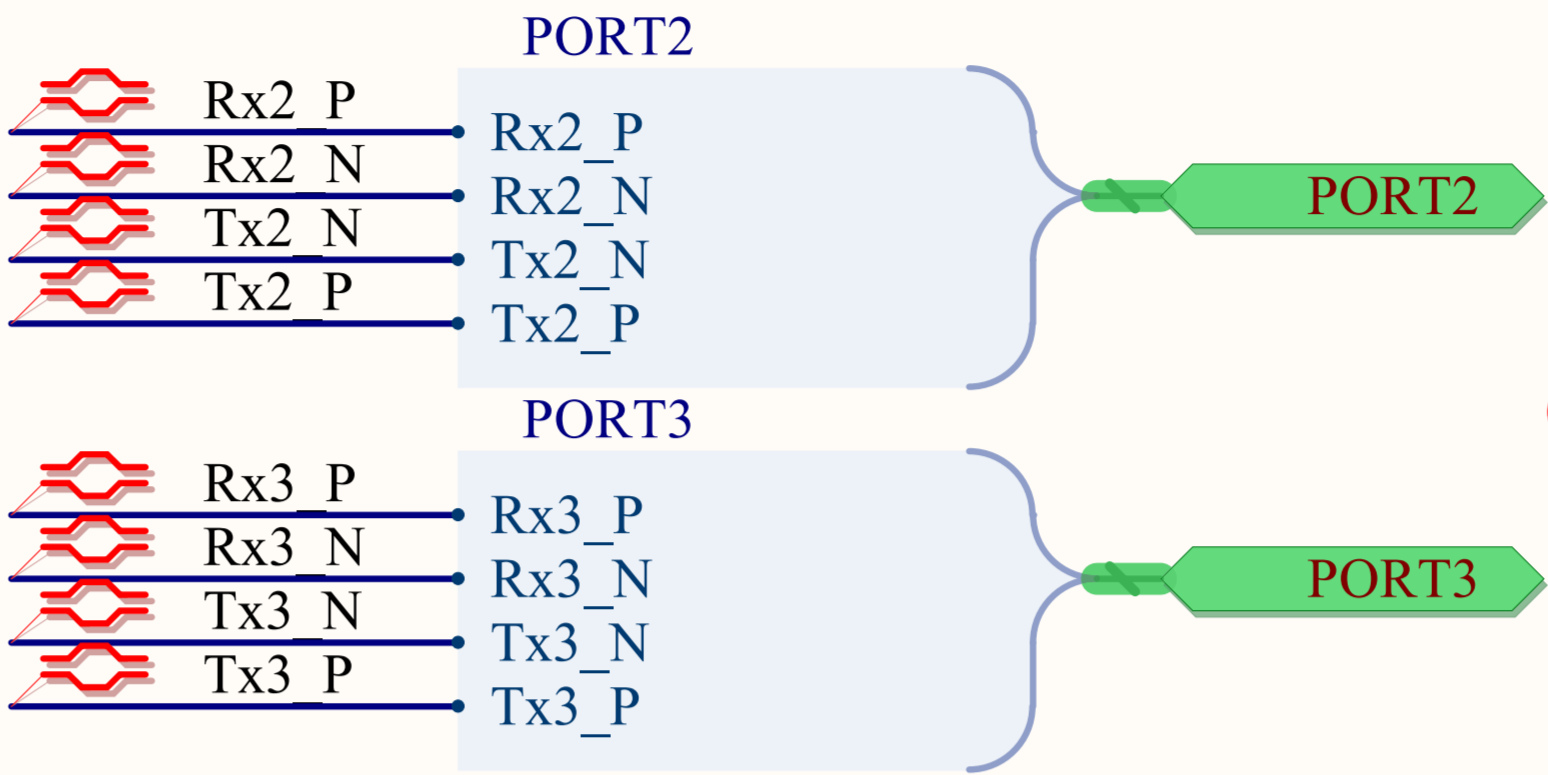
SATA naming is relative to HOST

Apply to all AMC ports: see table 6-1 PICMG AMC.0 R2.0 1.5.11.2006

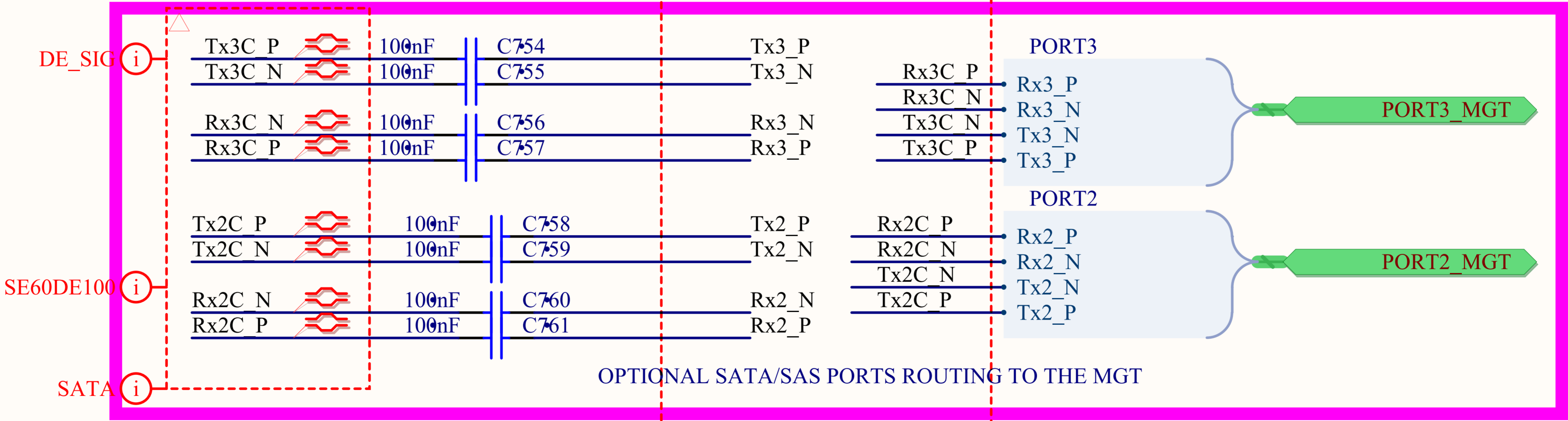
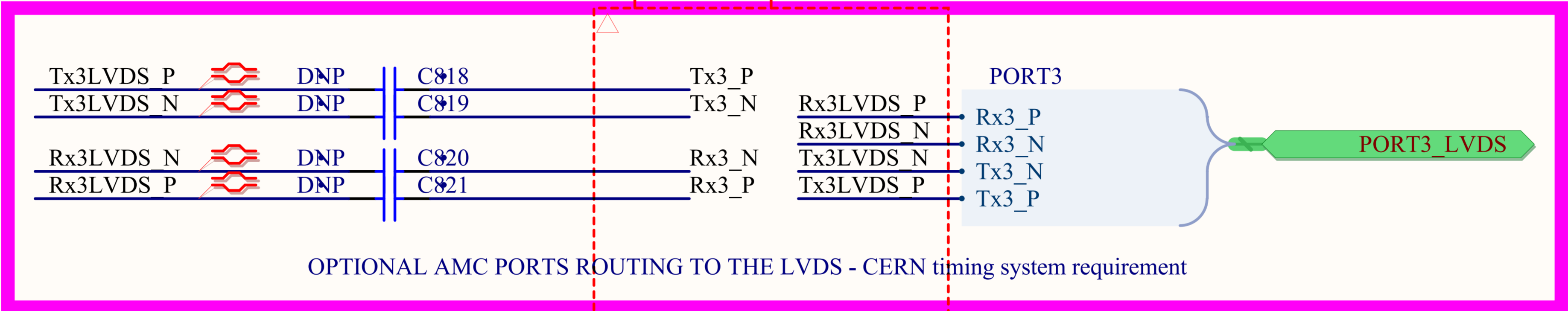
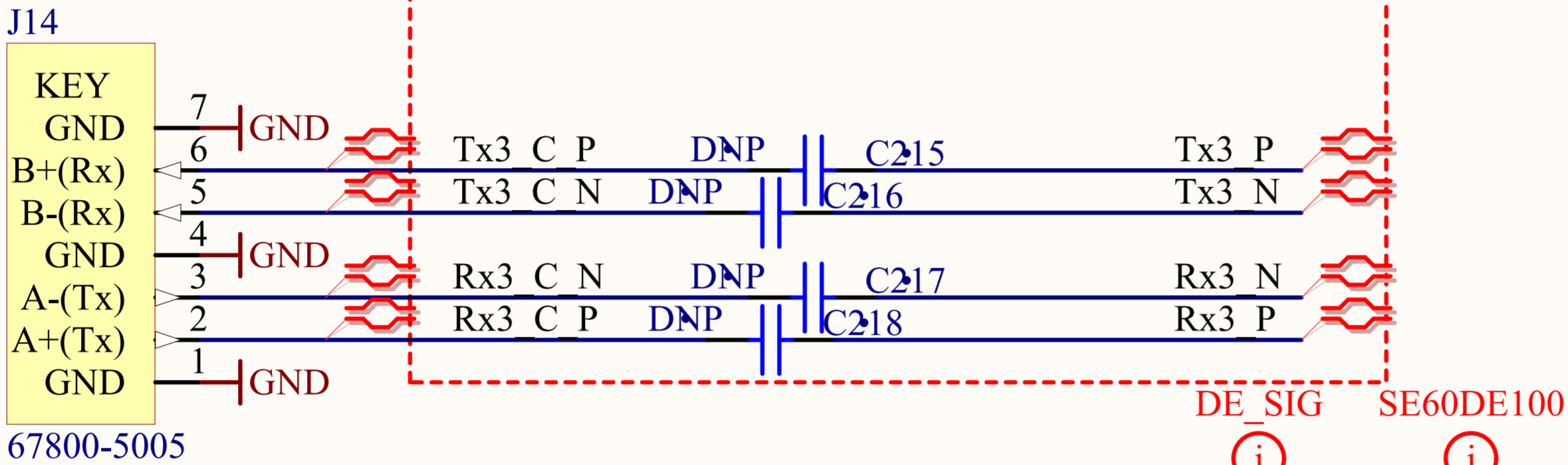
For normal SATA cables apply:  
B = HOST SATA RX  
A = HOST SATA TX



RXes are CARRIER-OUTPUT  
TXes are CARRIER-INPUT



There also Exist a Cross-Over SATA Cable so always there is a possibility to change that



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Title		
Size	Number	Revision
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\AMC-SATA.SchDoc	Drawn By:

A

A

B

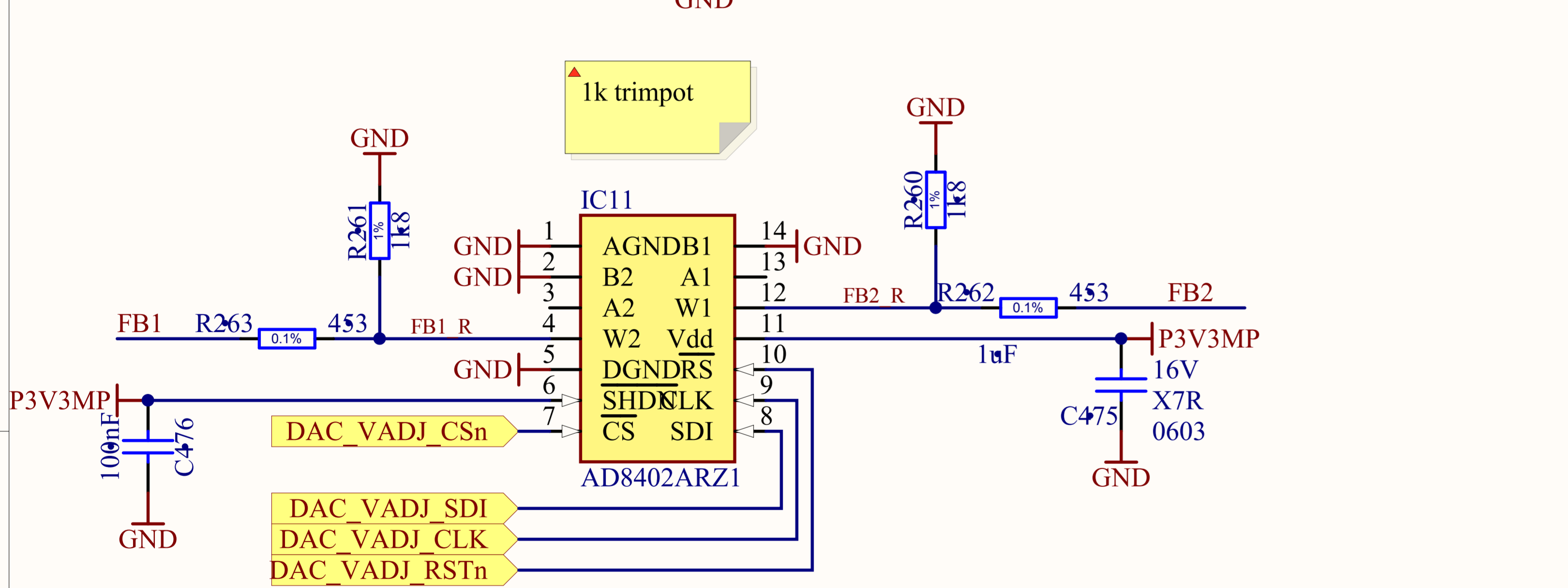
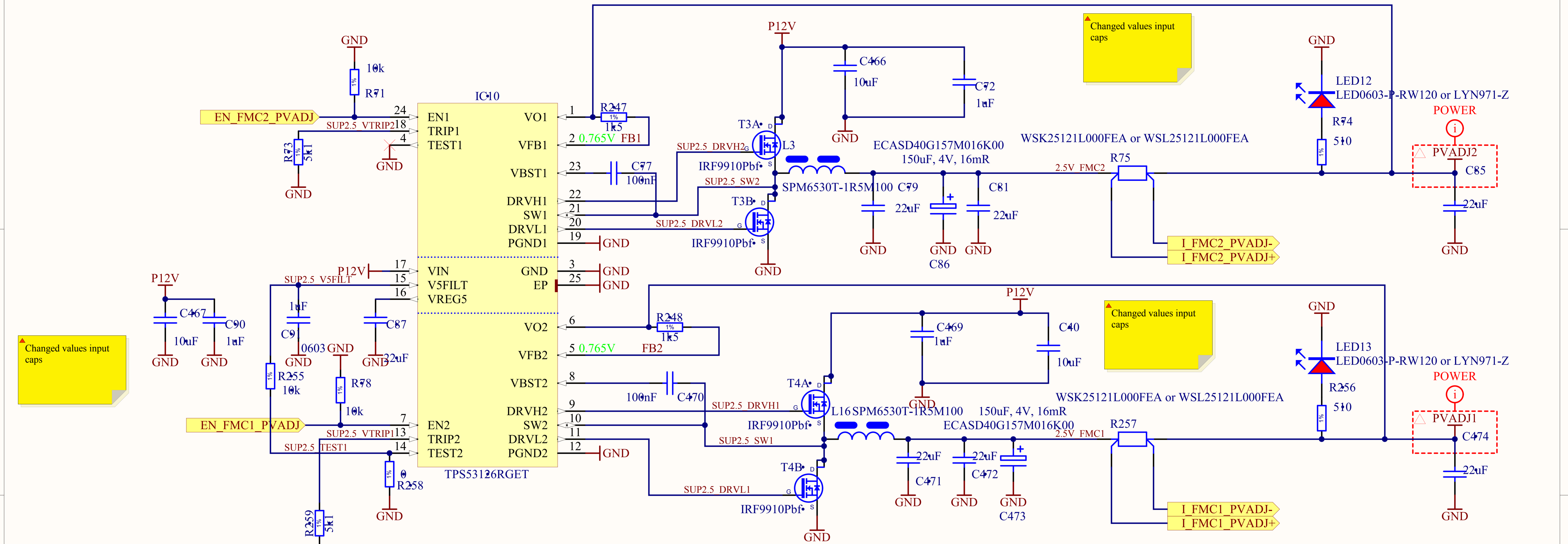
B

C

C

D

D



R1	R2	I <sub>r</sub>	V <sub>out</sub>	R1/R2	Error
150.0 ?	110.0 ?	6.955 mA	1.808 V	1.364	0.79 %
270.0 ?	200.0 ?	3.825 mA	1.798 V	1.350	0.22 %
300.0 ?	220.0 ?	3.477 mA	1.808 V	1.364	0.79 %
1100.0 ?	820.0 ?	0.933 mA	1.791 V	1.341	0.95 %

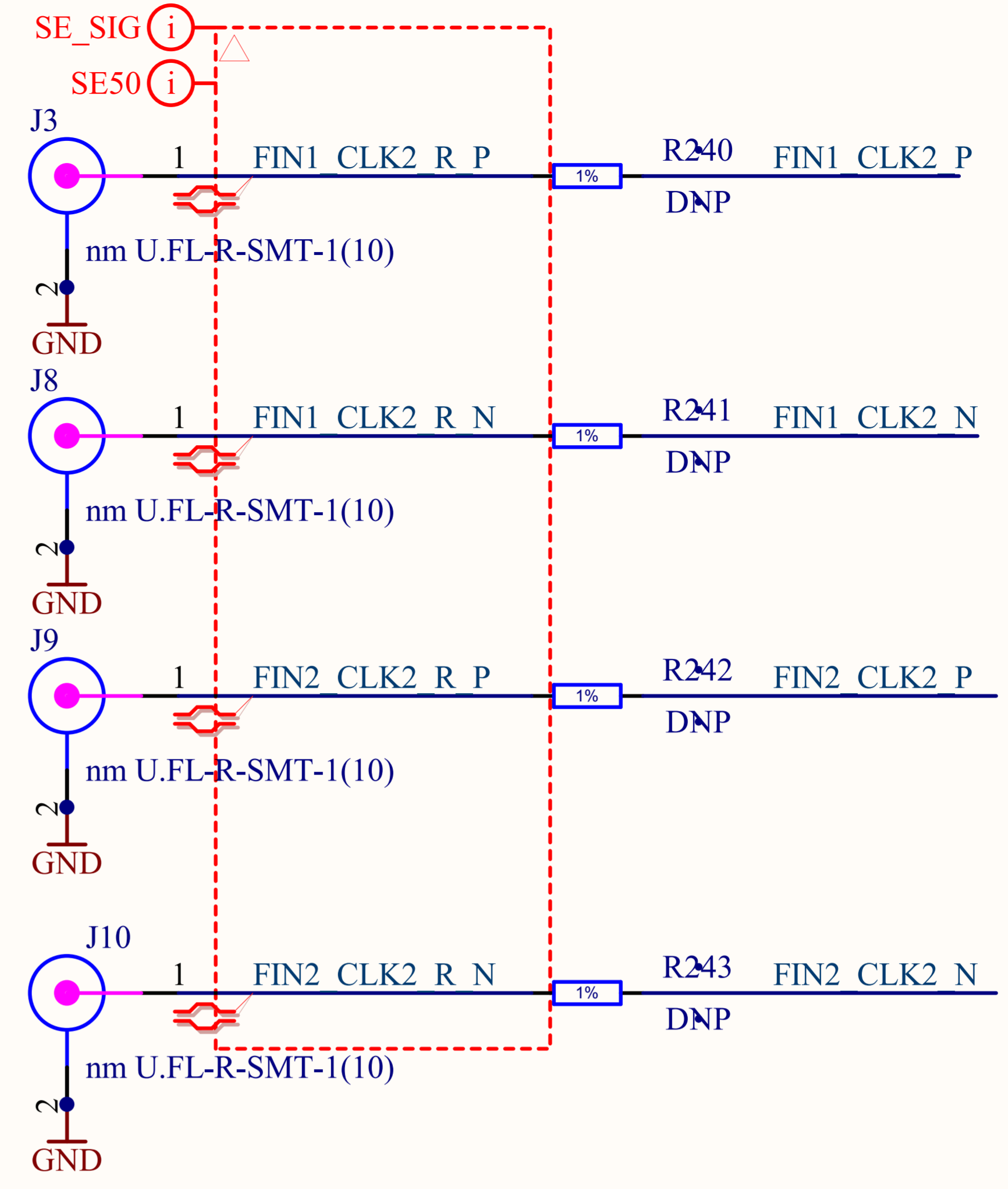
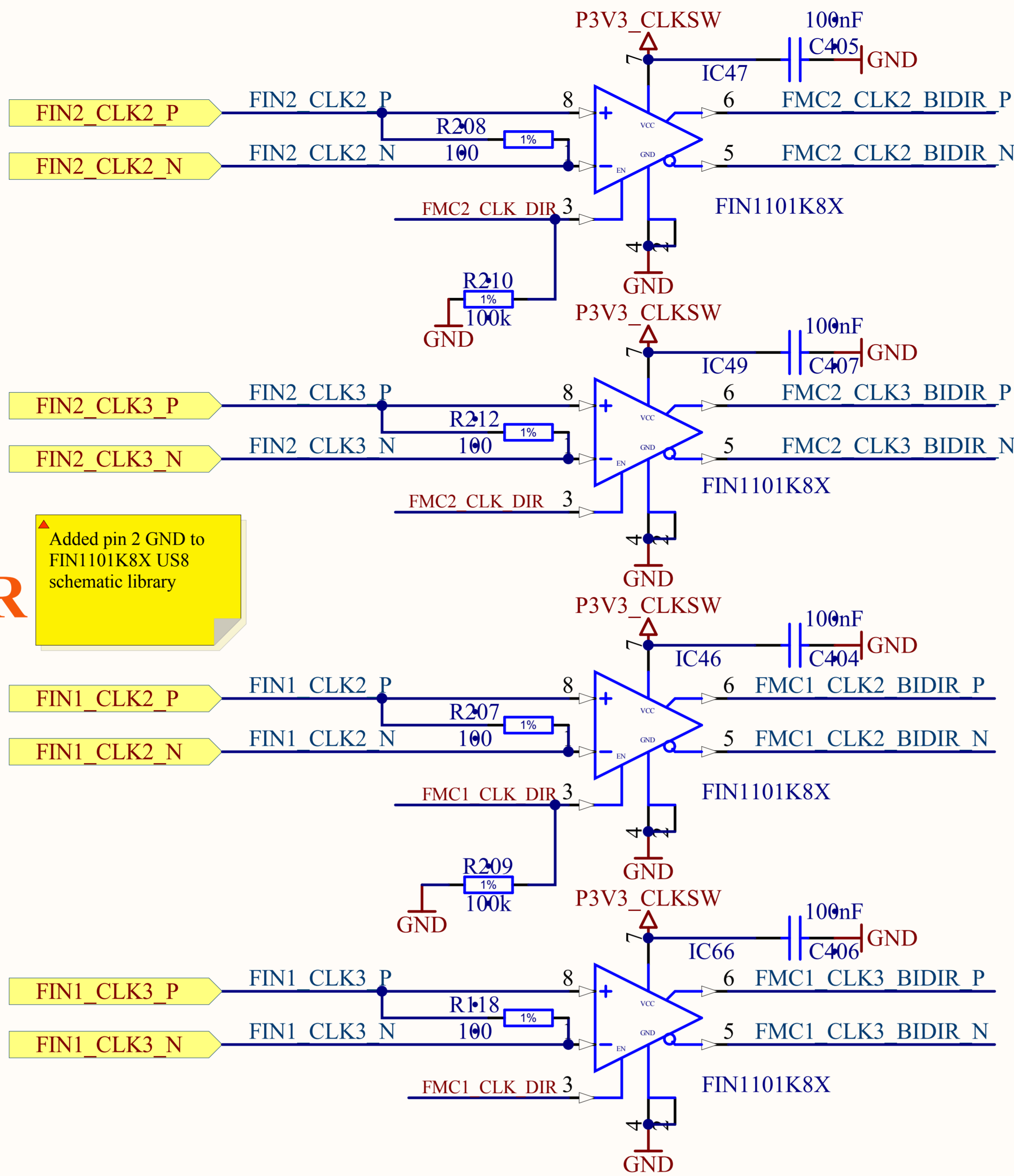
R1	R2	I <sub>r</sub>	V <sub>out</sub>	R1/R2	Error
1100.0 ?	100.0 ?	7.650 mA	9.180 V	11.000	2.19 %
1200.0 ?	110.0 ?	6.955 mA	9.110 V	10.909	1.34 %
1300.0 ?	120.0 ?	6.375 mA	9.053 V	10.833	0.64 %
1600.0 ?	150.0 ?	5.100 mA	8.925 V	10.667	0.91 %
1800.0 ?	160.0 ?	4.781 mA	9.371 V	11.250	4.51 %
2000.0 ?	180.0 ?	4.250 mA	9.265 V	11.111	

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Title		
Size	Number	
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\SUP_2.5_FMC.SchDoc	Drawn By:

A



A

B

# IPUT FROM CROSSBAR

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- FMC1\_CLK0\_M2C\_N FMC1\_CLK0\_M2C\_P
- FMC1\_CLK0\_M2C\_P FMC1\_CLK1\_M2C\_N
- FMC1\_CLK1\_M2C\_N FMC1\_CLK1\_M2C\_P
- FMC1\_CLK2\_BIDIR\_N FMC1\_CLK2\_BIDIR\_P
- FMC1\_CLK2\_BIDIR\_P FMC1\_CLK3\_BIDIR\_N
- FMC1\_CLK3\_BIDIR\_N FMC1\_CLK3\_BIDIR\_P

C

# TO FMC CON



- FMC2\_CLK0\_M2C\_N FMC2\_CLK0\_M2C\_P
- FMC2\_CLK0\_M2C\_P FMC2\_CLK1\_M2C\_N
- FMC2\_CLK1\_M2C\_N FMC2\_CLK1\_M2C\_P
- FMC2\_CLK2\_BIDIR\_N FMC2\_CLK2\_BIDIR\_P
- FMC2\_CLK2\_BIDIR\_P FMC2\_CLK3\_BIDIR\_N
- FMC2\_CLK3\_BIDIR\_N FMC2\_CLK3\_BIDIR\_P

C

D

Title		
Size	Number	Revision
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\FMC_Clocks.SchDoc	Drawn By:

D

A

B

C

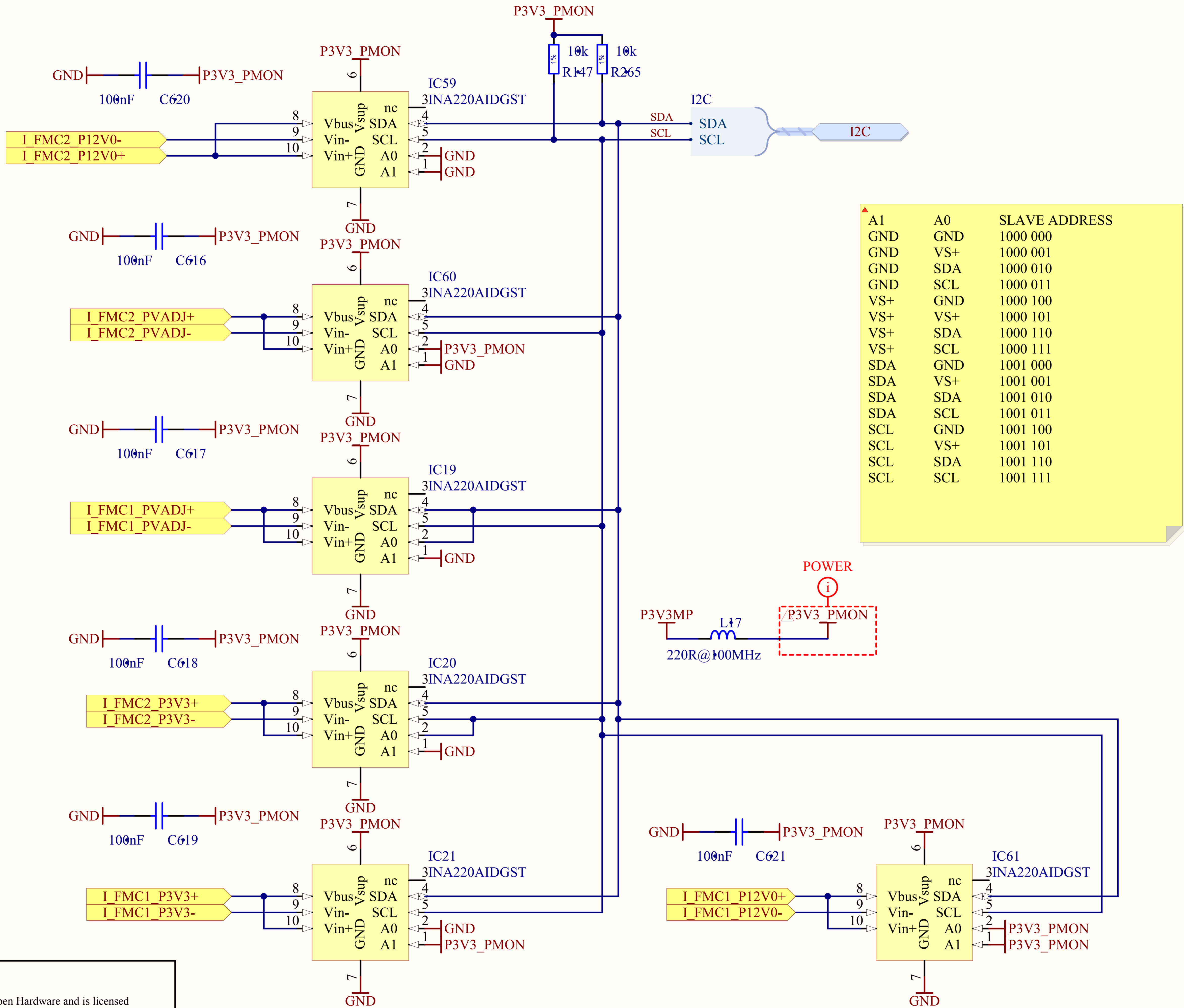
D

A

B

C

D



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Title		
Size	Number	
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\UI_mon.SchDoc	Drawn By:

A

A

B

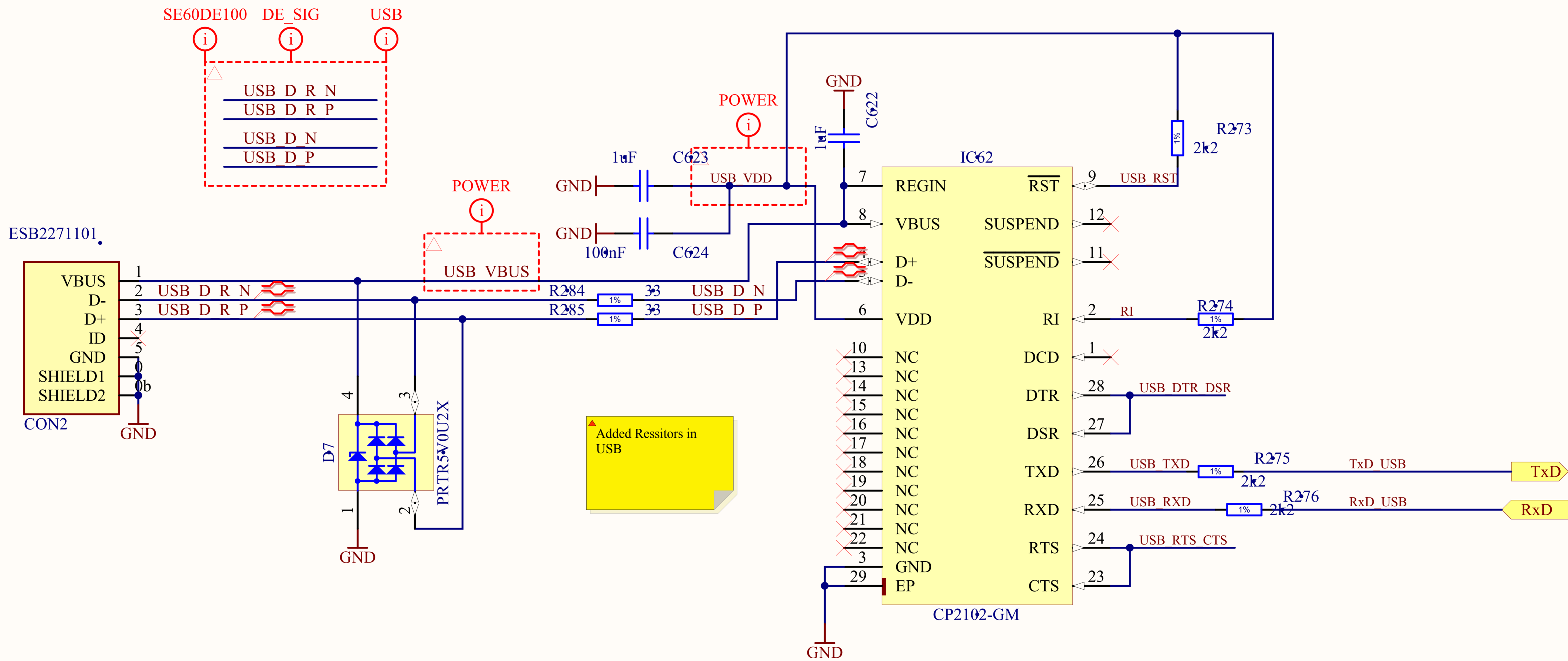
B

C

C

D

D



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Title		
Size	Number	Revision
A4		
Date:	2014-08-01	Sheet of
File:	C:\Users\...\USB_UART.SchDoc	Drawn By:

A

B

C

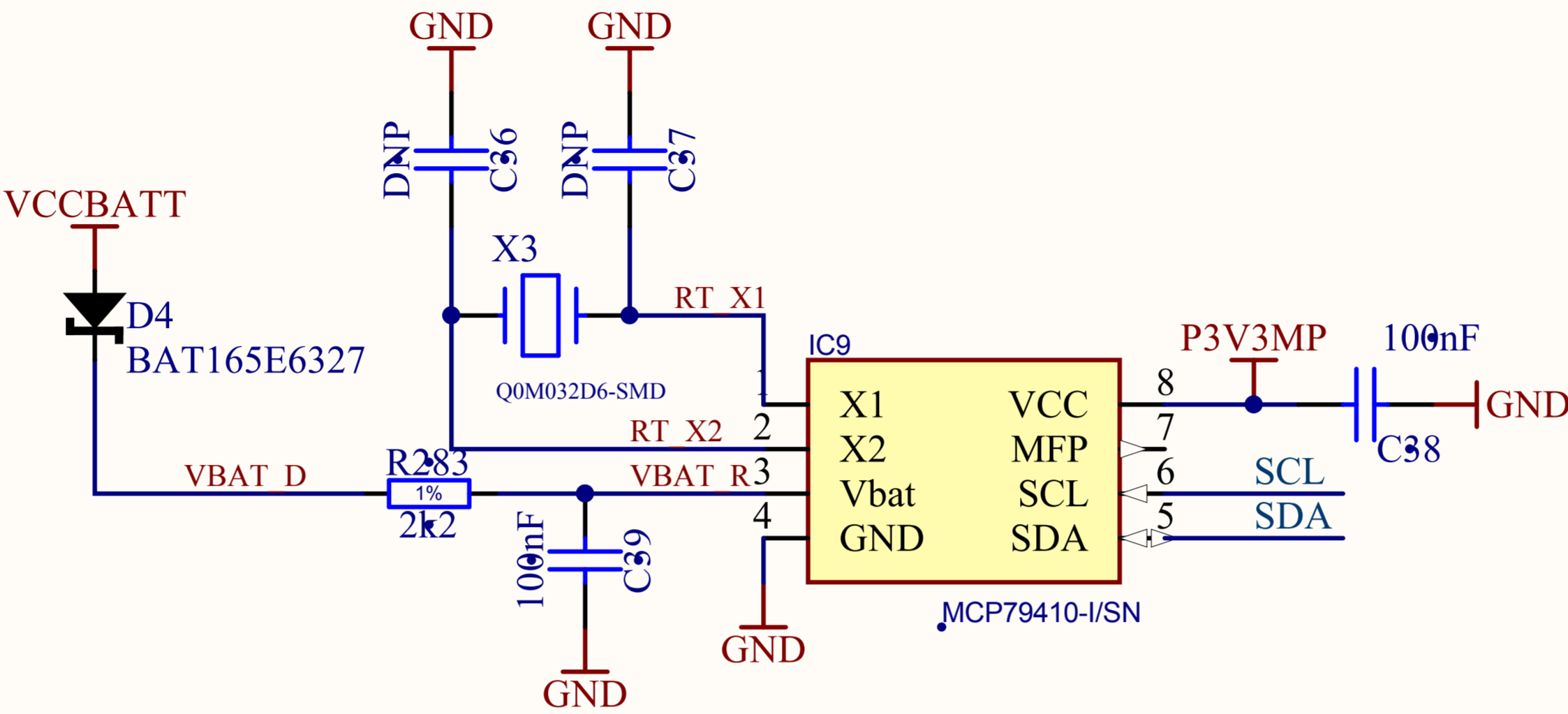
D

A

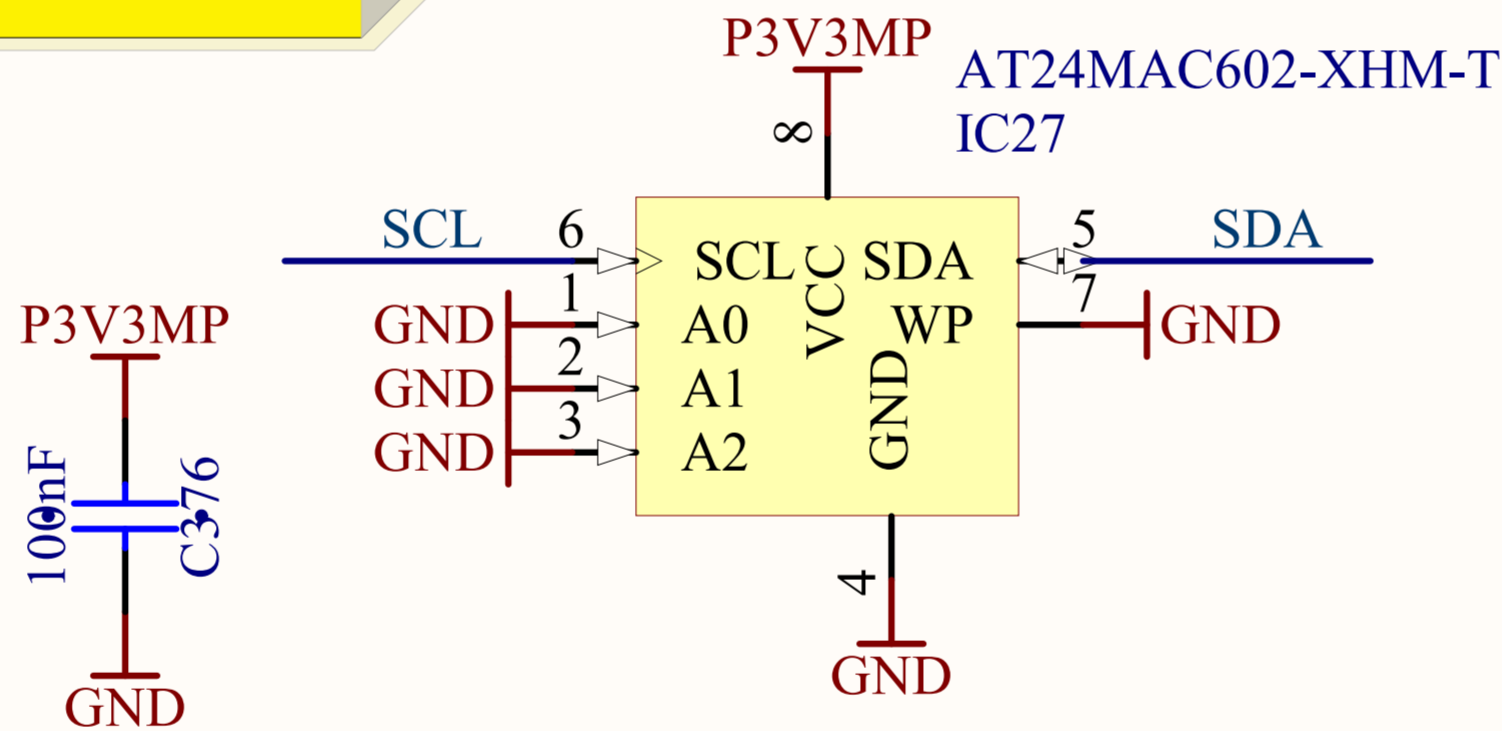
B

C

D



Added Resistor and schotky to Vbat



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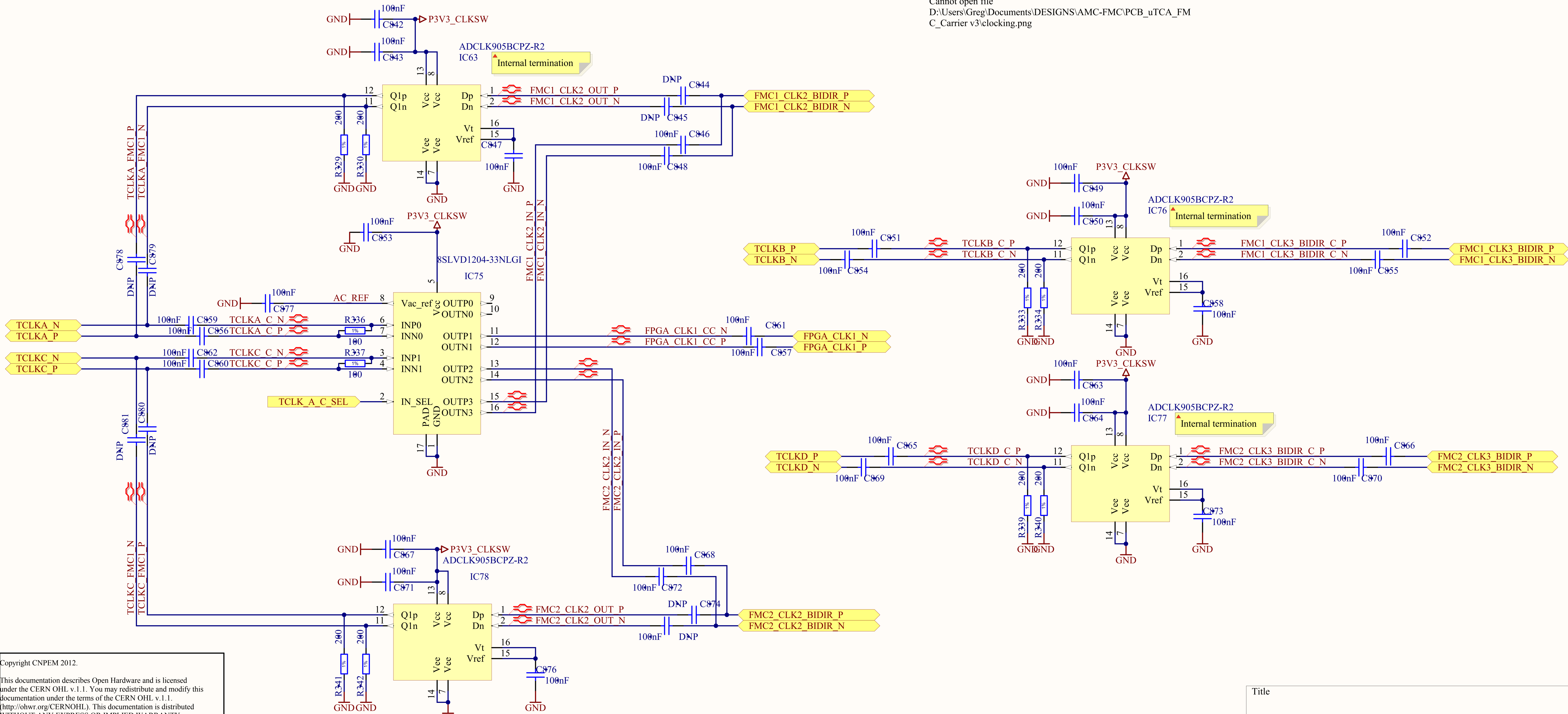
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Title		
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SE60DE100

TCLKB\_C\_P  
TCLKB\_C\_N  
TCLKD\_C\_P  
TCLKD\_C\_N  
TCLKA\_C\_P  
TCLKA\_C\_N  
TCLKC\_C\_P  
TCLKC\_C\_N  
TCLKC\_FMC1\_N  
TCLKC\_FMC1\_P  
TCLKA\_FMC1\_P  
TCLKA\_FMC1\_N  
FMC1\_CLK3\_BIDIR\_C\_P  
FMC1\_CLK3\_BIDIR\_C\_N  
FMC2\_CLK3\_BIDIR\_C\_P  
FMC2\_CLK3\_BIDIR\_C\_N  
FMC2\_CLK2\_IN\_N  
FMC2\_CLK2\_IN\_P  
FMC1\_CLK2\_IN\_P  
FMC1\_CLK2\_IN\_N  
FPGA\_CLK1\_C\_P  
FPGA\_CLK1\_C\_N  
FMC1\_CLK2\_OUT\_P  
FMC1\_CLK2\_OUT\_N  
FMC2\_CLK2\_OUT\_P  
FMC2\_CLK2\_OUT\_N

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C\_Carrier v3\clocking.png



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Title		
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A3		
Date:	2014-08-01	Sheet of
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