
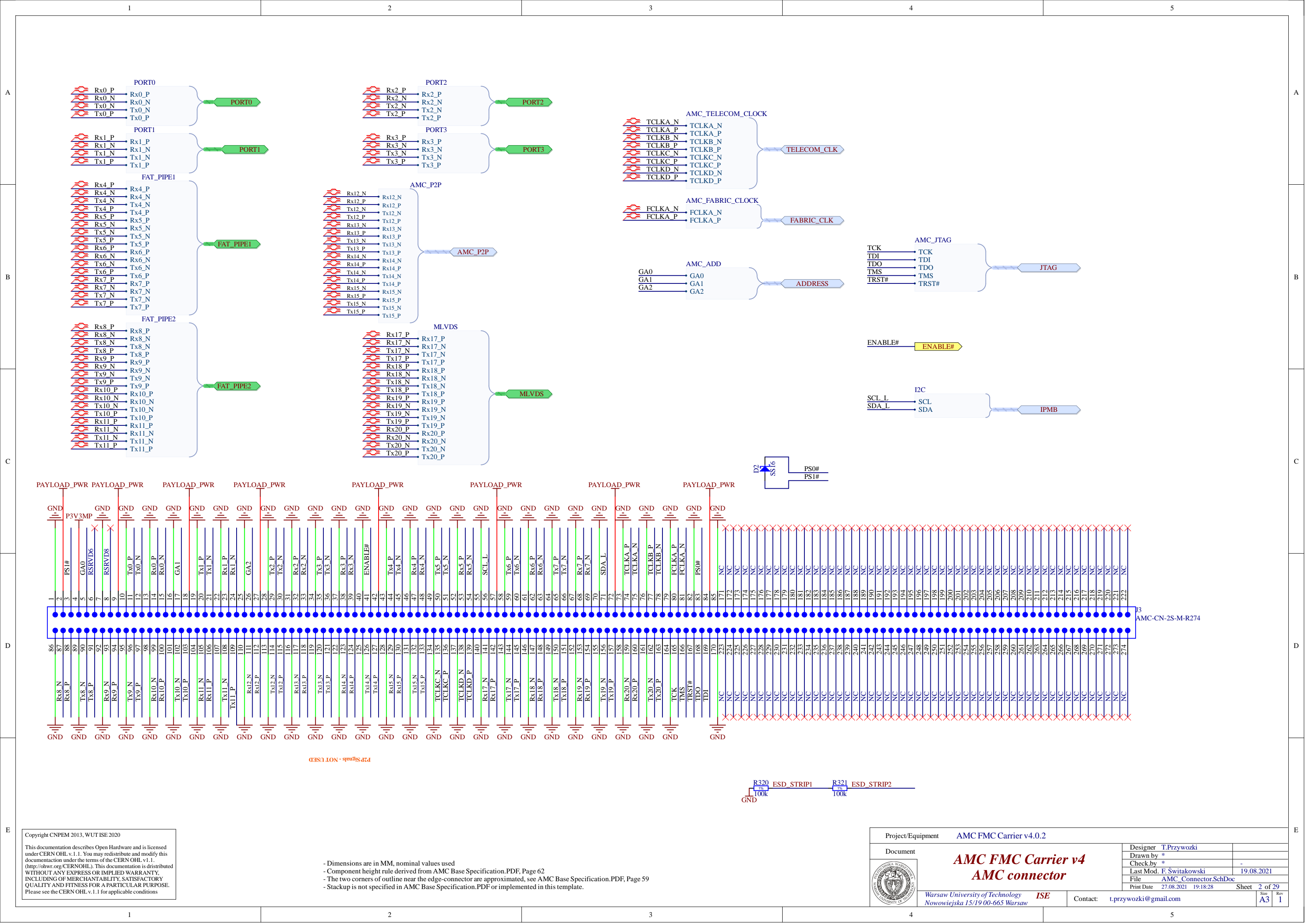
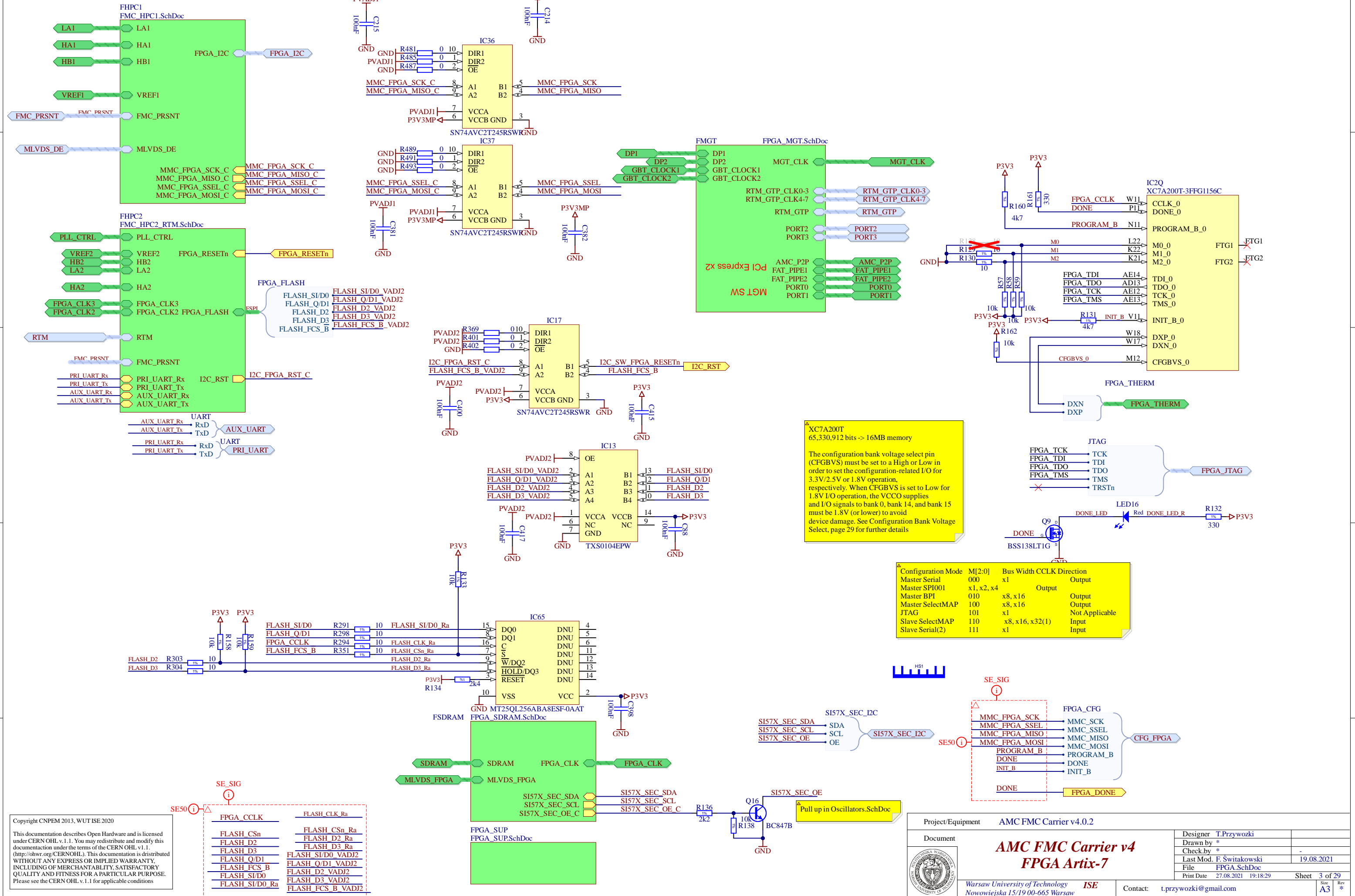


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Project/Equipment		AMC_FMC_Carrier v4.0.2	
Document		<div><div>AMC FMC Carrier v4</div><div>Top</div><div><div><div><div></div><div></div></div><div>Warsaw University of Technology</div><div>Nowowiejska 15/19 00-665 Warsaw</div></div><div>ISE</div><div>Contact: t.przywozki@gmail.com</div></div></div>	
	Designer	T.Przywozki	
	Drawn by	*	XX/XX/XXXX
	Check by	*	-
	Last Mod.	F. Switakowski	24.08.2021
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	Print Date	27.08.2021 19:18:28	Sheet 1 of 29
		Size	Rev
		A3	1





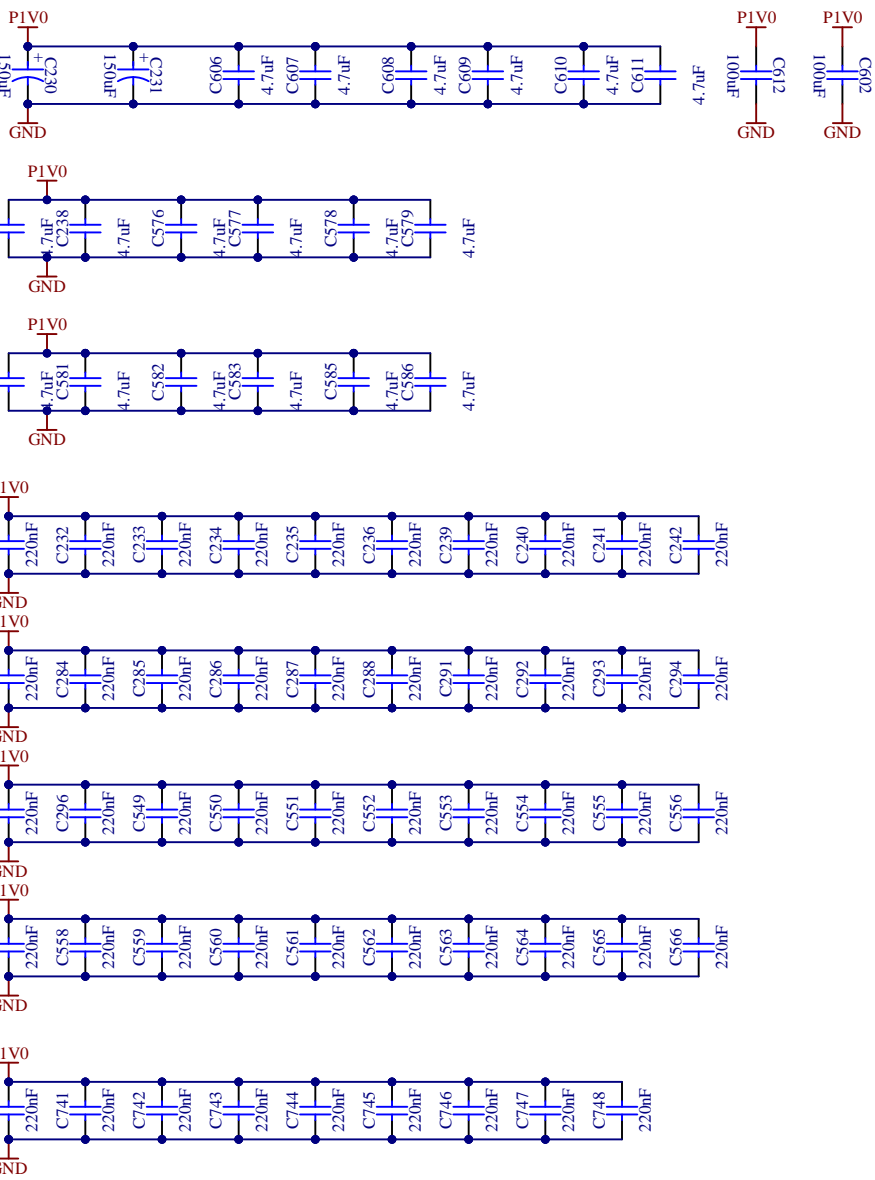
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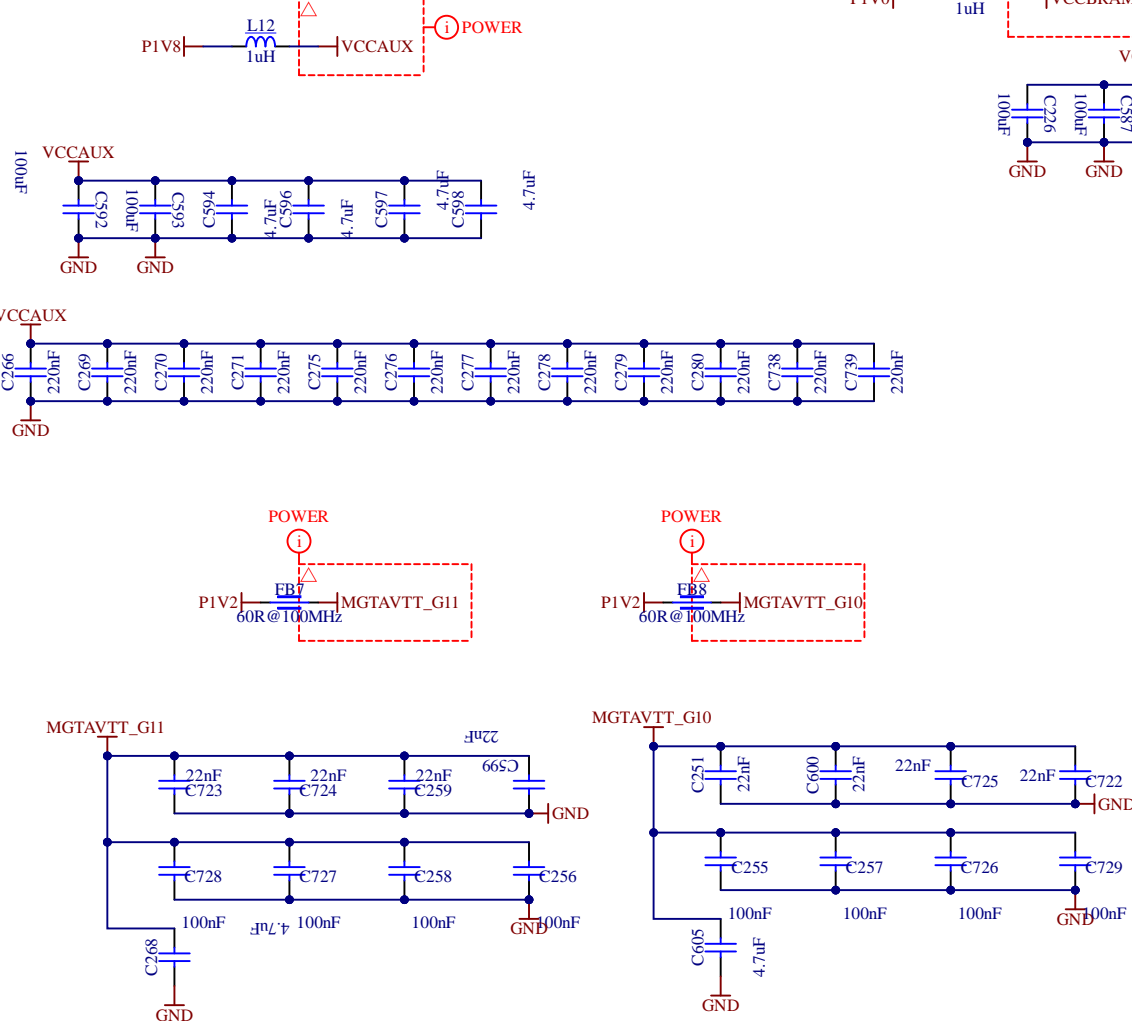
## VCCINT

1x680uF, 2x100uF, 28x4.7uF  
42x0.47uF on PG.34



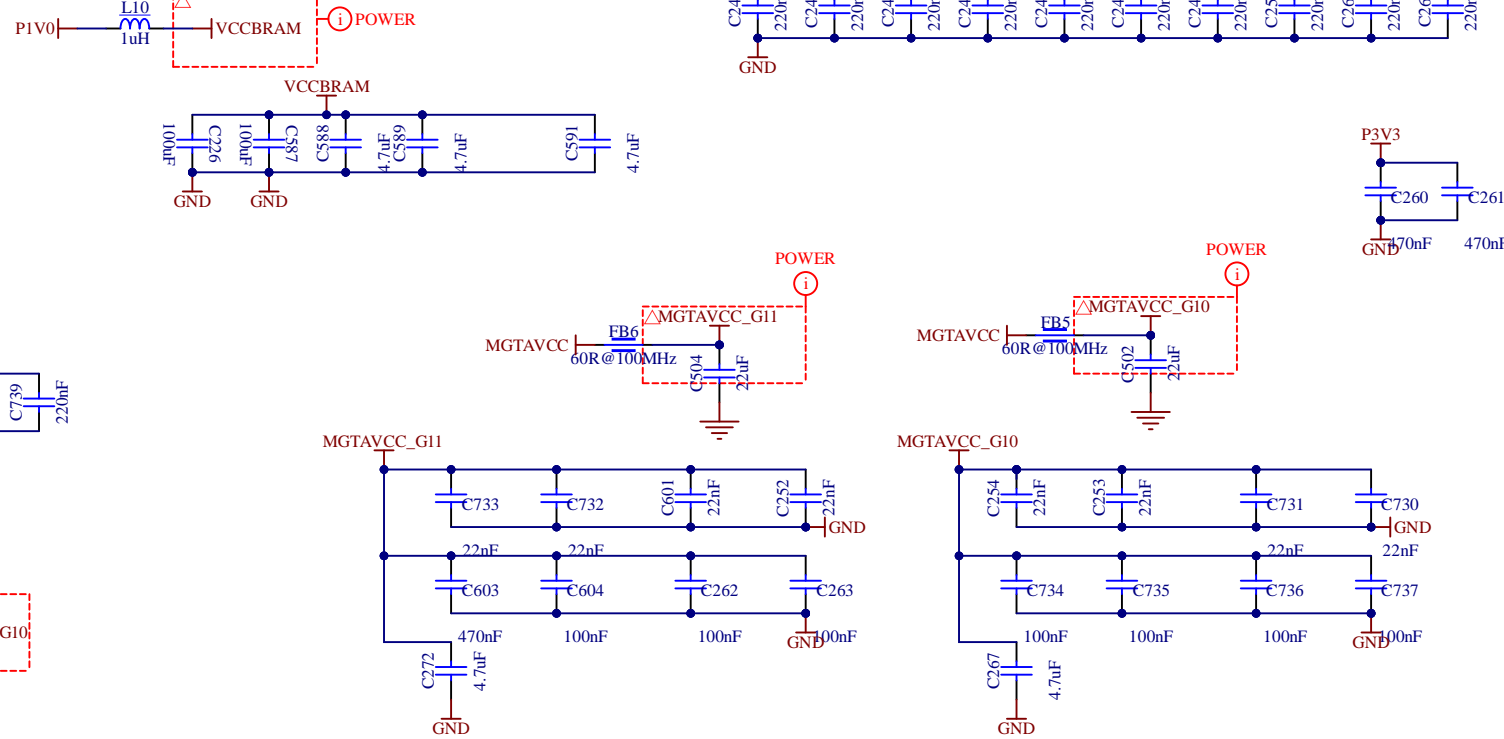
## VCCAUX

3x47uF, 4x4.7uF, 7x0.47uF



## VCCBRAM

2x100uF, 4x4.7uF, 8x0.47uF



MGTAVCC	1V	2.3A		
MGTAVTT	1.2V	1.5A		
MGTVCCAUX	1.8V	0.5A		
VCCAUX	1.8V	1A		seq1
VCCAUX_IO	1.8/2V	01A		seq1
VCCBRAM	1V	1.8A		seq0
VCCINT	1V	6A		seq0
VCCO_1.2	1.2V	3.2A		seq2
VCCO_1.35	1.35V	0.9A		seq2
VCCO_1.5	1.5V	0.9A		seq2
VCCO_1.8	1.8V	0.9A		seq2
VCCO_2.5	2.5V	0.9A		seq2
VCCO_3.3	3.3V	0.9A		seq2

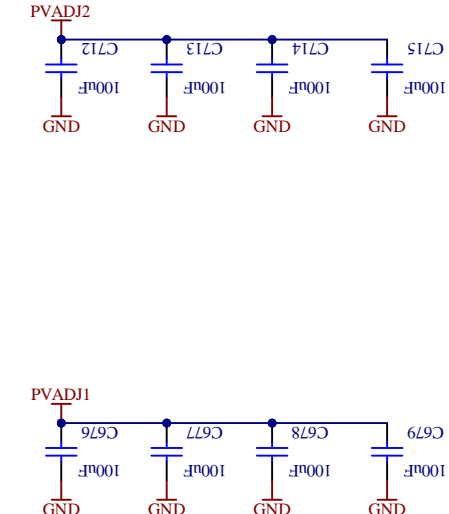
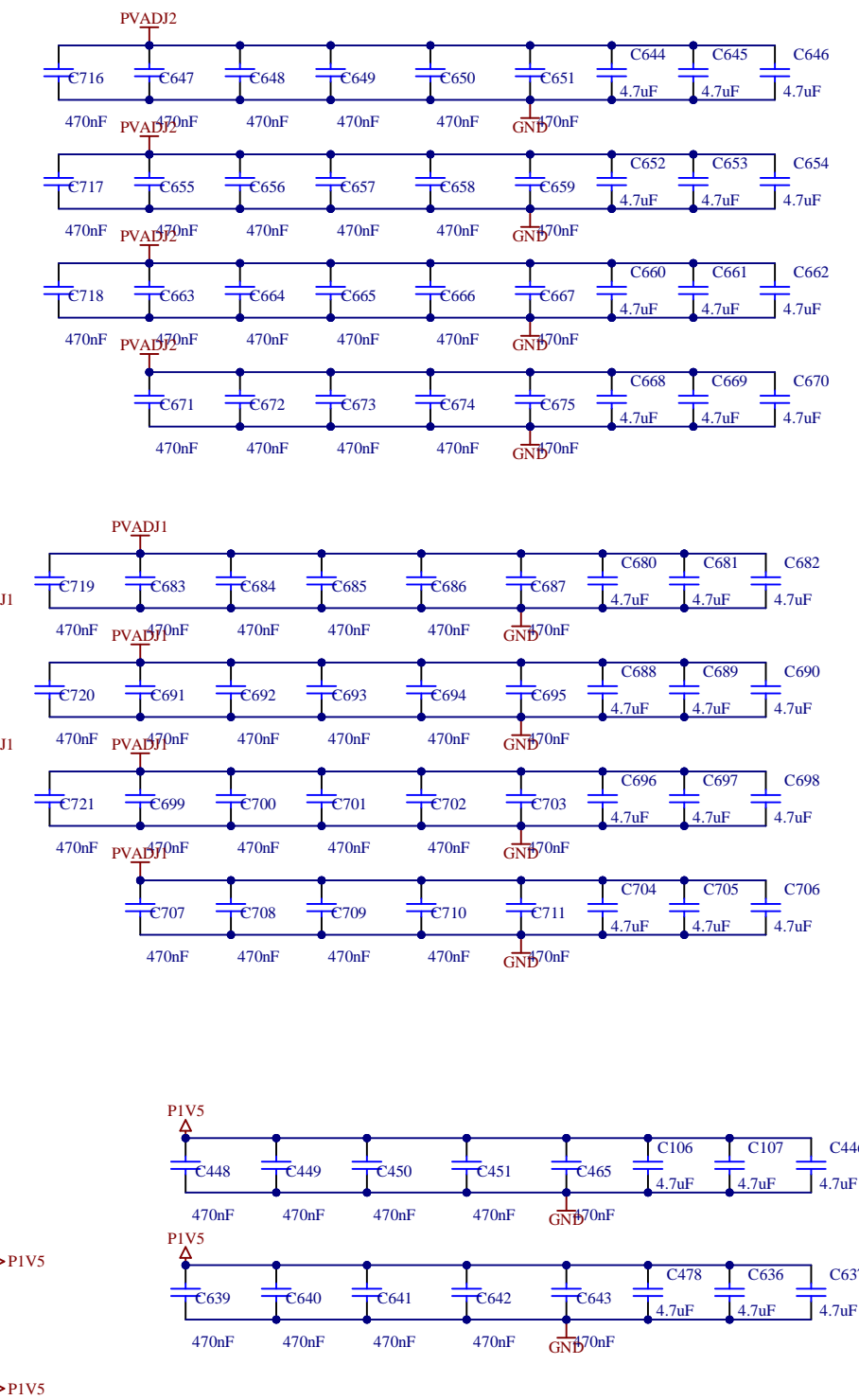
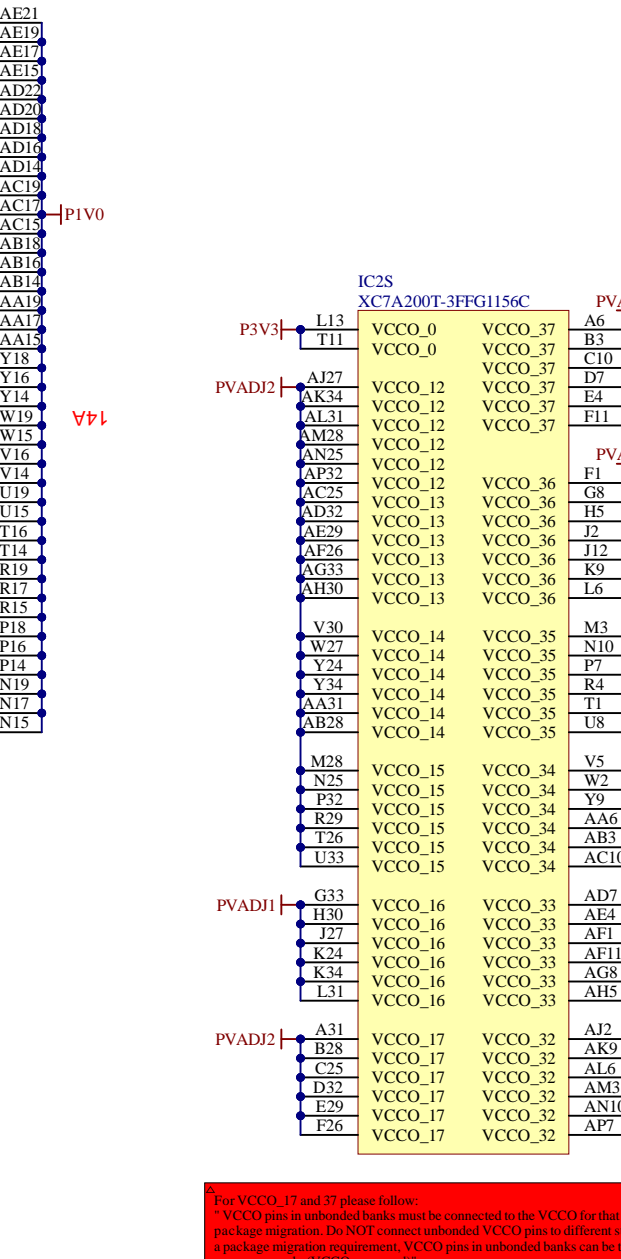
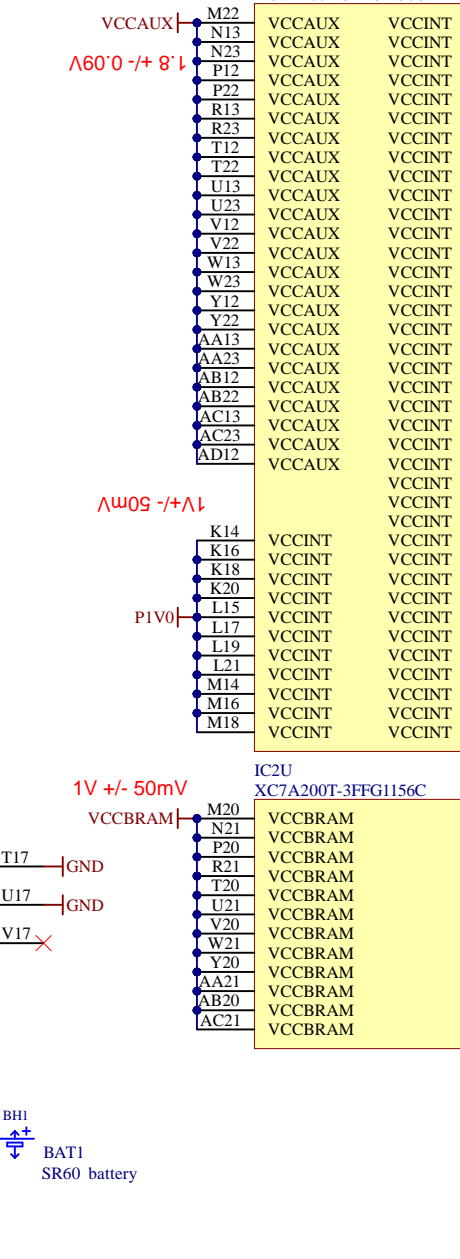
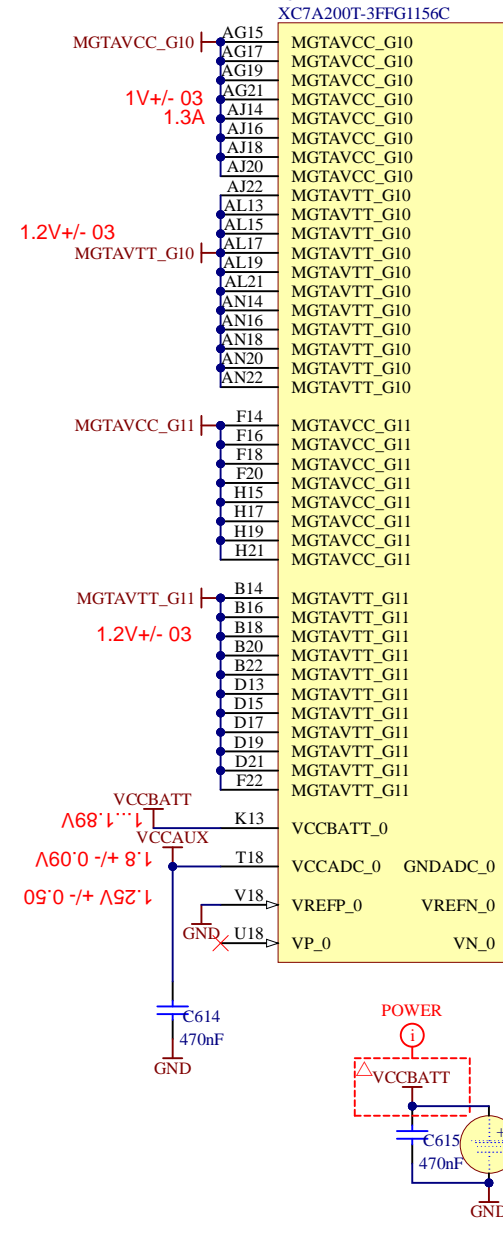
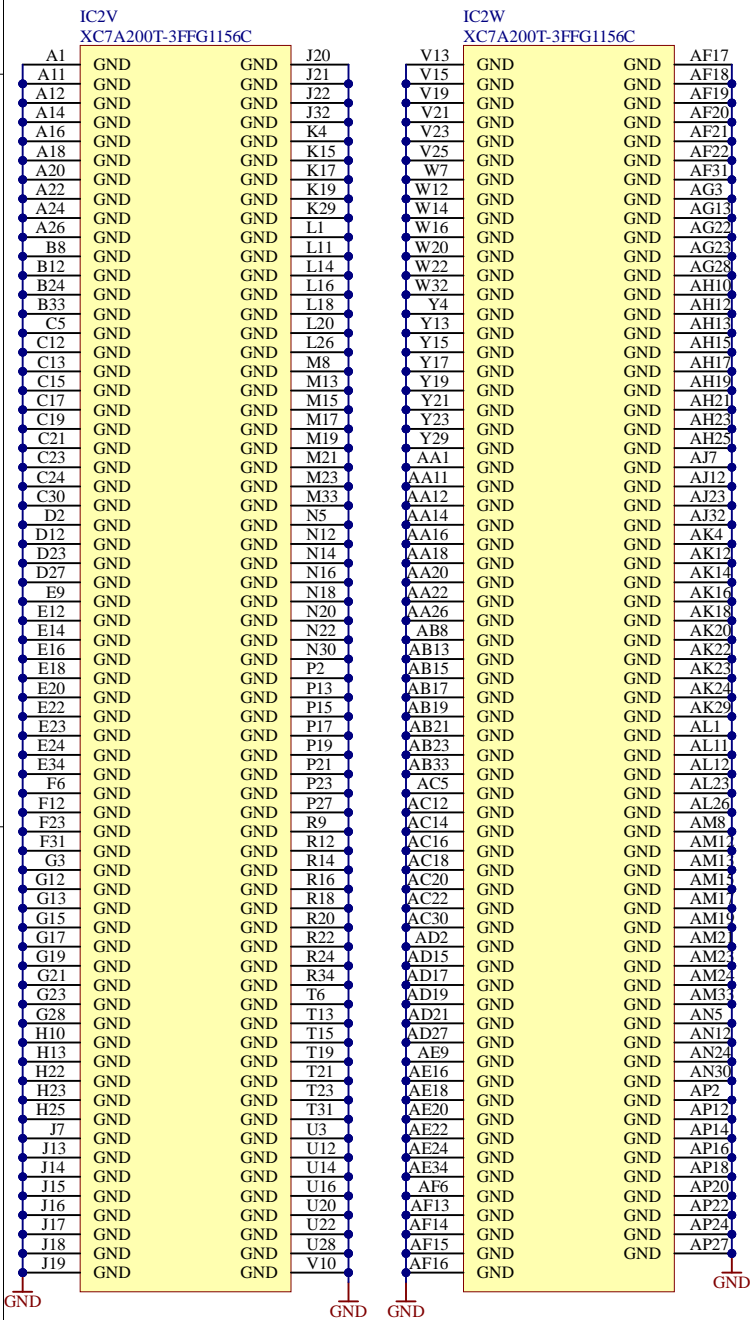
power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO voltage difference between VCCO and VCCAUX must not exceed 2.625V for longer than TVCCO2VCCAUX

power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC.

VMGTAVTT OR VMGTAVCC, VCCINT, VMGTAVTT. There is no recommended sequencing for VMGTVCCAUX. Both VMGTAVCC and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

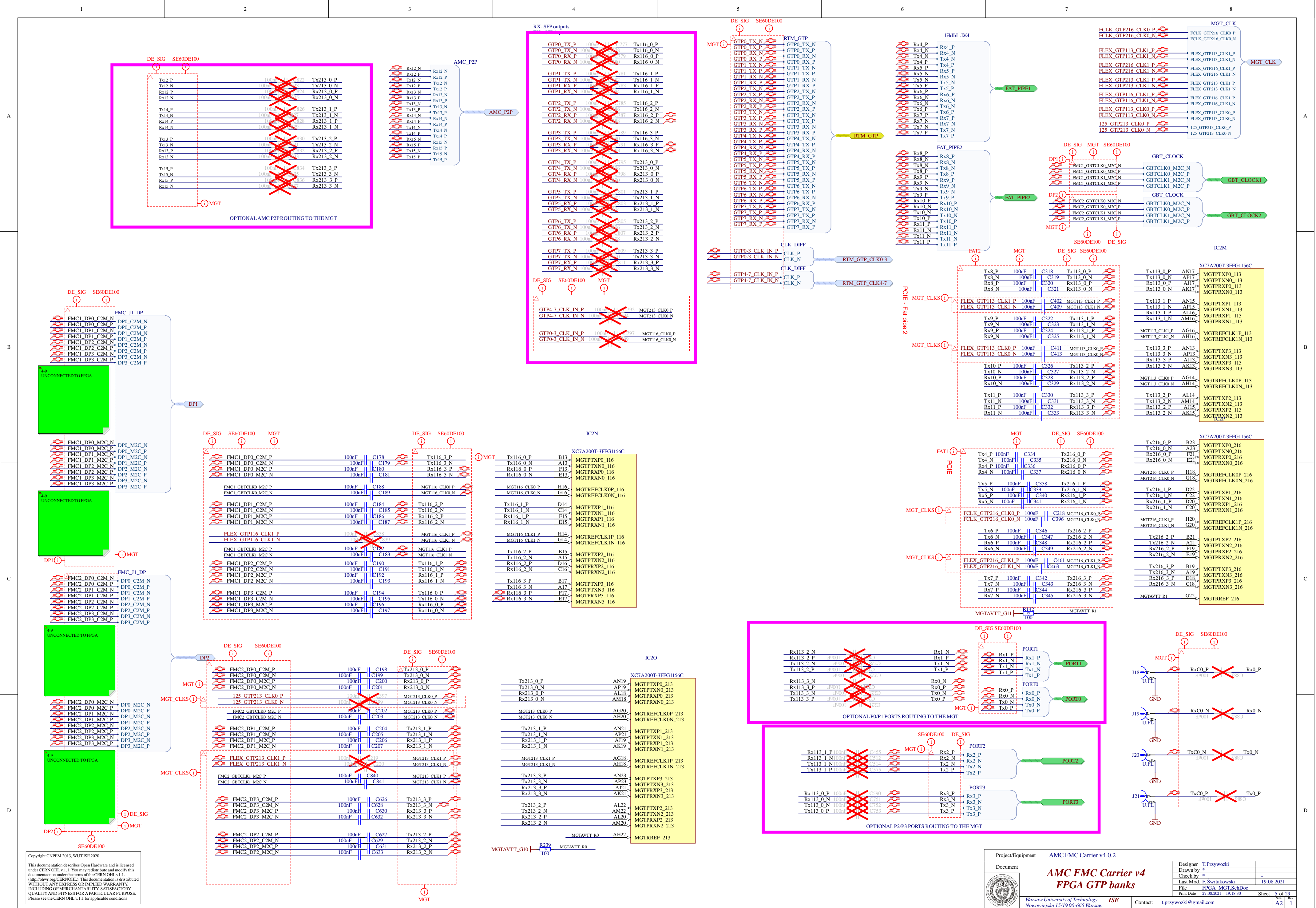
When VMGTAVTT is powered before VMGTAVCC and VMGTAVTT - VMGTAVCC > 150 mV and VMGTAVCC < 0.7V, the VMGTAVTT current draw can increase by 50 mA per transceiver during VMGTAVCC ramp up. The duration of the current draw can be up to 0.3 x TMGTAVCC (ramp time from GND to 90% of VMGTAVCC). The reverse is true for power-down.

• When VMGTAVTT is powered before VCCINT and VMGTAVTT - VCCINT > 150 mV and VCCINT < 0.7V, the VMGTAVTT current draw can increase by 50 mA per transceiver during VCCINT ramp up. The duration of the current draw can be up to 0.3 x TVCCINT (ramp time from GND to 90% of VCCINT). The reverse is true for power-down.



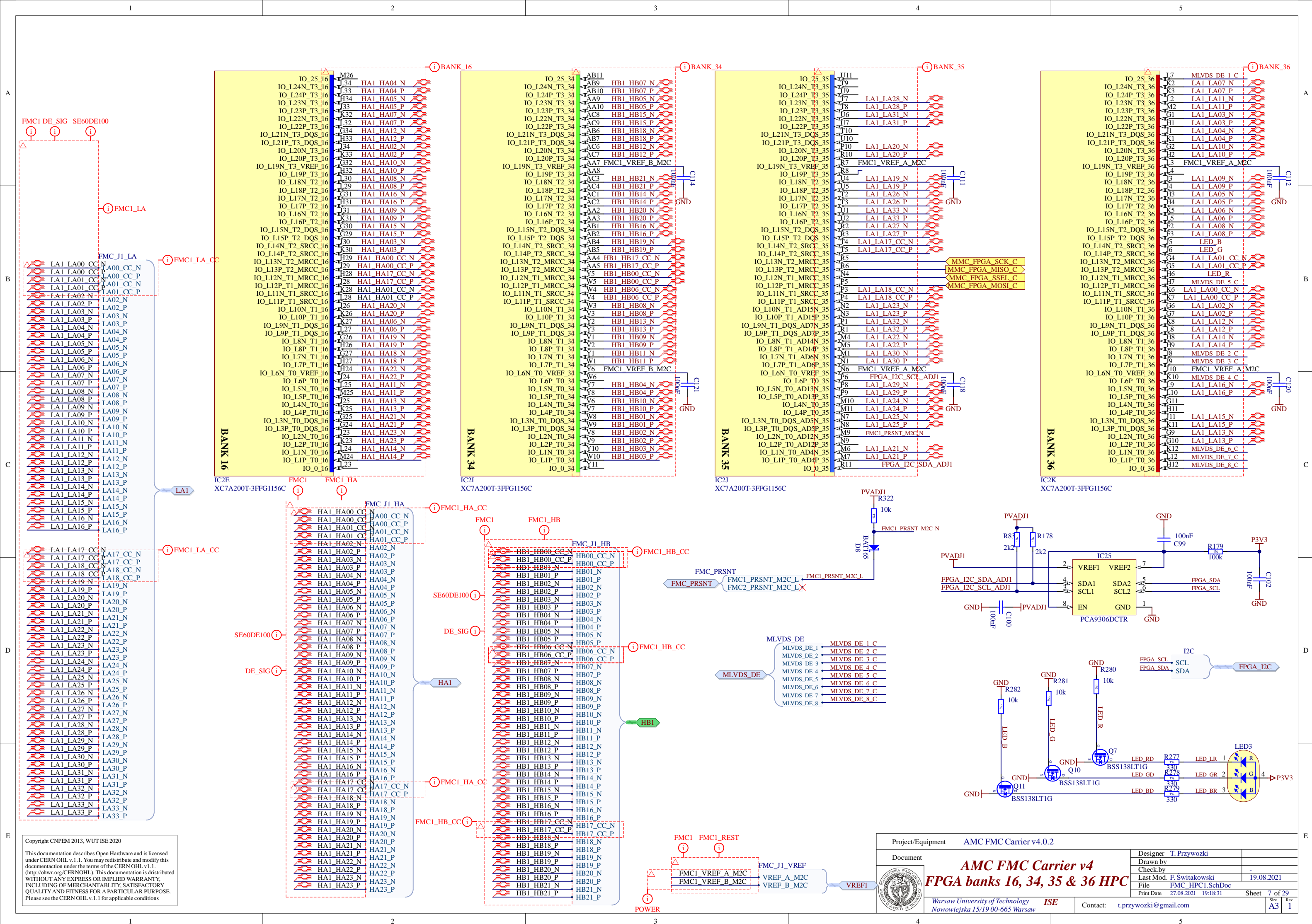
For VCCO\_1.7 and 3.7 please follow:  
- VCCO pins in unbonded banks must be connected to the VCCO for that bank for package migration. Do NOT connect unbonded VCCO pins to different supplies. Without package migration requirement, VCCO pins in unbonded banks can be tied to a common supply (VCCO or ground).  
- No migration available (since there is no SMD) - recommend connecting to carry power rail and using as power decoupling placeholder for decaps. Remove banks C222 and C219



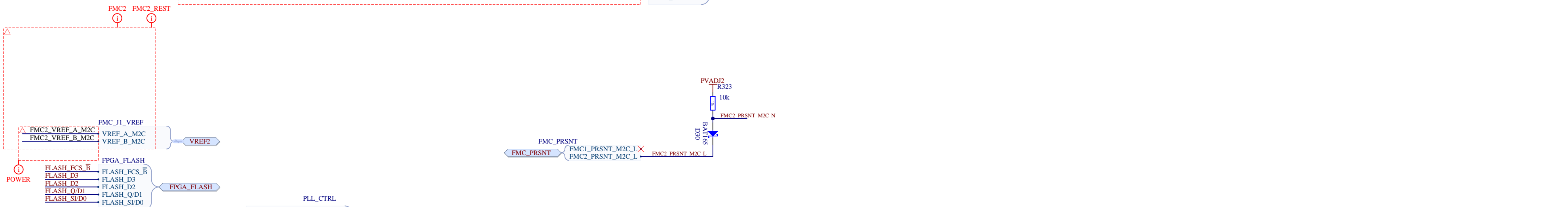
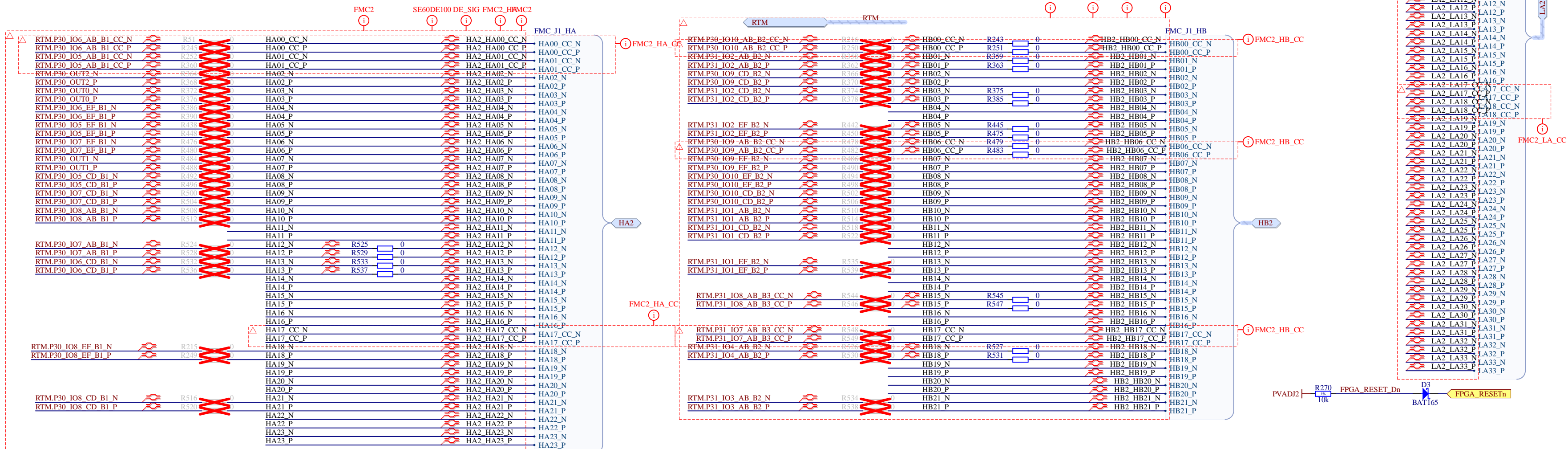
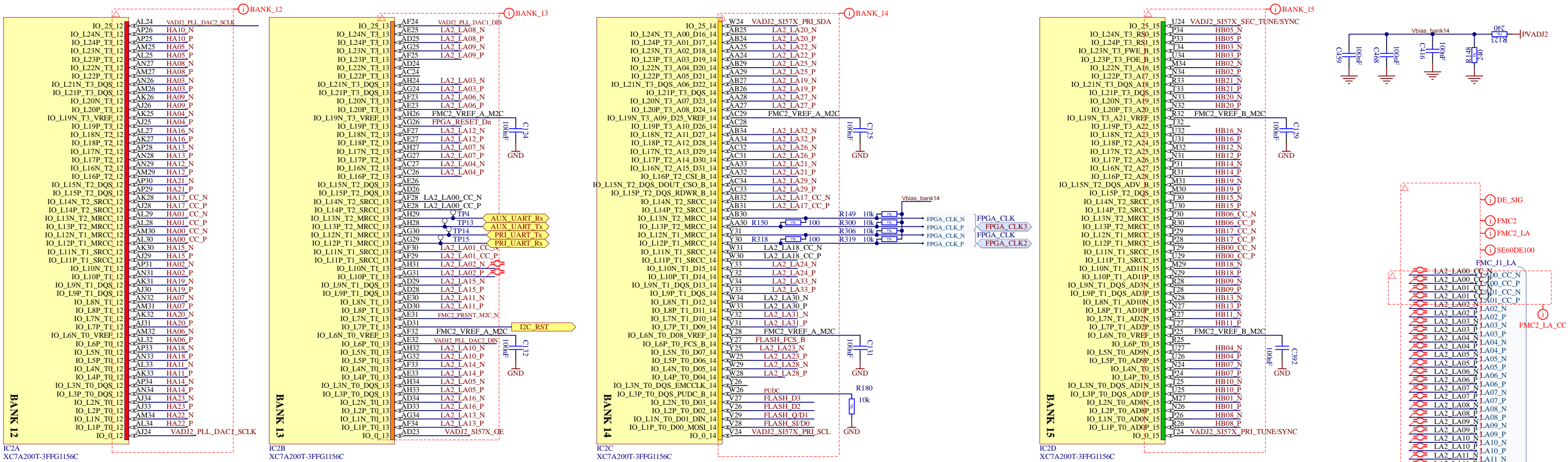








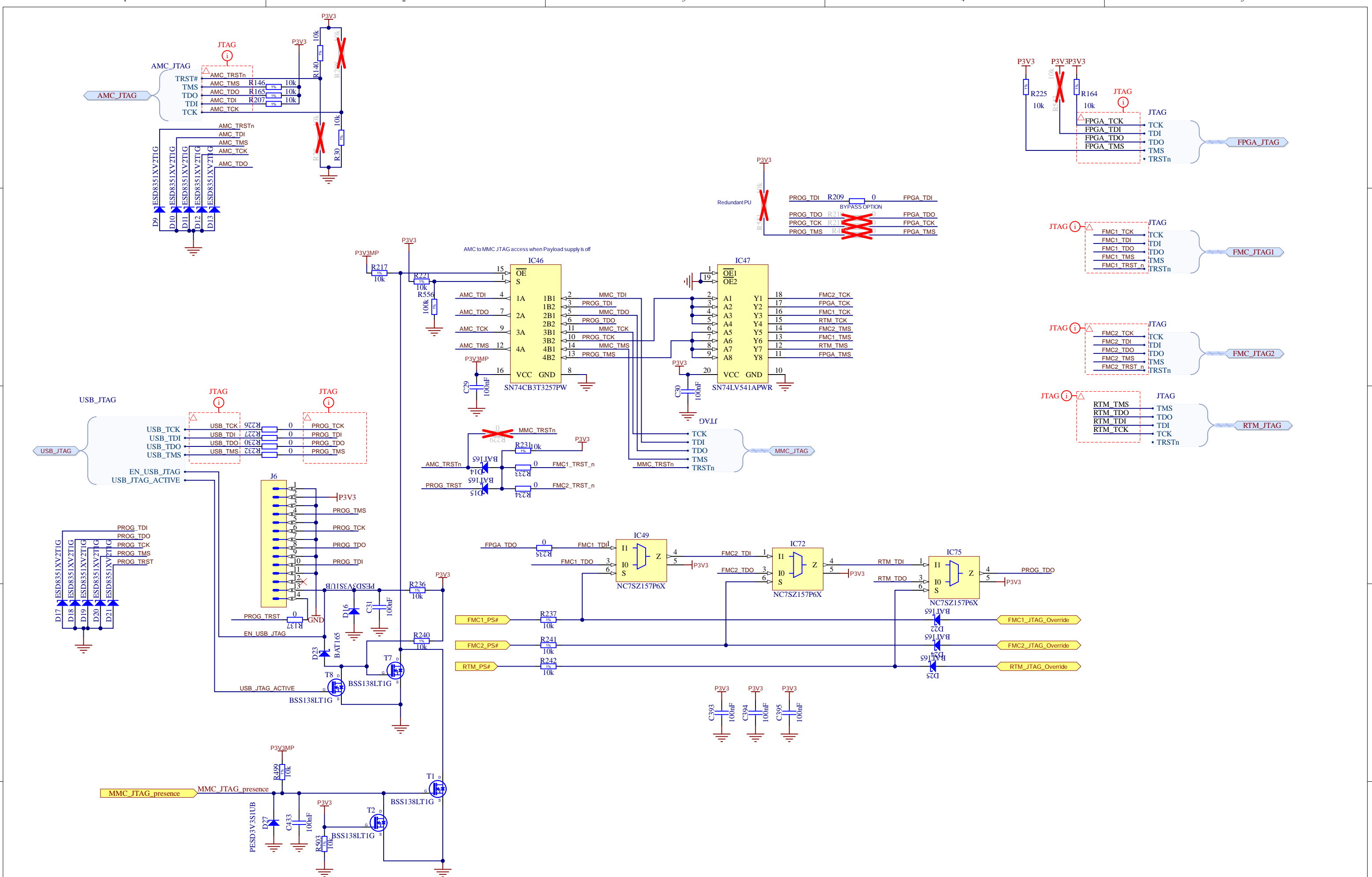




IC2A	IC2B
XC7A200T-3FFG1156C	XC7A200T-3FFG1156C

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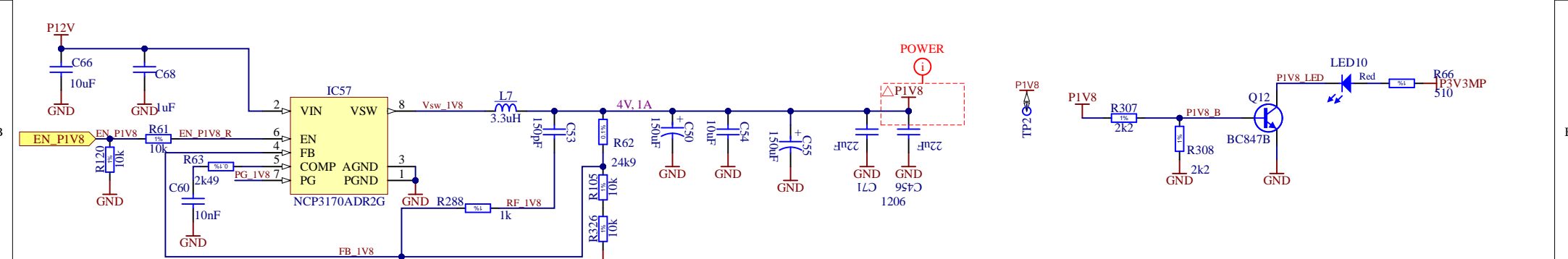
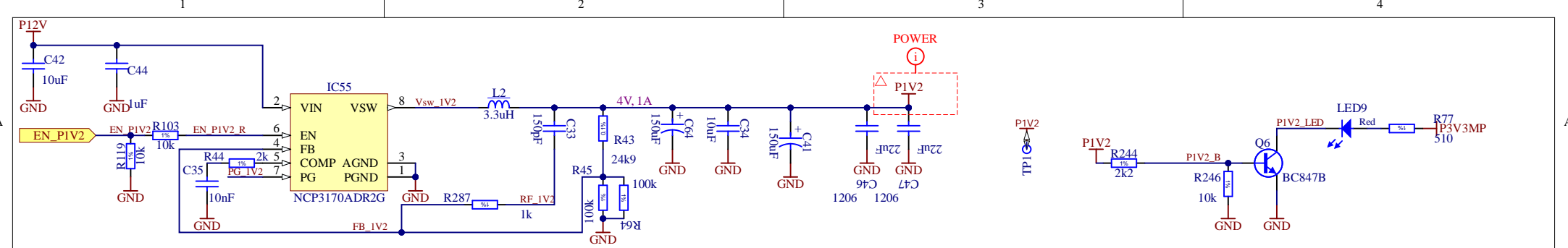
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GND

The diagram shows a circuit configuration for a power supply unit (PSU). A block labeled "PSU\_PG" is connected to a node. This node is connected to a "PSU\_PG" signal line. There are two parallel branches, each containing a resistor (R289 and R290) and a 1% tolerance box. The branches are labeled "PG\_1V8" and "PG\_1V2". There are red "X" marks on the "PG\_1V8" and "PG\_1V2" labels. The node is also connected to a 0V ground symbol.

Δ	VIN	Vout	Lout	R1	R2	Rf	Cf(pF)	Cc(nF)	Rc(k)	Cp(pF)	Resistance for Current Gain
12	0.8	1.8	24.9	NI	NI	NI	NI	NI	15	3.6	
12	1.0	2.5	24.9	100	1	150	15	0.825	NI	4	
12	1.1	2.5	24.9	66.5	1	150	10	2	NI	20	
12	1.2	2.5	24.9	49.9	1	150	10	2	NI	20	
12	1.5	3.6	24.9	28.7	1	150	10	2.49	NI	20	
12	1.8	3.6	24.9	20	1	150	10	2.49	NI	20	
12	2.5	4.7	24.9	11.8	1	150	8.2	3.74	NI	25	
12	3.3	4.7	24.9	7.87	1	150	6.8	4.99	NI	27	
12	5.0	7.2	24.9	4.75	1	150	3.9	10	NI	27	

D

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PSU\_PG

PG\_IV8 R289 1% 0

PG\_IV2 R290 1% 0

PSU\_PG

Project/Equipment AMC FMC Carrier v4.0.2

Document

Designer T. Przywozki

Drawn by

Check by

Last Mod. F. Świtkowski 19.08.2021

File SUP\_1.2\_1.8.SchDoc

Print Date 27.08.2021 19:18:33

Sheet 11 of 29

Size A4

Rev 1

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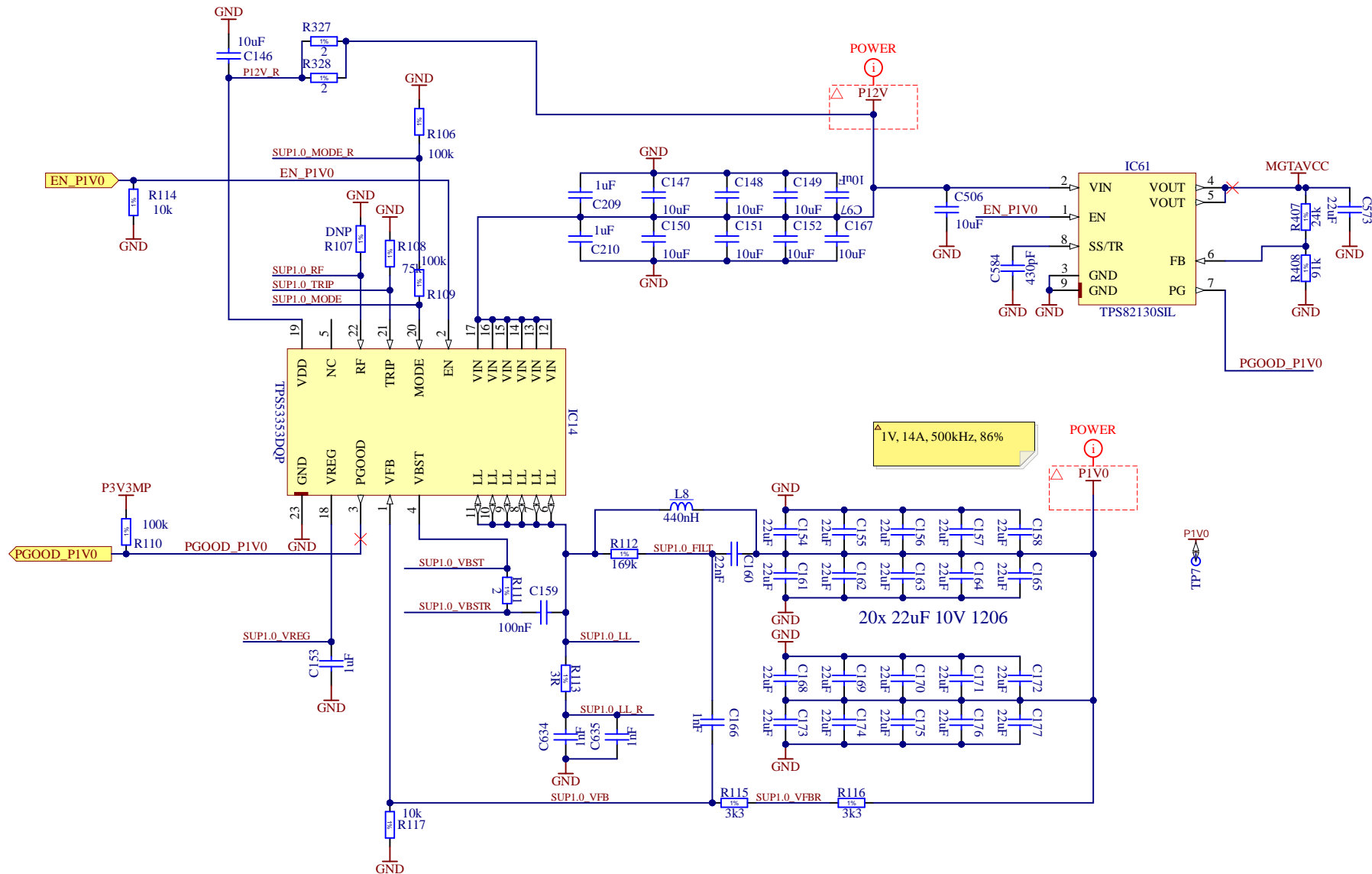
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Project/Equipment **AMC FMC Carrier v4.0.2**

Document



*AMC FMC Carrier v4*  
*Power P1V0*

Designer	T. Przywozki
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Last Mod. F. Świtakowski	19.08.2021
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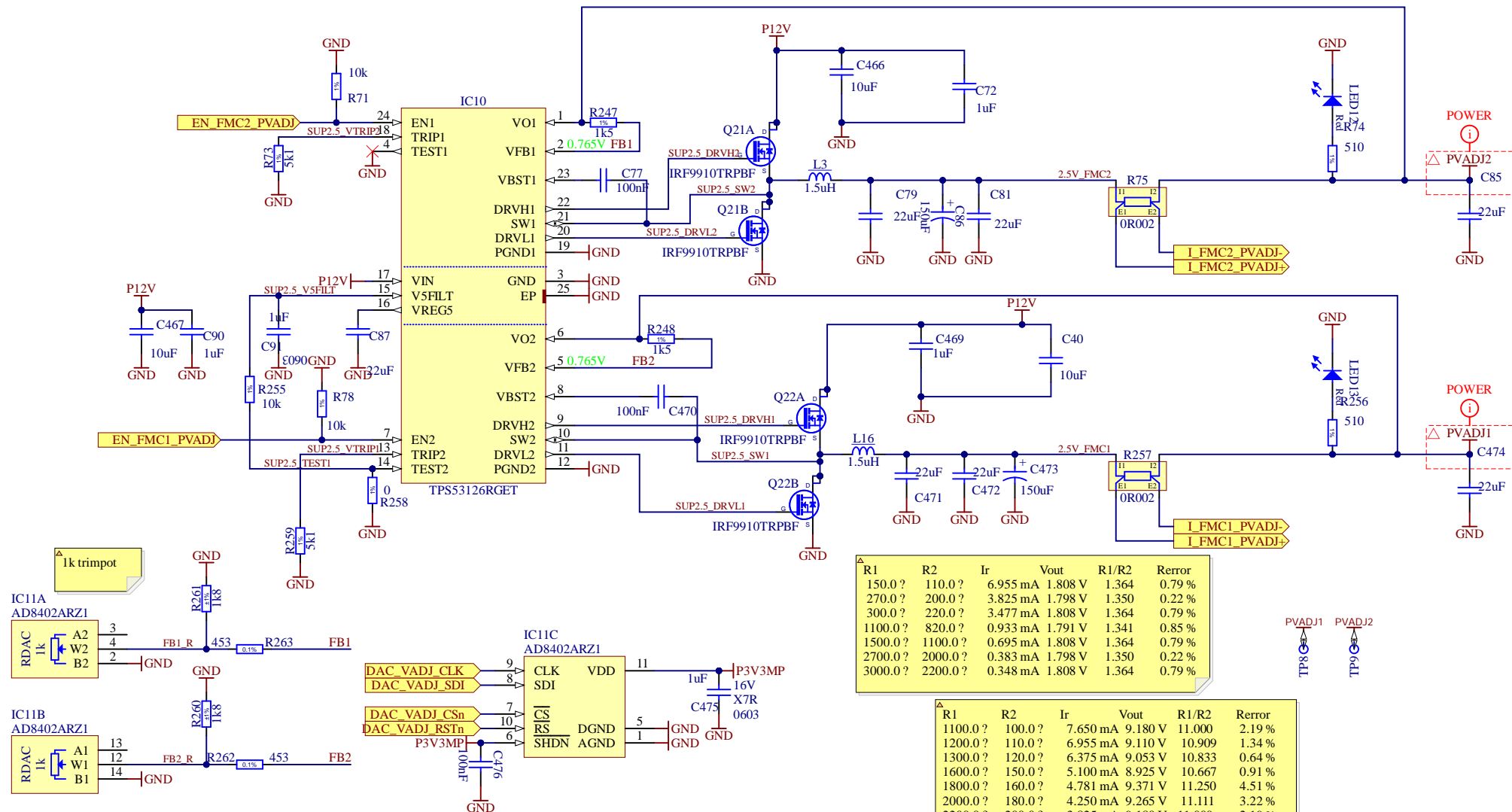
Sheet 14 of 29

Size	Rev
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Rev	
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Contact:	<a href="mailto:t.przywozki@gmail.com">t.przywozki@gmail.com</a>
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Project/Equipment **AMC FMC Carrier v4.0.2**

Document



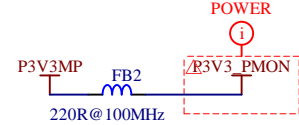
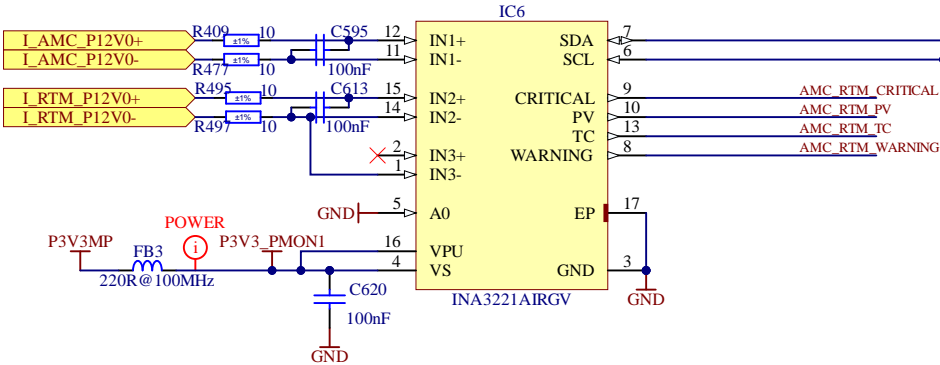
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Nowowiejska 15/19 00-665 Warsaw

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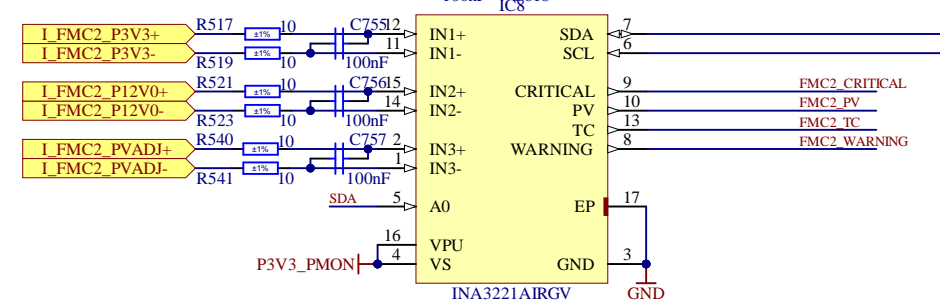
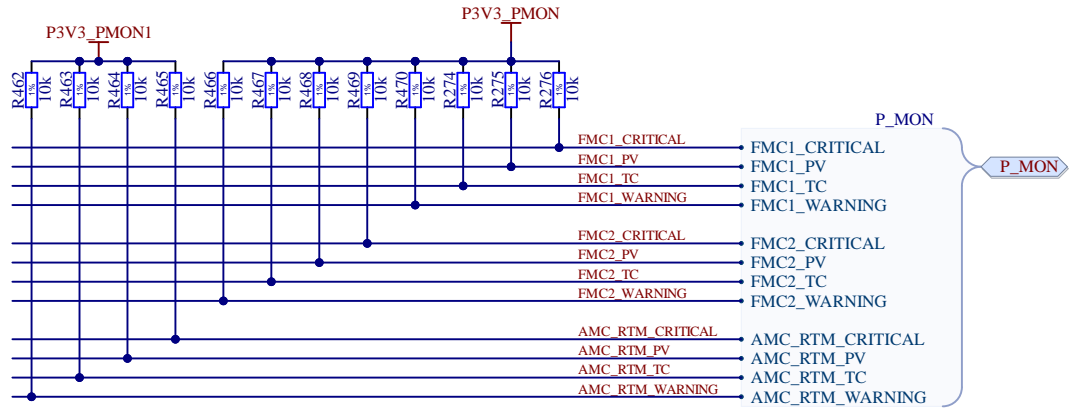
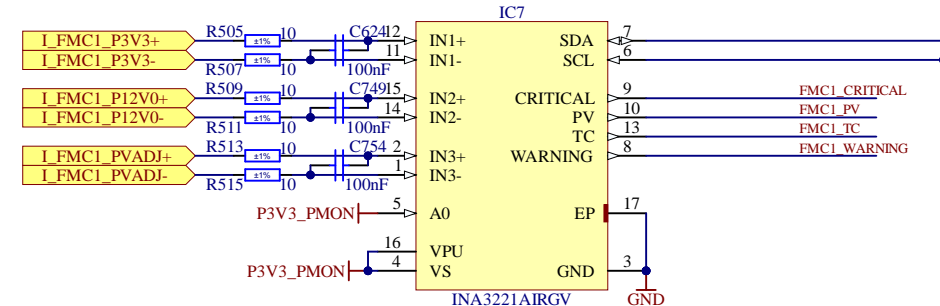
Contact: [t.przywozki@gmail.com](mailto:t.przywozki@gmail.com)

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Drawn by		XX/XX/XXXX
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Last Mod.	F. Świątkowski	19.08.2021
File	SUP_2.5_FMC.SchDoc	
Print Date	27.08.2021 19:18:34	Sheet 15 of 29

Size A4  
Rev 1



A1	SLAVE ADDRESS
GND	1000000
VS	1000001
SDA	1000010
SCL	1000011



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Check by		Last Mod.	F. Świtkowski 19.08.2021
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Sheet	16 of 29	Size	A4
Rev	1	Contact:	t.przywozki@gmail.com

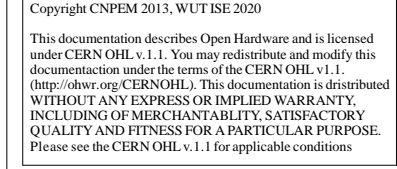


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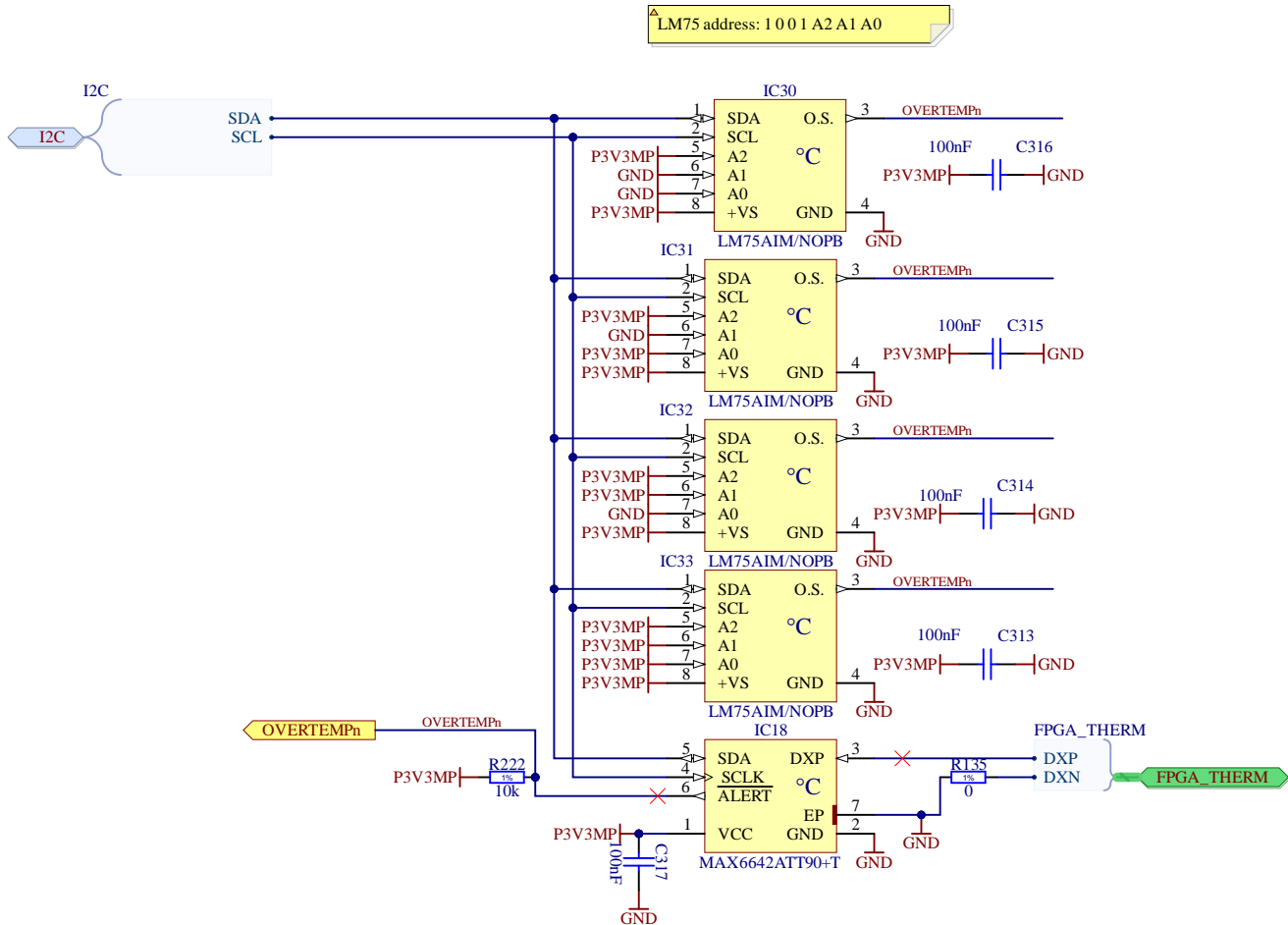
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Contact: t.przywozki@gmail.com








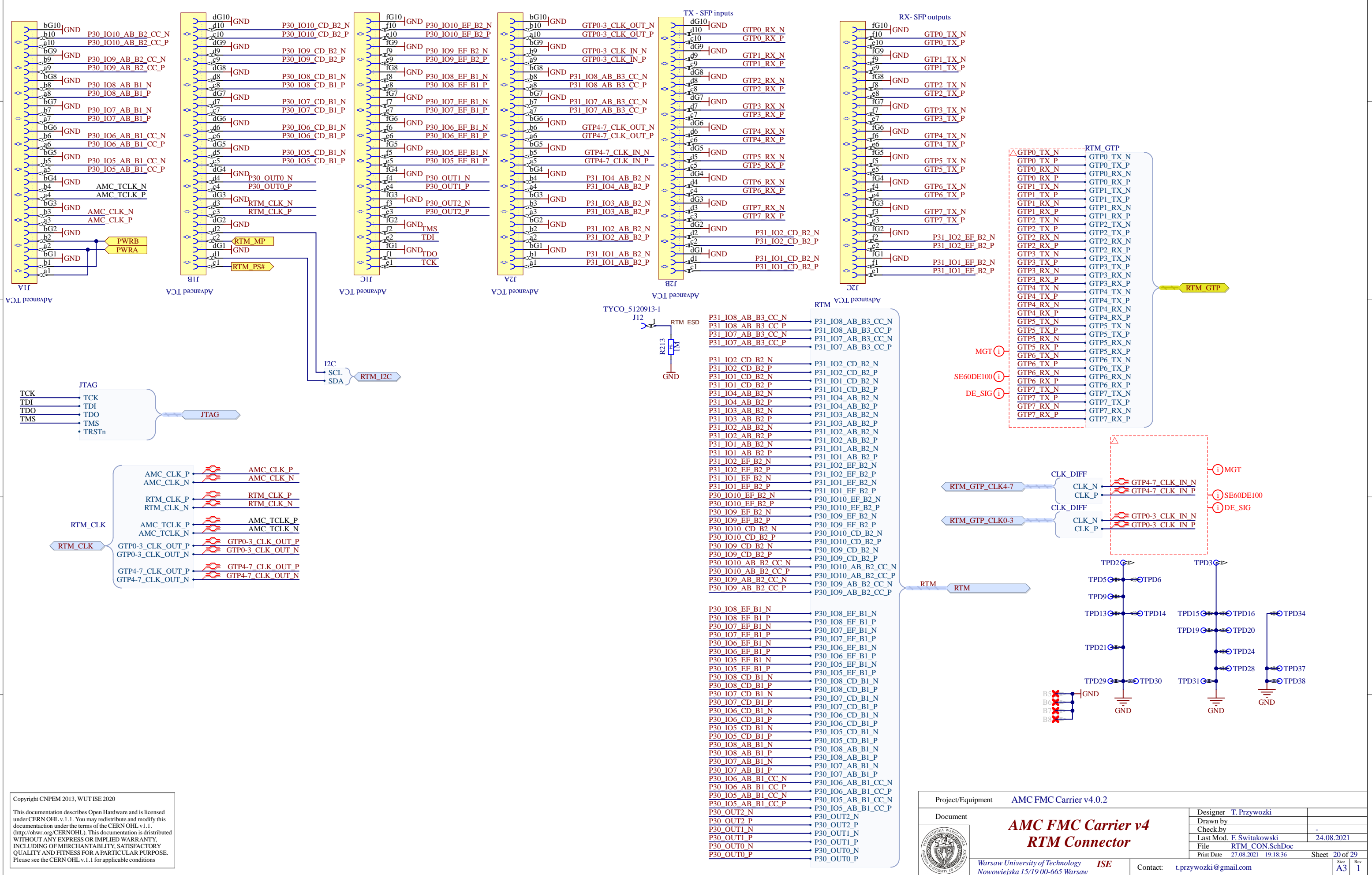


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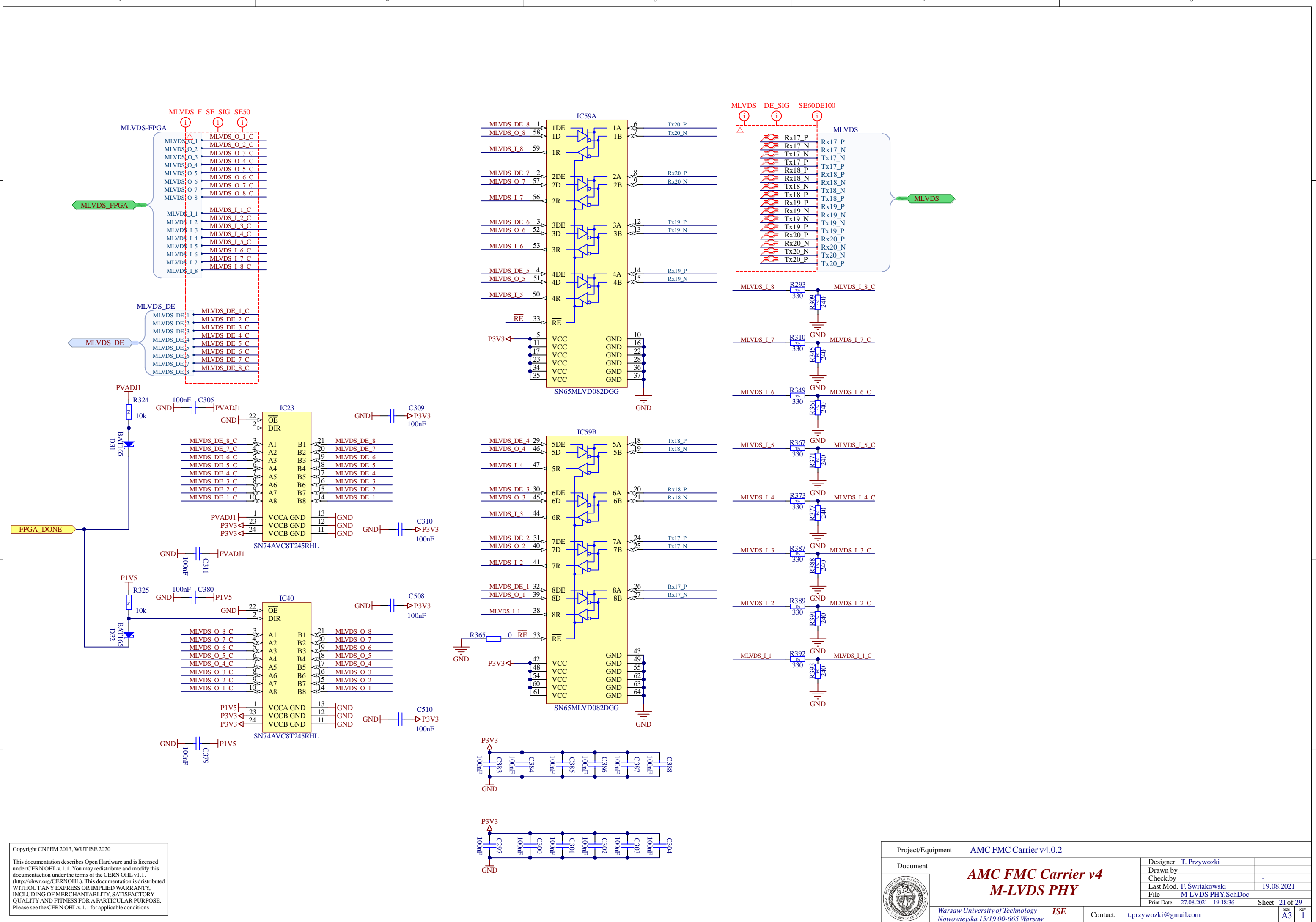
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			Print Date 27.08.2021 19:18:36	Sheet 19 of 29
	Warsaw University of Technology ISE Nowowiejska 15/19 00-665 Warsaw		Contact: t.przywozki@gmail.com	Size A4









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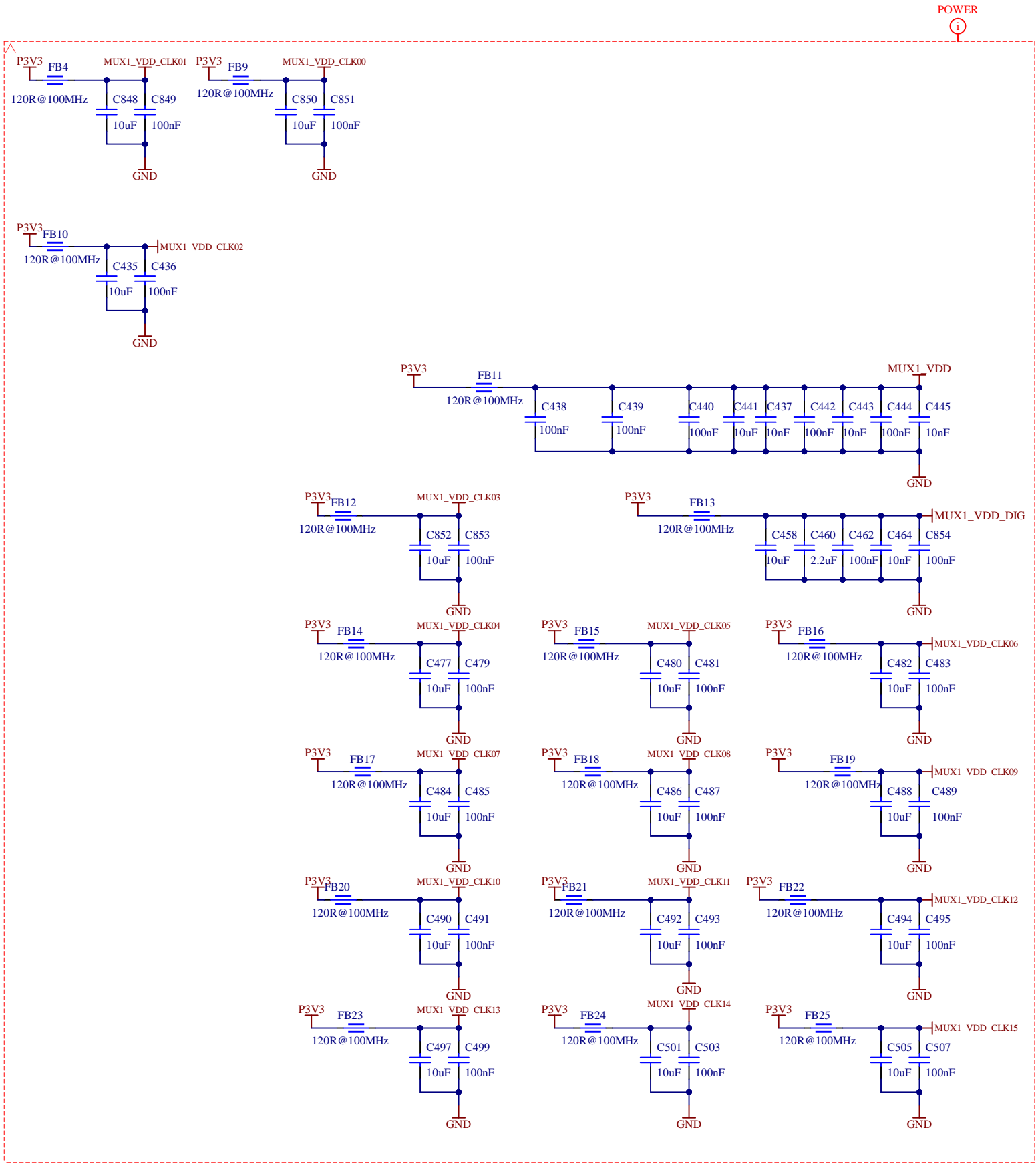
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Nowowiejska 15/19 00-665 Warsaw

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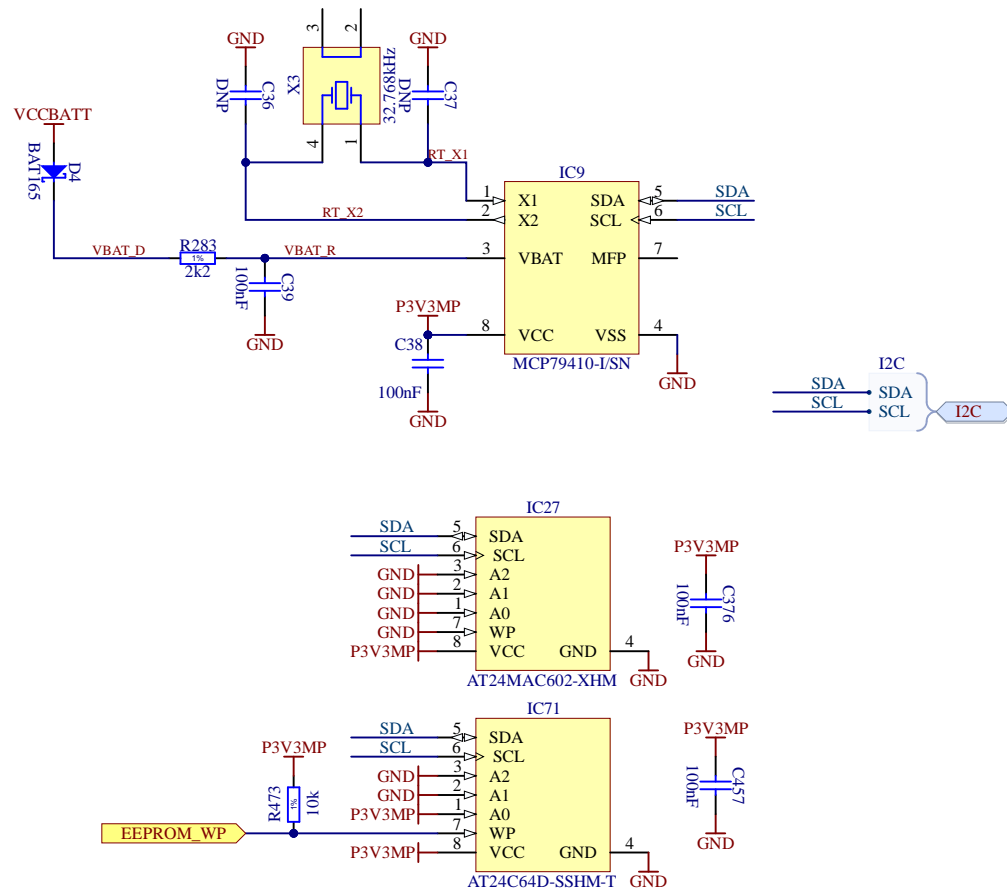




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Project/Equipment		AMC FMC Carrier v4.0.2	
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	Designer		T. Przywozki
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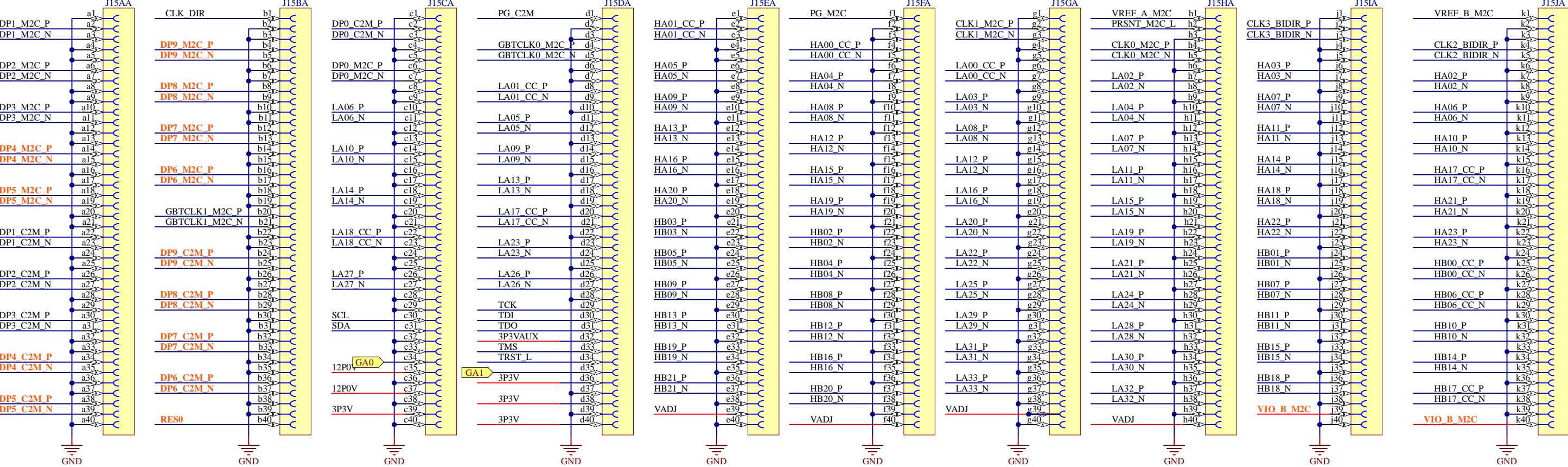
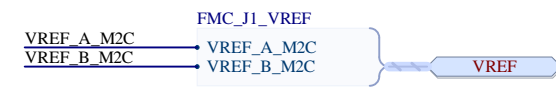
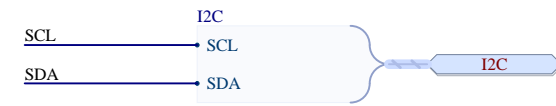
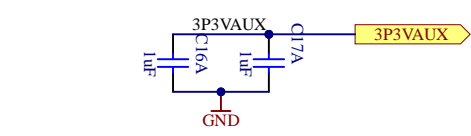
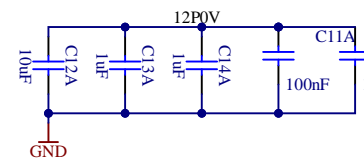
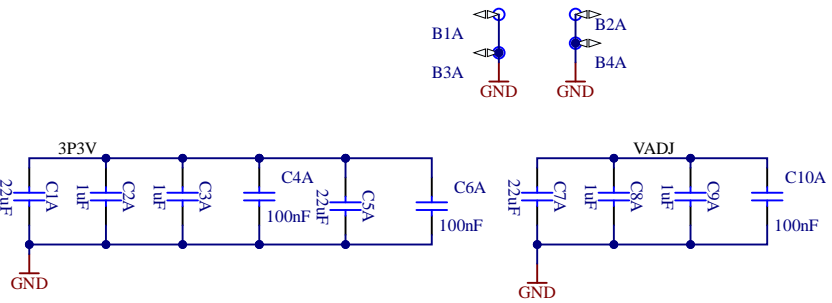
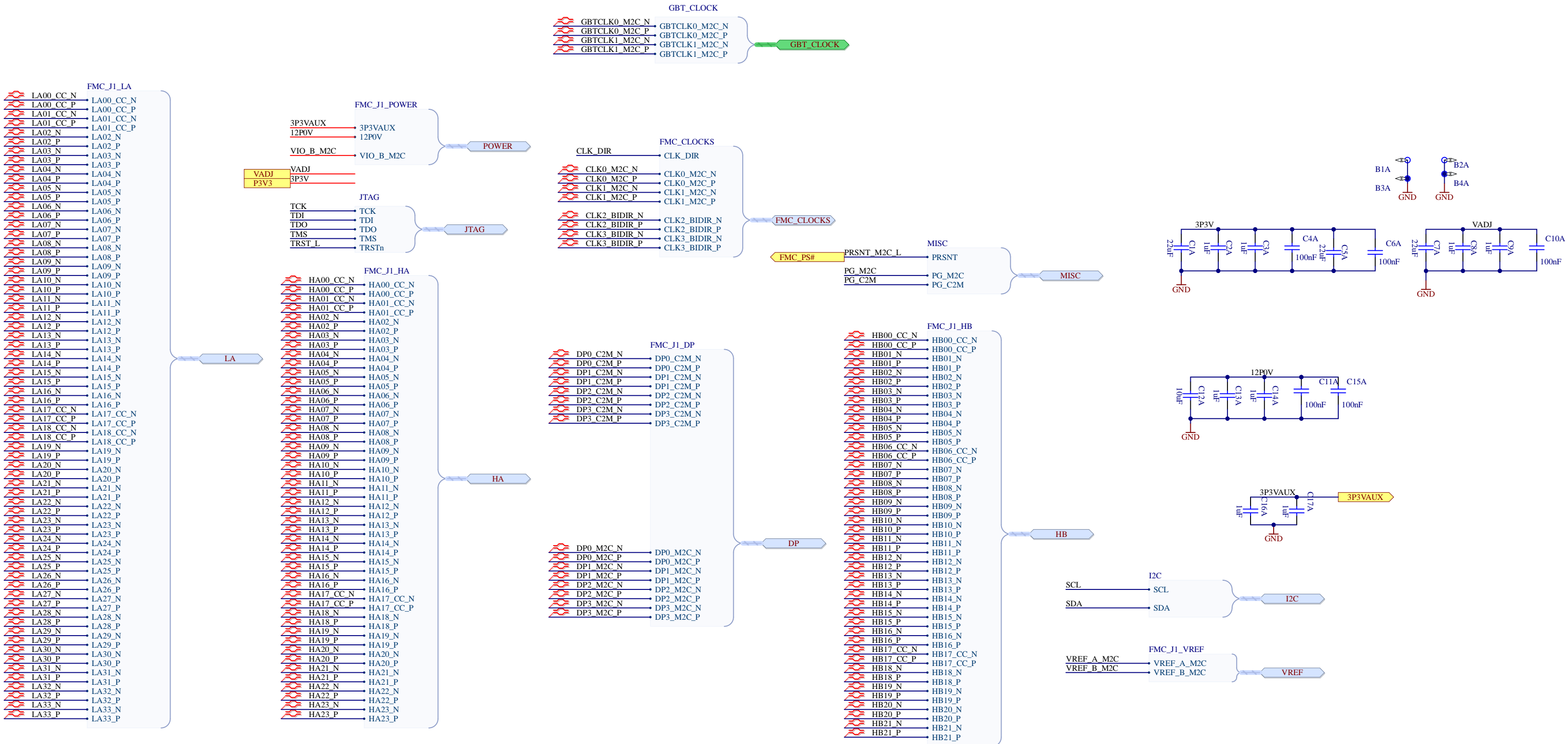


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Warsaw University of Technology Nowowiejska 15/19 00-665 Warsaw		ISE	Contact:	t.przywozki@gmail.com	Size	A4	Rev	1

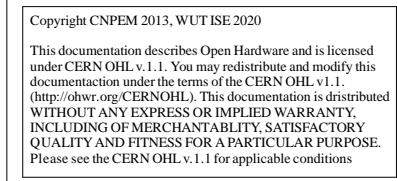




Vadj is not defined as power supply and therefore as global signal as it might differ for the 2 FMC









A

A

B

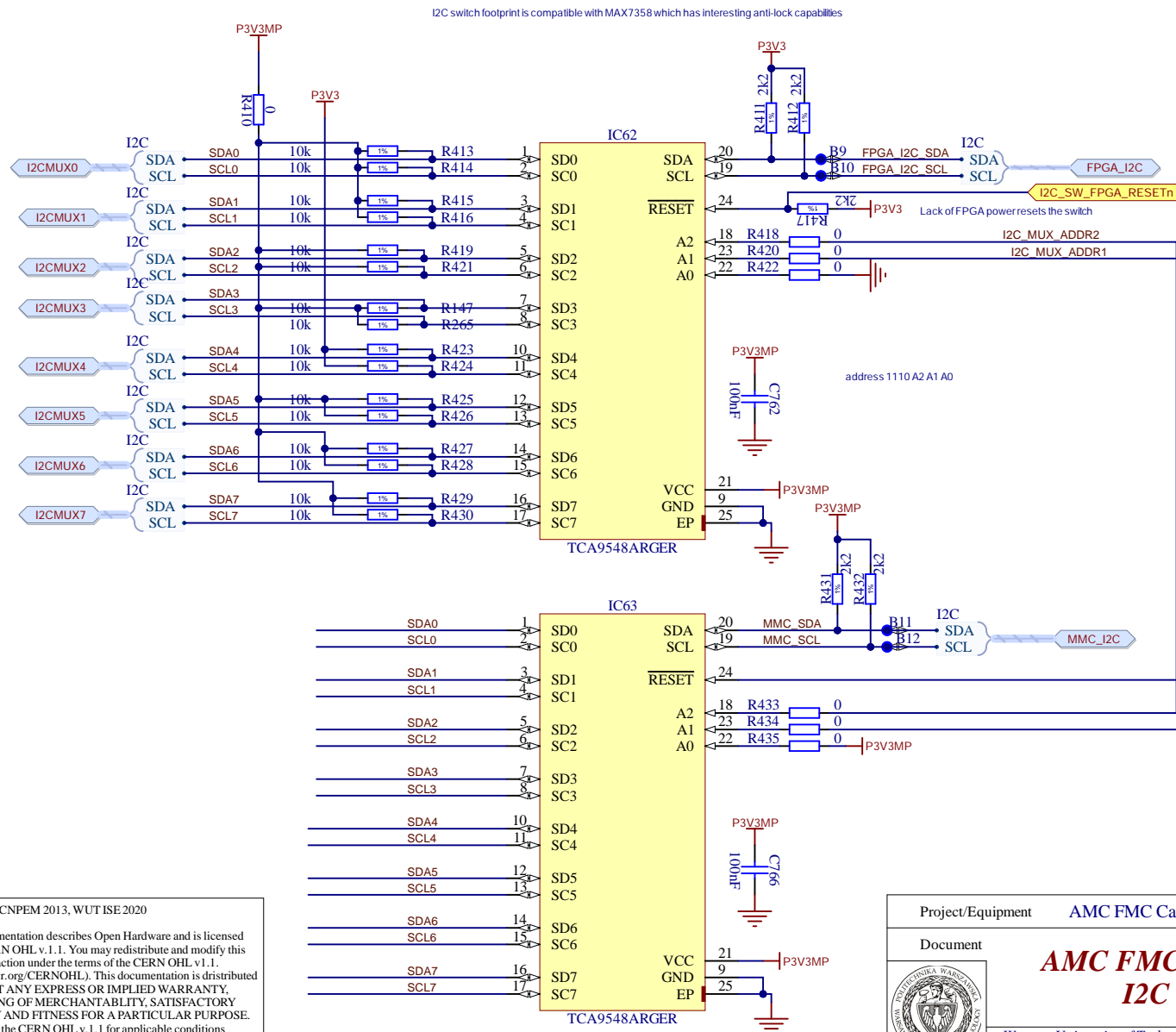
B

C

C

D

D



## I2C device address map

The resources are available from TCA9548s SW: MMC I2C1, addr 1110 A2 A1 0 FPGA I2C and MMC I2C2, addr 1110 A2 A1 1 where A2=P2[28], A1=P2[29] default addr is 0x70 and 0x71

MUX Port 0	MAX6642 0x48
Temp sensors	LM75: 0x4C
	LM75: 0x4D
	LM75: 0x4E
	LM75: 0x4F
MUX Port 1	RTC EEPROM: 0x57
RTCE	SRAM/RTCC reg: 0x6F
	EEPROM 2k: 0x50
	EUI-ID: 0x59
	EEPROM 64k: 0x51
MUX Port 2	
MUX Port 3	INA3221AIRGV: 0x40
Power	INA3221AIRGV: 0x41
	INA3221AIRGV: 0x42
MUX Port 4	8V54816ANLG: 0x5B
Clock switch	
MUX Port 5	RTM devices
MUX Port 6	EEPROM 0x52
FMC2	
MUX Port 7	EEPROM 0x50
FMC1	

mux address 1110 A2 A1 0 from FPGA side 0x7x  
mux address 1110 A2 A1 1 from CPU side 0x7x

I2C\_MUX\_ADDR1[2..1] I2C\_MUX\_ADDR2[2..1]

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Project/Equipment AMC FMC Carrier v4

Document



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ISE

## AMC FMC Carrier v4.0.2

### I2C switches

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